



NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
2. The netname "P2P5V" represents connection to the +2.5V digital power plane.
3. The netname "P1P8V" represents connection to the +1.8V digital power plane.
4. The netname "P1P2V" represents connection to the +1.2V digital power plane.
5. The netname "P12V" represents connection to the +12V digital power plane.
6. The symbol  represents connection to the digital ground plane.
7. The symbol  represents connection to a ground plane isolated from digital ground.
8. A "Z" suffix on a signal name indicates an active low signal.
9. A "HC\_X" suffix on a signal name indicates a high current trace.  
The "X" portion is the required current rating in Amps.
10. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
11. All resistor values are in ohms, 1/16W and 5% unless otherwise specified.

Z\_PCB1  
PCB, DLP HUD Formatter  
DLP007  
2514133



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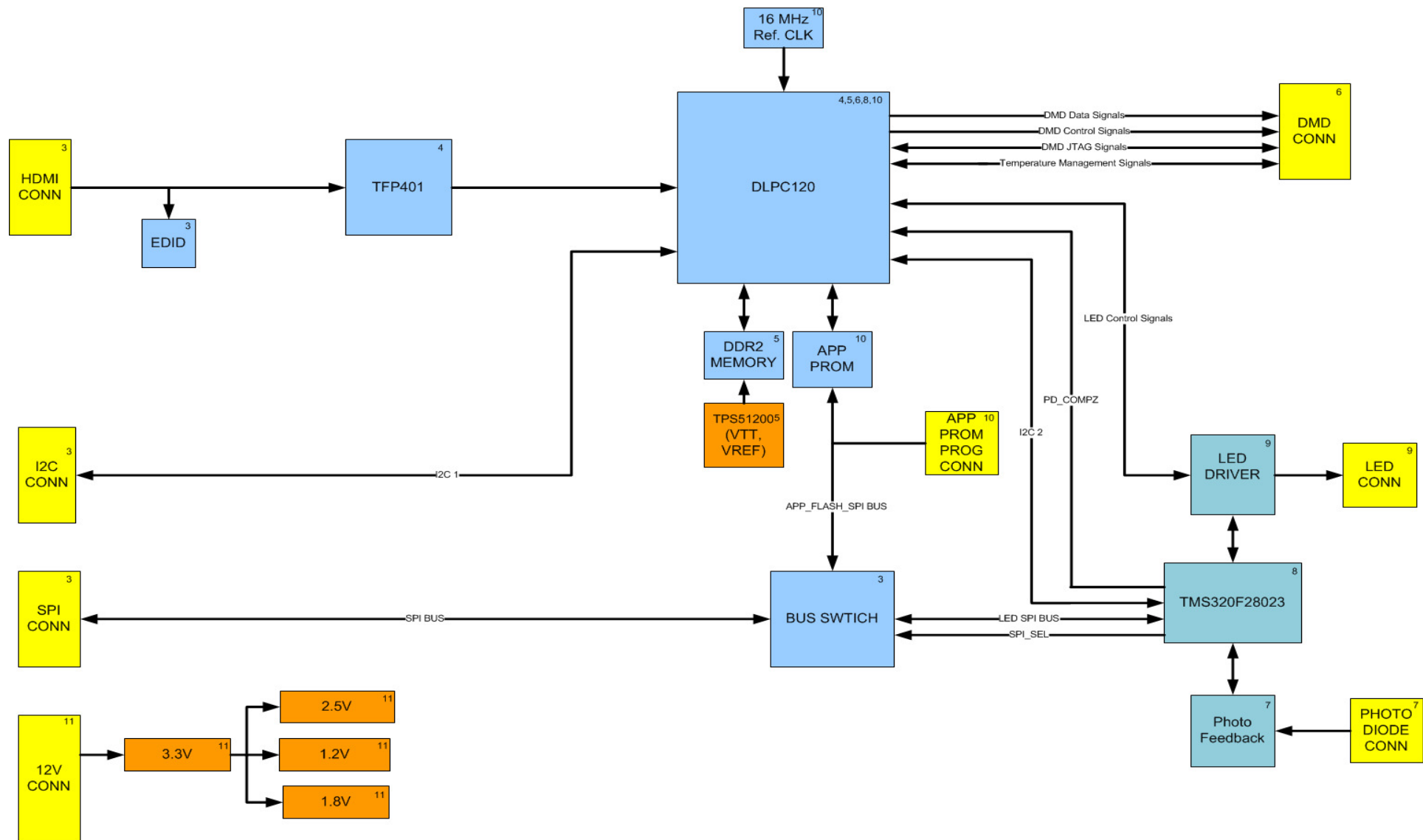
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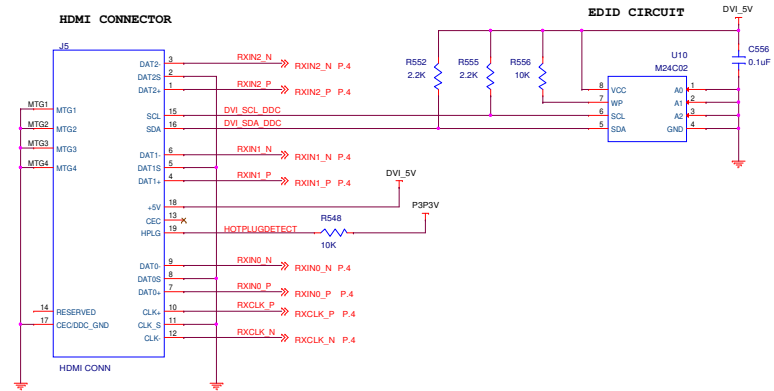
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COMPONENT GENERATED DRAWING. DO NOT REVISE MANUALLY			
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	Initial Board Release	08/15/18	

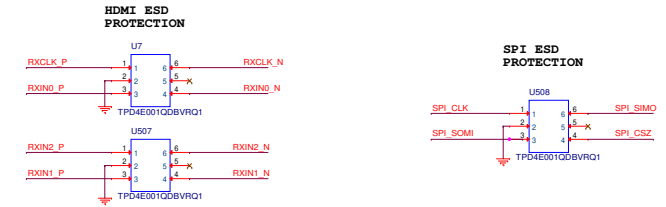
		OWN Jackson Thomas	DATE 08/17/18	<b>TEXAS INSTRUMENTS</b> (C) COPYRIGHT 2014 TEXAS INSTRUMENTS ALL RIGHTS RESERVED	
		ENGR Jackson Thomas			
		SYST Jeff Farris			
		PRJ Jason Thompson			
		QA Scott Croff		TITLE Schematic, Automotive HUD Formatter Board	
NEXT ASSY	USED ON			TIDA-080004	
APPLICATION		SW Cadence Capture 16.6		D	DRWING NO 2516391
				SCALE	SHEET 1 of 11
					REV A



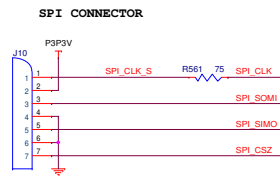
# HDMI INPUT BLOCK



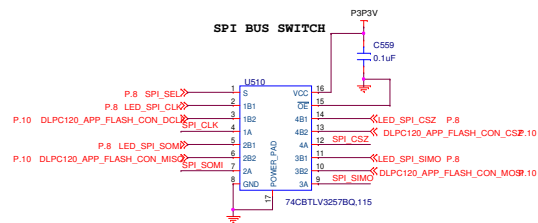
# INPUT ESD PROTECTION



# SPI INPUT BLOCK

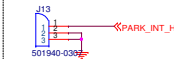


# SPI BUS SWITCH

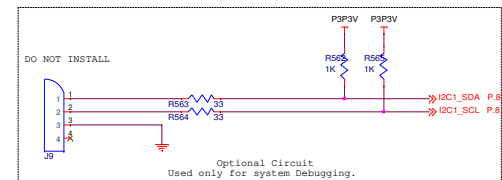


The SPI bus switch allows for one SPI connector to be used for both normal SW control operations and reprogramming the asic application flash.

# High Priority Park Interrupt Signal



# I2C 1 INPUT

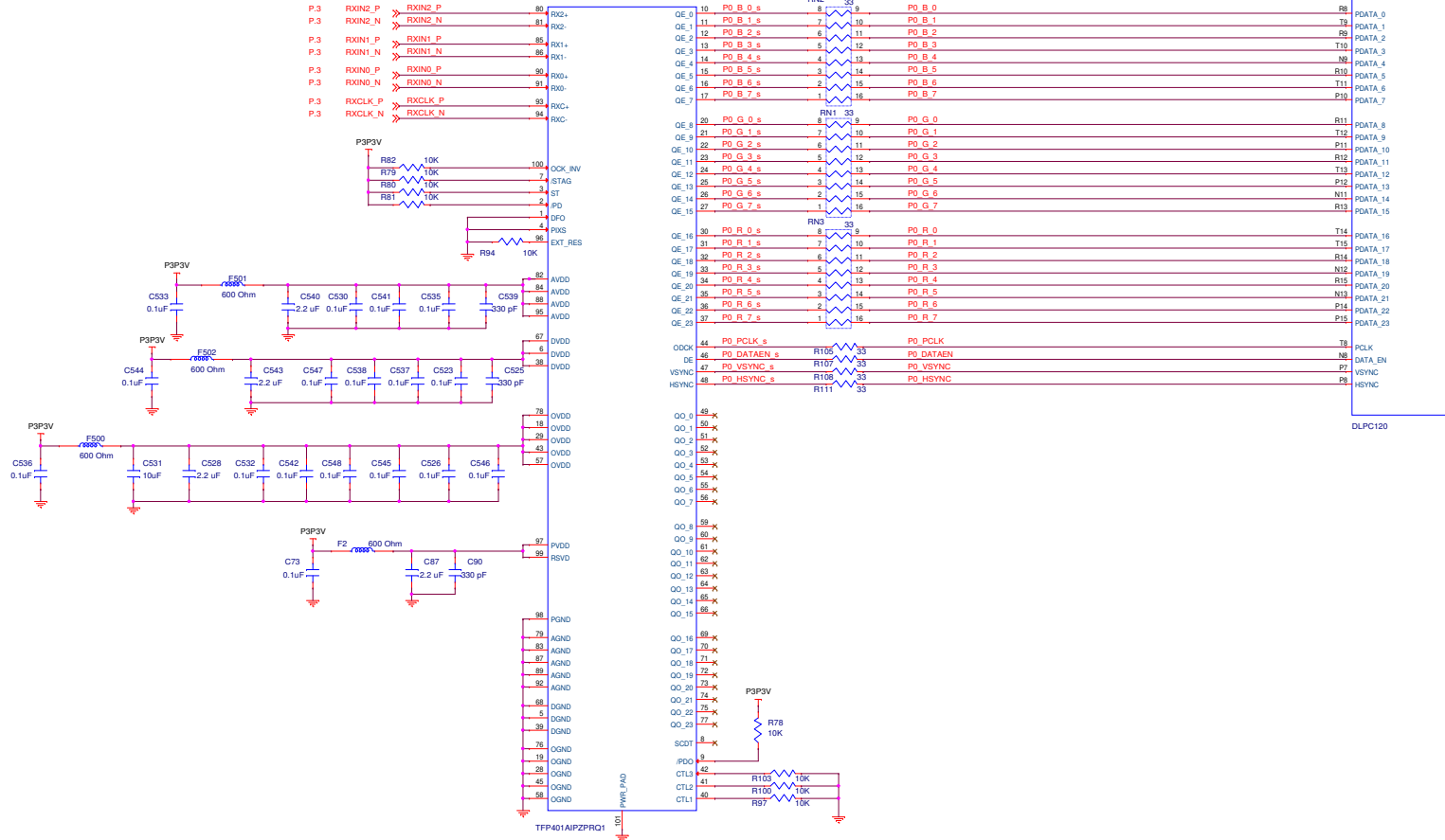


Optional Circuit  
Used only for system Debugging.

# DVI RECEIVER

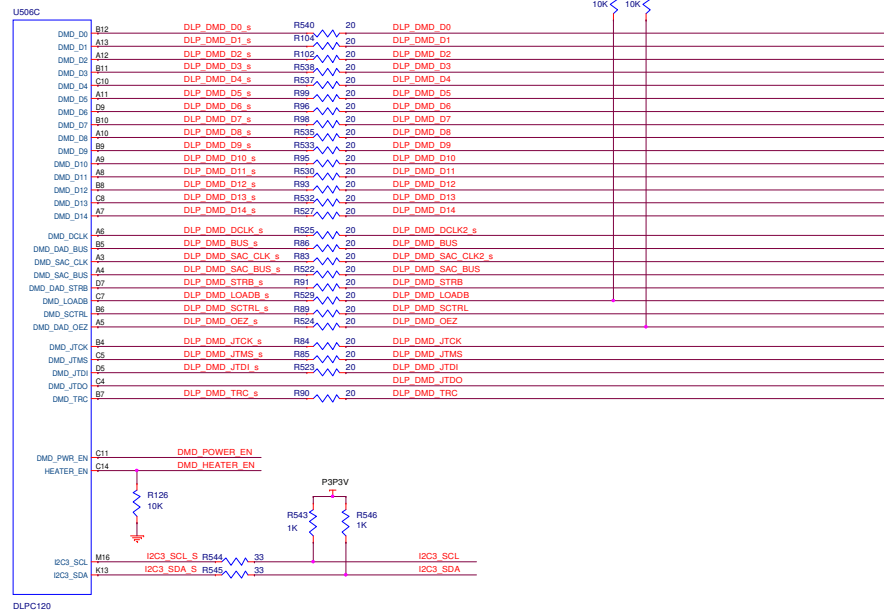
U6

U506A

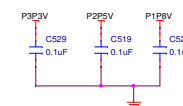
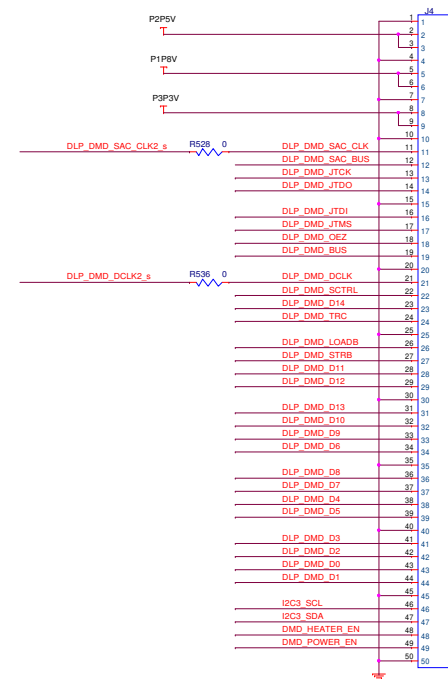




# DLPC120 DMD Interface



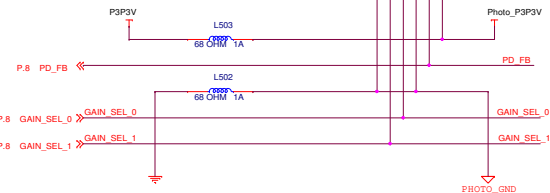
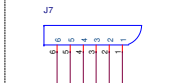
## DMD Connector



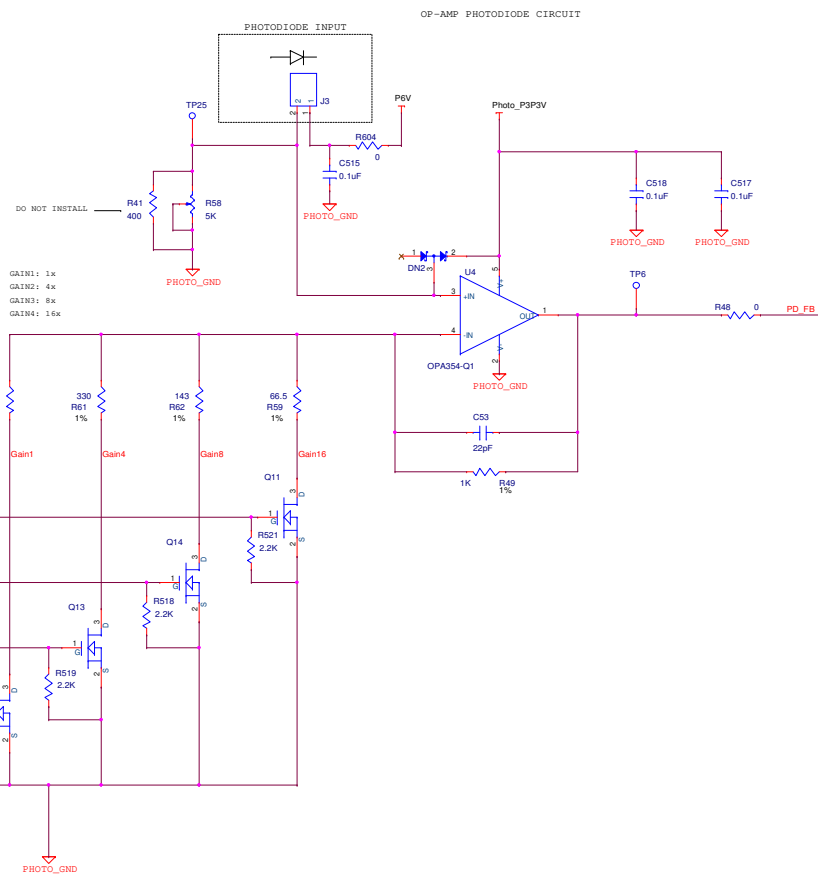
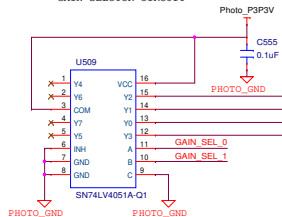
This entire circuit needs to be isolated from the rest of the board to prevent noise issues. Please note the analog ground to digital ground ferrite bead separating the ground planes.

# EXTERNAL PHOTODIODE CIRCUIT CONNECTOR

Optional Circuit  
Used only for system testing.  
DO NOT INSTALL

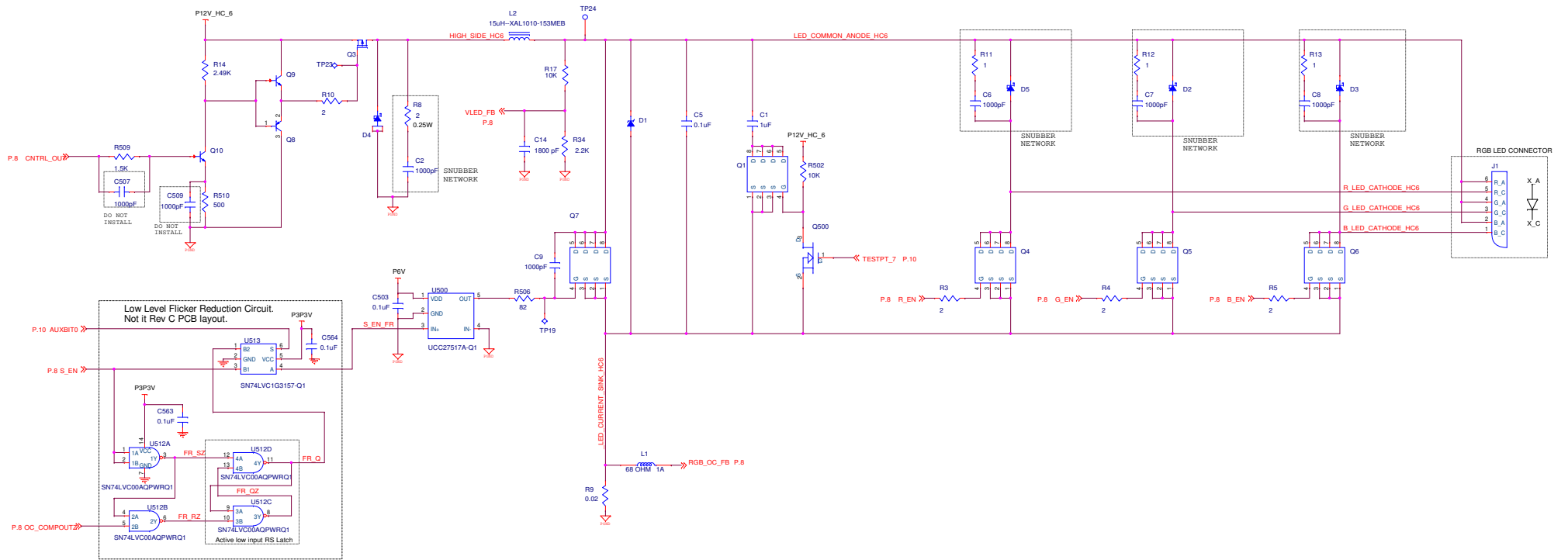


## GAIN SELECTOR CIRCUIT

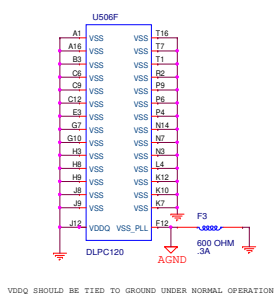
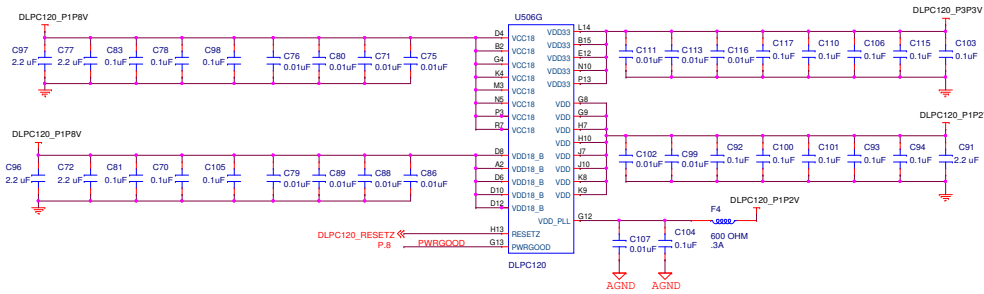


The schematic diagram shows the reset circuit for the ATmega328P. It includes a P3P3V supply, resistors R88 (10K) and R541 (2.2K), a MOSFET Q501, a diode DN1, and a push-button SW1 (CVS-01TB). The reset signal is connected to the MON\_RESET pin (P.10) and the MCU\_RESET pin (P.4). A note indicates 'DO NOT INSTALL' for the SW1 component.

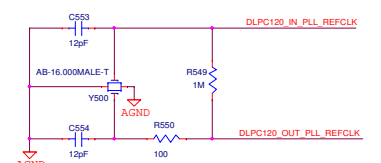




# DLPC120 POWER

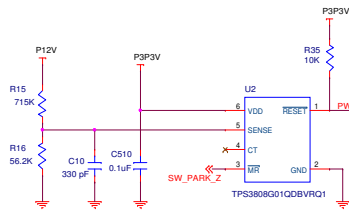


## DLPC120 PLL REFERENCE CLOCK CIRCUITS

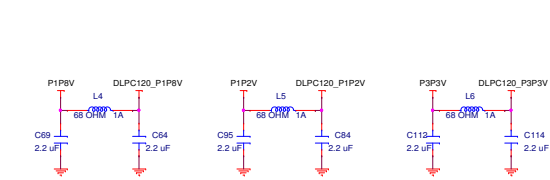


Place Circuit as Close as Possible to the ASIC.

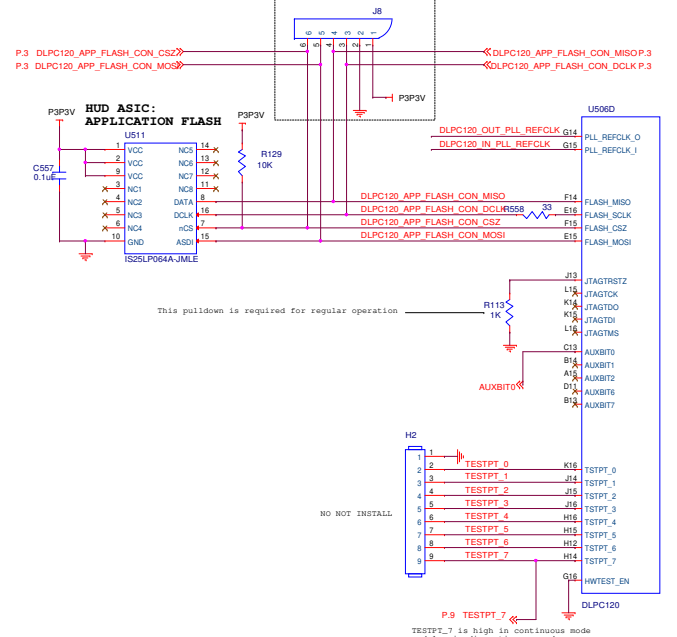
## BATTERY VOLTAGE MONITOR



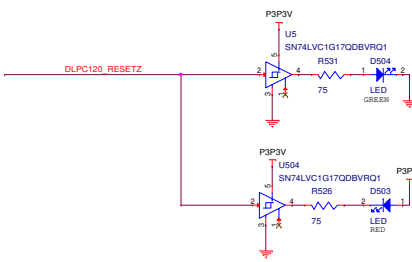
## ASIC EMC FILTER



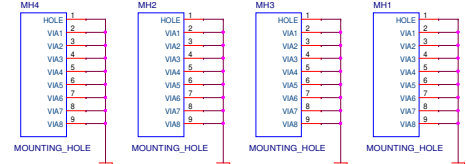
## DLPC120 TEST AND CONFIGURATION INTERFACES



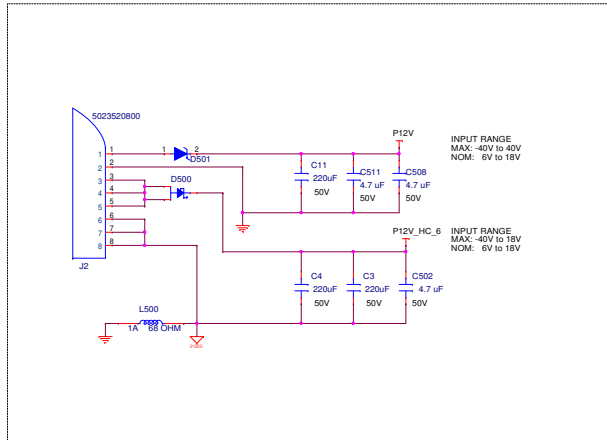
## SYSTEM POWER/RESET INDICATORS



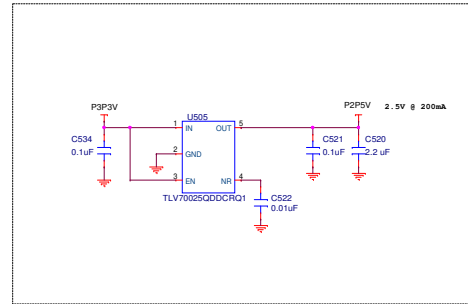
## PBC MOUNTING HOLES



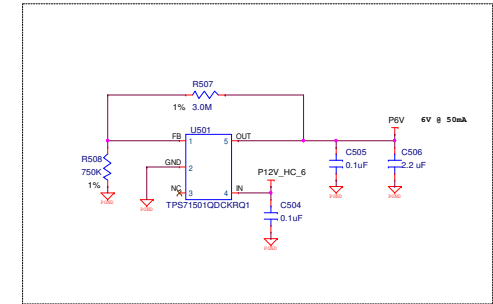
# 12V POWER INPUT



# 2.5V REGULATOR

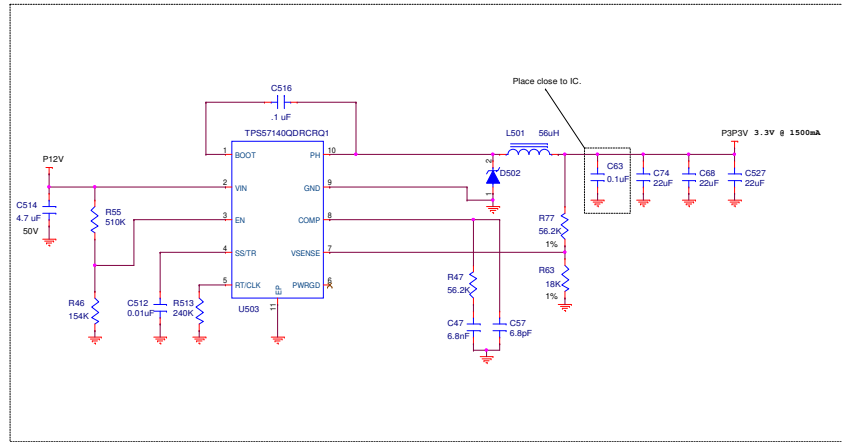


# 5V REGULATOR



Optional Circuit  
Used only for system testing.

# 3.3V REGULATOR



# 1.2V AND 1.8V REGULATOR

