Design Guide: TIDA-010982

Field Transmitter Platform: 4mA to 20mA Loop-Powered Interface Reference Design

Description

This reference design gives an example implementation of a 4–20mA interface for 2-wire loop-powered sensors. The design enables evaluation of the AFE881H1 and AFE882H1 in a lower power application-like environment with a 1.8V signal chain. The AFE881H1 and AFE882H1 integrates a high precision 16-bit DAC and a HART® modem. The reference design provides a serial peripheral interface (SPI) and universal asynchronous receiver-transmitter (UART) interface on a pin header to connect to a microcontroller. This pin header provides 3.3V and 1.8V to power a connected microcontroller and a 1.25V reference voltage to be used for an ADC.

Resources

TIDA-010982	Design Folder
AFE881H1, AFE882H1	Product Folder
OPA391, TPS7A03	Product Folder
REF35, TVS3301	Product Folder
TMUX1219, SN74LV8T165	Product Folder

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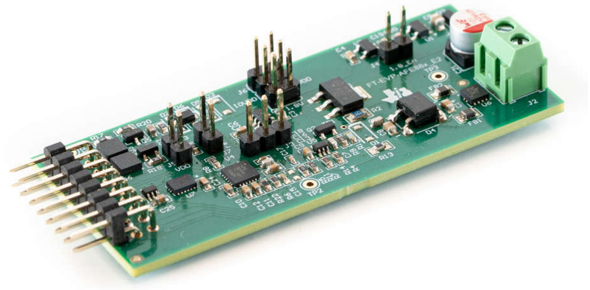
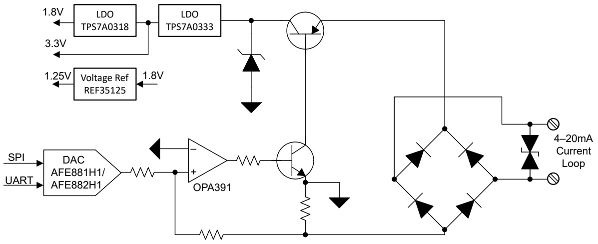
Features

- Implementation of 4–20mA loop interface for 2-wire loop-powered sensor
- Complete 1.8V signal chain allows low power consumption and maintains high accuracy
- AFE88xH1 16-bit DAC with integrated reference and HART modem
- MCU interface providing power output (1.8V, 3.3V, 1.25V reference voltage), SPI and UART interface

Applications

- Flow transmitter
- Level transmitter
- Pressure transmitter
- Temperature transmitter
- Analog output module





1 System Description

This reference design implements the 4–20mA current loop interface for loop powered sensors. The design incorporates a 16-bit DAC, either the AFE881H1 or AFE882H1. The DAC output voltage drives an OPA391 op amp converting the voltage to current.

Power supplies with 1.8V or 3.3V output options are integrated into this design. Configuration settings dictate whether 1.8V or 3.3V is used for powering the analog circuit on the board and the connected MCU. Low dropout (LDO) regulators (TPS7A0333 and TPS7A0318) with low I_Q are used to maintain a stable and efficient power output keeping the available power for the system high.

The design incorporates a discrete P-channel Metal-Oxide-Semiconductor field-effect transistor (PMOSFET) CSD25404 power switch for an MCU. This power switch controls the 1.8V and 3.3V rail on a connector attached to the MCU. Additional bulk capacitance supports start-up currents exceeding loop limits. The capacitor powers MCU initialization prior to entering low-power mode.

1.1 Key System Specifications

PARAMETER	SPECIFICATION
Loop supply voltage	8V to 30V
Loop current range	3mA to 24mA
Resolution	16 bit
RMS noise	< 0.5μA
Peak-to-peak noise	< 3μA
Settling time	< 1ms
Power supply output	3.3V, 1.8V
Power supply output current	2mA
Reference voltage output	1.25V
Interface to MCU	SPI, UART

2 System Overview

2.1 Block Diagram

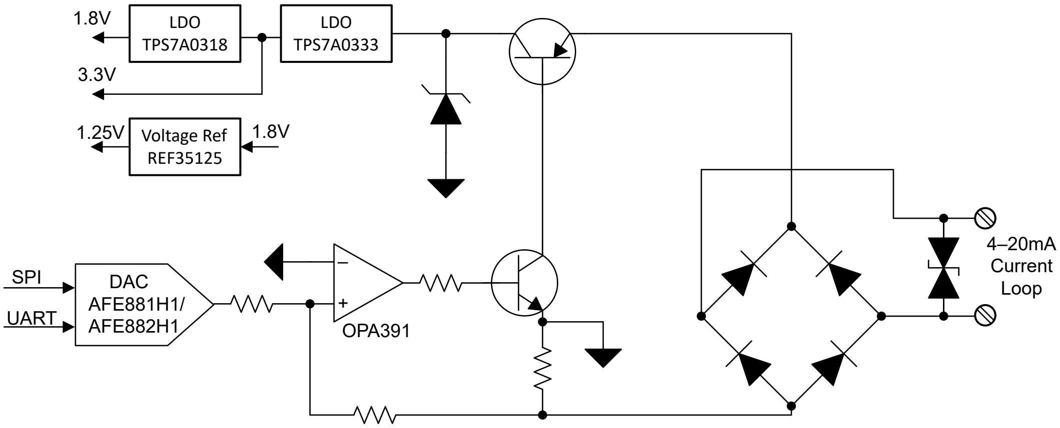


Figure 2-1. TIDA-010982 Block Diagram

2.2 Design Considerations

This design implements the 4mA to 20mA output stage for field transmitters and sensors. AFE881H1 and AFE882H1 integrates digital-to-analog conversion capabilities with high resolution up to 16 bits. Low power consumption allows the system to operate directly from a loop supply. Moreover the AFE has an integrated MODEM to enable HART communication functionality. With AFE881H1, the whole design can be operated on a single 1.8V power supply.

Polarity reversal protection is achieved through the use of a Graetz bridge at the input, enabling operation in either polarity. Overvoltage protection is provided by the TVS3301 TVS diode, safeguarding against excessive voltage levels. High-frequency noise is reduced by the presence of a ferrite bead.

Current regulation is achieved through a pass transistor paired with a Zener diode and the first LDO. The system sinks part of the current and sinks the rest mostly in the Zener diode, allowing power dissipation to be shared among multiple devices and minimizing thermal stress. A dedicated operational amplifier translates the output voltage of the DAC into the loop current.

Two power supplies, 1.8V and 3.3V, are available from LDOs to power the components of the system. A stable 1.25V reference voltage is provided directly on the board circuit. The reference voltage output is also accessible through a pin header.

2.3 Highlighted Products

2.3.1 TPS7A03

The TPS7A03 is an ultra-small, ultra-low quiescent current low-dropout linear regulator (LDO) that can source 200mA with excellent transient performance.

The TPS7A03, with an ultra-low I_Q of 200nA, is designed specifically for applications where very-low quiescent current is a critical parameter. This device maintains low I_Q consumption even in dropout mode to further increase battery life. When in shutdown or disabled mode, the device consumes ultra-low, 3nA I_Q that helps increase the shelf life of the battery.

The TPS7A03 has an output range of 0.8V to 5.0V available in 50mV steps to support the lower core voltages of modern microcontrollers (MCUs).

The TPS7A03 features a smart enable circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is left floating and helps minimize the external components used to pulldown the EN pin. This circuit also helps minimize the current drawn through the external pulldown circuit when the device is enabled.

2.3.2 REF35

The REF35 is part of a family of nanopower, low-drift, high-precision series reference devices. The REF35 family features ±0.05% initial accuracy with 650nA typical power consumption. The temperature coefficient (12ppm/°C) and long-term stability (40ppm at 1000 hours) of the device can help improve system stability and reliability. The low power consumption combined with high-precision specifications are designed for a wide variety of portable and low-current applications.

The REF35 supplies up to 10mA current with $3.3\text{ppm}_{\text{p-p}}$ noise and 20ppm/mA load regulation. With this feature set, REF35 creates a strong low-noise, high accuracy power supply for precision sensors and 12–16b data converters.

2.3.3 TVS3301

The TVS3301 device shunts up to 27A of IEC 61000-4-5 fault current to protect systems from high-power transients or lightning strikes. The device survives the common industrial signal line EMC requirement of 1kV IEC 61000-4-5 open circuit voltage coupled through a 42Ω impedance. The TVS3301 uses a feedback mechanism to provide precise flat clamping during a fault, keeping system exposure lower than traditional TVS diodes. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness. The TVS3301 has a ±33V operating range to enable operation in systems that require protection against reverse wiring conditions.

In addition, the TVS3301 is available in a small SON footprint designed for space constrained applications, offering a significant size reduction compared to standard SMA and SMB packages. Low device leakage and capacitance provide a minimal effect on the protected line. To provide robust protection over the lifetime of the product, TI tests the TVS3301 against 5000 repetitive surge strikes at 125°C with no shift in device performance.

2.3.4 OPA391

The OPA391, OPA2391, and OPA4391 (OPAx391) devices feature a unique combination of high bandwidth (1MHz) along with very-low quiescent current (24µA) in high-precision amplifiers. These features combined with rail-to-rail input and output make these devices an exceptional choice in high-gain, low-power applications. Ultra-low input bias current of 10fA, only 45µV of offset (maximum), and 1.2µV/°C of drift overtemperature help maintain high precision in ratiometric and amperometric sensor front ends that have demanding low-power requirements.

The OPAx391 uses Texas Instruments' proprietary e-trim™ operational amplifier technology, enabling a unique combination of ultra-low offset and low-input offset drift without the need for any input switching or auto-zero techniques. The CMOS-based technology platform also features a modern, robust output stage design that is tolerant of high-output capacitance, alleviating stability problems that are common in typical low-power amplifiers.

2.3.5 AFE881H1

The 16-bit AFE881H1 and 14-bit AFE781H1 (AFEx81H1) are highly integrated, high-accuracy, extremely low-power digital-to-analog converters (DACs) with voltage outputs designed for HART-enabled sensor-transmitter applications.

The AFEx81H1 devices include most of the components required to design a 4mA to 20mA, 2-wire (loop-powered) sensor transmitter. In addition to the highly accurate DAC, these parts include a HART-certified frequency-shift keyed (FSK) modem, 10ppm/°C voltage reference, and diagnostic analog-to-digital converter (ADC). To accommodate intrinsic and functional safety concerns, external voltage-to-current conversion and power regulation are required.

The internal diagnostic ADC is multiplexed to several internal nodes that enable an automatic self-health check. If any fault is detected from the diagnostic ADC, CRC frame-error checking, or windowed watchdog timer, the devices can optionally issue an interrupt, enter a fail-safe state corresponding to a standard NAMUR output value or user-specified custom value, or both.

These devices operate from supplies as low as 1.71V with 220µA maximum quiescent current. The devices are specified over the temperature range of –40°C to +125°C, but are functional from –55°C to +125°C.

2.3.6 AFE882H1

The 16-bit AFE882H1 and 14-bit AFE782H1 (AFEx82H1) are highly-integrated, high-accuracy, extremely low-power DACs with voltage-outputs designed for HART-enabled process control and industrial automation applications.

The AFEx82H1 devices include most of the components required to design a 4mA to 20mA, 3-wire or 4-wire sensor transmitter or analog output module. In addition to the highly accurate DAC, these devices include a HART®-compliant FSK modem, 10ppm/°C voltage reference, and diagnostic analog-to- digital converter (ADC). To accommodate intrinsic and functional safety concerns, external voltage-to-current conversion and power-regulation are required.

The internal diagnostic ADC is multiplexed to several internal nodes that enable an automatic self- health check. This check is capable of detecting errors or malfunctions of the internal bias sources, power regulator, voltage reference, DAC output, die temperature, and optional external voltage source. If any fault is detected from the diagnostic ADC, CRC frame-error checking, or windowed watchdog timer, the devices can optionally issue an interrupt, enter a user-specified fail-safe state, or both.

2.3.7 SN74LV8T165

The SN74LV8T165 device is a parallel- or serial-in, serial-out 8-bit shift register. This device has two modes of operation: load data, and shift data which are controlled by the SH/$\overline{\text{LD}}$ input. The output level is referenced to the supply voltage (VCC) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example 1.2V input to 1.8V output or 1.8V input to 3.3V output). In addition, the 5V tolerant input pins enable down translation (for example 3.3V to 2.5V output).

2.3.8 TMUX1219

The TMUX1219 is a general-purpose complementary metal-oxide semiconductor (CMOS) single-pole double-throw (SPDT) switch. The TMUX1219 switches between two source inputs based on the state of the SEL pin. A wide operating supply of 1.08V to 5.5V allows for use in a broad array of applications from personal electronics to building automation. The device supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from GND to VDD. A low supply current of 4nA enables use in portable applications.

All logic inputs have 1.8V logic compatible thresholds, making sure both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-safe logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

3 System Design Theory

This section provides information about the different blocks of this design. Figure 3-1 shows the location of these blocks.

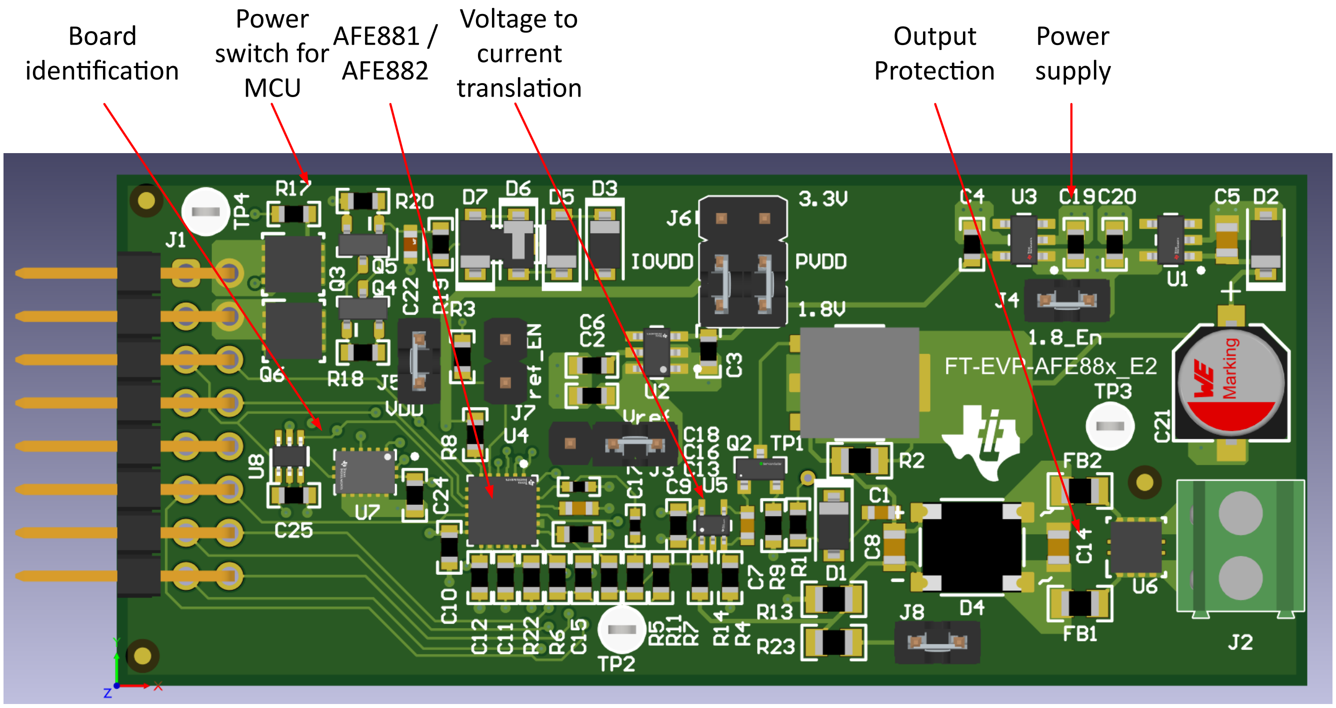


Figure 3-1. TIDA-010982 Functional Blocks

To be able to identify the board from the software, each board has a shift register of which the input pins code a board ID number, which can be read from the MCU through SPI.

The 1.8V and 3.3V voltages available on the header are switched on as soon as the voltages are stable using a PMOSFET as a discrete power switch.

The AFE881H1 or AFE882H1 is the main component of the design and is a voltage DAC with integrated HART modem. The output voltage is converted to a current using an operational amplifier, transistors, and some passives.

The output is protected against reverse polarity using a bridge rectifier and against transient voltages using a TVS3301 TVS diode. Some filtering from high frequency noise is available using a ferrite bead.

For the power supply, two LDOs are onboard to generate 3.3V and 1.8V from the loop voltage.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

To get the board working, the right connections must be made and the jumpers must be set accordingly. Figure 4-1 shows the TIDA-010982 jumpers and Table 4-1 gives a short description of the jumpers and connectors.

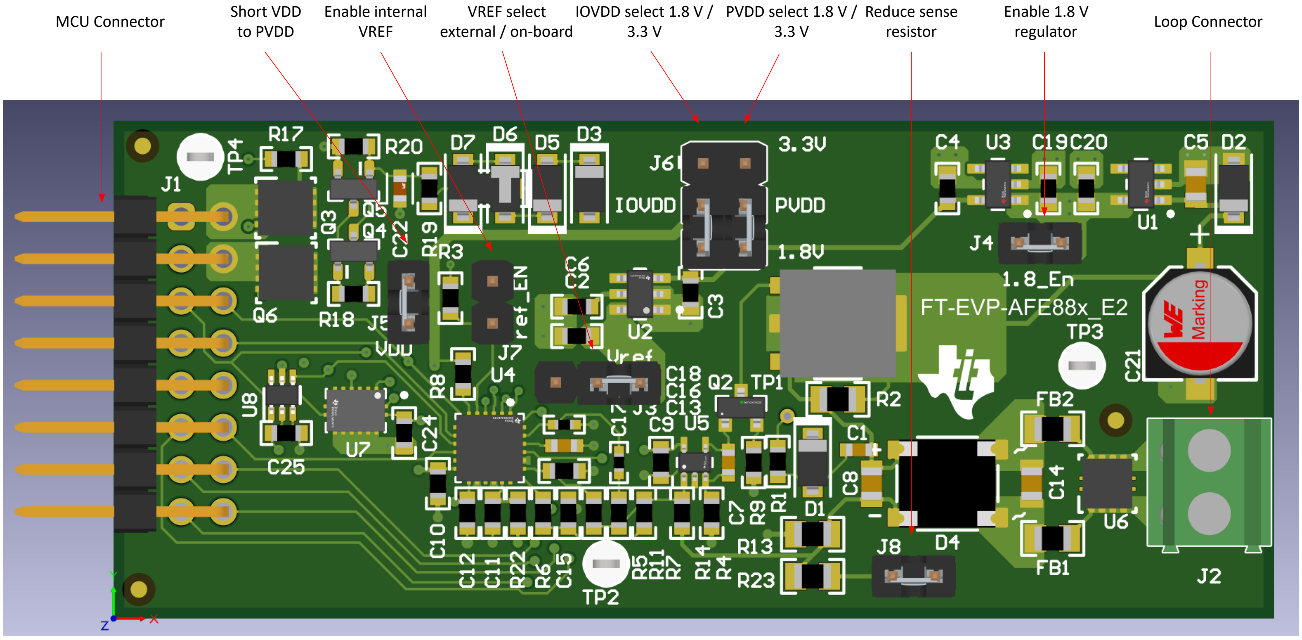


Figure 4-1. TIDA-010982 Jumpers

Table 4-1. Jumper and Connector Descriptions

DESIGNATOR	JUMPER, CONNECTOR	DESCRIPTION
J1	MCU Connector	Connection to microcontroller board
J5	Short VDD to PVDD	If using AFE881H1 with 1.8V this needs to be shorted, disabling the internal LDO
J7	Enable internal VREF	Setting this enables the internal reference voltage of AFE881H1 or AFE882H1
J3	VREF select	Set to 1-2 to use onboard REF35125. Set to 2-3 to use external reference voltage provided over MCU connector J1.
J6	IOVDD select	Set to 1-3 for 3.3V operation and 3-5 for 1.8V
J6	PVDD select	Set to 2-4 for 3.3V operation and 4-6 for 1.8V
J8	Reduce sense resistor	Reduces feedback resistor for voltage current translation. For 1.8V operation this jumper needs to be set.
J4	Enable 1.8V regulator	Set this jumper to enable 1.8V LDO
J2	Loop Connector	Connect to current loop

For different operating voltages, the jumpers need to be set different in order not to damage the devices. Figure 4-2 shows how to set the jumpers for 1.8V operation. Figure 4-3 shows the jumper configurations for 3.3V operation. The red boxes show how the jumpers need to be set for 3.3V operation.

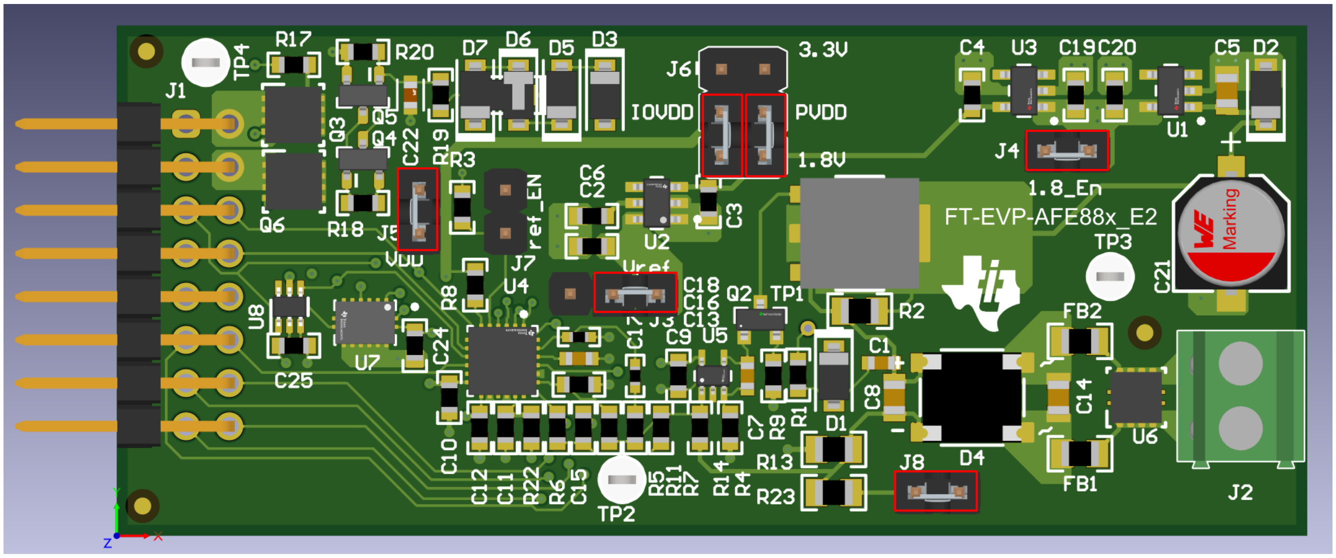


Figure 4-2. TIDA-010982 Jumper Configurations for 1.8V Operation

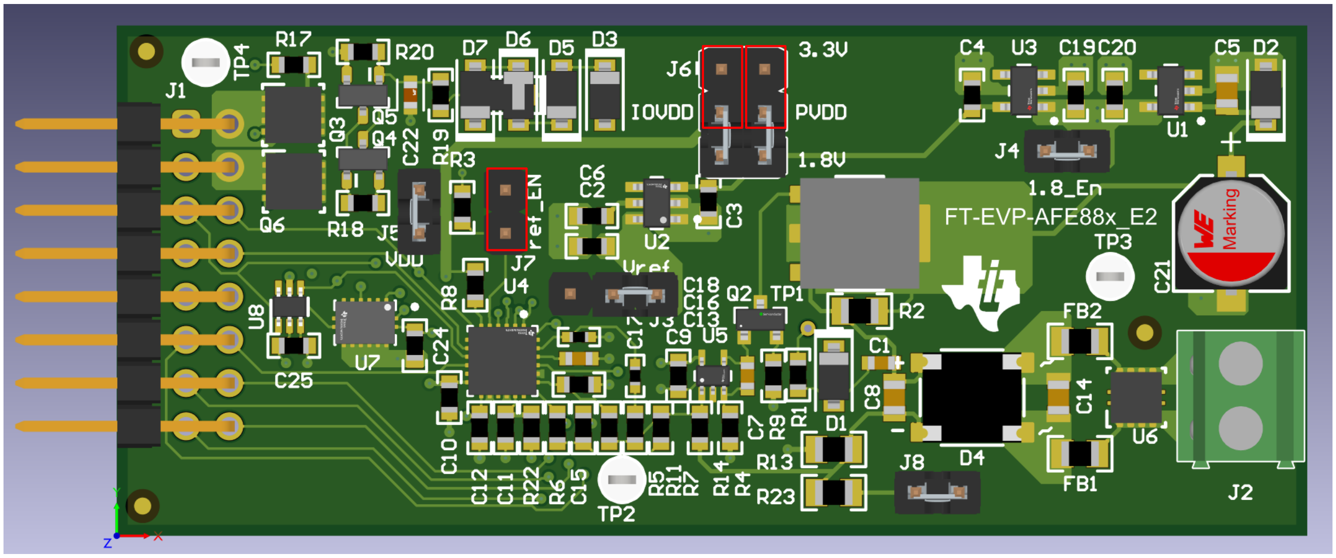


Figure 4-3. TIDA-010982 Jumper Configurations for 3.3V Operation

The connector J1 connects to an MCU board, Table 4-2 shows the pinout. Pin one is marked on the PCB.

Table 4-2. J1 Connector Pinout

PIN	SIGNAL
1	GND
2	VDD-3V3
3	VREF_EXT
4	VDD-1V8
5	ID0
6	SCLK
7	Not used
8	SDI
9	Not used
10	SDO
11	$\overline{\text{ALARM}}$

Table 4-2. J1 Connector Pinout (continued)

PIN	SIGNAL
12	$\overline{CS}$
13	CD
14	DAC_HART_RX
15	$\overline{RTS}$
16	DAC_HART_TX

4.2 Test Setup

For all tests, the reference design is combined with a ADS122S14 EVM which contains an ADC as well as an MCU controlling the AFE as well as the ADC. The different test setups are explained in the next section.

4.3 Test Results

4.3.1 Linearity Tests

For this test, this reference design is connected to a microcontroller for the SPI of the AFE and the analog output is connected to a power supply and an ammeter. The whole system is run from the current on the loop and interfaced to a PC through an isolated UART. All tests are done with 10V and 24V loop voltage, with AFE881H1 in 3.3V and 1.8V configuration, for AFE882H1 in 3.3V configuration. The DAC code is stepped and the current reading of the ammeter is recorded.

Figure 4-4 shows the complete setup.

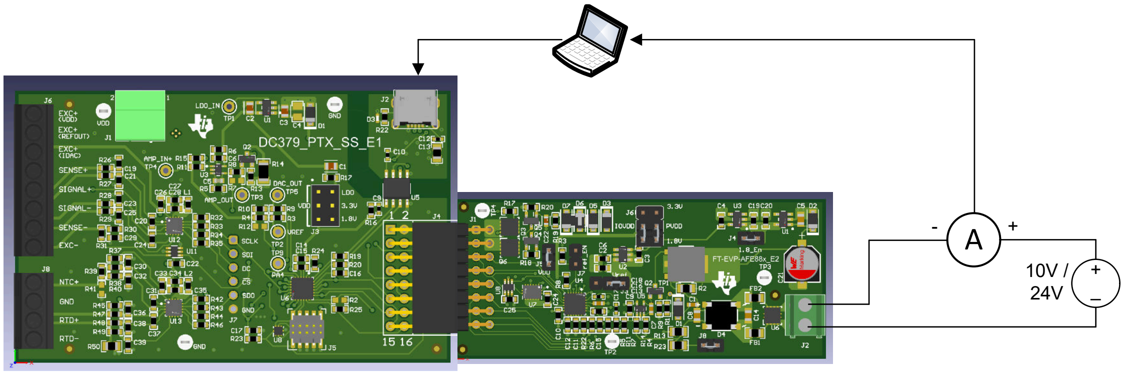


Figure 4-4. Test Setup for Linearity Test

Figure 4-5 through Figure 4-16 show the linearity including a linear trend line which is also used for calculating the error. Therefore the equation is used to calculate the *ideal* current and the difference to the measurement is shown. For each 10V to 24V configuration, the same equation is used to calculate the error, simulating a calibration at a bias point and then operating at a different one. The different equations are shown for reference.

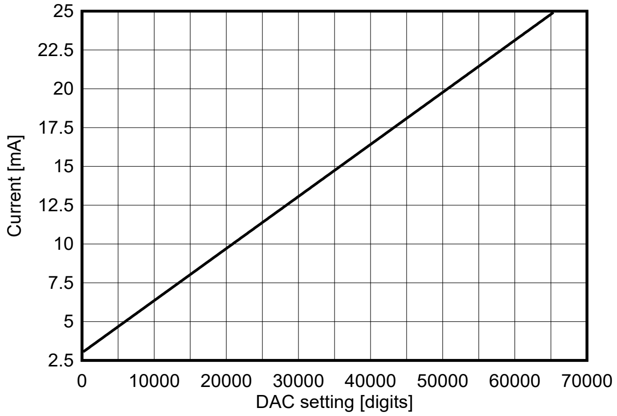


Figure 4-5. AFE881: 1.8V Supply, 10V Loop Linearity
y = 3.35466E–04x + 2.99760

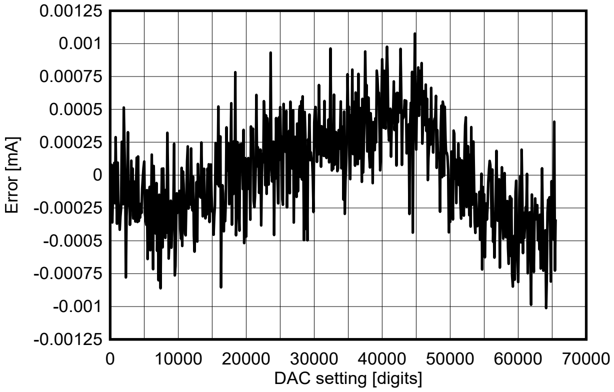


Figure 4-6. AFE881: 1.8V Supply, 10V Loop Error

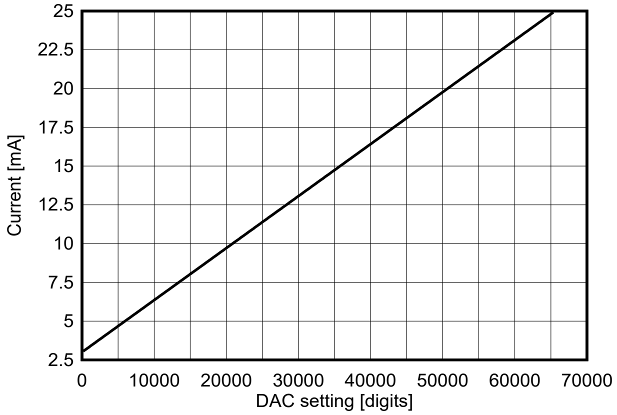


Figure 4-7. AFE881: 1.8V Supply, 24V Loop Linearity
y = 3.35485E–04x + 2.99755

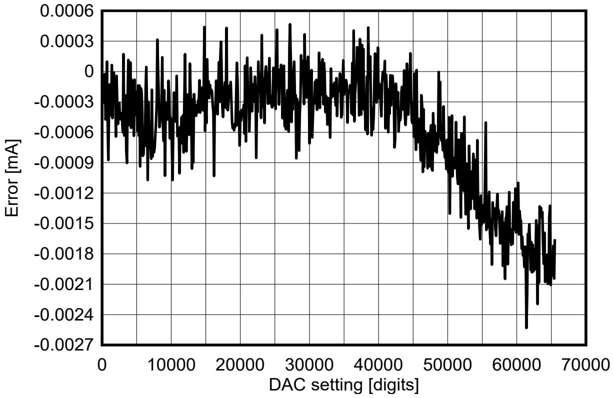


Figure 4-8. AFE881: 1.8V Supply, 24V Loop Error

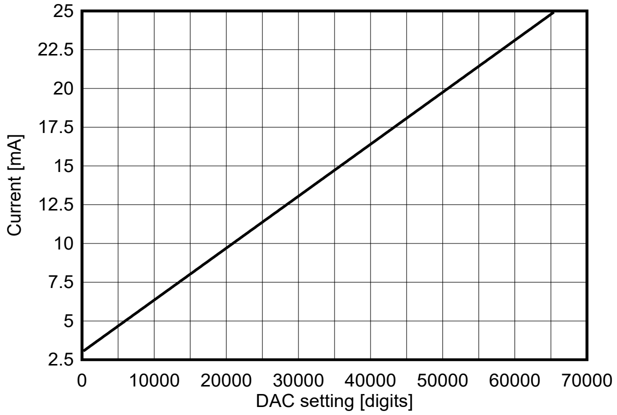


Figure 4-9. AFE881: 3.3V Supply, 10V Loop Linearity
y = 3.35189E–04x + 2.99416

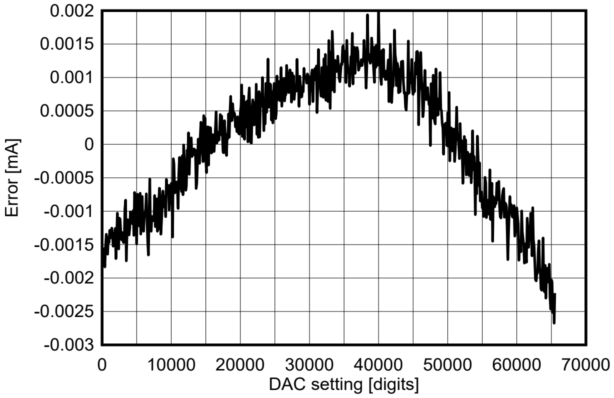


Figure 4-10. AFE881: 3.3V Supply, 10V Loop Error

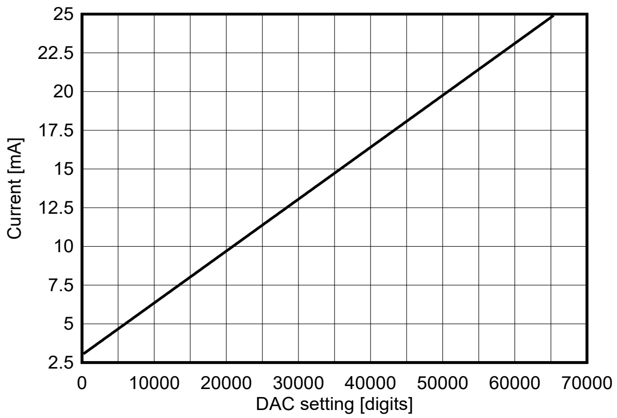


Figure 4-11. AFE881: 3.3V Supply, 24V Loop Linearity
y = 3.35312E–04x + 2.99208

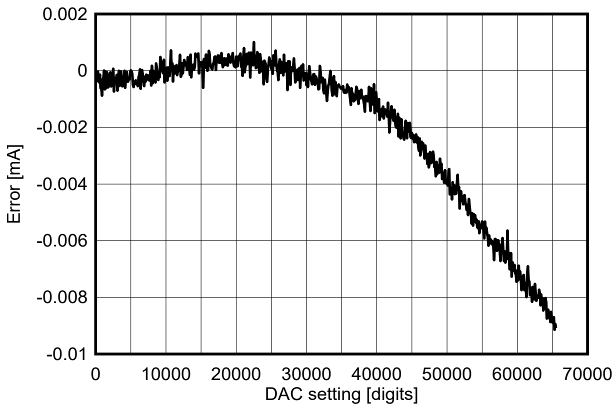


Figure 4-12. AFE881: 3.3V Supply, 24V Loop Error

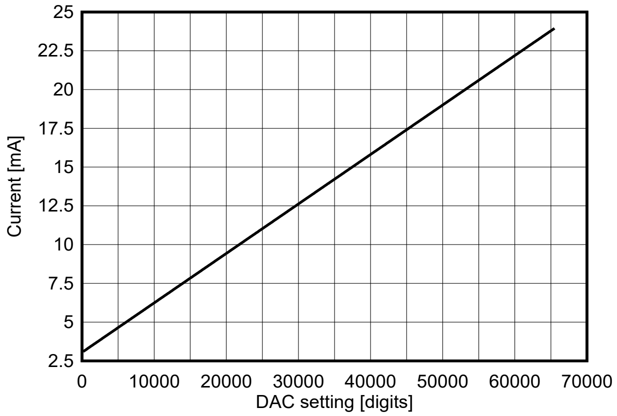


Figure 4-13. AFE882: 3.3V Supply, 10V Loop Linearity
y = 3.19149E–04x + 3.04646

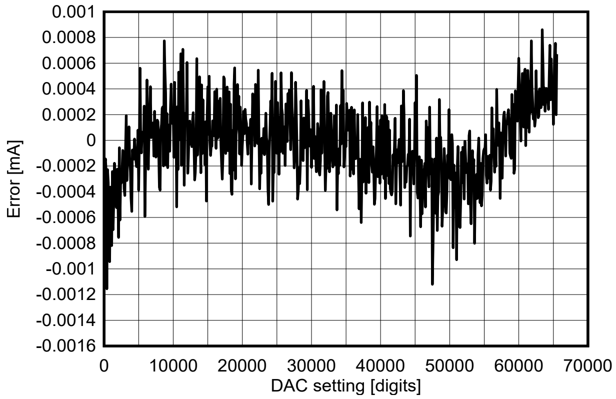


Figure 4-14. AFE882: 3.3V Supply, 10V Loop Error

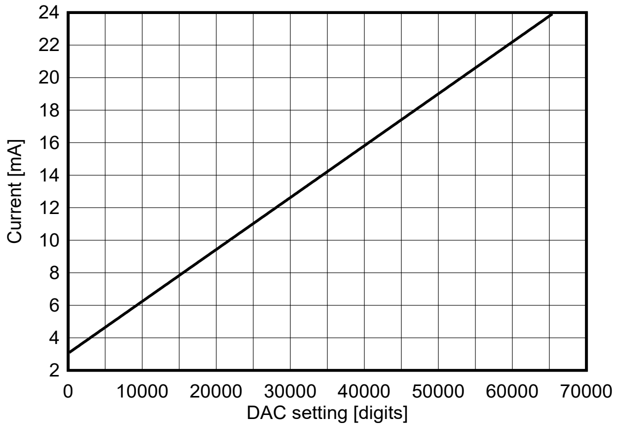


Figure 4-15. AFE882: 3.3V Supply, 24V Loop Linearity
y = 3.19127E–04x + 3.04673

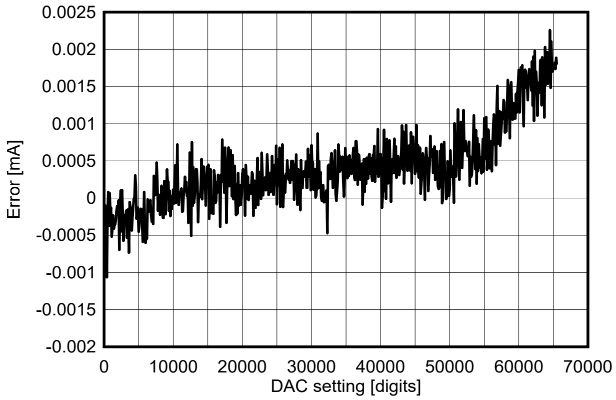


Figure 4-16. AFE882: 3.3V Supply, 24V Loop Error

4.3.1.1 Linearity Tests Summary

For all configurations, all results are well within the specification and no configuration shows signs of instability or other non-linear effects. With the AFE881 device, similar performance can be achieved with a 1.8V supply as with a 3.3V supply.

4.3.2 Noise Tests and Current Histogram

For this test, the test setup is similar to Section 4.3.1. For measuring the performance, the DAC is set to three different output currents (zero [minimum], midpoint, maximum) and the resulting current is measured 8192 times. From these values, the histogram is plotted, the other parameters are calculated from these readings.

Figure 4-17 shows the complete setup.

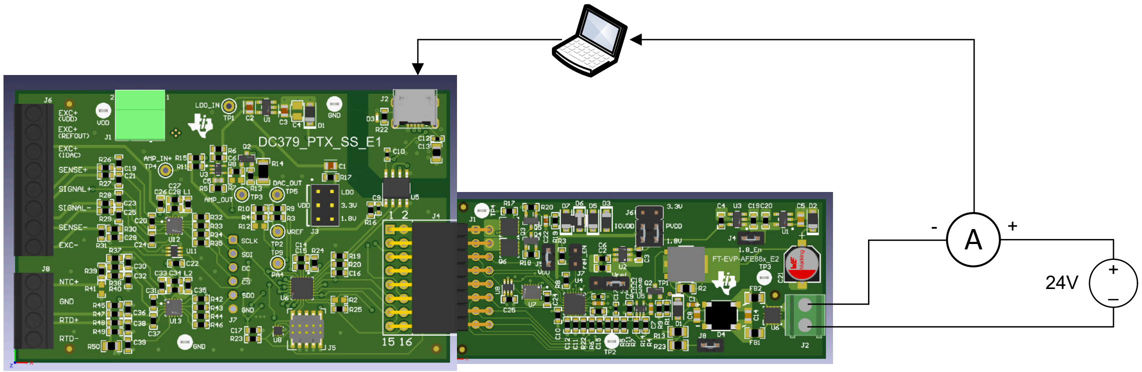


Figure 4-17. Test Setup Current Noise

Figure 4-18 through Figure 4-26 show the histogram of the measured current.

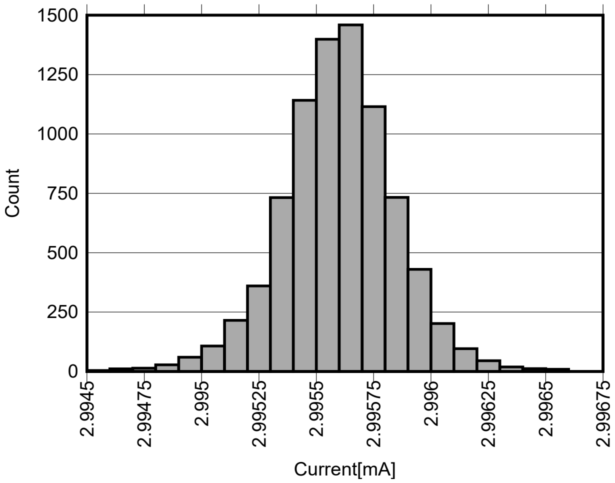


Figure 4-18. Histogram AFE881 Powered With 1.8V, Minimum DAC Setting

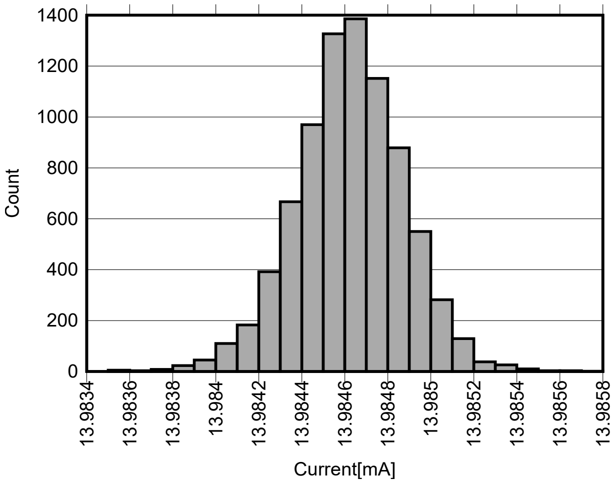


Figure 4-19. Histogram AFE881 Powered With 1.8V, Midpoint DAC Setting

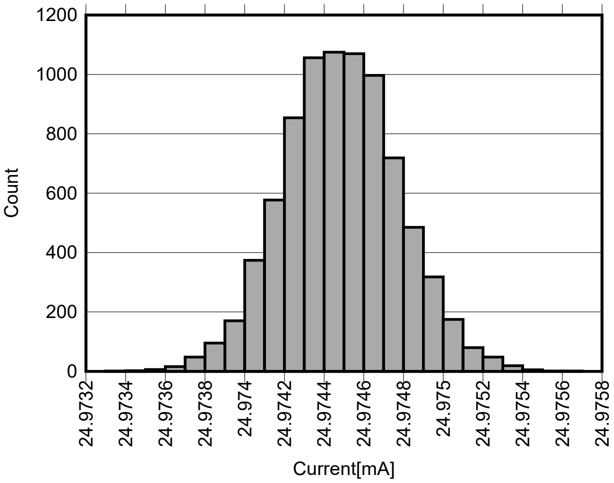


Figure 4-20. Histogram AFE881 Powered With 1.8V, Maximum DAC Setting

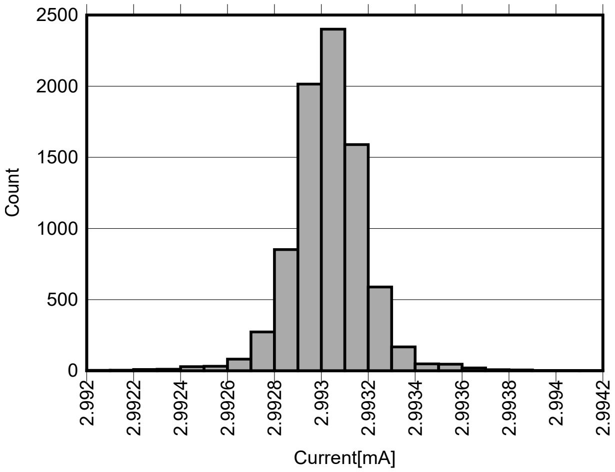


Figure 4-21. Histogram AFE881 Powered With 3.3V, Minimum DAC Setting

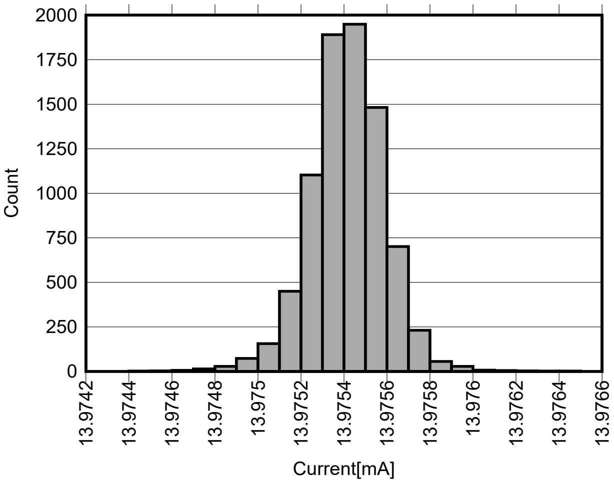


Figure 4-22. Histogram AFE881 Powered With 3.3V, Midpoint DAC Setting

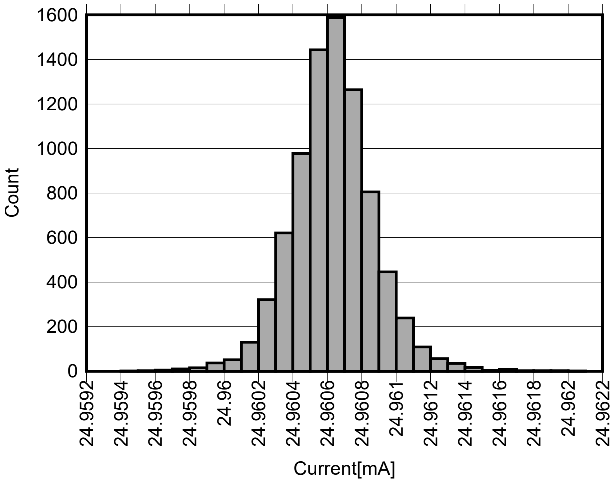


Figure 4-23. Histogram AFE881 Powered With 3.3V, Maximum DAC Setting

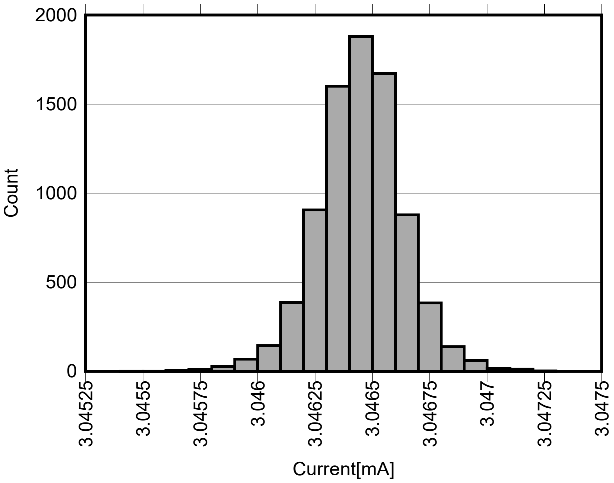


Figure 4-24. Histogram AFE882 Powered With 3.3V, Minimum DAC Setting

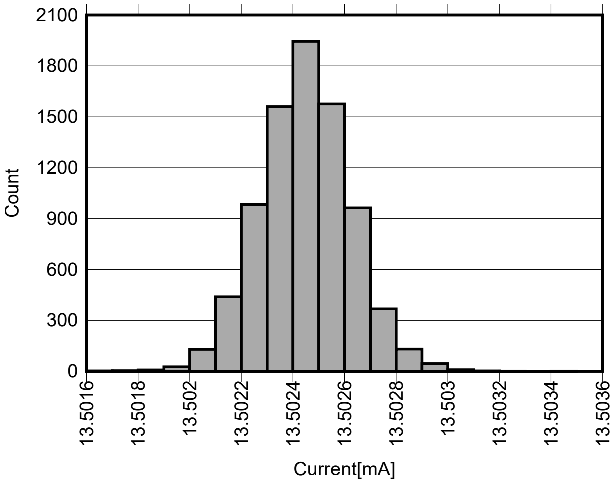


Figure 4-25. Histogram AFE882 Powered With 3.3V, Midpoint DAC Setting

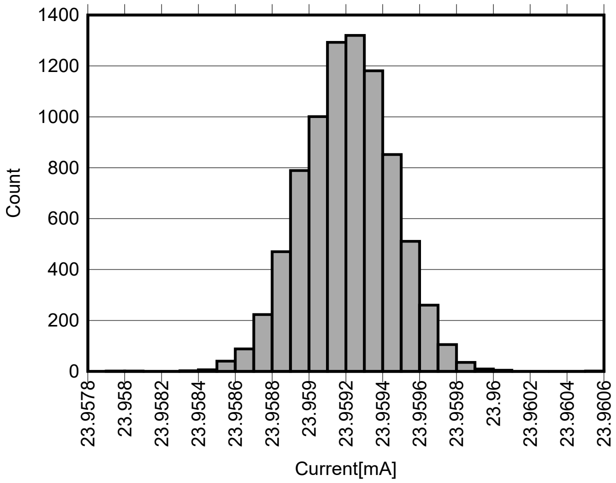


Figure 4-26. Histogram AFE882 Powered With 3.3V, Maximum DAC Setting

4.3.2.1 Noise Tests and Current Histogram Summary

Table 4-3 shows the calculated results from the raw data in Figure 4-18 through Figure 4-26.

Table 4-3. Noise Summary

AFE	SUPPLY (V)	DAC SETTING	MINIMUM CURRENT (mA)	AVERAGE CURRENT (mA)	MAXIMUM CURRENT (mA)	PEAK-TO-PEAK NOISE (µA)	RMS NOISE (nA)	NOISE-FREE BITS (NFB)	EFFECTIVE NUMBER OF BITS (ENOB)
AFE881	1.8	0	2.9945	2.9956	2.9966	2.05	247	15.6	18.6
AFE881	1.8	32768	13.9836	13.9846	13.9858	2.19	250	15.5	18.6
AFE881	1.8	65535	24.9734	24.9745	24.9757	2.25	289	15.4	18.4
AFE881	3.3	0	2.9920	2.9930	2.9942	2.15	160	15.5	19.3
AFE881	3.3	32768	13.9744	13.9754	13.9764	2.04	173	15.6	19.1
AFE881	3.3	65535	24.9595	24.9606	24.9621	2.62	239	15.2	18.7
AFE882	3.3	0	3.0455	3.0464	3.0473	1.76	184	15.8	19.1
AFE882	3.3	32768	13.5016	13.5024	13.5035	1.81	173	15.8	19.1
AFE882	3.3	65535	23.9580	23.9592	23.9606	2.6	241	15.2	18.7

Overall, the histogram plots show the expected Gaussian distribution for this type of signal without any oscillation or otherwise disturbed signal. This also proves, the peak currents drawn by the MCU when waking up are not seen on the loop and are regulated properly. There is no performance difference between a 1.8V and 3.3V signal chain.

4.3.3 Step Response

To test the step response of the circuit, the circuit is again connected to a 24V power supply. Current measurement is done with a current clamp with multiple turns of the loop wire in the clamp to increase the sensitivity.

The step is generated by sending the corresponding DAC values from a PC to the AFE88x. In this test a step from zero to maximum and back as well as midpoint current is performed. This shows the slew rates of the analog circuit and is also testing the stability.

Figure 4-27 shows the complete setup.

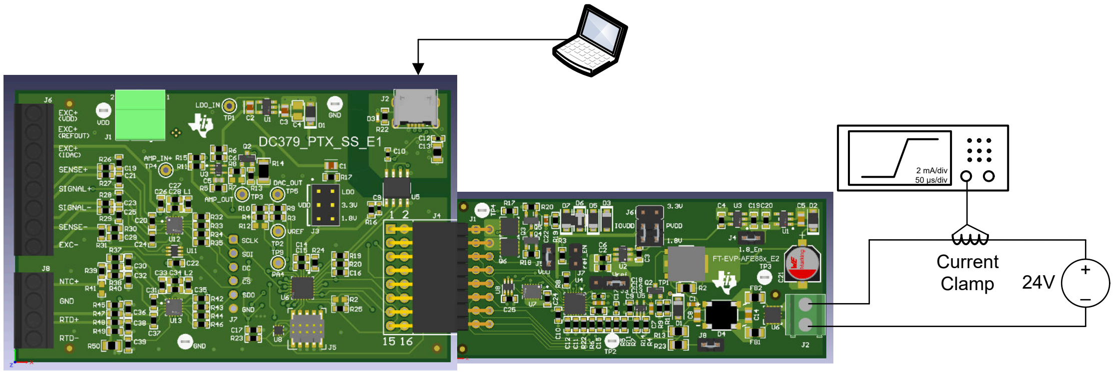


Figure 4-27. Test Setup for Step Response Measurements

The following figures show the step responses of the current.

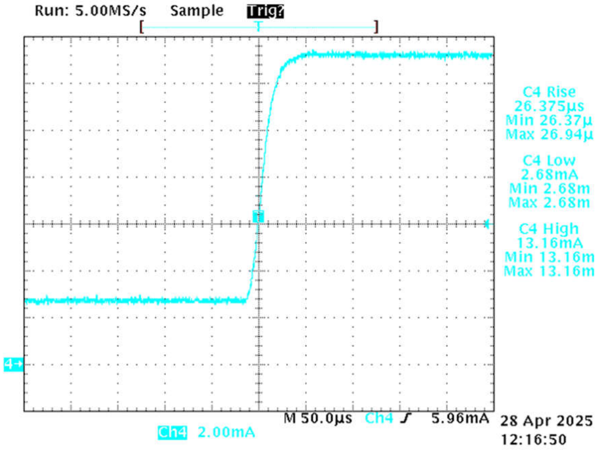


Figure 4-28. AFE881: 3.3V, Rise Time 0 to 65535

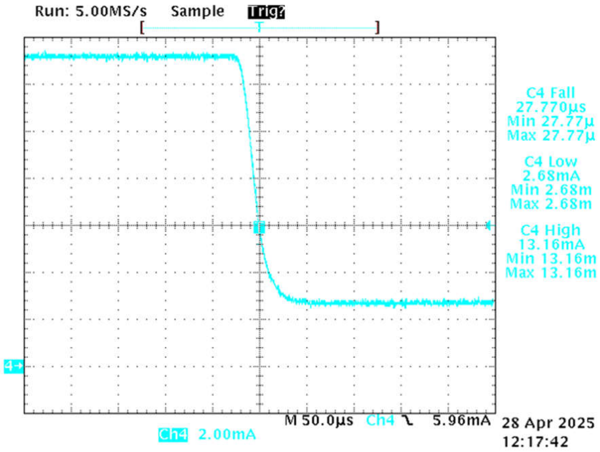


Figure 4-29. AFE881: 3.3V, Fall Time 65535 to 0

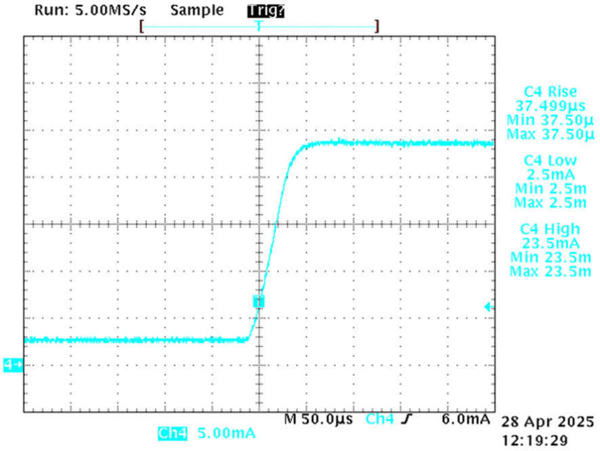


Figure 4-30. AFE881: 3.3V, Rise Time 0 to 32768

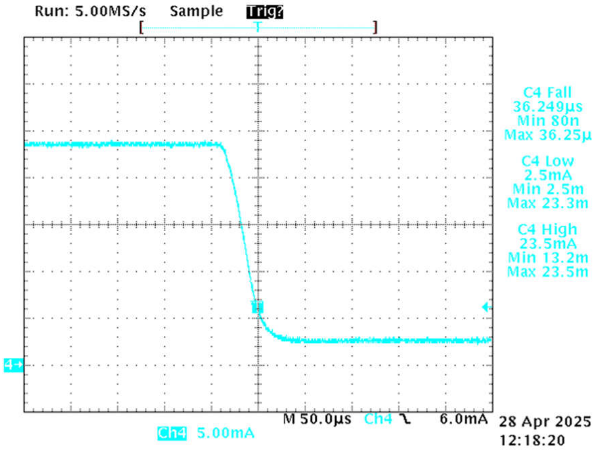


Figure 4-31. AFE881: 3.3V, Fall Time 32768 to 0

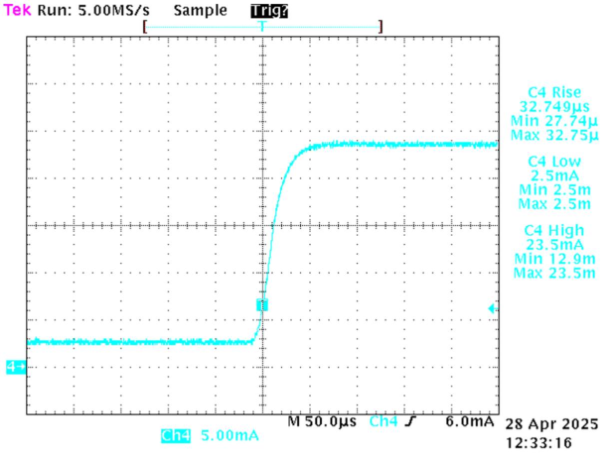


Figure 4-32. AFE881: 1.8V, Rise Time 0 to 65535

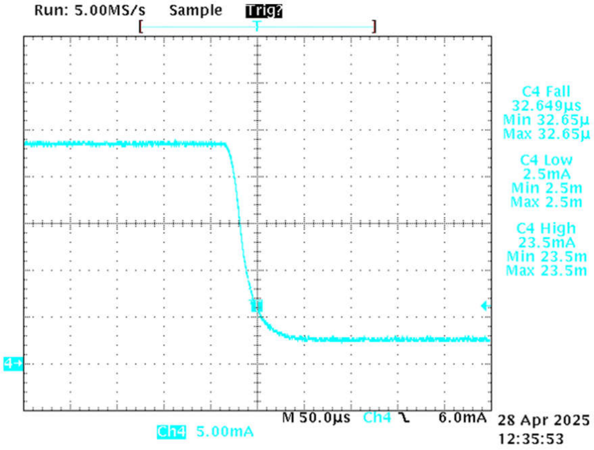


Figure 4-33. AFE881: 1.8V, Fall Time 65535 to 0

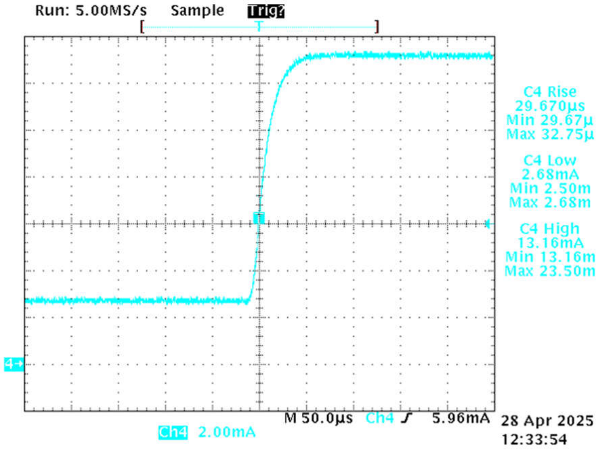


Figure 4-34. AFE881: 1.8V, Rise Time 0 to 32768

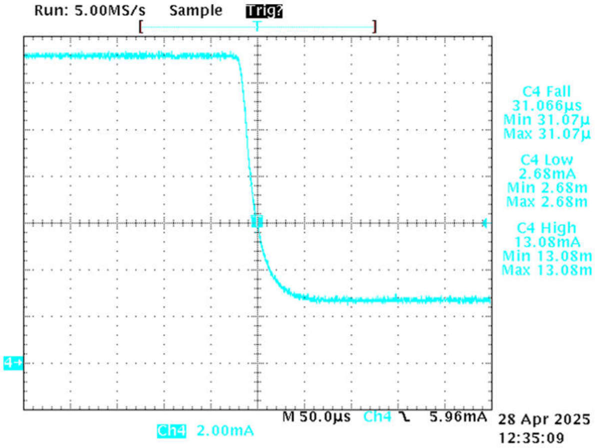


Figure 4-35. AFE881: 1.8V, Fall Time 32768 to 0

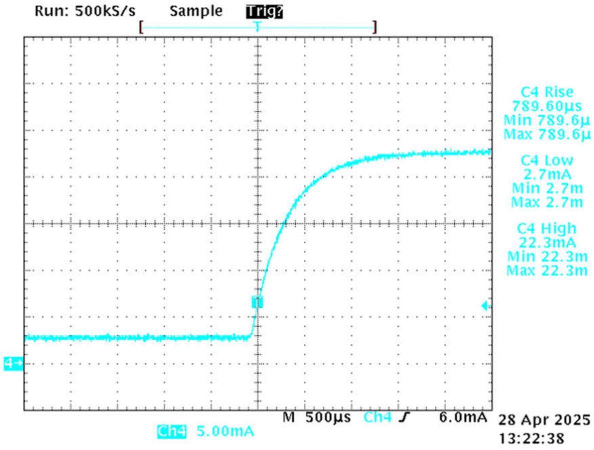


Figure 4-36. AFE882: 3.3V, Rise Time 0 to 65535

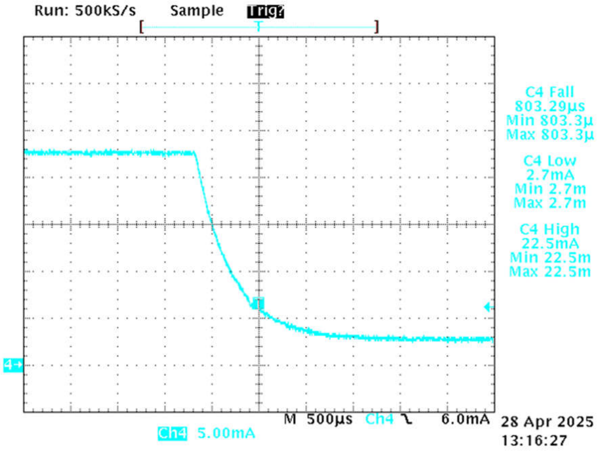


Figure 4-37. AFE882: 3.3V, Fall Time 65535 to 0

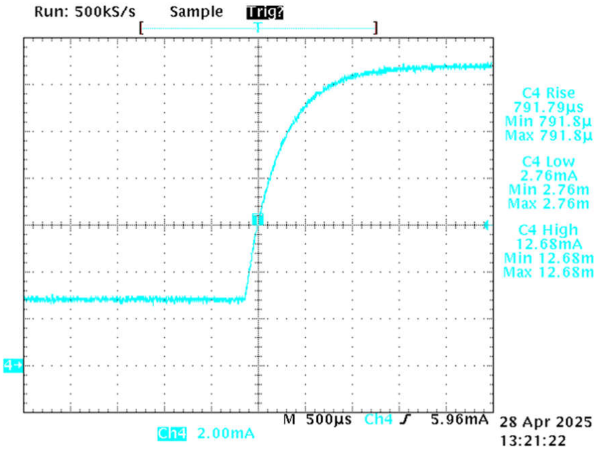


Figure 4-38. AFE882: 3.3V, Rise Time 0 to 32768

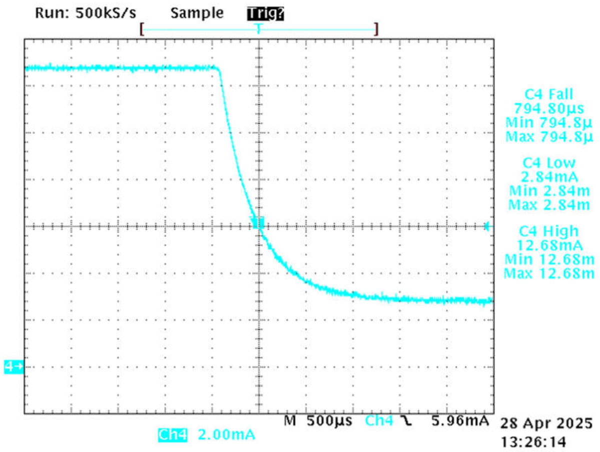


Figure 4-39. AFE882: 3.3V, Fall Time 32768 to 0

4.3.3.1 Step Response Summary

Table 4-4 shows a summary of the rise and fall times. The AFE882H1 hardware is designed to have slower rise and fall times. Nevertheless, the plots show there are no overshoots, undershoots, or oscillations.

Table 4-4. Rise Time and Fall Time Summary

AFE	SUPPLY (V)	DAC SETTING	RISE TIME (µs)	FALL TIME (µs)
AFE881	3.3	65535	26	28
AFE881	3.3	32768	38	36
AFE881	1.8	65535	33	33
AFE881	1.8	32768	30	31
AFE882	3.3	65535	790	803
AFE882	3.3	32768	792	795

4.3.4 Start-Up

Investigating the start-up behavior of the system is also interesting. Especially determining if the minimum current of less than 4mA can be maintained during the whole start-up phase and how long the start-up phase takes. Figure 4-40 shows how the start-up is monitored in a first step.

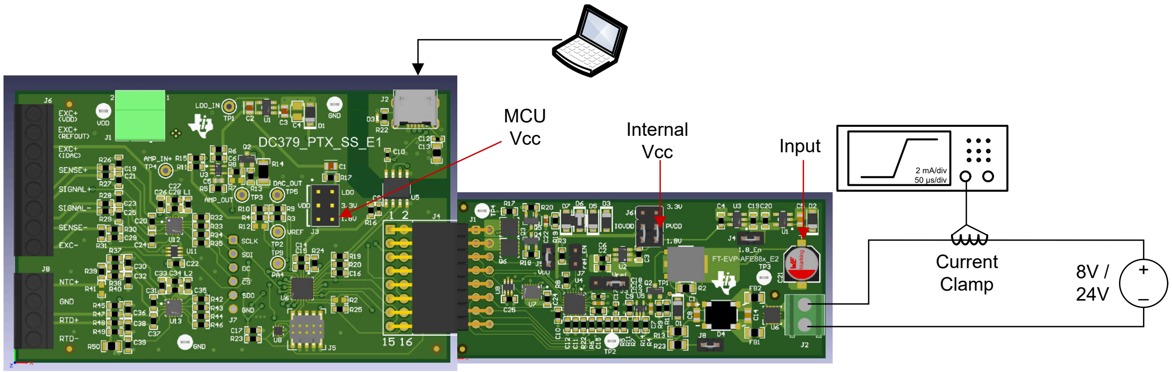


Figure 4-40. Test Setup for Start-Up Measurements

Taking a measurement using the configuration in Figure 4-40 yields the scope picture illustrated in Figure 4-41.

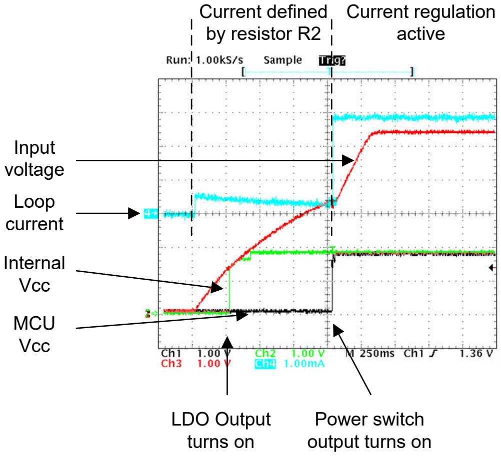


Figure 4-41. AFE881 1.8V to 8V Loop Voltage Start-Up

Figure 4-42 shows why the current looks as measured. The current at the very beginning is defined only by the bypass resistor R2, which is the only part allowing current flow before the internal voltage is up and the amplifier is powered and regulating the current.

After 250ms the voltage is high enough, so that the LDO turns on and provides 1.8V internally. After 750ms more, the internal power switch turns on. This switch monitors the intermediate 3.3V rail to be stable and adds some delay. Turning on enables the MCU and the IO rail of the AFE. This allows the AFE to leave the power on reset and the current regulation begins, though the measured input current steps to 3mA.

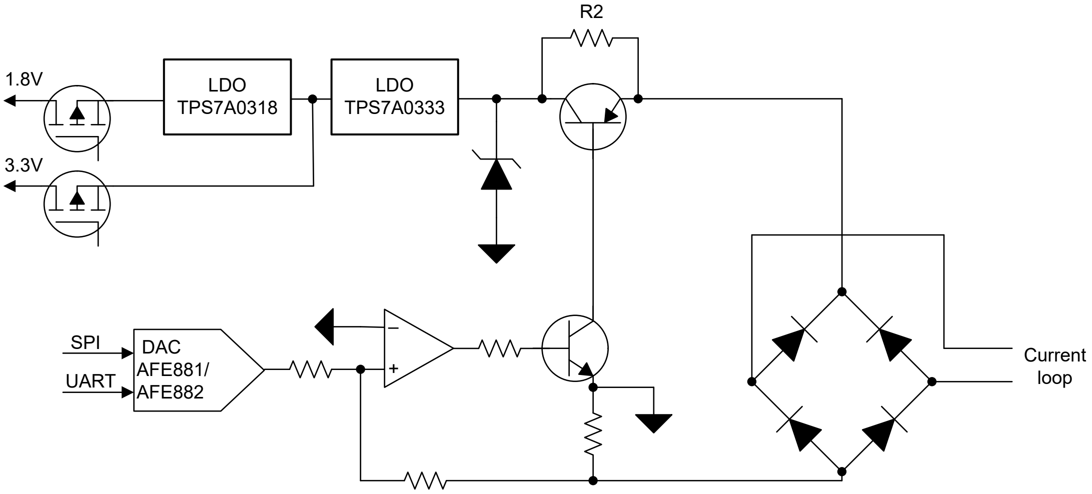


Figure 4-42. Simplified Schematic

With a supply of 24V the system starts up much faster, as this initial current is higher. Figure 4-43 shows the same measurement as before but with 24V loop voltage. The current at the beginning of power up sequence is approximately 2mA. The MCU completes the full start-up process in about 150ms.

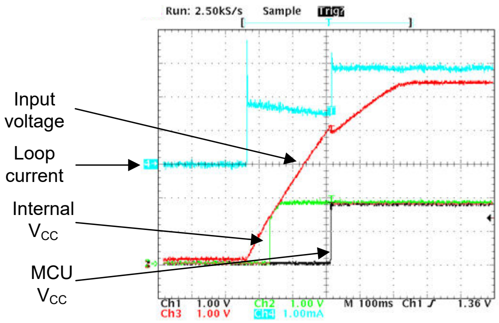


Figure 4-43. AFE881 1.8V to 24V Loop Voltage Start-Up

Figure 4-44 to Figure 4-47 show the same test for different configurations.

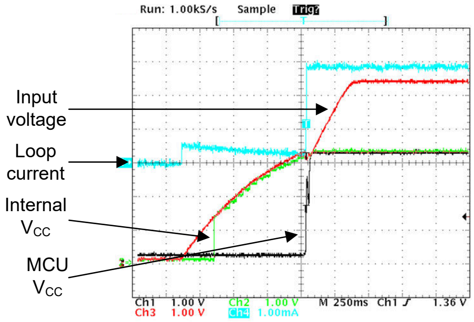


Figure 4-44. AFE881: 3.3V to 8V Loop Voltage Start-Up

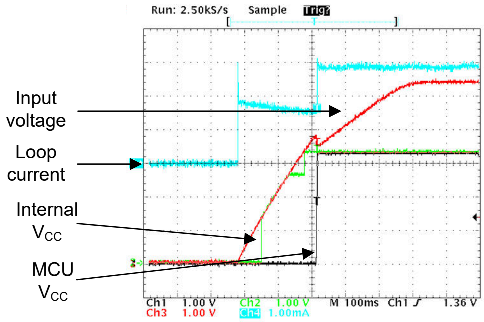


Figure 4-45. AFE881: 3.3V to 24V Loop Voltage Start-Up

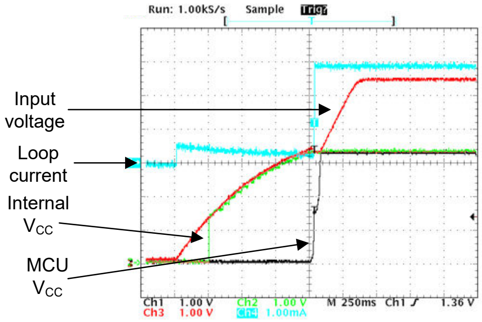


Figure 4-46. AFE882: 3.3V to 8V Loop Voltage Start-Up

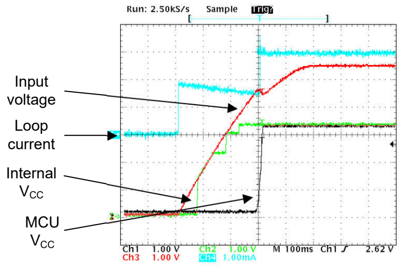


Figure 4-47. AFE882: 3.3V to 24V Loop Voltage Start-Up

4.3.5 MCU Current

Besides the start-up behavior and currents, it is interesting to closely examine the current profile of the microcontroller.

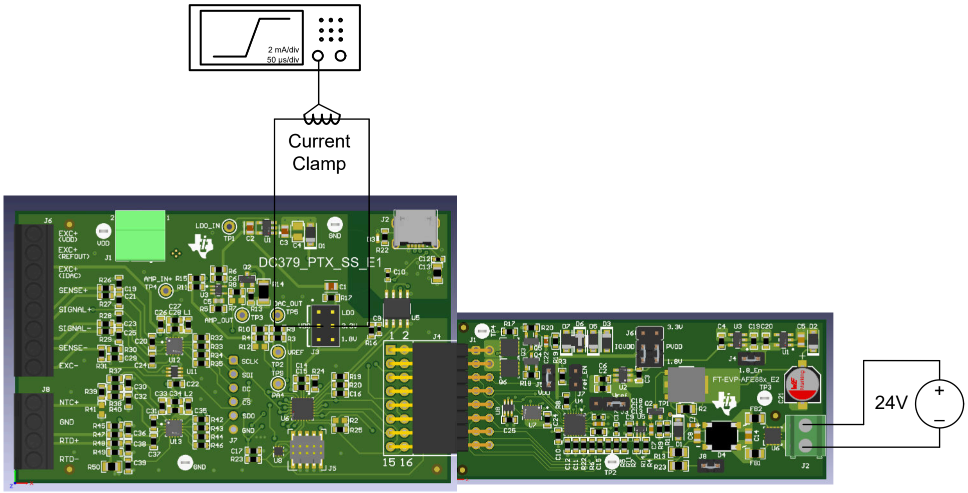


Figure 4-48. Test Setup for MSPM0 Current Consumption

Figure 4-48 shows the setup for this measurement. The system is powered as usual from 24V and the current going into the MCU is measured using a current clamp directly on the MCU board. Only the MCU and the bypass capacitors are included in the measurement.

Figure 4-49 through Figure 4-52 show the inrush current of the MSPM0 under different conditions and zoom factors.

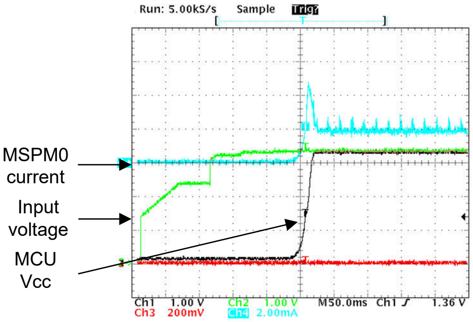


Figure 4-49. MSPM0 Start-Up 3.3V Supply

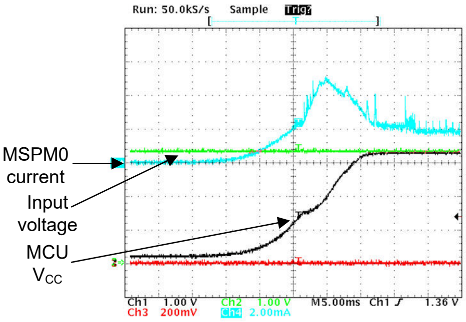


Figure 4-50. MSPM0 Start-Up 3.3V Supply - Detail

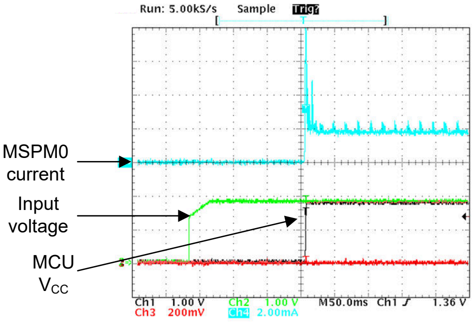


Figure 4-51. MSPM0 Start-Up 1.8V Supply

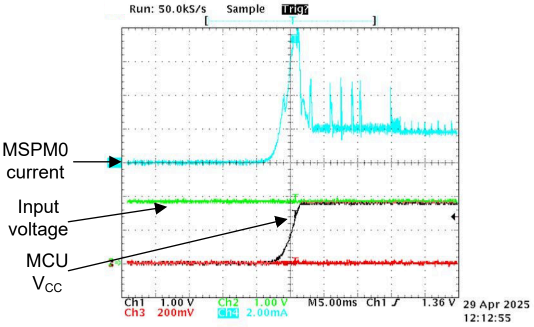


Figure 4-52. MSPM0 Start-Up 1.8V Supply - Detail

4.3.5.1 MCU Current Summary

In Figure 4-49 through Figure 4-52, the measurements show the inrush current of the MSPM0 circuit easily exceeds 4mA. This current peak is not visible at the input of the complete system and does not interfere with the current regulation circuit.

4.3.6 System Currents

To see which parts of the system contribute to the power consumption, the currents in different rails are measured. In 3.3V configuration, the AFE881 uses the internal voltage reference and an internal LDO to create VDD from PVDD, whereas in 1.8V configuration, an external reference voltage is used and the VDD supply is provided from the 1.8V rail of the system.

Figure 4-53 shows where on the board the currents are measured. Figure 4-54 shows that in 1.8V configuration, one more rail is measured.

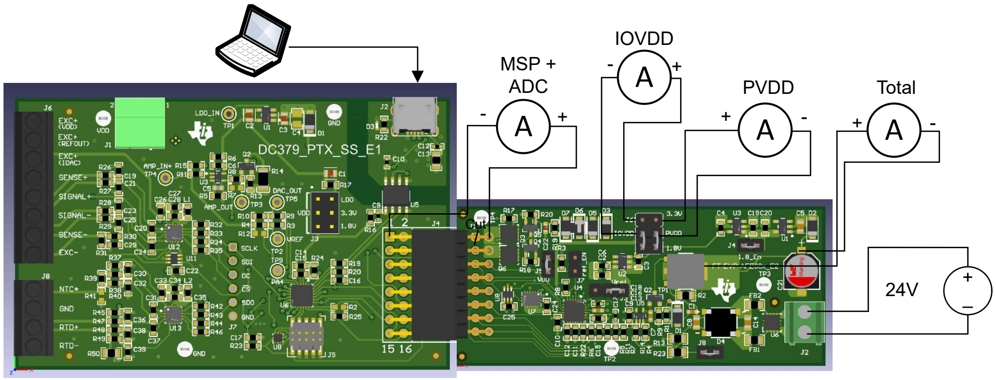


Figure 4-53. Test Setup for Current Measurements: 3.3V

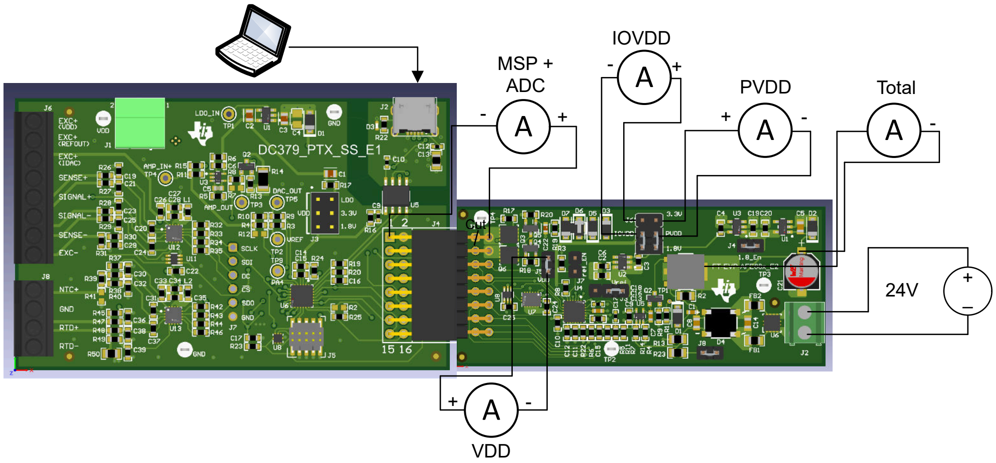


Figure 4-54. Test Setup for Current Measurements: 1.8V

Figure 4-55 shows the connection of major components and power rails.

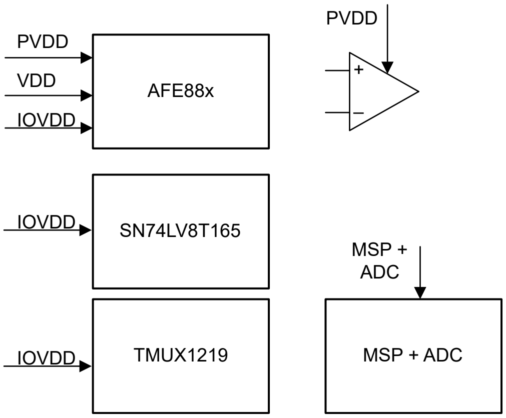


Figure 4-55. Simplified Power Tree

4.3.6.1 Summary of System Currents

Table 4-5 shows the measured currents in different configurations. The total current in the table is the measured total current going into the system measured between the loop driving transistor and the input of the LDO. The total measured current also includes all current not measured separately, for example the quiescent current of the LDOs and reference voltage.

Table 4-5. Measured Currents in Different Configurations

AFE	SUPPLY (V)	DAC SETTING	P_{VDD} (µA)	IOVDD (µA)	MSP + ADC (mA)	VDD (µA)	TOTAL (mA)
AFE882	3.3	0	200	1.2	1.958	NA	2.214
	3.3	32768	217	1.2	1.958	NA	2.231
	3.3	65535	230	1.2	1.958	NA	2.244
AFE881	3.3	0	192	1.1	1.99	NA	2.266
	3.3	32768	203	1.1	1.99	NA	2.276
	3.3	65535	216	1.1	1.99	NA	2.289
	1.8	0	50	0.6	1.92	89	2.135
	1.8	32768	55.5	0.6	1.92	89	2.140
	1.8	65535	61.3	0.6	1.92	89	2.146

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010982.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010982.

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010982.

5.2 Tools and Software

Tools

AFE881H1EVM	AFE881H1 evaluation module for a 16-bit, voltage-output, precision DAC and 16-bit ADC
AFE882H1EVM	AFE882H1 evaluation module for a 16-bit, voltage-output, precision DAC and 16-bit ADC
LP-MSPM0G3507	MSPM0G3507 LaunchPad™ development kit for 80MHz Arm® Cortex®-M0+ MCU

Software

MSPM0-SDK	MSPM0 software development kit

5.3 Documentation Support

1. Texas Instruments, *AFEx81H1 16-Bit and 14-Bit, Low-Power DACs With Internal HART® Modem, Voltage Reference, and Diagnostic ADC for 4mA to 20mA Loop-Powered Applications Data Sheet*
2. Texas Instruments, *AFEx82H1 16-Bit and 14-Bit, Low-Power Digital-to-Analog Converters (DACs) With Internal HART® Modem, Voltage Reference, and Diagnostic ADC for Process Control Data Sheet*
3. Texas Instruments, *OPAx391 Precision, Ultra-Low I_Q, Low Offset Voltage, e-trim™ Operational Amplifiers Data Sheet*
4. Texas Instruments, *TPS7A03 Nanopower I_Q, 200nA, 200mA, Low-Dropout Voltage Regulator With Fast Transient Response Data Sheet*
5. Texas Instruments, *REF35 Ultra-Low-Power, High-Precision Voltage Reference Data Sheet*
6. Texas Instruments, *TVS3301 33V Bidirectional Flat-Clamp Surge Protection Device Data Sheet*
7. Texas Instruments, *TMUX1219 5V Bidirectional, 2:1 General Purpose Switch Data Sheet*
8. Texas Instruments, *SN74LV8T165 Parallel-Load 8-Bit Shift Registers Data Sheet*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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