Design Guide: TIDA-010256

128-Channel Ultrasound Transmitter System Reference Design

Description

The ultrasound transmission reference design uses TI's TX7516 five-level pulse transmitter and the high-voltage TMUX9832 switch. The transmitter and switch are connected in a 1:4 manner to address the compact hardware design requirements for high channel count ultrasonic analog front end systems. This design also reduces overall power supply size through the adoption of TI's high-efficiency, small-footprint power modules and SEPIC topologies.

Resources

TIDA-010256	Design Folder
TX7516, TMUX9832, TPSM63603	Product Folder
LM5155, TPS7A9401, TPS7A3301	Product Folder
LMK00304, LMK6D	Product Folder
AM2431, DAC53401	Product Folder

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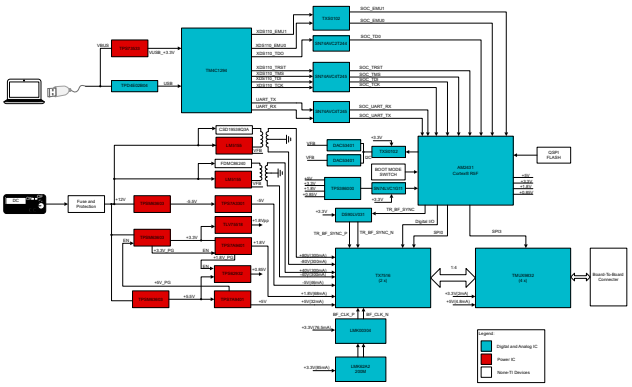
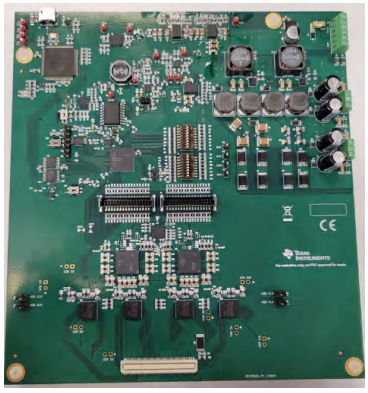
Features

- Small size, 128-channel maximum, ±80V five-level or three-level pulser output with integrated programmable beamformer
- Programmable transistor drive current to optimize second harmonic distortion performance
- Dynamic power management system to optimize transmit power consumption
- One clock cycle can update the state of all switch channels during scans with interwoven input routing topology
- High-voltage circuit with maximum ±80V, 300mA output capability

Applications

- Ultrasound scanner
- Ultrasound smart probe





1 System Description

The principle of ultrasound imaging is based on transmitting a high-voltage pulse to excite the transducer and then receive an echo from the object. The amplitude of the echo signal modulates the light-intensity into an image. In modern ultrasound systems, there are from 1 to 256 transducers and this means the system needs a lot of transmitters. The B-mode imaging system has 16 to 256 transducers in modern ultrasound systems for a larger acoustic aperture, a clearer lateral resolution, and an improved signal-to-noise ratio, as well as for enhanced imaging quality. Figure 1-1 shows a simplified system block diagram.

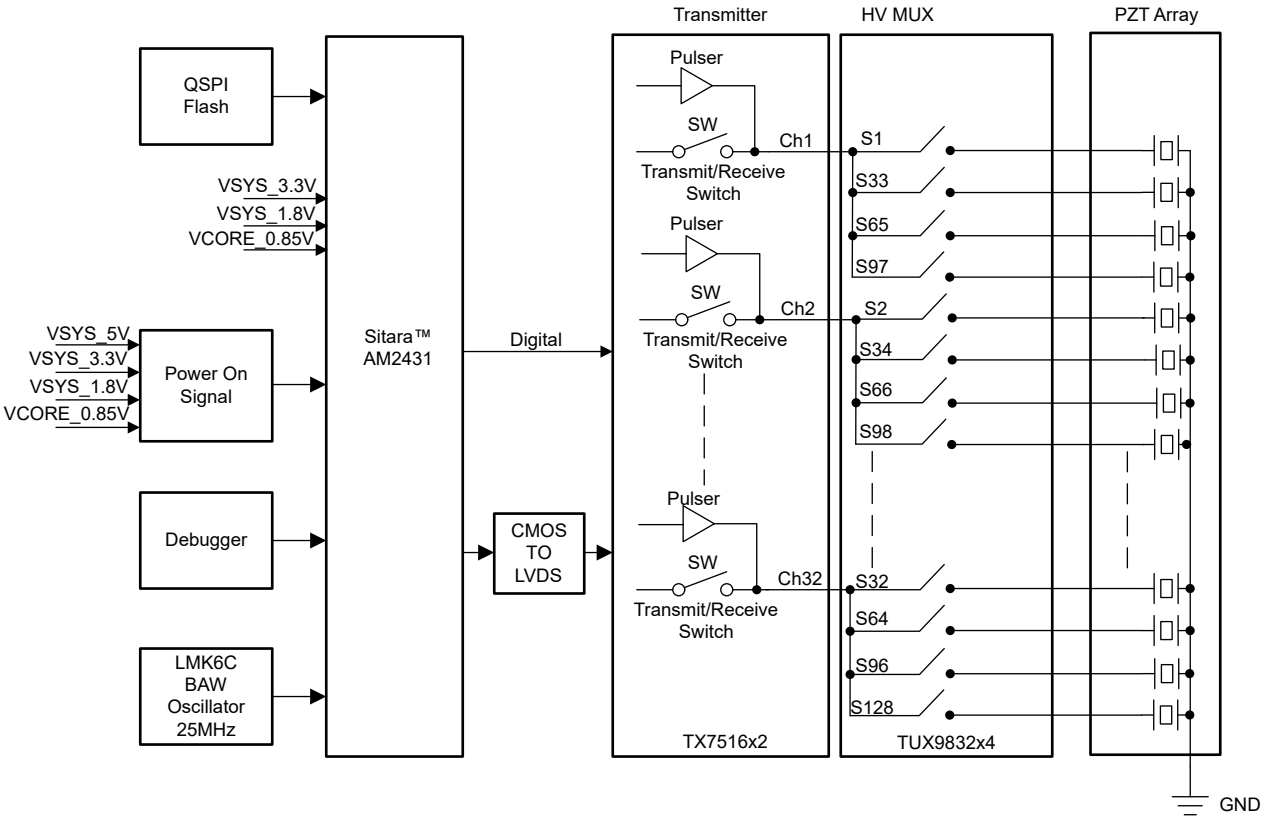


Figure 1-1. Simplified System Block Diagram

The design employs four TMUX9832 devices, which integrate bleed resistors on the drain (Dx) pins to discharge capacitive loads, allowing for a compact interface between the transducers and the front-end main board. TX7516 is a 16-channel transmitter. The design uses two TX7516 devices to reduce the amount of wire and transmitters by approximately 75%.

To simplify the beamforming process, the system incorporates a built-in beamforming pattern generator within the transmitter device (TX7516), which controls pulse transmission through a high-performance general-purpose microcontroller (AM2431). The complex beamforming can be accomplished using only a Serial Peripheral Interface (SPI) with a maximum rate of 50MHz. Additionally, the SPI of the TMUX9832 device can be controlled using the Programmable Real-time Unit (PRU) IO, which supports up to 100MHz for TMUX9832.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
System input voltage (V_{IN})	12V (Power source)	
Switcher output voltage (positive)	5.5V	Power module, no external inductor needs
+5V Output	5V, 800nV_{RMS}, (10Hz–100kHz)	
Switcher output voltage (negative)	–5.5V	Power module, inverting buck topology
–5V Output	–5V, 16.48µV_{RMS}	
TX7516 Supply rails with low-noise LDOs	+5V (800mA), –5V (800mA) 1.8V (400mA)	Surge current (±5V) when floating low dropout (LDO) regulators are powered up. This table only shows the maximum surge current of the TX7516.
Switcher output voltage (digital IO)	0.85V, 1.8V, 3.3V	
High-voltage output	Maximum ±80V(300mA), Maximum ±40V(300mA)	
SEPIC switch frequency	150kHz	Can switch to 100kHz
SEPIC output voltage ripple	1% of the output voltage	
Load resistor	220Ω | 220pF	
BF_CLK input	200MHz	
Beamformer	Yes	On-chip beamformer
Pulser output mode	CW mode, B mode, elastography	
TMUX9832 control mode	Single-ended SPI with daisy chain	
MCU boot mode	QSPI, none-boot, universal asynchronous receiver-transmitter (UART)	
SPI bandwidth	50MHz maximum (SPI peripheral), 100MHz (PRU IO)	

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the overall system block diagram.

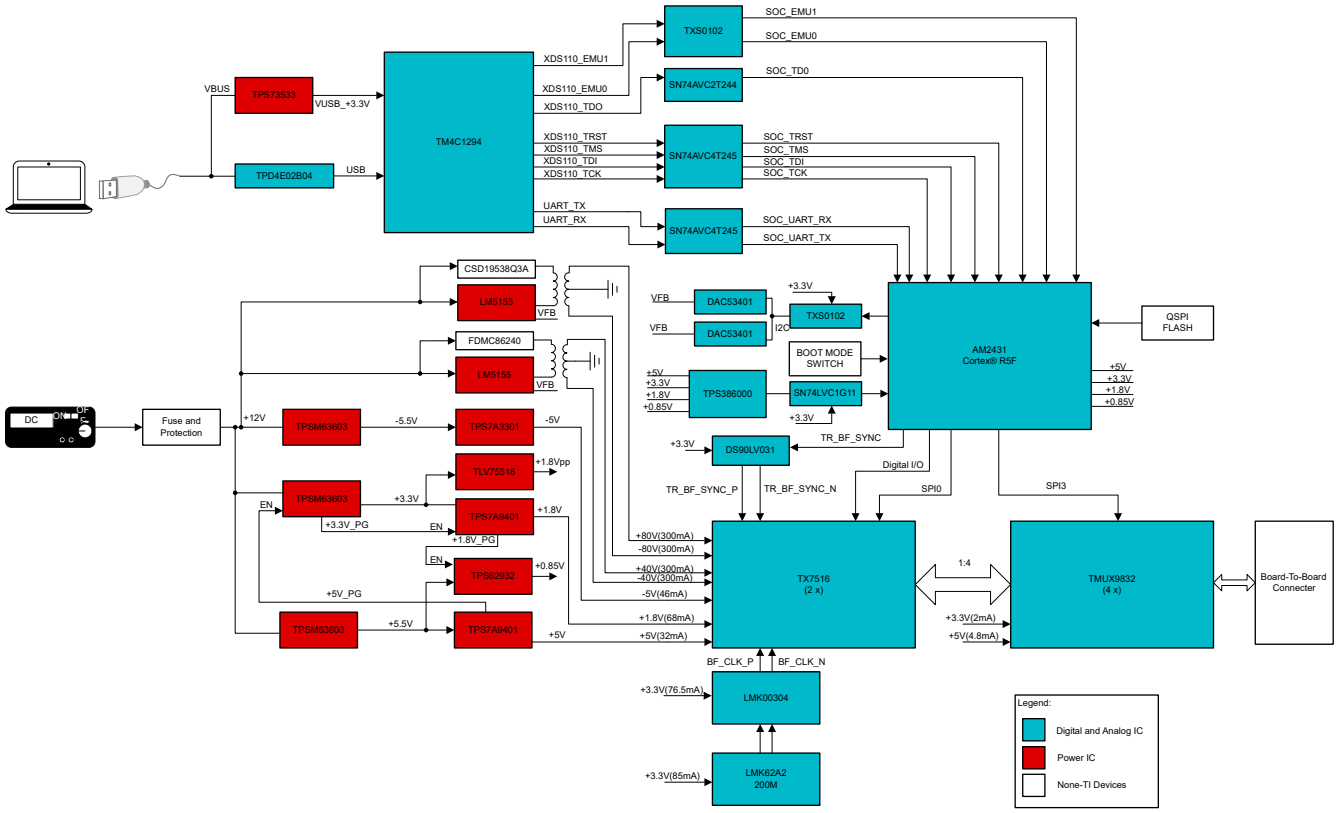


Figure 2-1. TIDA-010256 Overall System Block Diagram

Low voltage power supply (LVPS) is mainly used in microcontrollers, FPGA, digital IO, and analog power supply in ultrasound systems. TI proposes using modules in low-power supply designs for reduced noise, compact size, high efficiency, easy design, low cost, and rapid manufacturing.

TI recommended using TPS63603 module, which offers low noise and high efficiency, converting 12V bus voltage to ±5.5V, 3.3V. For the low voltage supplies for TX7516 and TMUX9832 analog rail, each DC/DC covert is followed by a low noise LDO TPS7A9401 to remove power noise to achieve higher PSRR. In terms of MCU, FPGA core are powered by TPS62932, TLV75518.

TI offers several high-voltage power supply topologies for different ultrasound systems. In handheld or portable ultrasound where the SEPIC and CUK combined high-voltage topologies are designed for those application scenarios due to high efficiency at light load and overall smaller size. In this design, LM5155 non-synchronous boost controller to drive external metal-oxide semiconductor field-effect transistor (MOSFET) to provide four channel high-voltage power output and an external high-voltage input interface is reserved for powering the TX7516 during shear wave elastography tests at high load.

Phase shift (frequency domain) and jitter (time domain) of the clock signal are key parameters that affect ultrasound imaging quality and high phase noise can often cause image artifacts. This is why the design uses high-performance, low-jitter, standard oscillator LMK62A2 (LMK62D recommended for new designs) and ultra-low-jitter buffer LMK00304 provides a low jitter, high quality clock signal to TX7516.

The TMUX output is required to be connected to the load network through board-to-board connectors, the load is in the form of a 220Ω resistor and a 220pF capacitor in parallel.

2.2 Design Considerations

2.2.1 High-Voltage Generator Circuit

Figure 2-2 shows the high-voltage topology. This topology generates the ±80V and ±40V power supply from the 12V bus power supply to power TX7516 through a SEPIC and Cuk circuit. This section mainly introduces SEPIC circuit design procedures (±80V power rail) and key device selection.

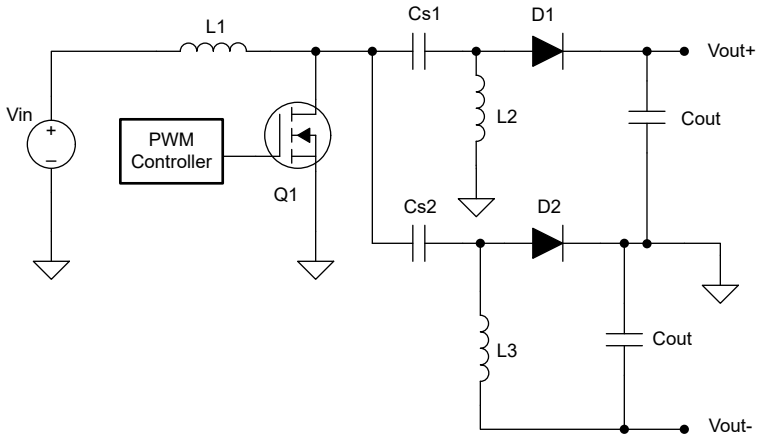


Figure 2-2. High-Voltage Power Supply Topology

Table 2-1. High-Voltage Power Supply Formulas

PARAMETERS	FORMULA	RESULT
Duty Cycle	$D_{max} = \frac{V_{out} + V_d}{V_{inmin} + V_{out} + V_d}$	87.3% where • $V_d \cong 0.7V$ • $V_{inmin} = 11.7V$
Switch Frequency	According to the *maximum duty cycle vs frequency* graph of the *LM5155x 2.2MHz Wide Input Nonsynchronous Boost, SEPIC, Flyback Controller* data sheet, the switching frequency can be as low as 100kHz.	150kHz, 100kHz
Inductor	$L1 = L2 = L3 = \frac{V_{inmin} \times V_{inmax} \times D_{max}}{2 \times I_{out} \times V_{out} \times 0.4 \times f_{SW}} = 42.55\mu H.\ n = 0.88$ $I(L1_{peak}) = \frac{I_{out} \times (V_{out} + V_d) \times \left(1 + \frac{0.4}{2}\right)}{V_{inmin} \times n} = 2.81A$ $I(L2_{peak}) = I_{out} \times \left(1 + \frac{0.4}{2}\right) = 0.36A$	L1 = 47µH, DCR = 0.0459Ω, and I_{sat} = 3.8A L2 = 47µH, DCR = 0.095Ω, and I_{sat} = 1.45A
Power MOSFET Q1	$V_{peak} = V_{in} + V_{out} + V_d = 12 + 100 + 0.7 = 112.7V$ $I_{Q1RMS} = I_{out} \times \sqrt{\frac{(V_{out} + V_{min} + V_d) \times (V_{out} + V_d)}{V_{inmin}^2}} = 2.21A$ $P_{Q1} = I_{Q1RMS}^2 \times R_{DS(on)} \times D_{max} + (V_{inmin} + V_{out}) \times I_{Q1peak} \times \frac{Q_{GD} \times f_{sw}}{I_G} = 0.249W$	FDMC86240 150V, 4.6A MOSFET $T_{J(MAX)}$ = 150°C > T_J where • $R_{DS(on)}$ = 0.0447Ω • Q_{GD}= 2.3nC • I_G = 1.5A • $T_J = P_{Q1} \times R_{\theta JA} + T_A = 0.249 \times 53 + 25 = 38.197°C$
Diode D1, D2	$V_{reverse} \geq V_{inmax} + V_{outmax} = 92V$ $I_{peak} \geq I_{L1peak} + I_{L2peak} = 3.17A$ $P_d = I_{out} \times V_d = 0.21W$	MBRS4201T3G Schottky, 200V, 4A where • V_d = 0.7V

Table 2-1. High-Voltage Power Supply Formulas (continued)

PARAMETERS	FORMULA	RESULT
Coupling Capacitor Cs1, Cs2	$I_{cprmsmax} = I_{out} \times \sqrt{\frac{V_{out} + V_d}{V_{inmin}}} = 0.788A$ If target ripple in C_s < 0.8V, then according to the following equations: $\Delta_{cp} \leq \frac{I_{out} \times D_{max}}{C_s \times f_{SW}} + ESR \times \max\left(Il1peak,\ Il2peak\right)$ $C_s \text{ must be} \geq \frac{I_{out} \times D_{max}}{\Delta_{cp} \times f_{SW}} = 2.182\mu F$ $ESR \leq \frac{\Delta_{cp}}{\max(Il1peak,\ Il2peak)} = 285m\Omega$	$C_{s1} = C_{s2} = 2.2\mu F$
Output Capacitor	$I_{cout,\,RMS} = I_{out} \times \sqrt{\frac{D_{max}}{1 - D_{max}}} = 0.787A$ If target ripple in C_{out} < V_{out} × 1%, then according to the following equations: $C_{out} \text{ must be} \geq \frac{I_{out} \times D_{max}}{\Delta_{cout} \times f_{SW}} = 2.18\mu F$ $ESR \leq \frac{\Delta_{cout}}{Il1peak + Il2peak} = 252m\Omega$	18122C105JAT2A × 2 200V
Input Capacitor	$C_{inmin} = \frac{\frac{P_{out}}{V_{supplymin}} \times \left(1 - D\right)}{\Delta_{Vsupply} \times f_{SW}} = 6.95\mu F$	10µF, 25Vdc where • $\Delta_{Vsupply}$ = 0.25V
Compensation	R_{FBB} = 11kΩ, R_{FBT} = 618kΩ $F_{RHPZ} = \frac{(1 - D_{max})^2 \times V_{out}}{2\pi D_{max} \times L_2 \times 0.5 \times I_{out}} = 33.37kHz$ $F_R = \frac{1}{2\pi\sqrt{L_2 \times C_s}} = 15.651kHz$ $F_{cross} = \frac{F_R}{6} = 2.608kHz$ $R_{comp} = \frac{2\pi \times C_{out} \times R_s \times V_{out}^2 \times F_{cross} \times \left(1 + Dmax\right)}{G_{comp} \times g_m \times V_{inmin} \times Dmax}$ $= \frac{2 \times \pi \times 2.2 \times 10^{-6} \times 0.01 \times 80 \times 80 \times 2608 \times 1.873}{0.142 \times \frac{2mA}{V} \times 11.7 \times 0.873} = 1.49k\Omega$ $F_{Z\_EA} = \sqrt{F_{cross} \times \frac{1}{\pi \times C_{out} \times \frac{V_{out}}{I_{out}}}} = 1189.55Hz$ $C_{comp} = \sqrt{\frac{C_{out} \times \frac{V_{out}}{I_{out}}}{4\pi R_{comp}^2 \times F_{cross}}} = 89.79nF$ $C_{HF} = \frac{C_{comp} \times L_2}{C_{comp} \times (1 - Dmax)^2 \times \frac{Vout}{Iout} \times R_{comp} - L2} = 7.39nF$	R18 = 1.5kΩ C26 = 100nF C25 = 6.8nF R_s = 10mΩ

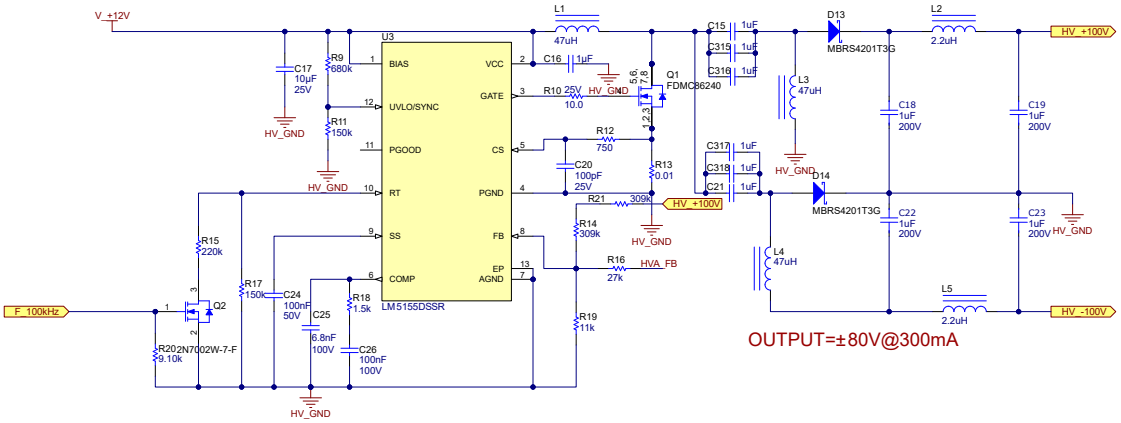


Figure 2-3. 80V High-Voltage Power Supply Schematic

The ±40V high-voltage output channel calculation is also referenced from the table. In addition, for more convenient regulation of the output voltage, a 10-bit DAC53401 is used to control the positive voltage feedback loop of the SEPIC. Figure 2-4 shows the DAC trim circuit for a ±80V output channel.

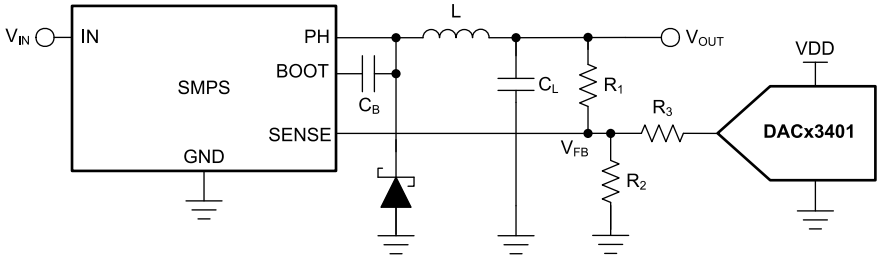


Figure 2-4. DACx3401 Power Supply Control

The DAC53401 features a Hi-Z power-down mode that is set by default at power-up, unless the device is programmed otherwise using the non-volatile memory. When the digital-to-analog converter (DAC) output is at Hi-Z, the current through R3 is zero and SEPIC is set to the nominal output voltage, also to avoid no current flowing through R3 during power up of the DAC. Use Equation 1 to calculate the value of R3 assuming a current limit of 10µA.

$$R_3 = \frac{|V_{DACmax} - V_{FB}|}{I_{set}} = \frac{\frac{1000}{1024} \times 1.21 \times 3 - 1}{10\mu A} = 25.45k \quad (1)$$

where

- DAC code is limited to 1000
- Internal reference = 1.21V
- Gain = 3
- R3 select 27kΩ

Based on Equation 2, assuming the output code of the DAC is 0 when R_B is 11kΩ, R_T can be calculated as 618kΩ. When the DAC code is 1024, the calculated output voltage becomes negative; therefore, restrict the maximum value of DAC code to 924, which yields an output voltage of approximately 5.09V.

$$V_{OUT} = \left(1 + \frac{R_T}{R_B} + \frac{R_T}{R_3}\right) \times V_{ref} - \frac{R_T}{R_3} \times \frac{Code}{1024} \times V_{DACref} \times Gain \quad (2)$$

2.2.2 Low-Voltage Switching Mode Power Supply

The TPSM63603 synchronous buck power module is a highly integrated 36V, 3A, DC/DC device that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for VIN and VOUT located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

TPSM63603 module design can be done quickly based on WEBENCH® circuit design and selection simulation services with corresponding input parameters shown in Table 2-2.

Table 2-2. WEBENCH® Simulation Parameters of 5.5V Power Rail

PARAMETERS	TYPICAL VALUE	WEBENCH INPUT
DC input	12V	V_{inmin} = 11.7V, V_{max} = 12V
Output voltage	+5.5V	5.5V
Output voltage ripple	As low as possible	±5%
Output current	3A	3A
Maximum ambient	–40°C to 105°C	30°C
External sync frequency	Yes	500kHz
Set En_Sync pin to with UVLO	N/A	Yes

Table 2-3. WEBENCH® Simulation Parameters of 3.3V Power Rail

PARAMETERS	TYPICAL VALUE	WEBENCH INPUT
DC input	12V	V_{inmin} = 11.7V, V_{max} = 12V
Output voltage	+3.3V	3.3V
Output voltage ripple	As low as possible	±5%
Output current	3A	3A
Maximum ambient	–40°C to 105°C	30°C
External sync frequency	Yes	500kHz
Set En_Sync pin to with UVLO	N/A	Yes

Figure 2-5 and Figure 2-6 show the schematic resulting from WEBENCH for 5.5V and 3.3V, respectively.

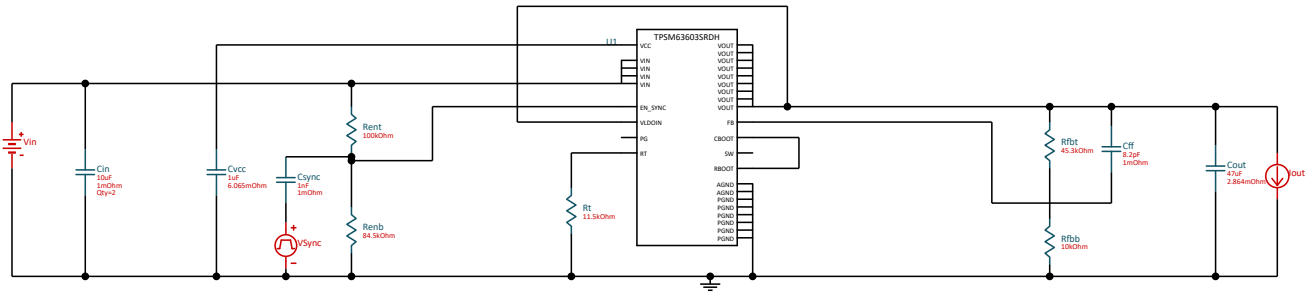


Figure 2-5. Positive 5.5V Power Rail Schematic

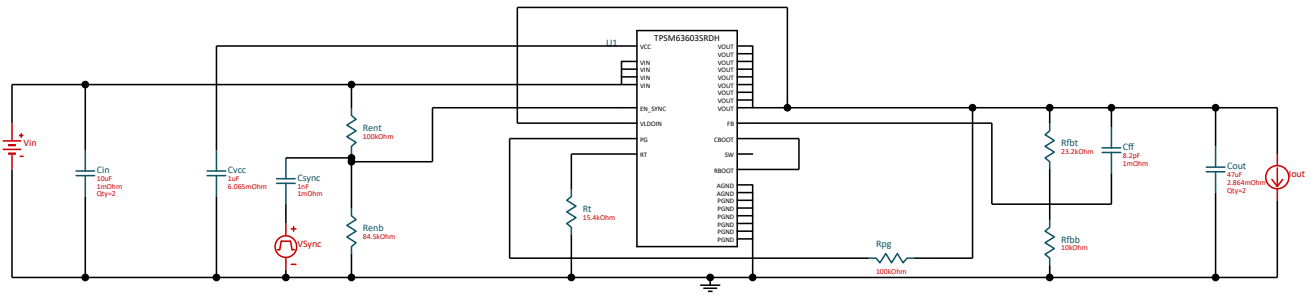


Figure 2-6. Positive 3.3V Power Rail Schematic

Figure 2-7 through Figure 2-10 show the efficiency and output voltage peak-to-peak graphs.

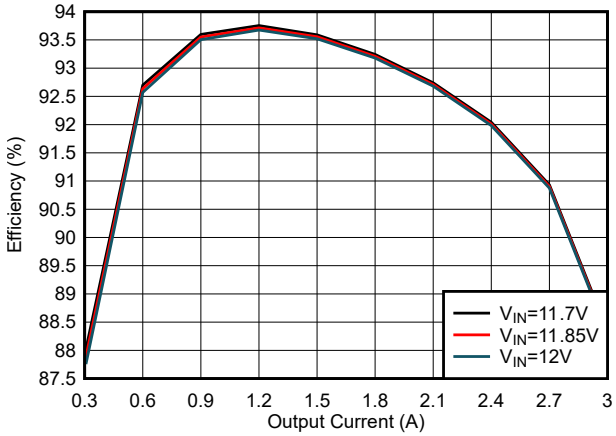


Figure 2-7. Efficiency of 12V to 5.5V

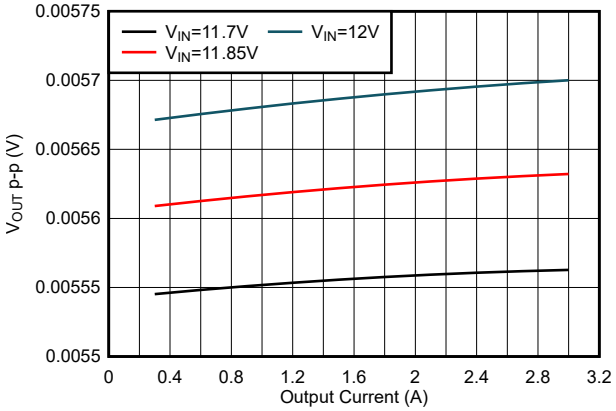


Figure 2-8. V_{p-p} Noise of 12V to 5.5V

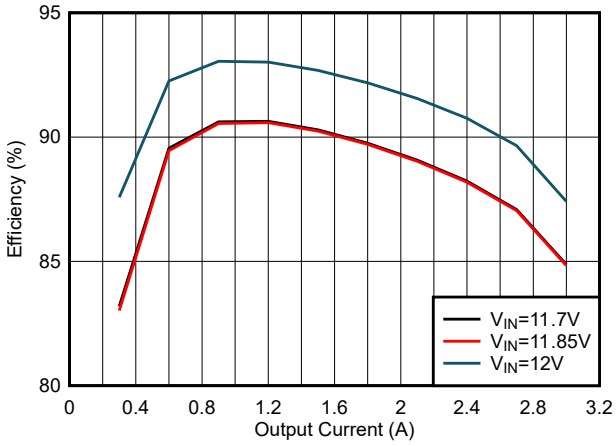


Figure 2-9. Efficiency of 12V to 3.3V

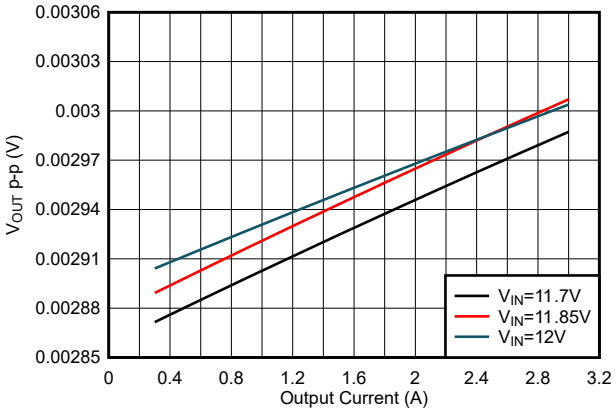


Figure 2-10. V_{p-p} Noise of 12V to 3.3V

The –5.5V output can be designed to the same parameters but needs to be configured as an inverting Buck according to the *inverting buck-boost regulator with a –5V output* section of the *TPSM63603 High-Density, 3V to 36V Input, 1V to 16V Output, 3A Power Module With Enhanced HotRod™ QFN Package* data sheet. Since the switching mode power supply circuits in the ultrasound equipment all require synchronization of the switching frequency, an additional synchronization clock input is required and the –5.5V synchronization signal requires the input level shift. See also the *Working With Inverting Buck-Boost Converters* application note.

The DC/DC output goes to the TPS74001 and TPS733031 LDO devices which help to lower the noise of the analog power supply. The TPS7A94 is an ultra-low-noise (0.46μV_{RMS}), low dropout (LDO) voltage regulator capable of sourcing 1A with only 150mV of dropout and the TPS7A3301 output noise can be lowered to 16μV_{RMS}.

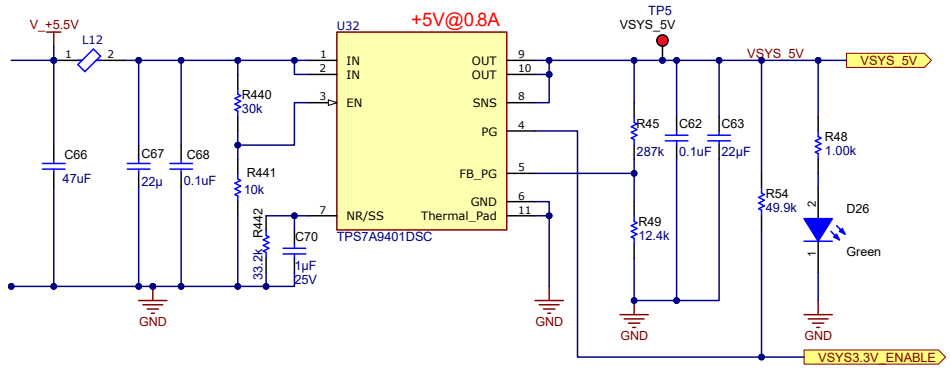


Figure 2-11. Positive 5V Schematic

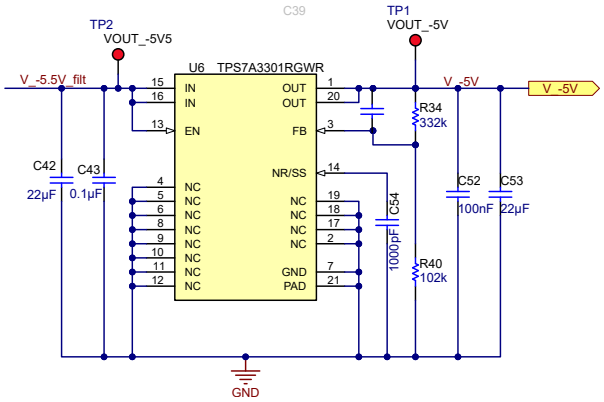


Figure 2-12. Negative 5V Schematic

2.2.3 Sitara™ MCU AM2431 Reset and Power Rail Monitoring Circuit

The AM2431 processor wakeup needs to meet specific power-up sequencing conditions. To avoid errors in the control system from a drop in the system voltage, there is additional circuit to monitor the primary power rail. TPS386000 is an open-drain, quad-supply voltage supervisor with a programmable delay and watchdog timer. Figure 2-13 shows the reset circuit schematic.

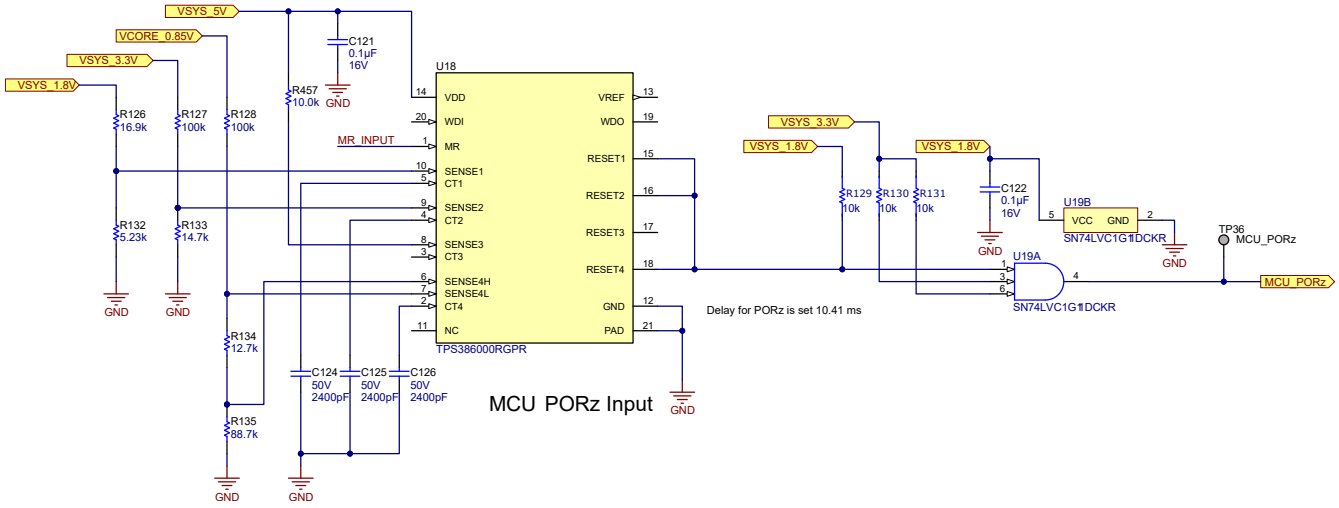


Figure 2-13. Reset Circuit Schematic

When the voltage on the specified SENSEx pin is lower than the V_{ITN} in the data sheet (typically 400mV), the corresponding reset output is asserted. In this design, the threshold voltages are 1.692V for 1.8V and 3.12V for 3.3V.

The CPU core power rail (0.85V), which is highly sensitive to voltage changes, requires additional window monitoring configuration. TPS386000 also supports window voltage monitoring design, such as shown in the schematics, where the window voltages can be calculated using the following formulas.

$$V_{MON(UV)} = \left(1 + \frac{R_{128}}{R_{134} + R_{135}}\right) \times 0.4 = \left(1 + \frac{100}{101.4}\right) \times 0.4 = 0.7956V \quad (3)$$

$$V_{MON(OV)} = \left(1 + \frac{R_{128} + R_{134}}{R_{135}}\right) \times 0.4 = \left(1 + \frac{100 + 12.7}{88.7}\right) \times 0.4 = 0.9082V \quad (4)$$

To program a user-defined adjustable delay time, an external capacitor must be connected between CTn and GND. Use Equation 5 to calculate the adjustable delay time.

$$C_{CT}(nF) = \left[t_{delay(ms)} - 0.5ms\right] \times 0.242 = 2.39822nF \quad (5)$$

where

- t_{delay} = 10.41ms

After the power rail output has been established and stabilized for a predetermined delay time, the output is asserted high with the PORZ signal, which corresponds to the logic level high of the gate logic IC SN74LVC1G11DCKR. Conversely, as soon as any power rail experiences a voltage dropout, the processor is reset.

2.2.4 Clock Generator

The clock plays a crucial role in ultrasound systems, and is constructed with the low-jitter standard oscillator LMK62A2-200M and configurable output clock buffer LMK00304, as Figure 2-14 shows.

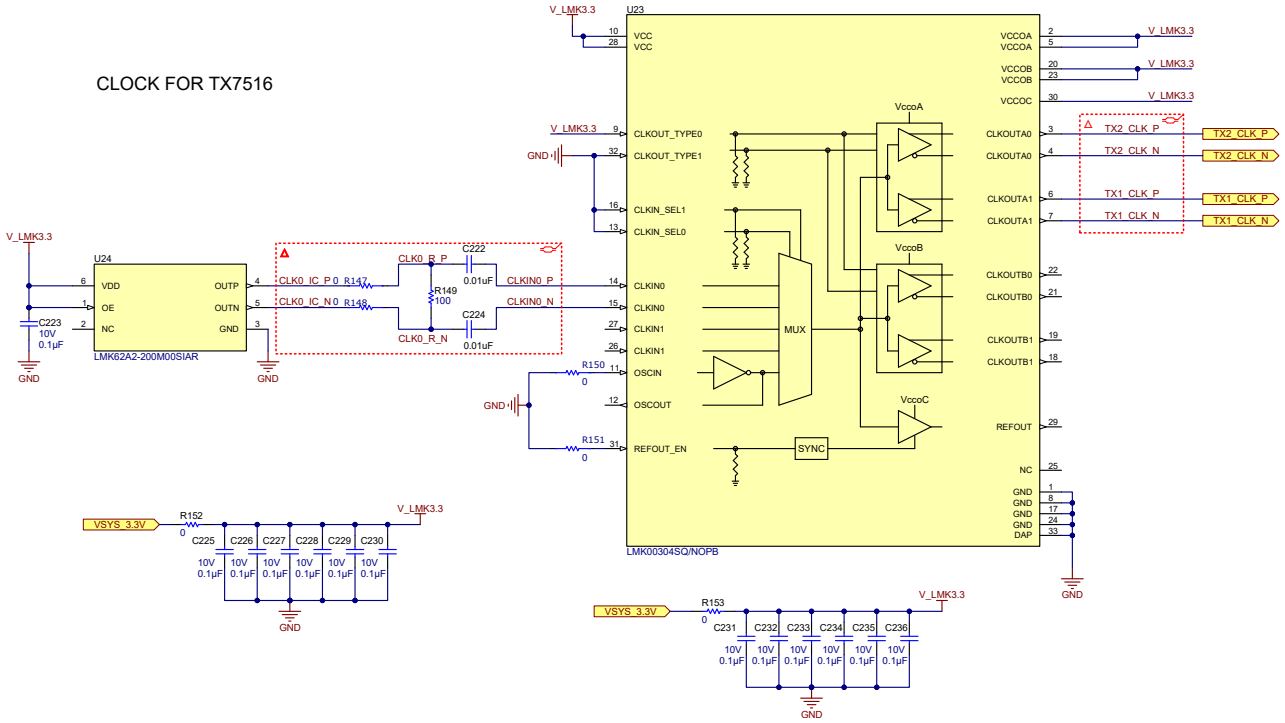


Figure 2-14. Clock Circuit

In the PCB design, place R149 near the LVDS receiver end.

2.2.5 CMOS to LVDS Driver

The synchronous trigger signal TR_BF_SYNC for TX7516 only supports LVDS input, while the Sitara MCU (AM2431) only outputs CMOS or Low-Voltage Complementary Metal Oxide Semiconductor (LVCMOS). Figure 2-15 shows the resulting required external LVCMOS and LVCMOS-to-LVDS translation circuit.

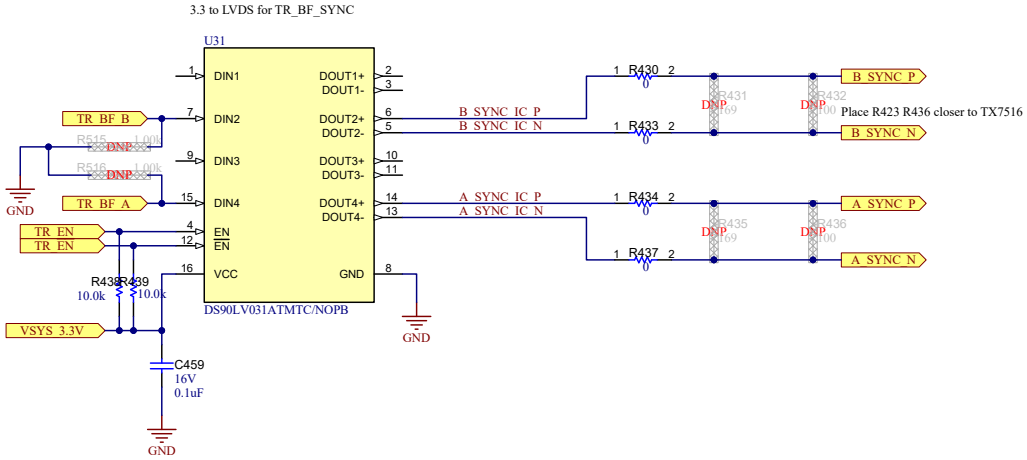


Figure 2-15. CMOS to LVDS Driver Circuit

The TR_BF_SYNC signal on the TX7516 supports internal LVDS terminal resistance configuration, defaulting to 100Ω.

2.2.6 Layout Guidance

The connection between the TX7516 and the TMUX9832 can be either star or daisy-chain. The turn-on of the TMUX channel in the daisy-chain path clearly causes large impedance discontinuities and bad signal reflections. The star routing topology between the TX7516 and TMUX9832 definitely causes pulser signal reflections. The worst-case scenario is that the signal reflection ringing exceeds the input limit of the TMUX9832 (maximum ±120V); therefore, following the simulation results before PCB routing and components placements is the best design practice. This section shows the transient simulation results based on the TMUX9832 IBIS model using Advanced Design Systems (ADS). Table 2-4 shows the simulation parameters.

Table 2-4. Advanced Design System Transient Simulation Setup

PARAMETERS	ADS SETUP
Step input sources	V_{peak} = 100V, V_{rise} = 16.6ns, t_{Delay} = 10ns
PCB layers	16, MLSUBSTRATE16 set same with PCB stackup
PCB Trace	ML1CTL_C trace length set to 80mm, trace on top layer and refer to MLSUBSTRATE16. Width = 5mil.
Load	220Ω | 220pF at TMUX9832 output pin

Figure 2-16 shows the daisy-chain schematic and Figure 2-17 shows the star connection schematic.

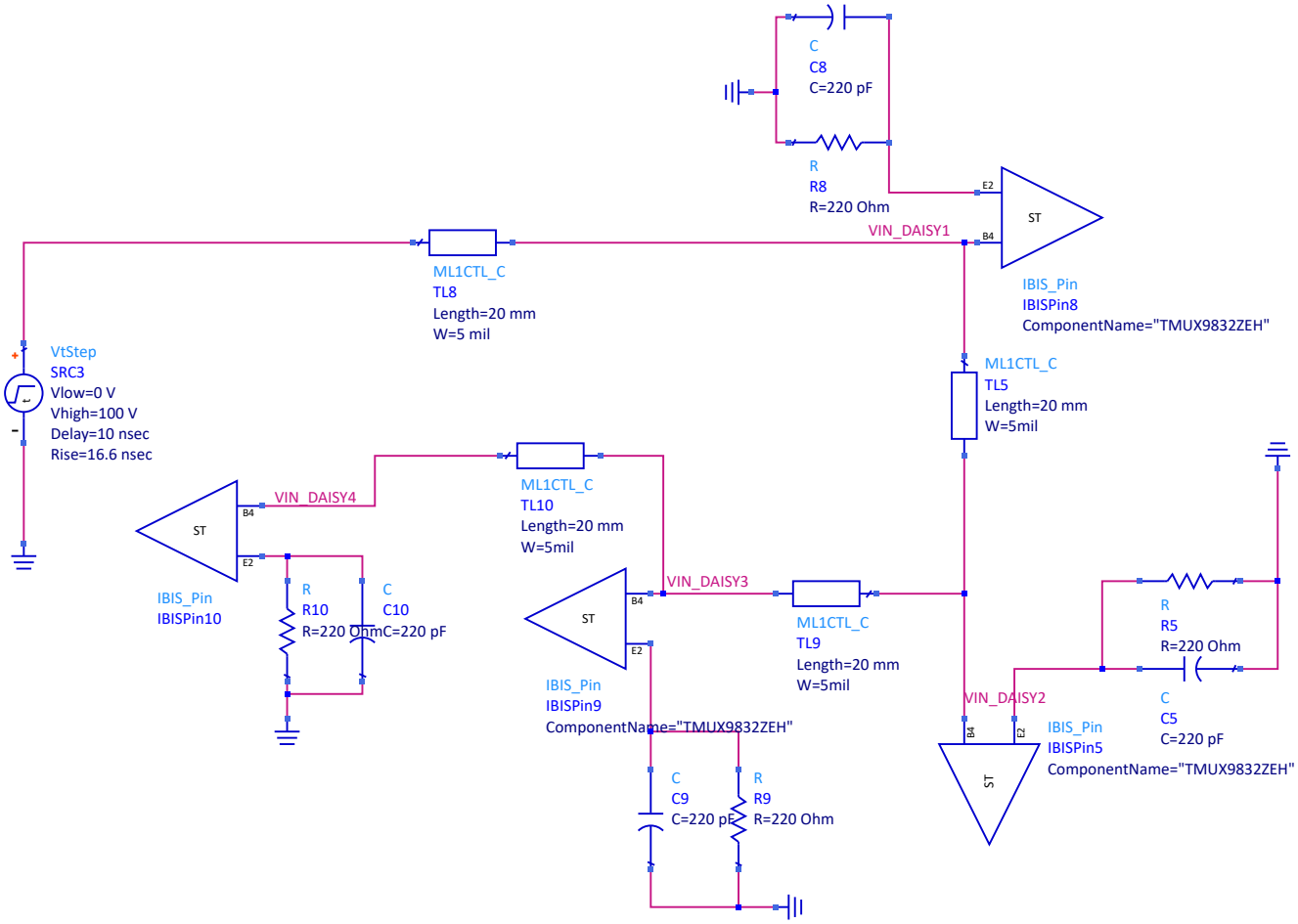


Figure 2-16. Daisy-Chain Schematic

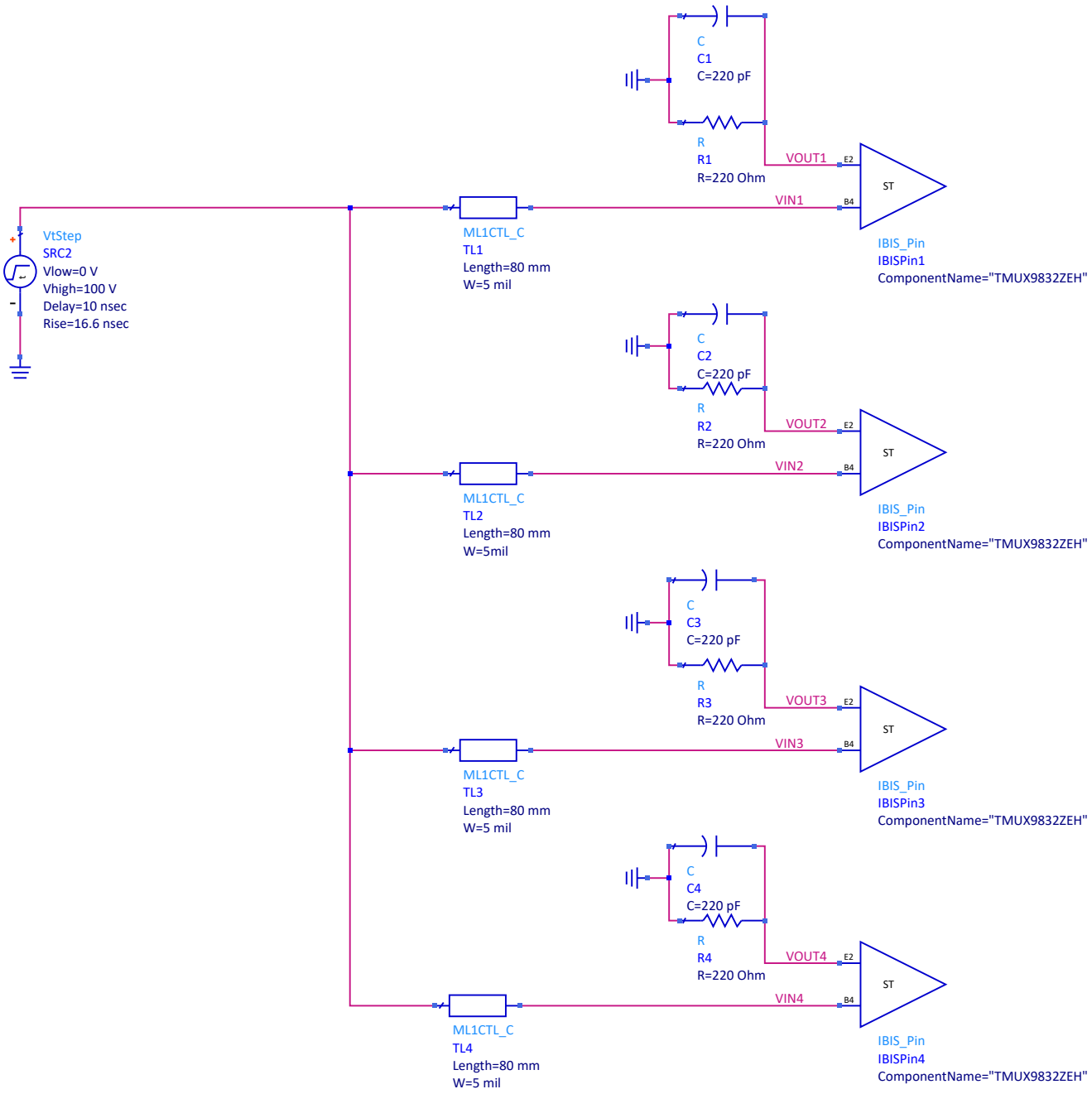


Figure 2-17. Star Connection Schematic

Figure 2-18 and Figure 2-19 show the simulation results. These results indicate that a maximum peak ringing visible at the TMUX9832 input reaches 107.546V for a 100V power supply when connected as tree. The maximum peak ringing of the daisy-chain connection is already over 120.086V for same power supply, which exceeds the input voltage limit of the TMUX9832. To suppress ringing on the TMUX9832 input, limit PCB trace lengths as short as possible and maintain consistency with pre-layout simulation results.

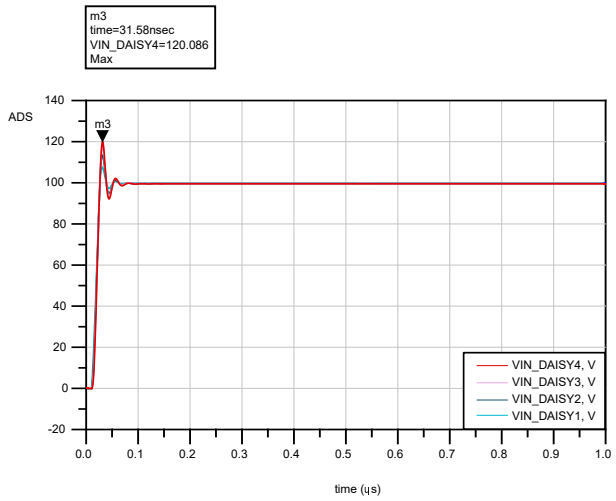


Figure 2-18. TMUX9832 ADS Simulation (Daisy Chain)

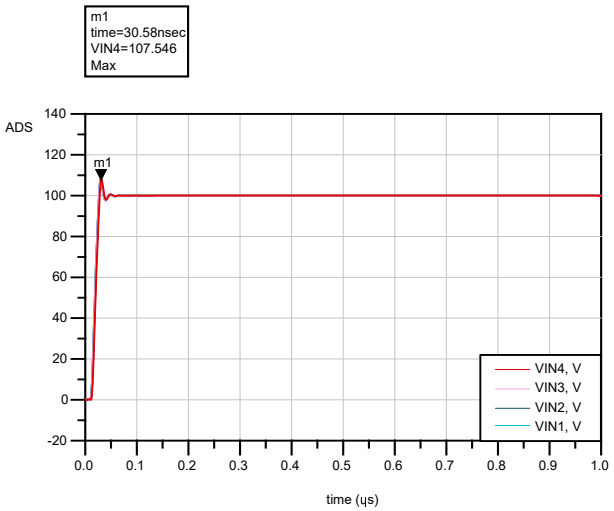


Figure 2-19. Result of the ADS Simulation (Star)

Figure 2-20 shows the component placement.

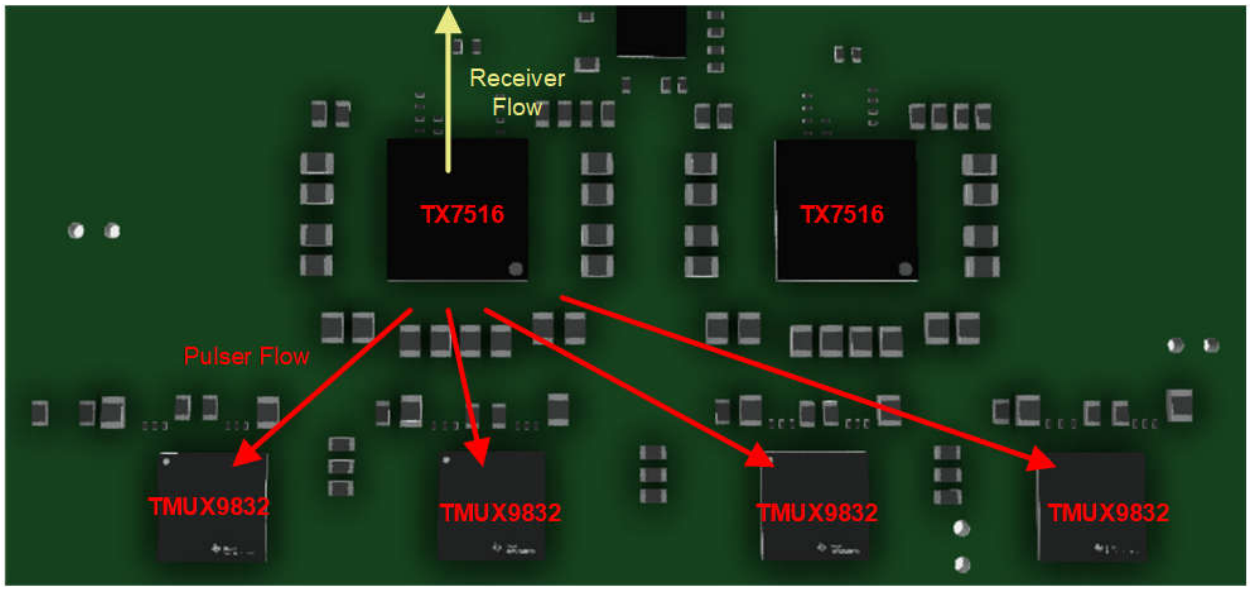


Figure 2-20. Components Placement Section

Figure 2-21 shows the flows of how the input and output signals to the TMUX were optimized. The red arrows indicate the pulse input direction and the yellow arrows indicate the pulse output. The adjacent trace spacing needs to meet the 4W–5W rule; for example, the 5mil PCB trace width and the spacing needs to be set to 20–25mils. The design goal is to maintain the same GND reference from origination to termination for the entirety of any pulser signal trace. If unable to meet this goal, via-stitch both GND planes to provide continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200mils (closer is better). For BGA fan-out of TX7516 and split of GND plane, see also the *TX7516 Five-Level, 16-Channel Transmitter With T/R Switch, and On-Chip Beamformer* data sheet and EVM PCB layout section.

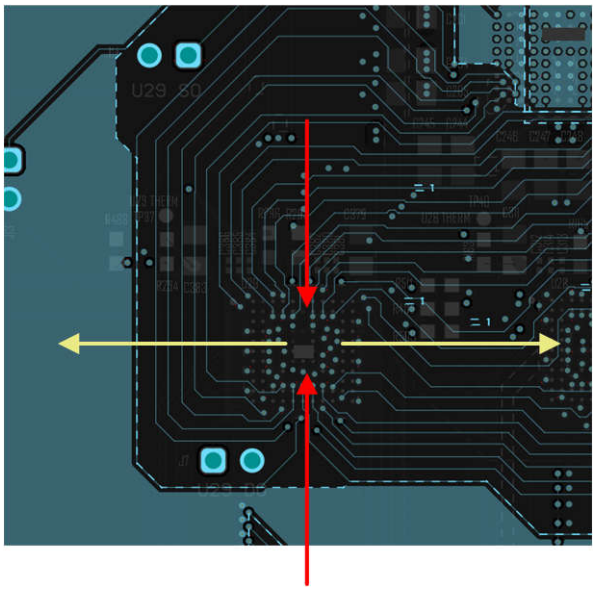


Figure 2-21. TMUX9832 PCB Layout Section

2.3 Highlighted Products

2.3.1 TX7516

The TX7516 is a highly integrated, high-performance transmitter for ultrasound imaging systems. The device has a total of 16-channel high-voltage (±100V) five-level pulser circuits,16 transmit-receive switches (referred to as T/R or TR switches), and supports an on-chip beamformer (TxBF). The device also integrates on-chip floating power supplies that reduce the number of required high-voltage power supplies. Figure 2-22 shows the TX7516 block diagram.

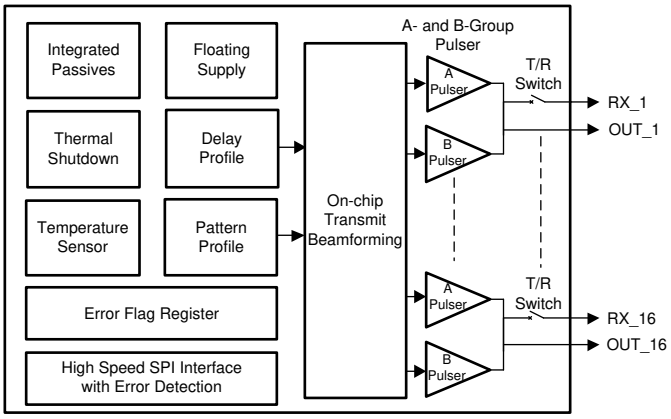


Figure 2-22. Simplified Block Diagram

2.3.2 TMU9832

The TMUX9832 is a 32-channel low-harmonic-distortion, low-resistance, low-capacitance, high-voltage analog switch integrated circuit (IC) with latch-up immunity. Each device has 32 independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device only requires a +5V analog supply, while still being able to support ±110V analog signals. The TMUX9832 also integrates bleed resistors on the drain (Dx) pins to discharge capacitive loads, like piezoelectric transducers. TMUX9832 is an excellent choice for medical ultrasound imaging and other piezoelectric transducer driver applications.

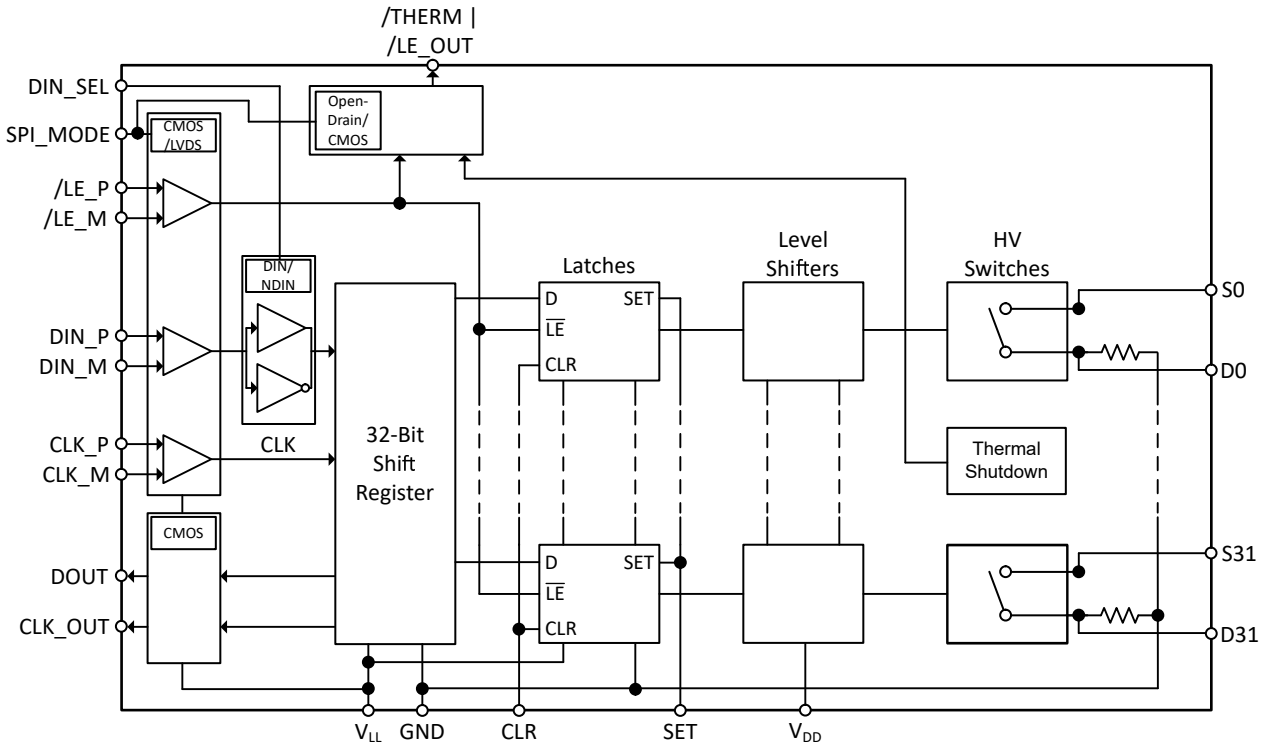


Figure 2-23. TMUX9832 Simplified Schematic

To reduce noise in the signal path due to potential clock feedthrough, the active low latch enable can be held high while data is loaded into the shift registers. The cascadable 32-bit shift register of the TMUX9832 also supports Low-Voltage Differential Signaling (LVDS) and single-ended complementary metal-oxide semiconductor (CMOS) mode.

2.3.3 AM2431

The AM243x is an extension of the Sitara™ industrial-grade portfolio into high-performance microcontrollers. The AM243x device is built for industrial applications, such as motor drives and remote I/O modules, which require a combination of real-time communications and processing. The AM243x family provides scalable performance with up to four Cortex-R5F MCUs, one Cortex-M4F, and two instances of the gigabit TSN-enabled PRU_ICSSG from Sitara. The SoC provides flexible industrial communications capability including full protocol stacks for EtherCAT target, PROFINET device, EtherNet/IP adapter, and IO-Link controller. The PRU_ICSSG further provides capability for gigabit and TSN-based protocols. In addition, the PRU_ICSSG enables additional interfaces including a UART interface, sigma-delta decimation filters, and absolute encoder interfaces.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.1.1 TIDA-010256 PCB Overview

Figure 3-1 and Figure 3-2 show labeled views of the TIDA-010256 PCB.

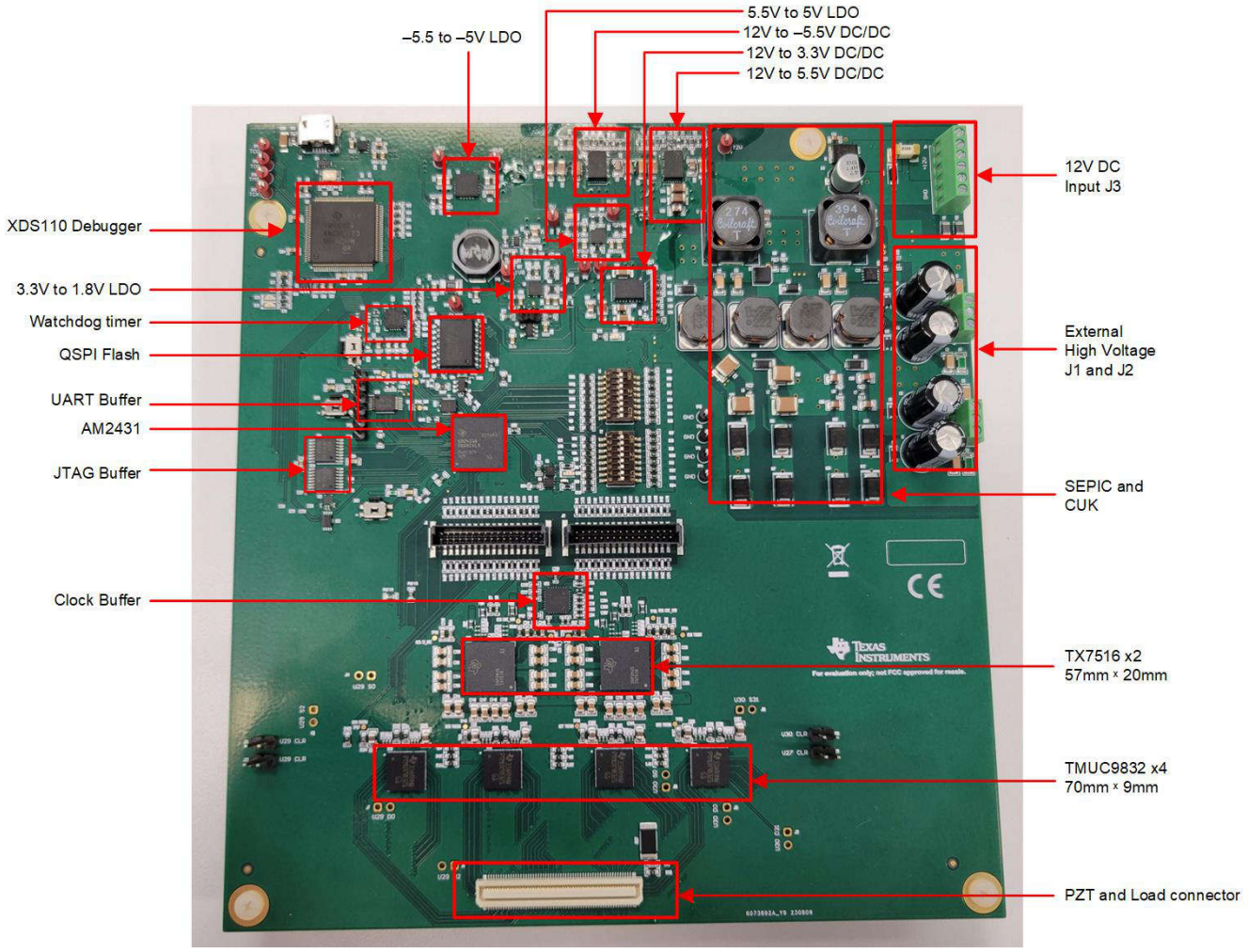


Figure 3-1. TIDA-010256 PCB Top View

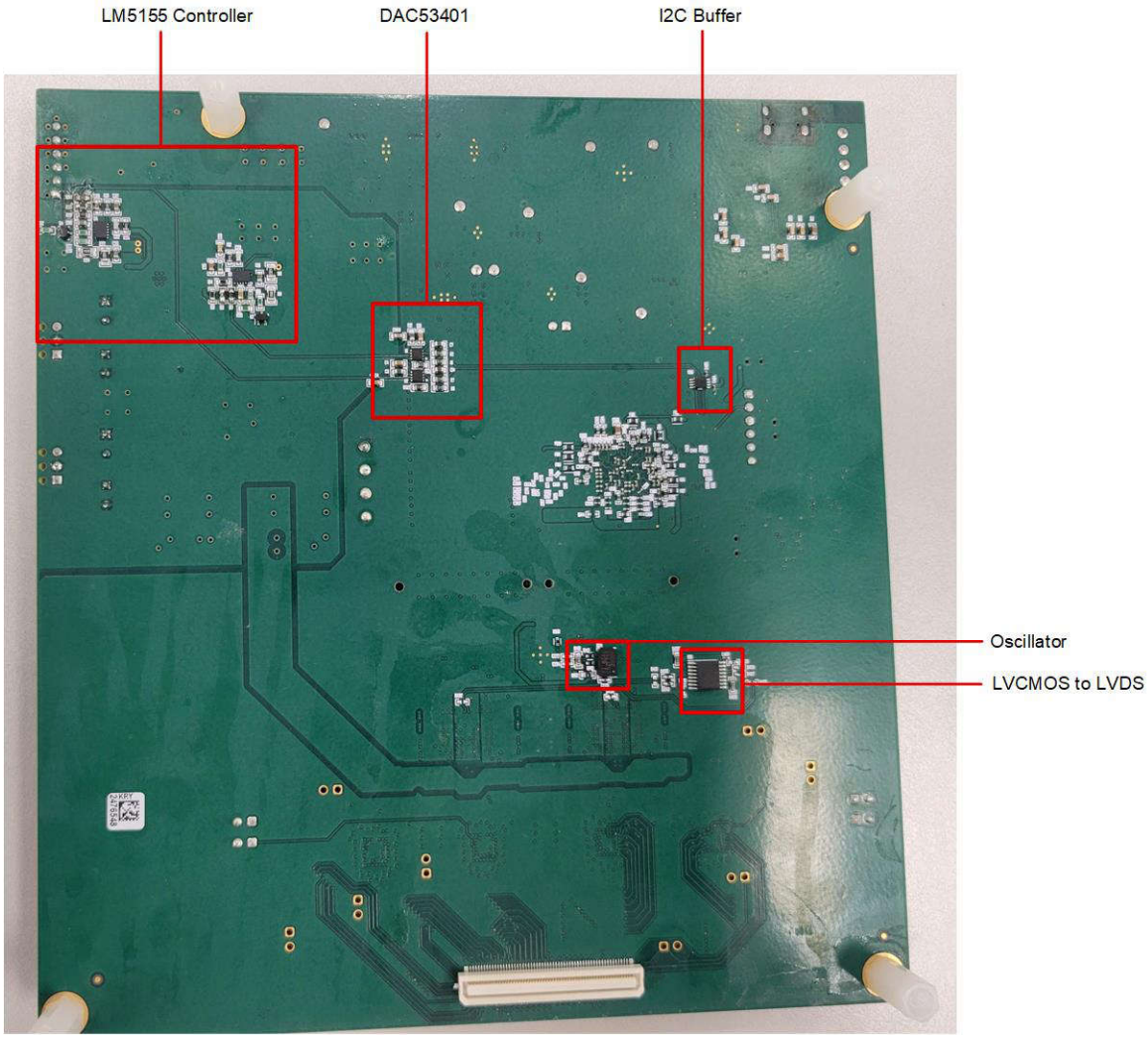


Figure 3-2. TIDA-010256 PCB Bottom View

3.1.2 TIDA-010256 Connector Settings

Table 3-1 shows the TIDA-010256 connector settings.

Table 3-1. TIDA-010256 Connector Settings

CONNECTORS	FUNCTION
J3	+12V DC input. Preferred use is 3A to 5A.
J1(1)	±80V external high-voltage connector
J2(1)	±40V external high-voltage connector
J5	USB connector
J6(2)	External UART jumper
J9	PZT and load connector
J10	PZT and load connector
J11 and J12	TX7516 Receive channel connector

(1) When connecting an external high-voltage power supply, make sure that the voltage exceeds both SEPIC and Cuk circuit outputs. This is because of a shared diode on the PCB, which only allows the board to be powered by the external supply when the input voltage surpasses the onboard programmed output voltage.
(2) J6 does not require any external debug serial port, by default use the XDS110 serial port.

3.2 Software Requirements

To test TIDA-010256, all of the software was developed based on AM2431 software development kit, the firmware is not available for public use. For support on the software, please refer to AM2431SDK and TI E2E design support forum.

3.3 Test Setup

Table 3-2 lists the equipment used for the TIDA-010256 testing session. Figure 3-3 shows the test setup.

Table 3-2. TIDA-010256 Required Equipment for Setup

TEST EQUIPMENT	PART NUMBER
High-voltage source(1)	Agilent® 6030A, ITECH® IT6724H
Low-voltage source	Keithley® 2230G-30-1
Oscilloscope	Tektronix® DPO3054
Probes	Tektronix® P5050B

(1) The TIDA-010256 board requires two high voltage ±100V power supply source each with a 500mA current range.

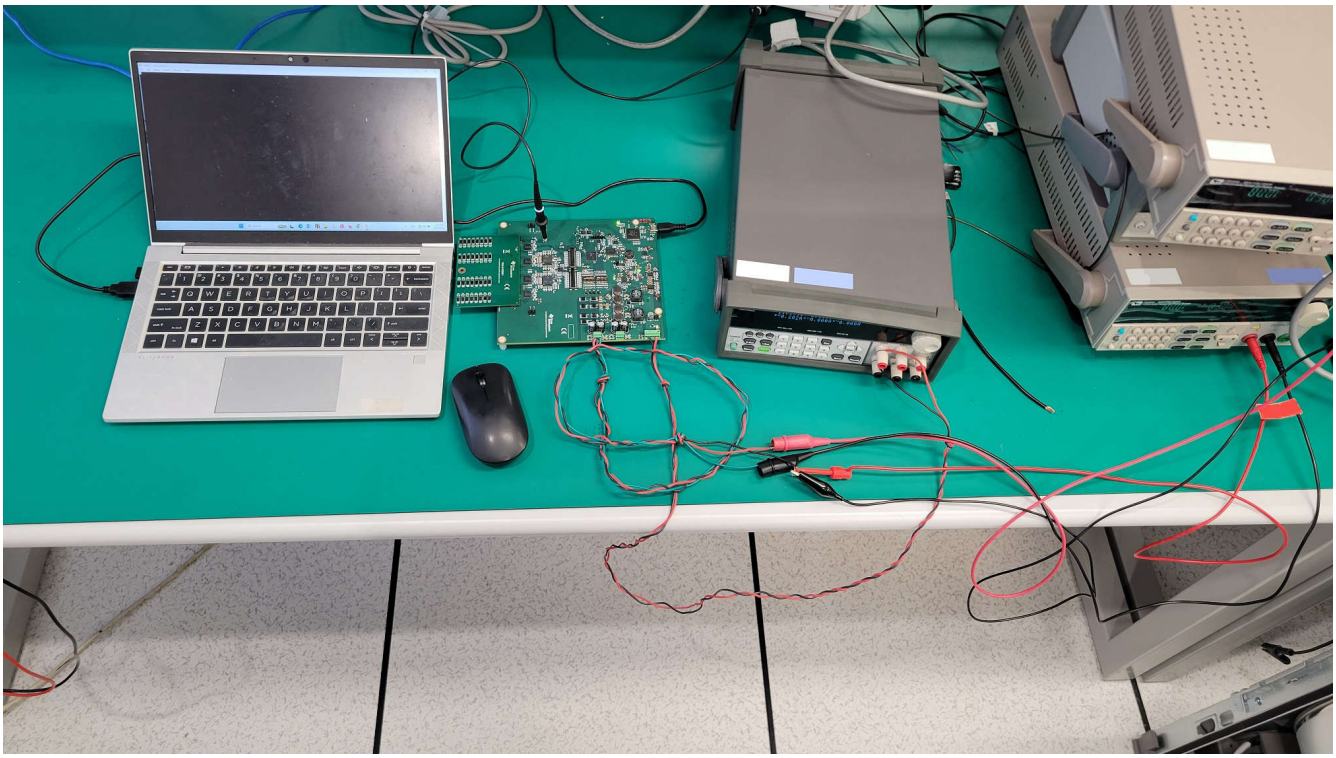


Figure 3-3. TIDA-010256 System Test Setup

In the tests, an additional PC was required to send commands through the TeraTerm terminal.

3.4 Test Results

3.4.1 High-Voltage Power Supply Output Ripple

Figure 3-4 and Figure 3-5 show the high-voltage supply noise waveforms and are measured after the passive filter.

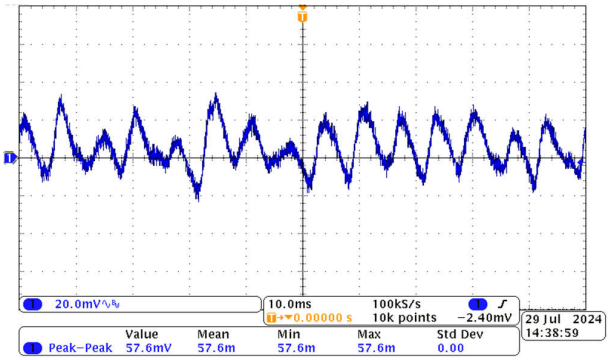


Figure 3-4. +80V With Load 300mA

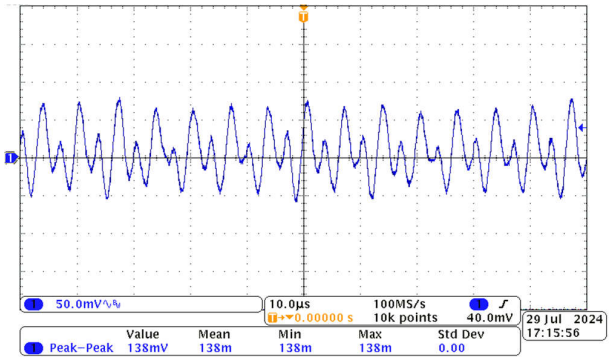


Figure 3-5. +40V With Load 300mA

3.4.2 Output Waveform

Table 3-3, Table 3-4, and Table 3-5 show part of the register configuration for TX7516 in CW-mode, B-mode, and elastography mode. Since the pulser input substations are identical for each TMUX9832, all channels of the first TMUX9832 are turned on for testing, measured at TMUX9832 output, and load resistance is 220Ω|220pF.

Table 3-3. CW Mode Register Configuration

BF_CLK	BF_CLK_DIV	CLK_DIV	HVB PERIOD	CW OUTPUT FREQUENCY
200MHz	2	2	50	1MHz

Table 3-4. B-Mode Pattern Memory Configuration

ADDR	BYTE 4	BYTE 3	BYTE 2	BYTE 1
0x40	0xCA Level = 010(HVP_B), Period = 25	0xC8 Level = 000(GND), Period = 25	0x01 LOCAL_REP_NUM = 1	0x00 GBL_REP_NUM = 0
0x41	0x00	0xC8 Level = 000(GND), Period = 25	0xCA Level = 010(HVP_B), Period = 25	0xc9 Level = 001(HVP_A), Period = 25
0x42	0x00	0x00	0x00	0xff

Table 3-5. Elastography Mode Pattern Memory Configuration

ADDR	BYTE 4	BYTE 3	BYTE 2	BYTE 1
0x40	0x55 Level = 101(AVDDM_HV_A), Period = 10	0x51 Level = 001(AVDDP_HV_A), Period = 10	0x63 LOCAL_REP_NUM = 99	0x13 GBL_REP_NUM = 19
0x41	0x00	0x00	0xff	0x00

Figure 3-6 through Figure 3-9 show the waveforms for CW mode, B-mode, and elastography mode.

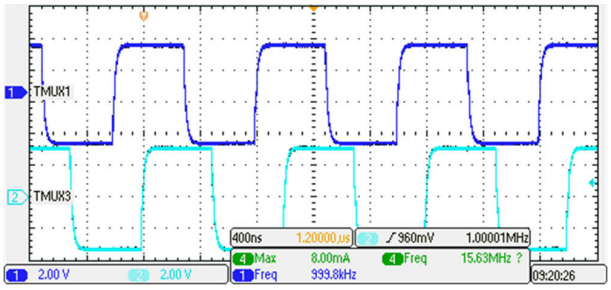


Figure 3-6. CW Mode Waveform

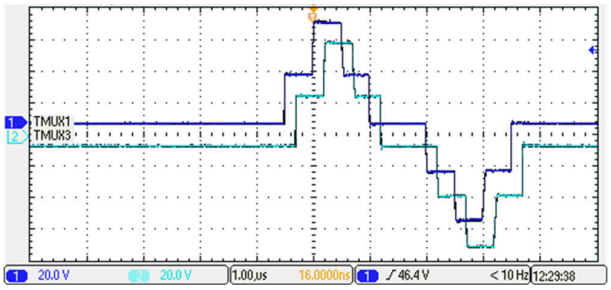


Figure 3-7. B-Mode Waveform

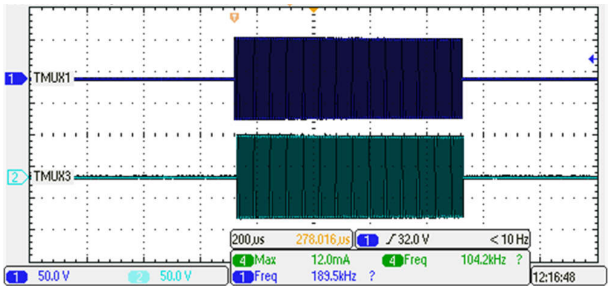


Figure 3-8. Elastography Mode Waveform

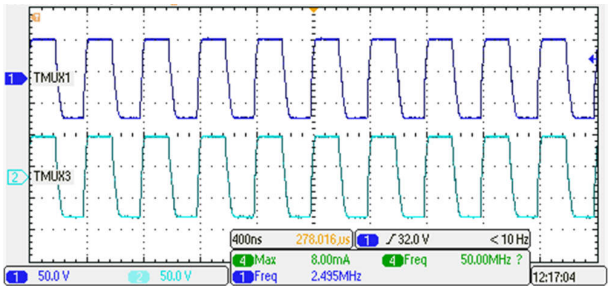


Figure 3-9. Elastography Mode Waveform (Zoomed In)

3.4.3 Thermal Test

During testing, the pulse output was connected to the real PZT probe. Next, the temperature rise of the TMUX9832 and TX7516 were tested after 10 minutes of continuous shear wave output. The TMUX9832 device was at the following conditions:

- Only 16 channels were open
- Elastography pulse repetition frequency (PRF) = 20Hz
- Frequency = 2.5MHz
- Transition pulser counts = 1250
- 70V peak voltage

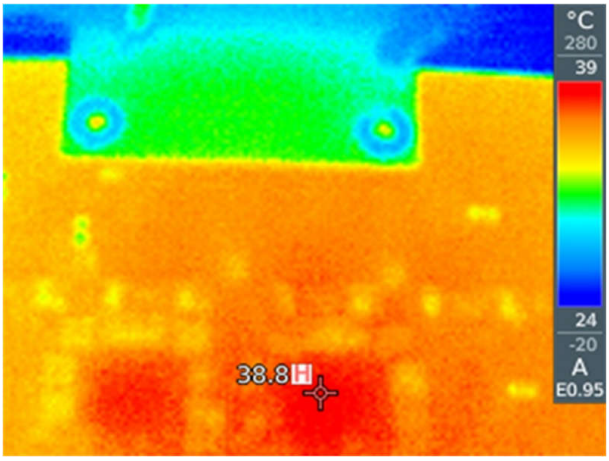


Figure 3-10. Start

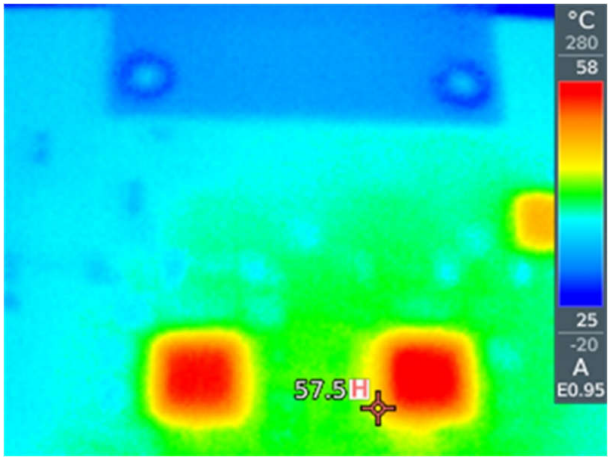


Figure 3-11. 10 Minutes

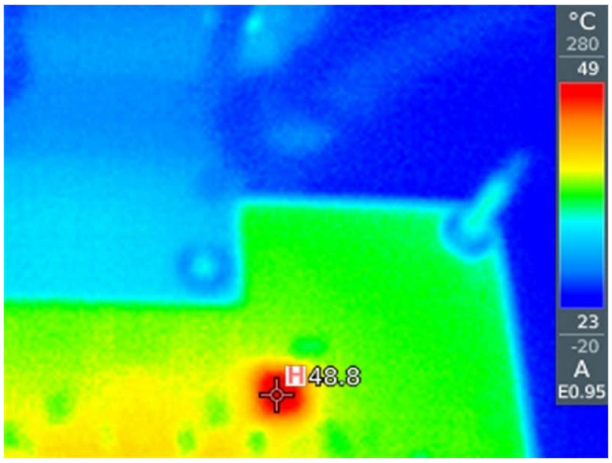


Figure 3-12. TMUX9832 (Zoomed In)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010256.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010256.

4.2 Tools and Software

Tools

XDS110 Debug Probe	The XDS110 debug probe is a low-cost system for debugging and tracing embedded systems centered on Texas Instruments (TI) microcontroller, microprocessor, and DSP® based systems.

Software

MCU-PLUS-SDK-AM243X	AM243x software development kit (SDK) for Sitara™ microcontrollers

4.3 Documentation Support

1. Texas Instruments, *TMUX9832 No High Voltage Bias, Beyond the Supply, 220V 1:1, 32-Channel Switch With Latch-Up Immunity Data Sheet*
2. Texas Instruments, *TX7516 Five-Level, 16-Channel Transmitter With T/R Switch, and On-Chip Beamformer Data Sheet*
3. Texas Instruments, *AM243x Sitara™ Microcontrollers Data Sheet*
4. Texas Instruments, *LM5155x 2.2MHz Wide Input Nonsynchronous Boost, SEPIC, Flyback Controller Data Sheet*
5. Texas Instruments, *LMK00304 3GHz 4-Output Ultra-Low Additive Jitter Differential Clock Buffer/Level Translator Data Sheet*
6. Texas Instruments, *TPSM63603 High-Density, 3V to 36V Input, 1V to 16V Output, 3A Power Module With Enhanced HotRod™ QFN Package Data Sheet*
7. Texas Instruments, *TPS7A94 1A, Ultra-Low Noise, Ultra-High PSRR, Low-Dropout Regulator Data Sheet*
8. Texas Instruments, *Designing Bipolar High Voltage SEPIC Supply for Ultrasound Smart Probe Application Note*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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