Design Guide: TIDA-010269

Handheld Ultrasound Imaging Device Power Supply Reference Design

Description

This reference design is built to power the next generation 128-channel ultrasound smart probe that adopts TI's new generation transmitter and receiver. The compact size (88mm × 45mm × 20mm) includes all power functions for a 128-channel smart probe with > 80% efficiency. This transformerless high-voltage power supply (±75V at 25mA), new boost regulator enables the reference design to meet most smart-probe applications.

Resources

TIDA-010269	Design Folder
TPS54218, LM5158, TPS61178, BQ25790	Product Folder
CDCE949, TPS7A39, TPS74401, LMZM23601	Product Folder
INA231, TPS7A96, LM3880, DAC53401	Product Folder

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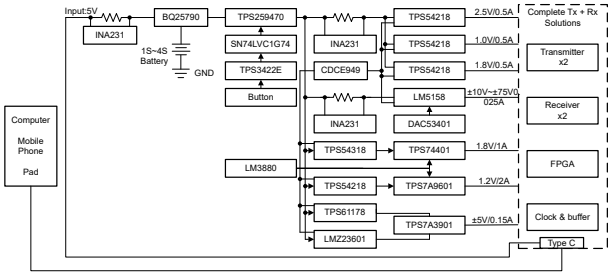
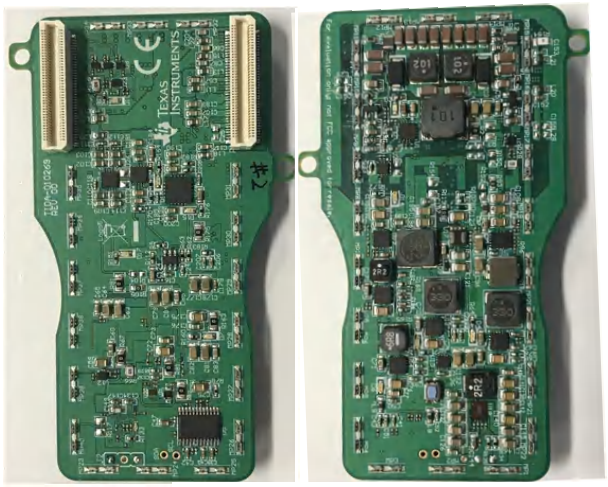


Features

- Transformerless, dual-rail, high-voltage (±75V at 25mA) generation from 5V USB Type-C® in single-stage implementation to meet component height requirement of < 5mm
- Compact board size (less than 88mm × 45mm × 20mm)
- End-to-end system efficiency – 80% running at full load
- Enable and Disable supplies for power optimization and all rails can be synchronized to external clock
- Accurate real-time power consumption measurement using high-performance current sensing amplifier INA231
- High-speed data acquisition over USB 2.0 up to 480Mbps

Applications

- Ultrasound smart probe



1 System Description

Ultrasound imaging is a widely used diagnostic technique. In addition to high-performance, cart-based ultrasound systems, it is now possible to use a handheld device (smart probe) to accomplish high-quality ultrasound imaging. These smart probes leverage the power and resources of a mobile phone or tablet to process and display ultrasound images. A typical use case for these systems is to bring modern medical imaging technology to remote places, providing a faster and much more efficient diagnosis. This small equipment is typically powered by battery (1S, 2S), or from a USB source. The data can be transferred over USB or Wi-Fi®.

Figure 1-1 (left) shows a generic picture of one such smart probe ultrasound scanner depicting a probe connected to a mobile device. Figure 1-1 (right) shows the block diagram of the smart probe, which includes a transmit (TX) and receive (RX) analog front end (AFE) for transmitting and receiving ultrasonic pulses and field programmable gate arrays (FPGA) to perform beamforming. The whole setup is powered through the power supply board, consisting of DC-DC converters to generate point-of-load voltages, the high-voltage circuit for powering the transmit chip (used in the design) and USB controller for data and power management.

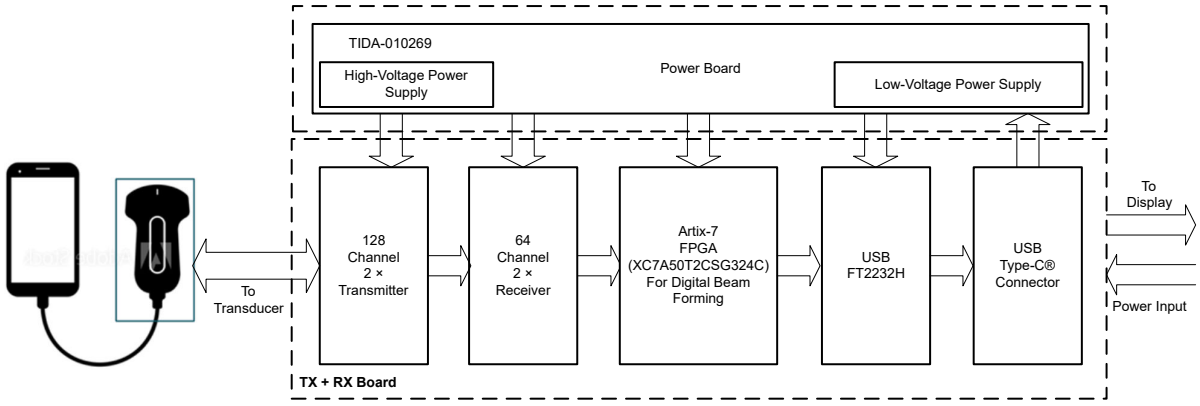


Figure 1-1. Generic Smart Probe (Left), Block Diagram of Smart Probe Ultrasound Scanner (Right)

One use case for these systems is to bring modern medical imaging technology to remote villages in developing countries. Smart ultrasound probes, or ultra-portable ultrasound systems, are an excellent fit for this task due to the cost-effectiveness. The day is fast approaching when most doctors carry a smart probe unit. With these tools, the physician can both hear and see inside the body—potentially leading to a market of a few million units worldwide within the next decade, complementing standard ultrasound systems. Figure 1-2 shows the factors that are the leading reasons for this boom in the smart probe market.

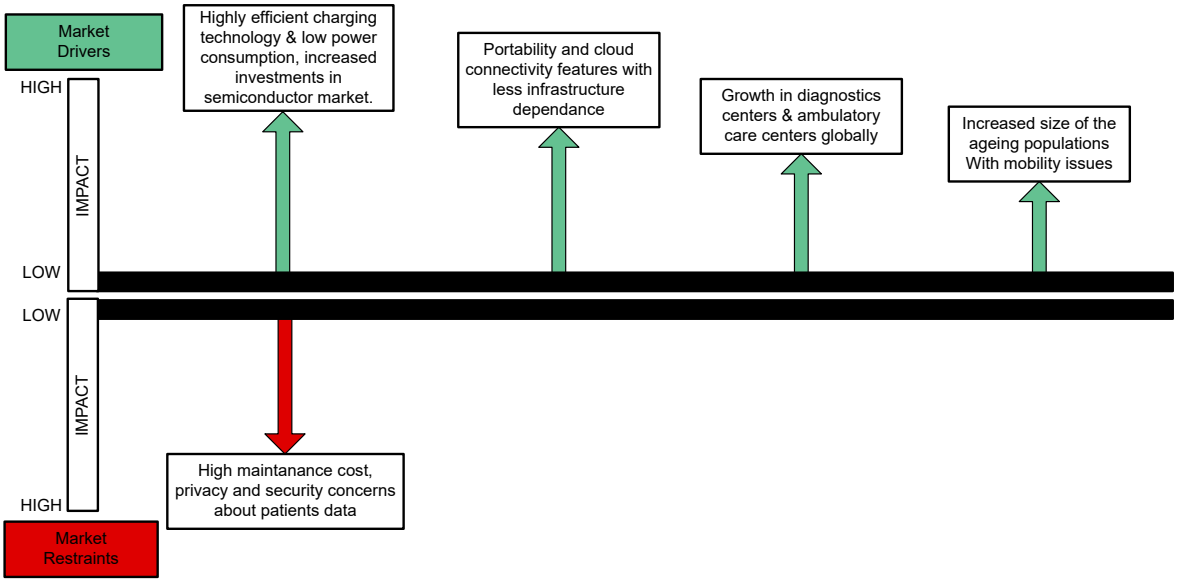


Figure 1-2. Market Drivers and Restraints for Ultrasound Smart Probe

1.1 Key System Specifications

Table 1-1 shows the complete system specifications of the power design of the smart probe. The table is divided into two sections describing specifications of the high-voltage circuit and low-voltage circuit.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
System Input Voltage (V_{IN})	4.25V–5.5V (USB Type-C)	Design supports 1S– battery input (3.3V–4.2V)
External Clock Synchronization	1MHz, 500kHz, and 250kHz	Onboard buffer or divider is used to provide the sync clock from 1MHz source
HIGH VOLTAGE CIRCUIT SPECIFICATIONS Architecture: Single-Ended Primary Inductance Converter and Cuk (SEPIC and Cuk)		
Positive Output Voltage (V_{OUT+})	Up to 75V	Symmetric positive and negative output. Can be set by external feedback resistors
Negative Output Voltage ($V_{OUT–}$)	Up to –75V	
Output Current (I_{OUT})	Up to 25mA per rail	
Total High Voltage Power (P_{HV})	2.25W + 2.25W	
Load Regulation	< 2%	Load applied symmetrically on positive and negative rail
Voltage Accuracy	< 1%	Voltage accuracy: voltage difference between positive and negative rail across the load
Output Voltage Ripple	0.1% of the output voltage	
Switching frequency	250kHz	
TRANSMIT LOW VOLTAGE SUPPLY (±5V) SPECIFICATIONS		
Switcher Output Voltage (positive)	5.7V	This boost output can be fed as input to the high-voltage supply or –5V supply to enable 1S operation.
LDO Output Voltage	5V	
Output Current	150mA	Maximum LDO output current
Output Voltage Ripple	10mV (V_{OUT} : 5.7V I_{OUT} : 1A)	
Switcher Output Voltage (negative)	–5.3V	Inverting Buck Topology
LDO Output Voltage	–5V	
Output Current	150mA	
Output Voltage Ripple	10mV (V_{OUT} : –5.3V I_{OUT} : 1A)	
RECEIVE LOW-VOLTAGE SUPPLY SPECIFICATIONS		
AFEs Supply Rails with Low Noise LDOs	1.2V (2A maximum), 1.8V (1A maximum),	TPS7A96, TPS74401 LDOs are used for respective rails followed after the TPS54218 DC-DC buck
Switcher Output Voltage	2V, 1.405V	Low dropout to maximize system efficiency
DC-DC Output Voltage Ripple (1.405V)	8mV	
TPS74401 (1.2V) PSRR (Output Ripple) at 500kHz	–40dB (80µV)	
DC-DC Output Voltage Ripple (2.0V)	8mV	
TPS7A9601 (1.8V) PSRR (Output Ripple) at 500kHz	–40dB (80µV)	
FPGA POWER SUPPLY SPECIFICATIONS		
Switcher Output Voltage	1V (0.5A maximum), 1.8V (0.5A maximum), 2.5V (0.5A maximum)	The inductance values are optimized for higher efficiency and load currents of 0.5A
Maximum Output Voltage Ripple	15mV	
System Power Measurement	Total Power; FPGA Power and TX Power	System current, voltage and power measurement of various subsystems using INA231

2 System Overview

There is a growing interest in a handheld ultrasound systems to help maximize the effectiveness of point-of-care support and diagnosis for patients. Traditionally, ultrasound systems are of a cart-based type, which integrates a higher number of channels to achieve higher performance and excellent image quality.

Ultrasound analog front ends and transmitter chips have achieved over 80% reductions in power and size. These advancements allow for higher channel integration and the lowest power possible, which is a requirement for handheld portable probes since the probes are typically battery operated (1S, 2S). Higher receiver and transmitter channel count in the system gives a better image resolution. Figure 2-1 shows the image quality difference between a 16-channel, 32-channel, and 64-channel system. Because of the power and area limitation in portable ultrasound systems, most of systems in the market are able to integrate 16- or 32-channel receivers and transmitters. The high-voltage MUX is used to excite 128 transducer elements; see Figure 2-2. Some of the limitations for the existing design are a lower image quality because of only a 16-channel receiver and a lower frame rate because of higher imaging time due to a limited number of channels. This reference design proposes a design which contains a complete power design for TI's high-performance, 128-channel TX, 64-channel RX ultrasound smart probe design. This reference design also can be used to power most ultrasound smart probes with a bit update.

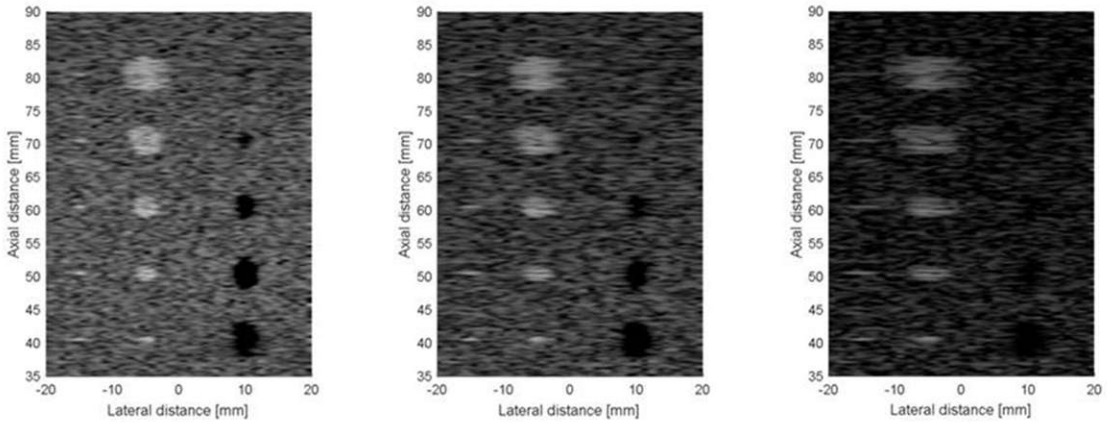


Figure 2-1. Image Resolution and Quality Across Channel Integration

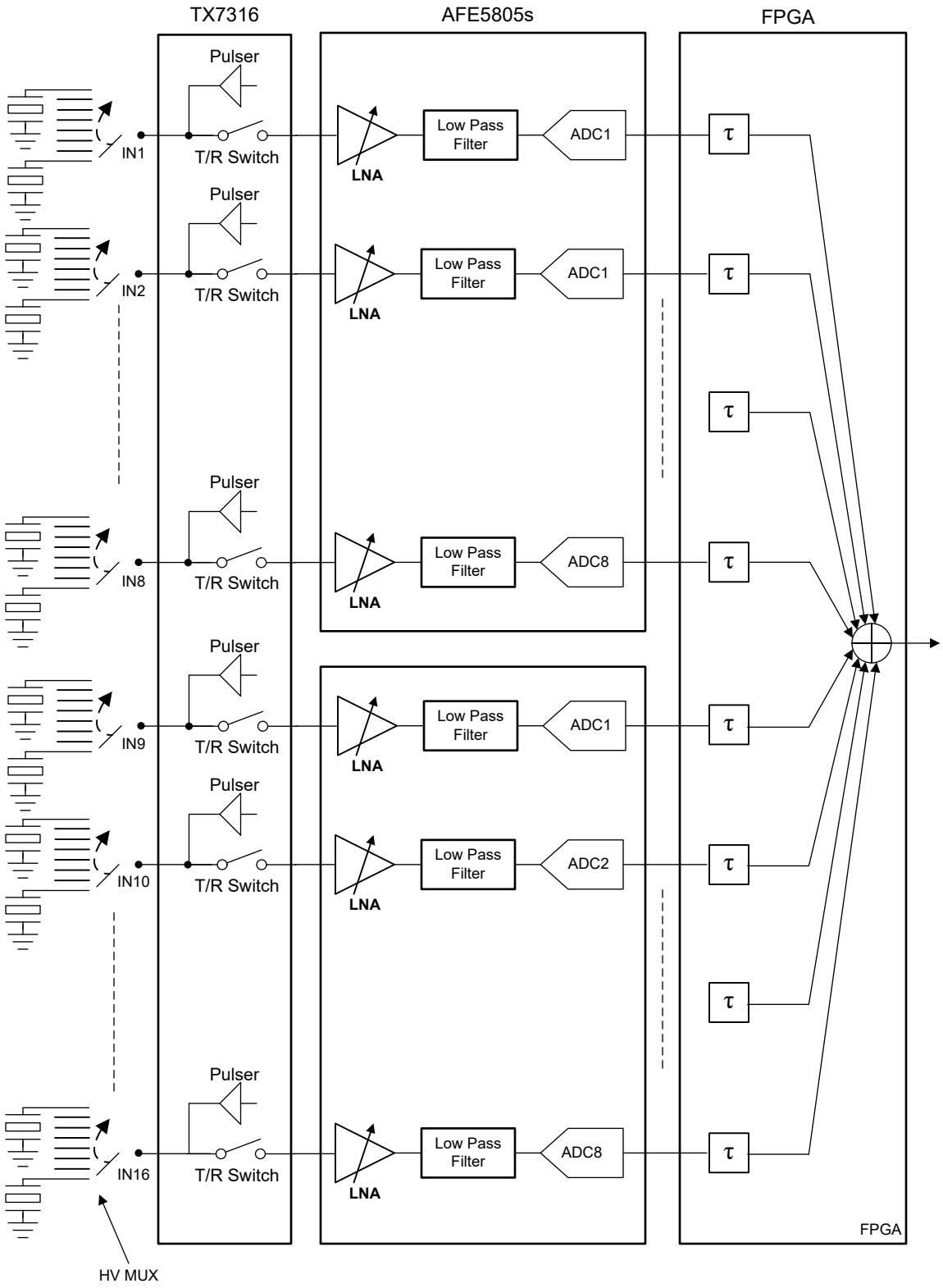


Figure 2-2. 16-Channel System

To achieve the target area, all the power supplies are kept on another PCB which is vertically stacked to the RX + TX board through the connector. The other advantage of having power supplies on a separate PCB is that this arrangement increases isolation of switching noise from the power supply to sensitive receiver and transmitter devices. This power-supply board generates a total of eight different supplies (Including ±75V) from USB Type-C 5V with a capability of delivering a maximum of 15W peak power. Using TI's CDC series or LMK

series clock buffer to generate synchronous clocks for the system is the usual practice. This approach leads to a higher power consumption and extra space on the board. In the proposed design, to reduce power and board space, the FPGA is used to provide clock to all the chips. The power supply board requires eight clock signals for synchronization. In ultrasound systems the transmitter is active only for 1% of imaging duration. For rest of the duration, the receiver device receives the echo to form the full image. On the same concept, the transmitter device is also kept active only for 1% duration which reduces the clock power further, the low-voltage differential signaling (LVDS) signals going to transmitter are programmed in tri-state mode for 99% duration. The LVDS buffer power in tri-state mode is 11mW/channel making the total power consumption of the clocking scheme 213mW. This is an improvement from a conventional clocking scheme power which is greater than 500mW.

2.1 Block Diagram

This design implements a full-power tree design that includes a single-stage transformerless high-voltage generation for transmit and the point-of-load low voltage for the AFEs and FPGA from a 5V USB Type-C input. The entire implementation is divided into two sections, the high-voltage power supply (see the *Designing Bipolar High Voltage SEPIC Supply for Ultrasound Smart Probe* application note) and a low-voltage supply. The system takes the input from a mobile phone, notebook, or desktop from a 5V USB Type-C connection. This 5V input is then used by different power management designs to power both the FPGA and the AFEs and transmitter to monitor the power consumption of various subsystems in the design. In the low-voltage supplies for both receiver and transmitter, each DC/DC converter is followed by an LDO to remove noise with a higher power supply rejection ratio (PSRR). Since the ultrasound smart probe is a noise-sensitive design, the high PSRR is a key specification for an increase in image quality. The FPGA, USB controller, and clocking supply are powered by highly efficient and low-power designs using the TPS54218, TPS7A96, and TPS74401 devices. Finally, INA231 devices are used to monitor the current of each power stage to provide a higher performing operation. Figure 2-3 shows the system block diagram.

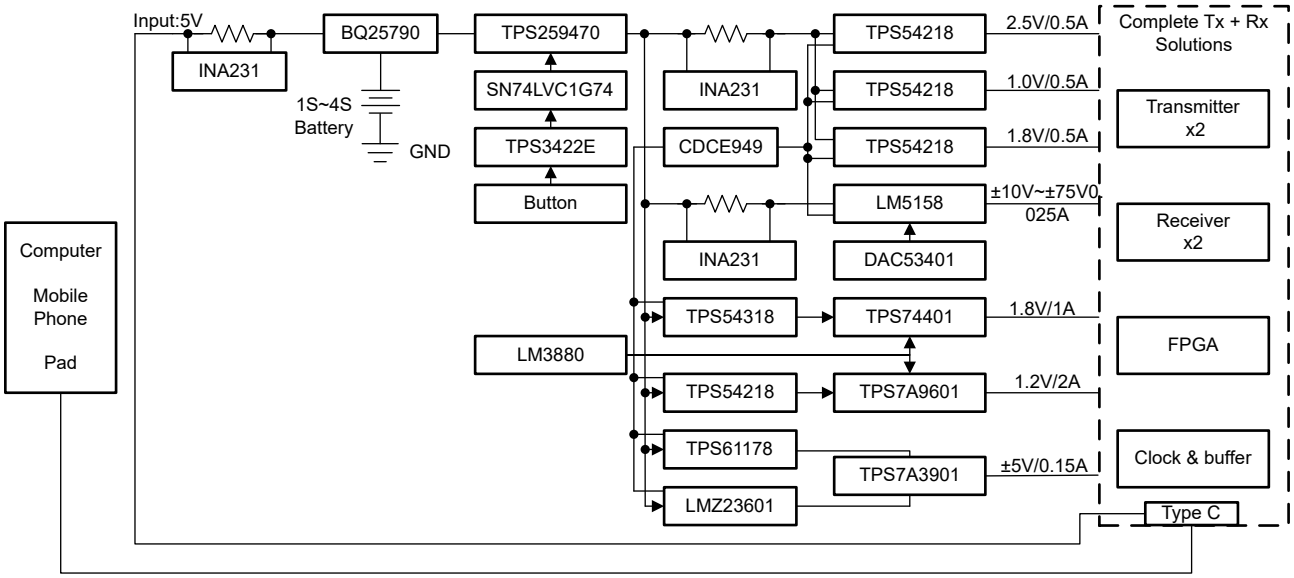


Figure 2-3. System Level Block Diagram of TIDA-010269

2.2 Design Considerations

The power design for a handheld ultrasound equipment is complex and comes with a lot of system-level challenges. All these challenges come primarily due to the small size of the complete design. Achieving high efficiency in low-power rails with a fixed synchronize frequency operation is the key concern since losses in the form of heat increase the temperature of the board. Typically, there are no cooling mechanisms employed in the end equipment due to the compact portable nature. The following sections provide the key design considerations in the smart-probe power design.

2.2.1 Small Compact Size

The size of the complete design is kept in a handheld form factor. The design includes:

- The transmit circuit with transducers. The design employs a 128-channel transmitter with the two newest 64-channel ultrasound transmitters in the industry.
- 64-channel receive
- High-performance FPGA for beamforming
- High-voltage circuit for transmit power
- Eight independent low-voltage rails to deliver point-of-load power and USB and data capture section to power and transfer the received data to the PC or tablet

All of these sections are placed on a two-board assembly with TX, RX, and FPGA on one and the remainder is on the *Power Board* discussed in this design. Figure 2-4 shows the height distribution of the complete system. The total height of the design is < 20mm. Figure 2-4 also shows the corresponding real image of the implemented design.

Figure 2-4. Total Height of the Complete Design

2.2.2 Transformerless Design

The design implements a transformerless power management design to meet a component height requirement of less than 5mm, and dual-rail, high-voltage (±75V at 25mA) generation from 5V USB with single-stage implementation and point of load (also supports 3.6V battery input). The following list shows the key constraints in the design for the power supply in smart-probe ultrasound scanners:

- Efficiency > 80%
- Thermal performance (temperature rise < 15°C above ambient)
- SNR > 55dB (noise floor below –90dB)
- High-voltage rail accuracy (between +ve and –ve high-voltage lines) 1%
- Load regulation accuracy within 2%

Figure 2-5 shows the board image of the portion of the high-voltage circuit implemented in the design. The corresponding section is highlighted in red.

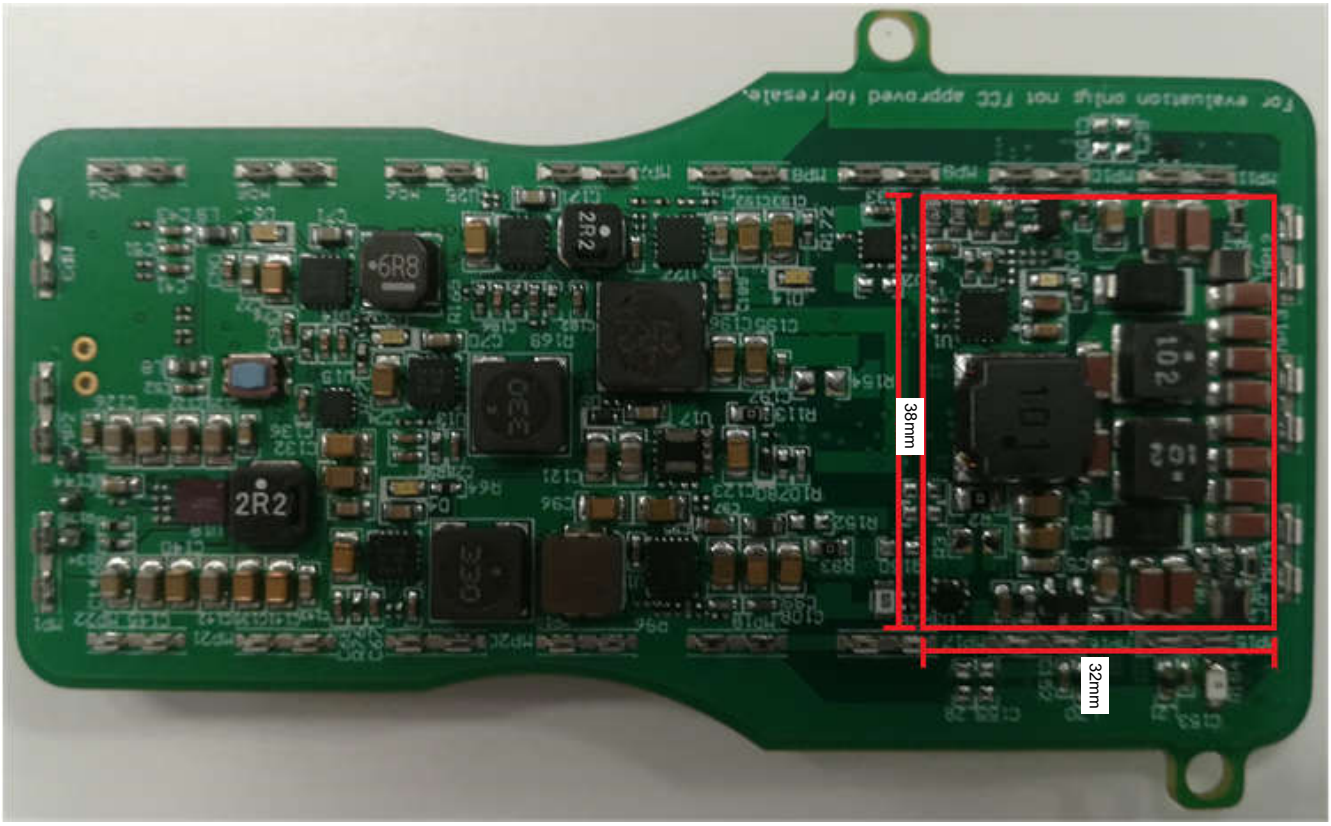


Figure 2-5. High-Voltage Section Implemented in 38mm × 32mm × 4.3mm (Complete Circuit Routed and Placed on the Bottom Layer)

2.3 Highlighted Products

This section briefly describes the devices used in this reference design.

2.3.1 BQ25790 I²C Controlled, 1–4 Cell, 5A Buck-Boost Battery Charger

The BQ25790 is a fully integrated switch-mode buck-boost charger for 1–4 cell Li-ion battery and Li-polymer battery. The integration includes four switching MOSFETs, input and charging current sensing circuits, the battery FET (QBAT) and all the loop compensation of the buck-boost converter. The device provides high power density and design flexibility to charge batteries across the full input voltage range for USB Type-C and USB power delivery (USB-PD) applications such as a smart phone, tablet and other portable devices. The charger supports the narrow VDC power path management, dual-input power selects, fast charging, and autonomous charging mode. The charger also provides various safety features for battery charging and system operations, including battery temperature negative thermistor monitoring, trickle charge, pre-charge and fast charge timers and overvoltage or overcurrent protections on the battery and input. The charger is available in a 56-pin, 2.9mm × 3.3mm WCSP.

2.3.2 TPS3422 Low-Power, Push-Button Controllers With Configurable Delay

The TPS3422 is a push-button reset device with an extended setup period that prevents resets from occurring as a result of short-duration switch closures. The TPS3422 is a single-channel device with an output that asserts when the PB1 input is held low for the push-button timer duration, and de-asserts after the reset time-out duration. The TPS3422 also has a TS pin that selects between two different push-button timing options by connecting the pin to either GND or VCC.

2.3.3 SN74LVC1G74 Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset

This single positive-edge-triggered D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation. NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package. A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

2.3.4 TPS259470 2.7V–23V, 5.5A, 28mΩ True Reverse Current Blocking eFuse

The TPS25947xx family of eFuses is a highly integrated circuit protection and power management design in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short circuits, voltage surges, reverse polarity and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making these devices well suited for power MUX or ORing applications as well as systems which need load side energy hold up storage in case input power supply fails. The devices use a linear ORing-based scheme to provide almost zero DC reverse current and emulate ideal diode behavior with minimum forward voltage drop and power dissipation. Output slew rate and inrush current can be adjusted using a single external capacitor. Loads are protected from input overvoltage conditions either by clamping the output to a safe fixed maximum voltage (pin selectable), or by cutting off the output if input exceeds an adjustable overvoltage threshold. The devices respond to output overload by actively limiting the current or breaking the circuit. The output current limit threshold as well as the transient overcurrent blanking timer are user adjustable. The current limit control pin also functions as an analog load current monitor. The devices are available in a 2mm × 2mm,10-pin HotRod QFN package for improved thermal performance and reduced system footprint.

2.3.5 TPS54218 2.95V to 6V Input, 2A Synchronous Step-Down SWIFT™ Converter

TheTPS54218 device is a full-featured, 6V, 2A, synchronous, step-down current-mode converter with two integrated MOSFETs. The TPS54218 device enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2MHz switching frequency, and minimizing the device footprint with a small, 3mm × 3mm, thermally enhanced, QFN package.

2.3.6 TPS54318 2.95V to 6V Input, 3A Synchronous Step-Down SWIFT™ Converter

TheTPS54318 device is a full-featured, 6V, 3A, synchronous, step-down current-mode converter with two integrated MOSFETs. The TPS54318 device enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2MHz switching frequency, and minimizing the device footprint with a small, 3mm × 3mm, thermally enhanced, QFN package.

2.3.7 LM5158 2.2MHz, Wide V_{IN}, 85V Output Boost, SEPIC, or Flyback Converter

The LM5158 is a wide input range, nonsynchronous boost converter with an integrated 85V,3.26A power switch. The device can be used in boost, SEPIC, and flyback topologies. The LM5158 can start up from a single-cell battery with a minimum of 3.2V and can operate with the input supply voltage as low as 1.5V if the BIAS pin is greater than 3.2V. The BIAS pin operates up to 60V (65V absolute maximum). The switching frequency is dynamically programmable from 100kHz to 2.2MHz with an external resistor. Switching at 2.2MHz minimizes AM band interference and allows for a small design size and fast transient response. The device provides a selectable Dual Random Spread Spectrum to help reduce the EMI over a wide frequency range.

2.3.8 TPS61178 20V Fully Integrated Sync Boost With Load Disconnect

The TPS61178x family is a 20V synchronous boost converter with the gate driver built-in for load disconnect. The TPS61178x integrates two low on-resistance power FETs: a 16mΩ switching FET and a 16mΩ rectifier FET. The TPS61178x uses the fixed-frequency peak current mode control with the slope compensation integrated. At the light load, the TPS61178 enters into the auto PFM mode while TPS611781 is in the forced PWM mode.

2.3.9 LMZM23601 36V, 1A Step-Down DC-DC Power Module in 3.8mm × 3mm Package

The LMZM23601 integrated-inductor power module is specifically designed for space-constrained industrial applications. The device is available in two fixed output voltage options of 5V and 3.3V, and an adjustable (ADJ) output voltage option supporting a 1.2V to 15V range. The LMZM23601 has an input voltage range of 4V to 36V and can deliver up to 1000mA of output current. This power module is extremely easy to use, requiring only 2 external components for a 5V or 3.3V output design. All aspects of the LMZM23601 are optimized for performance-driven and low-EMI industrial applications with space-constrained needs. An open-drain, power-good output provides a true indication of the system status and negates the requirement for an additional supervisory component, saving cost and board space. Seamless transition between PWM and PFM modes along with a no-load supply current of only 28µA provides high efficiency and excellent transient response for the entire load-current range. For easy output current scaling, the LMZM23601 is pin-to-pin compatible with the 500mA output current capable LMZM23600.

2.3.10 TPS7A39 Dual, 150mA, Wide-V_{IN}, Positive and Negative Low-Dropout (LDO) Voltage Regulator

The TPS7A39 device is a dual, monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150mA of current. The regulated outputs can be independently and externally adjusted to symmetrical or asymmetrical voltages, making this device an excellent dual, bipolar power supply for signal conditioning.

2.3.11 TPS74401 3.0A, Ultra-LDO With Programmable Soft Start

The TPS74401 low-dropout (LDO) linear regulators provide an easy-to-use robust power-management design for a wide variety of applications. The user programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and application-specific integrated circuits (ASICs). The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility lets the user configure a design that meets the sequencing requirements of FPGAs, digital signal processors (DSPs), and other applications with specific start-up requirements. A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. The TPS74401 family of LDOs is stable without an output capacitor or with ceramic output capacitors. The device family is fully specified from T_J = –40°C to 125°C. The TPS74401 is offered in two 20-pin small VQFN packages (a 5mm × 5mm RGW and a 3.5mm × 3.5mm RGR package), yielding a highly compact total design size. For applications that require additional power dissipation, the DDPAK (KTW) package is also available.

2.3.12 TPS7A96 2A, Ultra-Low Noise, Ultra-high PSRR RF Voltage Regulator

The TPS7A96 is an ultra-low noise (0.5µV_{RMS}), low dropout (LDO) voltage regulator capable of sourcing 2A with only 200mV of dropout. The low dropout, in conjunction with a wide bandwidth error amplifier, allows for very high Power Supply Rejection Ratio (PSRR) (104dB at 1kHz and 48dB at 1MHz) under low operating headroom (500mV) and high output current (1.75A). The device output is adjustable from 0.4V to 5.5V with an external resistor. With the wide input voltage range, the device supports operation as low as 1.9V and up to 5.7V. The device includes a programmable current limit, programmable PG threshold, and precision enable, allowing better control in the application. With the high-accuracy reference and wide-bandwidth topology, the device can be easily paralleled to achieve lower noise and higher current. With 1% output voltage accuracy (over line, load, and temperature) and soft-start capabilities to reduce inrush current, the device is designed for powering sensitive analog low-voltage devices.

2.3.13 LM3880 3-Rail Simple Power Sequencer With Fixed Time Delay

The LM3880 simple power supply sequencer offers the easiest method to control power-up sequencing and power-down sequencing of multiple independent voltage rails. By staggering the start-up sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system. Available in a 6-pin SOT-23 package, the simple sequencer contains a precision enable pin and three open-drain output flags. The open-drain output flags permit outputs can be pulled up to distinct voltage supplies separate from the sequencer VDD (only if these outputs do not exceed the recommended maximum voltage of 0.3V greater than VDD), so as to interface with ICs requiring a range of different enable signals. When the LM3880 is enabled, the three output flags sequentially release, after individual time delays, thus permitting the connected power supplies to start-up. The output flags follow a reverse sequence during power down to avoid latch conditions.

2.3.14 DAC53401 10-Bit, Voltage-Output DAC With Nonvolatile Memory

The 10-bit DAC53401 is a buffered voltage-output digital-to-analog converter (DAC). The device consumes very low power, and is available in a tiny 8-pin WSON package. The feature set combined with the tiny package and low power make the DAC53401 an excellent choice for applications such as LED and general-purpose bias point generation, power supply control, digitizers, PWM signal generation, and medical alarm tone generation. These devices have nonvolatile memory (NVM), an internal reference, and a PMBus-compatible I^2C interface. The DAC53401 operates with either an internal reference or the power supply as a reference, and provides full-scale output of 1.8V to 5.5V. The devices communicate through the I^2C interface. The devices support I^2C standard mode, fast mode, and fast+ mode. The DAC53401 is feature rich, and includes PMBus voltage margin commands, user-programmable power up to high impedance, standalone waveform generator, medical alarm tone generator, dedicated feedback pin, and more. The DAC53401 operates within the temperature range of –40°C to +125°C.

2.3.15 INA231 28V, 16-bit, I^2C Output Current, Voltage, and Power Monitor With Alert in WCSP

The INA231 is a current-shunt and power monitor with a 1.8V compliant I2C interface that features 16 programmable addresses. The INA231 monitors both shunt voltage drops and bus supply voltage, providing increased protection by asserting the ALERT pin if the values are outside the programmed range. Programmable calibration value, conversion time, and averaging, combined with an internal multiplier, enable direct readouts of current in amperes and power in watts, thus reducing host processing.

3 System Design Theory

This section describes the detailed implementation of each portion of the power supply and data communication implementation.

3.1 Input Section

The power-supply board gets 5V input from the transmitter and receiver board (main board). The main board has a USB Type-C connector for communication with an external imaging device and powers the device. The input section also includes an input power measurement circuit that uses INA231 to continuously measure the current, USB bus voltage, and real-time power consumption of the system. Figure 3-1 shows the schematic of the previously-discussed implementation.

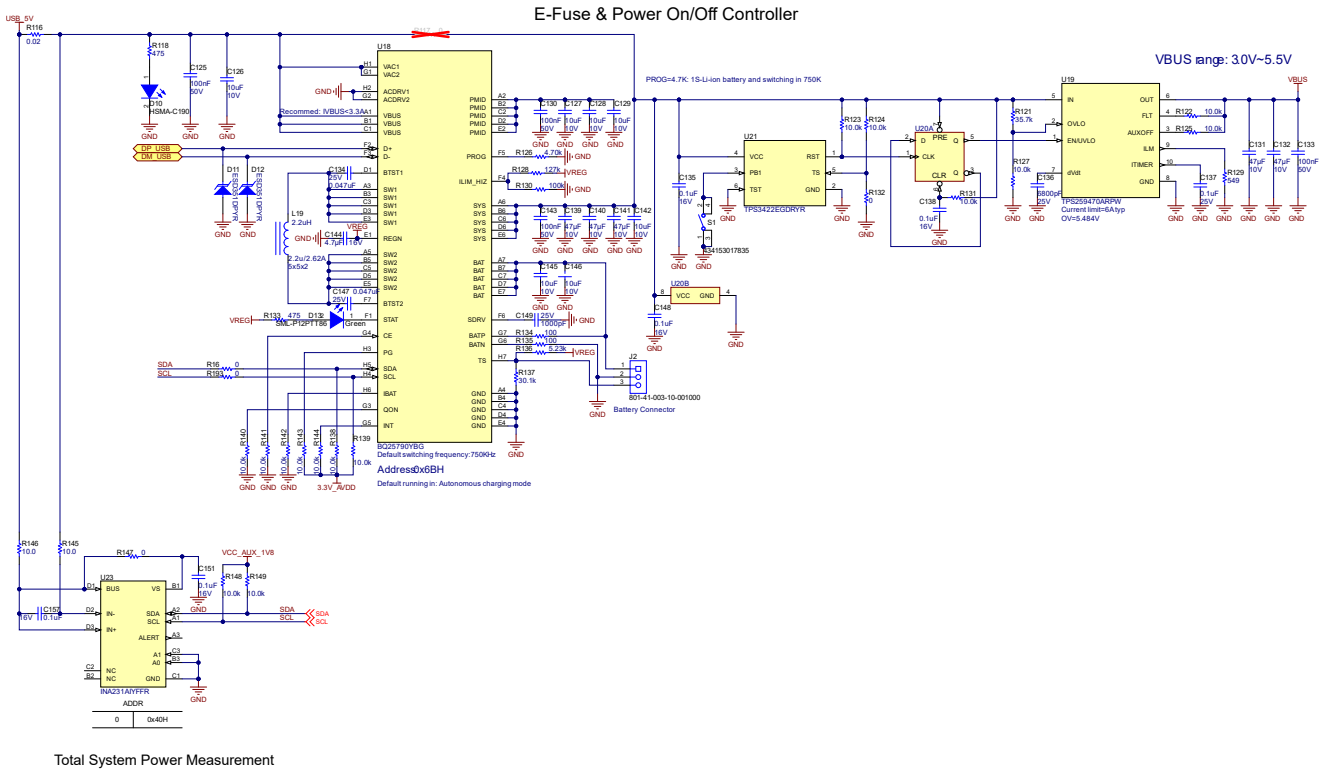


Figure 3-1. TIDA-010269 Input Section

3.1.1 Buck-Boost Charger

The first stage uses a BQ25790 buck-boost charger. The charger uses a 1-cell Li-ion or Li-polymer battery. The chip also integrates a smart power path function which can keep the system operating even when the battery is completely discharged or removed. When the load power exceeds the input source rating or is removed, the battery goes into supplemental mode and prevents the input source from being overloaded and the system from crashing. In the absence of input sources, BQ25790 supports the USB On-the-Go (OTG) function, discharging the battery to generate an adjustable 2.8V–22V voltage on VBUS with a 10mV step size. This action is compliant to the USB PD 3.0 specification defined by the programmable power supply (PPS) feature and can charge an external device. Besides the I^2C host-controlled charging mode, this charger also supports autonomous charging mode. After power up, the charging is enabled with default register settings. The device can complete a charging cycle without any software engagements. The BQ25790 detects battery voltage and charges the battery in different phases: trickle charging, pre-charging, constant current (CC) charging, and constant voltage (CV) charging. At the end of the charging cycle, the charger automatically terminates when the charge current is below a pre-set limit (termination current) in the constant voltage phase. When the full battery falls below the recharge threshold, the charger automatically starts another charging cycle.

TI uses autonomous mode to charge the battery but keeps the I^2C interface in this reference design. The designer can configure the PROG pin of BQ25790 with a 4.7kΩ resistor to ground and set up a switching frequency to 750kHz and default charge current to 2A. Tie VAC1 and VAC2 to VBUS and connect ACDRV1 and ACDRV2 to GND since there is only one USB Type-C connector for the external adapter and no external ACFET-RBFET. Equation 1 shows the input current limit setting calculation.

$$I_{input\_limit} = \frac{V_{ILIM} - 1}{0.8} = \frac{\frac{V_{REGN} \times R_{130}}{R_{128} + R_{130}} - 1}{0.8} \quad (1)$$

The designer can update R128 and R130 to get to the expected current limit. In this reference design, the designer follows the EVM board to configure the current limit at 1.4A.

3.1.2 Power On or Off

In an actual application, the end-user potential needs to power off the smart probe when the diagnosis is completed and save battery power. The TPS3422, SN74LVC1G74, and TPS259470 devices comprise a power on power off circuit. When the user pushes the button, the TPS3422 releases a pulse, this pulse is fed to a D-type flip-flop and drives the D-type flip-flop to high and the latch to a high level. The high level of the D-type flip-flop causes the TPS259470 to power on. The TPS3422 releases another pulse if user pushes the button again, then the pulse drives the D-type flip-flop to low level. The low level shuts down the TPS259470 and the smart probe powers off. The circuit repeats the previous steps if the user pushes the button again. During power on, the D-type flip-flop is cleared and reset, then the output of the D-type flip-flop is low level, so the circuit is in power off status. Figure 3-2 shows the scheme of power on or off.

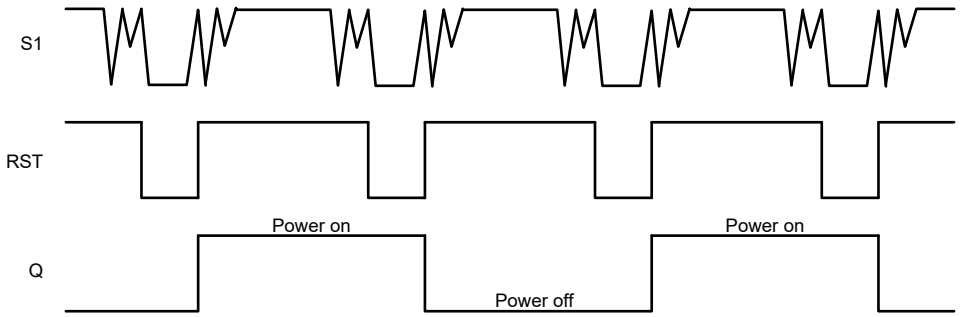


Figure 3-2. Power On or Off Scheme

3.2 Designing SEPIC and Cuk Based High-Voltage Power Supply

A high-voltage power supply is essential for ultrasound imaging. Designing a high-voltage power supply for ultrasound smart-probe applications is challenging since the design must compromise between efficiency, volume, height, and so forth. This reference design is based off of the legacy TIDA-010057 design but with new parts to save PCB area and to keep costs down.

3.2.1 Basic Operation Principle of SEPIC and Cuk Converters

In a single-ended primary inductance converter (SEPIC) and Cuk design, the output voltage can be higher or lower than the input voltage. Figure 3-3 shows the SEPIC topology using the two inductors: L1, L2 and Figure 3-4 shows the Cuk converter topology using the L3 and L4 inductors. The two inductors can be wound on the same core, or uncoupled since the same voltages are applied to them throughout the switching cycle. Figure 3-3 and Figure 3-4 illustrate that the Cuk topology was obtained by the exchange position of the diode and second inductor with the SEPIC topology.

Note

The output of Cuk is negative or minus but the output of SEPIC is positive.

To understand the voltages of the various circuit nodes for the SEPIC converter, analyze the circuit at DC when Q1 is off and not switching. During steady-state CCM, pulse-width modulation (PWM) operation, and neglecting ripple voltage, capacitor C1 is charged to the input voltage, V_{in}. When Q1 is off, the voltage across L2 must be

V_{out}. So, the voltage across Q1 when Q1 is switched off is equal to V_{in} + V_{out}, then the voltage across L1 is V_{out}. When Q1 is on, capacitor C1, charged to V_{in}, is connected in parallel with L2, so the voltage across L2 is $–V_{in}$.

Figure 3-3 shows the currents flowing through various circuit components. When Q1 is on, energy is being stored in L1 from the input and in L2 from C1. When Q1 turns off, the L1 current continues to flow through C1 and D1, and into C2 and the load. Both C1 and C2 get recharged to provide the load current and charge L2, respectively, when Q1 turns back on (see Figure 3-3 and Figure 3-5), see the *AN-1484 Designing A SEPIC Converter* application note.

To understand the voltages of at the various circuit nodes for the Cuk converter, analyze the circuit at DC when Q2 is off and not switching. During steady-state CCM, pulse-width modulation (PWM) operation, and neglecting ripple voltage, capacitor C3 is charged to $V_{in} – V_{out}$. When Q2 is off, the voltage across L4 must be V_{out}. The voltage across Q1 when Q1 is switched off equals $V_{in} – V_{out}$, then the voltage across L3 is $–V_{out}$. When Q2 is on, capacitor C3 is charged to $V_{in} – V_{out}$, thus connected in series with L4, so the voltage across L4 is $–V_{in}$. Figure 3-4 shows the currents flowing through various circuit components. When Q2 is on, energy is being stored in L3 from the input and in L4 from C3. When Q2 turns off, the current from L3 continues to flow through C3 and D2, the current of L4 is charged into C4 and the load. Both C3 and C4 get recharged so that these capacitors can provide the load current and charge L4, respectively, when Q1 turns back on. See Figure 3-4 and Figure 3-6 and see *TI-Cuk training* for more information.

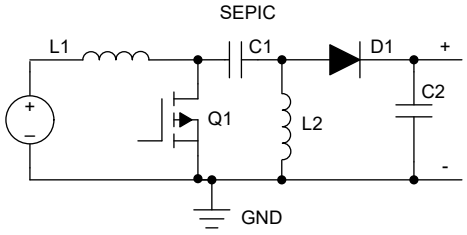


Figure 3-3. SEPIC Topology

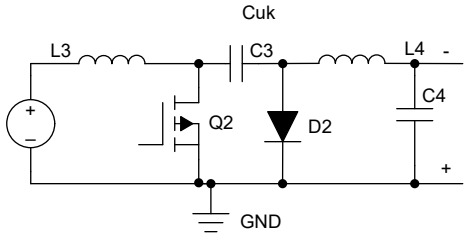


Figure 3-4. Cuk Converter Topology

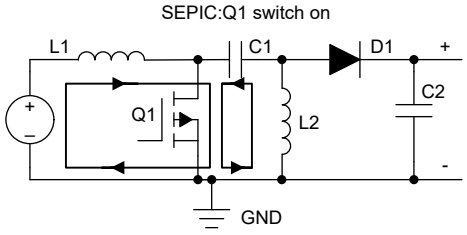


Figure 3-5. Current Loop When the SEPIC MOSFET Switch is On

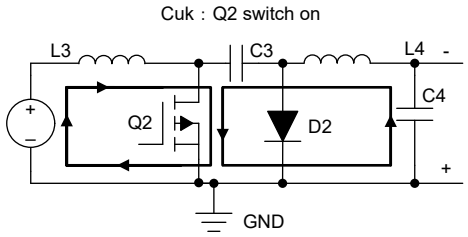


Figure 3-6. Current Loop When the Cuk MOSFET Switch is On

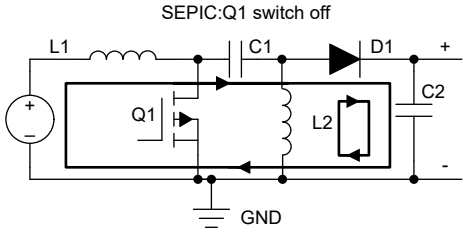


Figure 3-7. Current Loop When SEPIC MOSFET Switch is Off

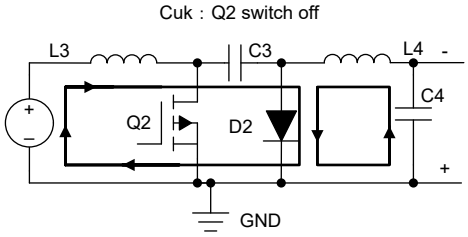


Figure 3-8. Current Loop When Cuk MOSFET Switch is Off

The formulas for the duty cycle between input voltage and output voltage for SEPIC (Equation 2) and Cuk (Equation 3) follow:

$$D = \frac{V_{output} + V_D}{V_{in} + V_{output} + V_D} \quad (2)$$

$$D = \frac{-V_{output} + V_D}{V_{in} - V_{output} + V_D} \quad (3)$$

Equation 2 and Equation 3 are exactly same since the output of Cuk is negative. Here V_{in} is input voltage, V_D is forward voltage of diode, V_{output} is output voltage. This hints that the output voltage keeps the amplitude the same, and under control if the load is same.

Equation 4 (SEPIC) and Equation 5 (Cuk) show the voltage calculation that MOSFET maximum endures during switching.

$$V_{Q1} = V_{in} + V_{output} + V_D + \frac{V_{C1\_ripple}}{2} \quad (4)$$

$$V_{Q2} = V_{in} - V_{output} + V_D + \frac{V_{C3\_ripple}}{2} \quad (5)$$

Equation 6 (SEPIC) and Equation 7 (Cuk) show the maximum voltage that the diode endures during switching.

$$V_{D1} = V_{in} + V_{output} + V_D + \frac{V_{C1\_ripple}}{2} \quad (6)$$

$$V_{D2} = V_{in} - V_{output} + V_D + \frac{V_{C3\_ripple}}{2} \quad (7)$$

Equation 8 (SEPIC) and Equation 9 (Cuk) show the maximum voltage that the couple capacitor can endure during switching.

$$V_{C1} = V_{in} + \frac{V_{C1\_ripple}}{2} \quad (8)$$

$$V_{C3} = V_{in} - V_{output} + \frac{V_{C3\_ripple}}{2} \quad (9)$$

Figure 3-9 and Figure 3-10 show the typical node waveform for SEPIC and Cuk, respectively.

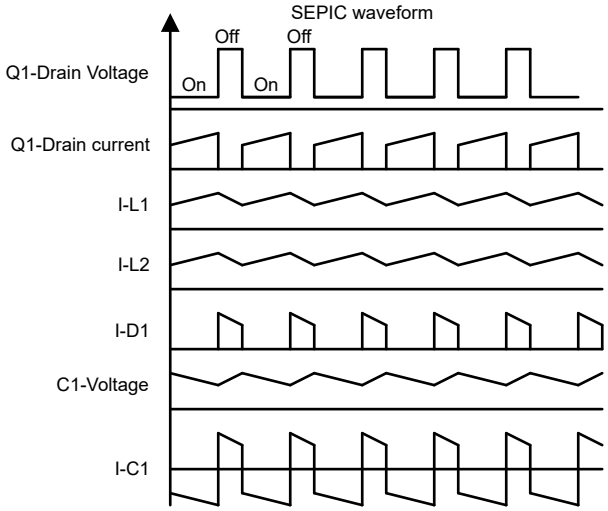


Figure 3-9. SEPIC Switching Waveforms

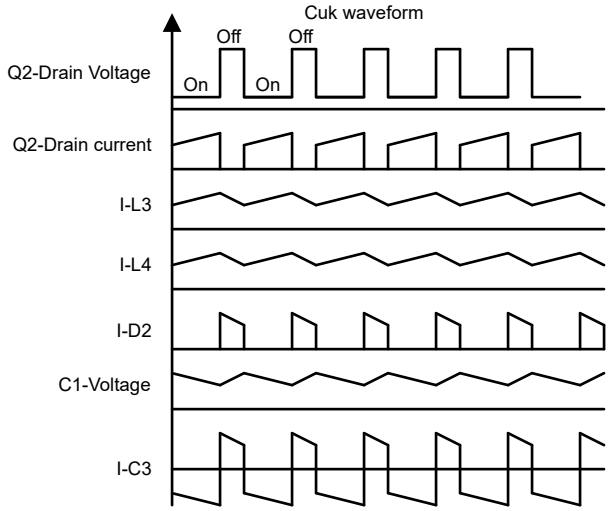


Figure 3-10. Cuk Converter Switching Waveforms

In ultrasound smart-probe imaging applications, the transmitter needs an amplitude that equals the positive and negative high-voltage power supply with a small package. As previously-mentioned, the designer can merge SEPIC and Cuk topologies together to meet the smart-probe application requirements. The output of positive and negative has an equal amplitude since the load in the ultrasound application is matched under any conditions, in theory, and the duty-cycle is exactly same for SEPIC and Cuk. So, in this reference design, SEPIC and Cuk topology was merged to generate a high-voltage power supply from a low-input voltage.

3.2.2 Dual High-Voltage Power Supply Design Using Uncoupled Inductors With SEPIC and Cuk

This section describes the implementation of the dual high-voltage supply using uncoupled inductors. The specifications of the dual supply are described in Table 1-1. Section 3.2.2.1 through Section 3.2.2.8 provide a step-by-step method to design the supply. This system can be thought of as two parallel output stages coupled through capacitors C1 and C15 with the primary side as shown in Figure 3-11. To create a high-voltage dual supply, the output stage of the high-voltage power supply (HVPS) was designed differently. As Figure 3-11 shows, the output capacitors are charged to the positive rail of 75V for the top stage (SEPIC). Similarly, the output capacitors of the bottom stage are charged to a negative supply of –75V (Cuk). This is due to the inclusion of the HVGND in Figure 3-11 between R7, R11, and R13. A dual high-voltage power supply was achieved using HVGND. Following the output of both rails, a Pi and Power Filter were used to attenuate the ripple of the high-voltage supply.

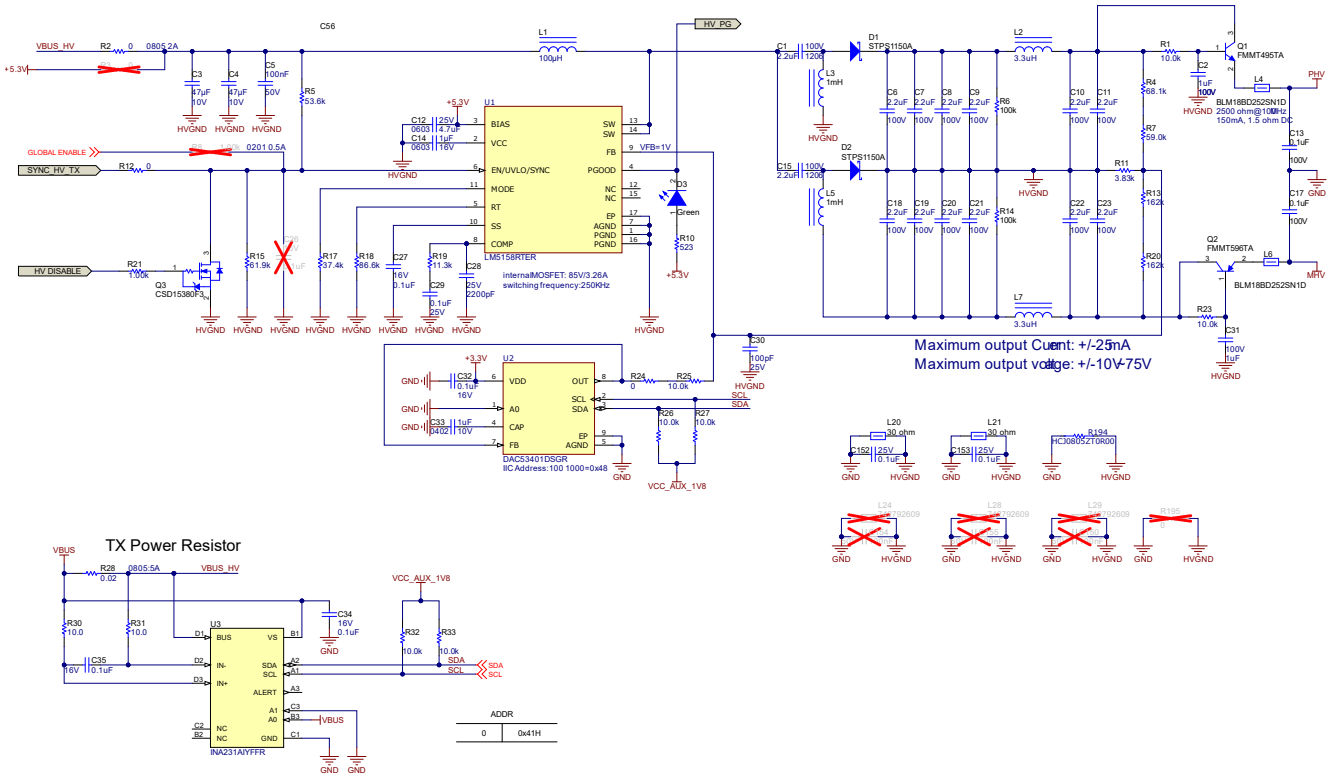


Figure 3-11. SEPIC and Cuk Converter Schematic

3.2.2.1 Duty Cycle

For a SEPIC converter operating in a continuous conduction mode (CCM) use Equation 10 to calculate the duty cycle.

$$D = \frac{V_{output} + V_D}{V_{in} + V_{output} + V_D} \quad (10)$$

For the high-voltage designs used in this reference design, the LM5158 can reach a duty cycle of 93% from 100kHz to 250kHz. Using Equation 10, the calculated duty cycle was 93.8%. So, the parts are running in current discontinue mode slightly. But with internal minimum 3.26A MOSFET and compact size, the parts were selected

for HVPS and can be output maximum ±25mA current. Assume the efficiency of circuit is 0.7, then the input current is (75 × 0.025 × 2) / (5 × 0.7) = 1.072A. The maximum current is approximately 2.57A if the designer selects exactly the same two inductors. It is clear that LM5158 supports a discontinue current mode. V_D is the forward voltage drop of the diode D1.

3.2.2.2 Inductor Selection

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. Equation 11 shows the ripple current flowing in equal value inductors L1 and L2.

$$\Delta I = I_{in} \times 40\% = \frac{V_{output} \times I_{output}}{V_{input} \times \eta} \times 40\% \approx 0.43A \quad (11)$$

Equation 12 and Equation 13 calculate the inductor values.

$$L_1 > \frac{V_{in} \times D}{f_{sw} \times \Delta I} \approx 43.6\mu H \quad (12)$$

$$L_2 > \frac{V_{output}^2 \times (1 - D)}{R \times f_{sw} \times P_{output}} = 897.2\mu H \quad (13)$$

The inductor value chosen for L1 was 100µH and 1000µH for L2 for easier component selection and availability.

The switching frequency is f_{sw} and D_{max} is the duty cycle at the minimum V_{in}. The peak current in the inductor, to make sure the inductor does not saturate, is calculated using Equation 14 and Equation 15.

$$I_{L1\_peak} = I_{output} \times \frac{V_{output} + V_D}{V_{in\_min} \times \eta} \times 1.2 = 2.17A \quad (14)$$

$$I_{L2\_Peak} = I_{out} \times \left(1 + \frac{40\%}{2}\right) = 30mA \quad (15)$$

3.2.2.3 Power MOSFET Verification

The parameters governing the selection of the MOSFET are the minimum threshold voltage $V_{th(min)}$, the on-resistance $R_{DS(on)}$, gate-drain charge Q_{GD}, and the maximum drain-to-source voltage, $V_{DS(max)}$. Use logic level or sublogic-level threshold MOSFETs based on the gate-drive voltage. The peak switch voltage is equal to V_{in} + V_{out}. Equation 16 shows the peak switch current calculation.

$$I_{MOSFET\_Peak} = I_{L1\_Peak} + I_{L2\_Peak} + I_{L3\_Peak} \approx 2.23A \quad (16)$$

Equation 17 calculates the peak switch voltage.

$$V_{Q1} = V_{in} + V_{output} + V_D + \frac{V_{C1\_ripple}}{2} = 82V \quad (17)$$

Equation 18 shows RMS current calculation through the switch.

$$I_{MOSFET\_RMS} = I_{output}\sqrt{\frac{(V_{output} + V_{input\_min} + V_D) \times (V_{output} + V_D)}{V_{input\_min}^2}} \quad (18)$$

The approximate MOSFET power dissipation P_{Q1} is calculated using Equation 19.

$$P_{MOSFET} = I_{MOSFET\_RMS}^2 \times R_{DS(on)} + (V_{output} + V_{input\_min}) \times I_{MOSFET\_Peak} \times \frac{Q_{GD} \times f_{sw}}{I_G} \quad (19)$$

where

- P_{MOSFET} is the total power dissipation for MOSFETs including conduction loss
- I_{MOSFET_RMS} is the switching loss

- I_G is the gate drive current

Select the $R_{DS(on)}$ value at the maximum operating junction temperature. This value is typically given in the MOSFET data sheet. Make sure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget. The LM5158 internal MOSFET has $V_{DS(max)}$ of 85V and an $R_{DS(on)}$ of 133mΩ.

3.2.2.4 Output Diode Selection

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current I_{Q1}(peak). Equation 20 shows the minimum peak reverse voltage the diode must withstand.

$$V_{D1} = V_{input\_Max} + V_{output} = 85V \tag{20}$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended to minimize the efficiency loss.

3.2.2.5 Coupling Capacitor Selection

The selection of a SEPIC or Cuk couple capacitor, C_S, depends on the RMS current, which is given in Equation 21.

$$I_{CS\_RMS} = I_{output} \times \sqrt{\frac{V_{output} + V_D}{V_{input\_min}}} \tag{21}$$

The SEPIC and Cuk capacitors must be rated for a large RMS current relative to the output power. This property requirement makes the SEPIC a better choice for lower-power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. A capacitor that meets the RMS current requirement mostly produces a small ripple voltage on C_S. Hence, the peak voltage is typically close to the input voltage. The SEPIC couple capacitor (C_S) value is based on a maximum voltage ripple that is based on the minimum input voltage. A maximum voltage ripple (ΔV_C) of 10% is recommended. This voltage ripple and the minimum SEPIC couple capacitor value can be found using Equation 22 and Equation 23.

$$\Delta V_C = 10\,\% \times V_{input\_min} = 0.3V \tag{22}$$

$$C_S = \frac{I_{load} \times D_{max}}{f_{sw} \times \Delta V_C} \approx 0.32\mu F \tag{23}$$

In the actual design, remember that the ceramic capacitor capacitance is greatly reduced with bias voltage. The capacitor capacitance was select here as 2.2µF, 1206, and 100V. So the ripple of nominal couple capacitor is calculated with Equation 24.

$$\Delta V_c = \frac{I_{load} \times D_{max}}{f_{sw} \times C_S} \approx 0.042V \tag{24}$$

3.2.2.6 Output Capacitor Selection

In a SEPIC converter, when the power switch Q1 is turned on, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor experiences large ripple currents. Thus, the selected output capacitor must be capable of handling the maximum RMS current. Equation 25 calculates the RMS current in the output capacitor.

$$I_{C\_output\_RMS} = I_{output} \times \sqrt{\frac{V_{output} + V_D}{V_{input\_min}}} \tag{25}$$

The ESR, ESL, and the bulk capacitance of the output capacitor directly control the output ripple. Assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance. Hence, Equation 26 and Equation 27 show the calculations.

$$ESR \le \frac{V_{ripple} \times 0.5}{I_{L1\_peak} \times I_{L2\_peak}} \le 42m\Omega \quad (26)$$

$$C_{output} \ge \frac{I_{output} \times D}{V_{ripple} \times 0.5 \times f_{sw}} \ge 2.355\mu F \quad (27)$$

The output capacitance must meet the RMS current, ESR and capacitance requirements. In surface mount applications, tantalum, polymer electrolytic, and polymer tantalum, or multilayer ceramic capacitors are recommended at the output.

3.2.2.7 Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor makes sure that the input capacitor experiences fairly low ripple currents. Equation 28 gives the RMS current in the input capacitor.

$$I_{C\_input} = \frac{\Delta I_L}{\sqrt{12}} = 0.18A \quad (28)$$

The input capacitor needs to be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10µF or higher value, a good quality capacitor prevents impedance interactions with the input supply.

3.2.2.8 Programming the Output Voltage With Adjustable function

The output voltage can be programmed with adjustable by using a resistor divider between the output and the feedback pins with a DAC. See Figure 3-12 for details. The resistors are selected such that the voltage at the feedback pin is 1.0V. R_T, R_B, and R_c can be selected using Equation 29.

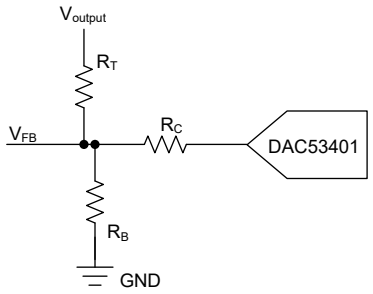


Figure 3-12. Output Adjust Scheme

$$V_{output} = \left(1 + \frac{R_T}{R_B} + \frac{R_T}{R_C}\right) \times V_{FB} - \frac{R_T}{R_C} \times V_{DAC} = \left(1 + \frac{R_T}{R_B} + \frac{R_T}{R_C}\right) - \frac{R_T}{R_C} \times V_{DAC} \quad (29)$$

when

- V_{DAC} = 0, V_{output} = 75V

when

- V_{DAC} = 3.3V, V_{output} = 5V

Fix R_c, then the designer can determine an equation group and can find the R_T and R_B values by solving the equation group.

3.3 Designing the Low-Voltage Power Supply

The different subsystems such as the transmit section, receive section, FPGA, and data section in the design use different power rails. Each of these subsystems have constraints such as analog supply, digital supply, low noise and so forth. The primary point of load is generated by using a switching buck converter followed by an LDO (for noise-sensitive rails). Figure 2-3 shows the block level representation of the various low-voltage rails and the architecture.

3.3.1 Designing the TPS54218 Through WEBENCH® Power Designer

Figure 3-13 shows a WEBENCH® design used to evaluate the TPS54218 with an output voltage of 3.3V at 200mA. The WEBENCH® Power Designer tool allows the user to simulate real-time data for the product selected (efficiency, transient response, start-up and so forth) and a capability to export Altium files to complete a board design.

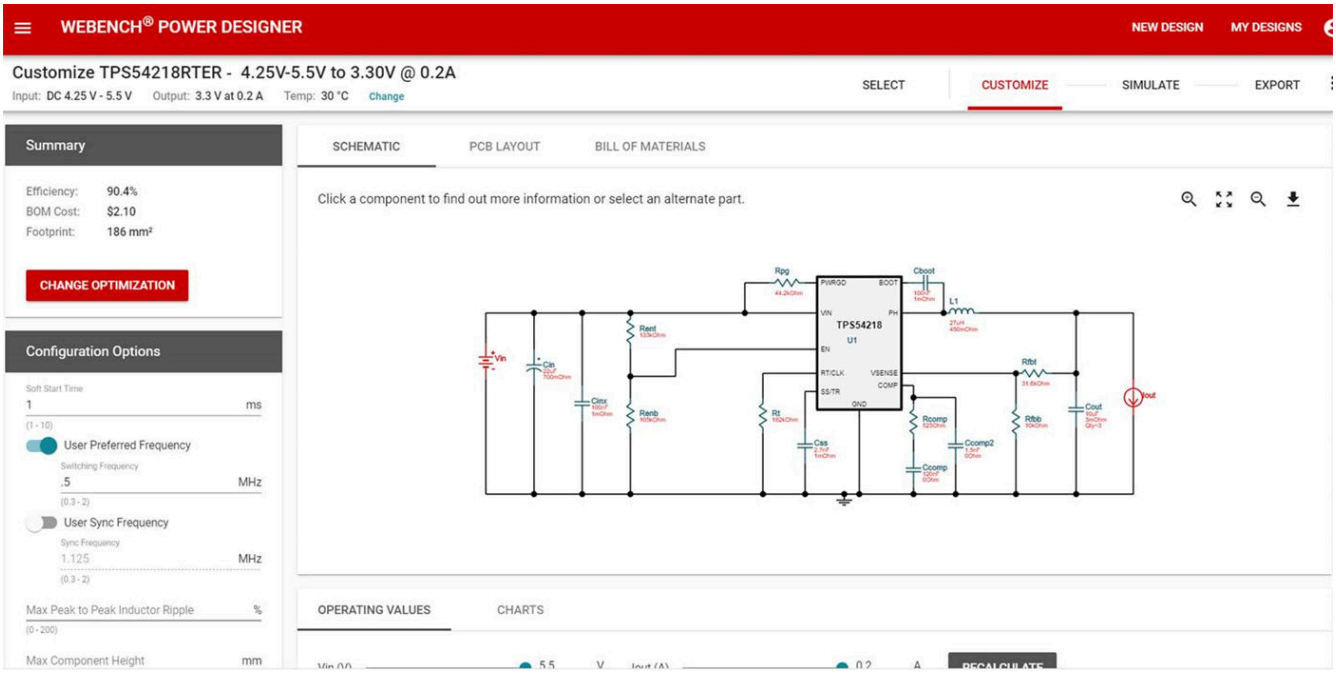


Figure 3-13. WEBENCH® Design Using the TPS54218

For the ultrasound power supply design, the TPS54218 was selected to power the low voltage for the FPGA and the AFEs. Since the size of the total design was a concern, a module was considered. The total system efficiency was evaluated comparing the difference between a power module and a DC/DC converter (internal inductor vs external inductor). The DC/DC converter design (TPS54218) allowed for more flexibility by increasing the inductor value, which led to an increase in efficiency.

When comparing how different inductor values affect the efficiency of a buck converter, the TPS54218 was evaluated with two different inductor values. In Figure 3-14, the TPS54218 efficiency was tested for two different inductor values (2.2µH versus 33µH) using a load generator. For light load conditions, the 33µH inductor had a much higher efficiency when compared to the 2.2µH design. This is due to the AC conduction losses of the inductor which decrease the efficiency of the design. Moving forward for the low-voltage power supply design, a 33µH inductor was chosen to improve the efficiency.

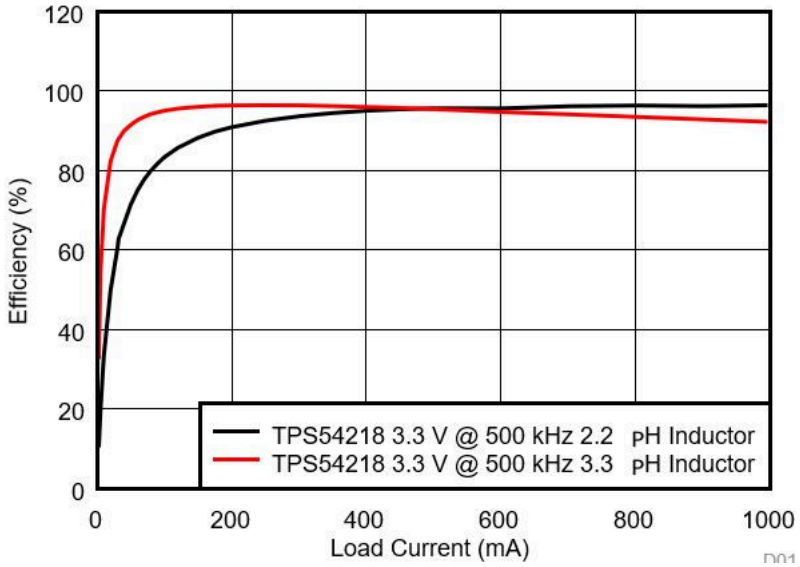


Figure 3-14. TPS54218 Efficiency (2.2µH vs 33µH)

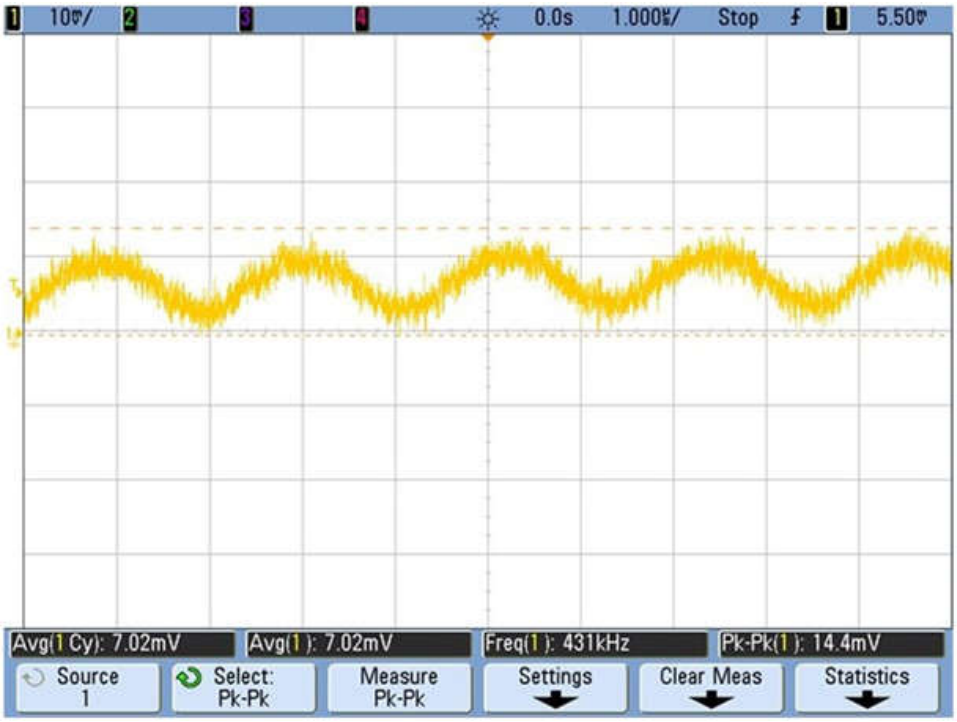


Figure 3-15. TPS54218 2V Supply Output Voltage Ripple

Figure 3-15 shows the 2V supply output voltage ripple of the TPS54218. The measured peak-to-peak ripple was measured at 14.4mV. The remaining low-voltage power supplies all had an output voltage ripple of less than 10mV.

3.3.2 ±5V Transmit Supply Generation

Figure 3-16 shows the transmit ±5V rail schematic. The boost device TPS61178 boosts the USB voltage (4.25V to 5.5V) to 5.7V and the LMZM23601 device which is set up in inverting buck mode generates –5.3V. Both the positive and the negative outputs are fed to the dual low noise TPS7A39 LDO to generate ±5V at a maximum of 150mA per rail. The TPS61178 device is also useful in the situation where the high-voltage requirement is high (100V) or the system is powered using the 3.6V (1S battery) source. This stage can be used as an intermediate input to the high-voltage circuit. This can be enabled by setting the required output voltage using the resistor divider (R95 and R98), then removing R2 to disable the existing USB input to the high-voltage circuit and placing R3, 0Ω resistor as the input.

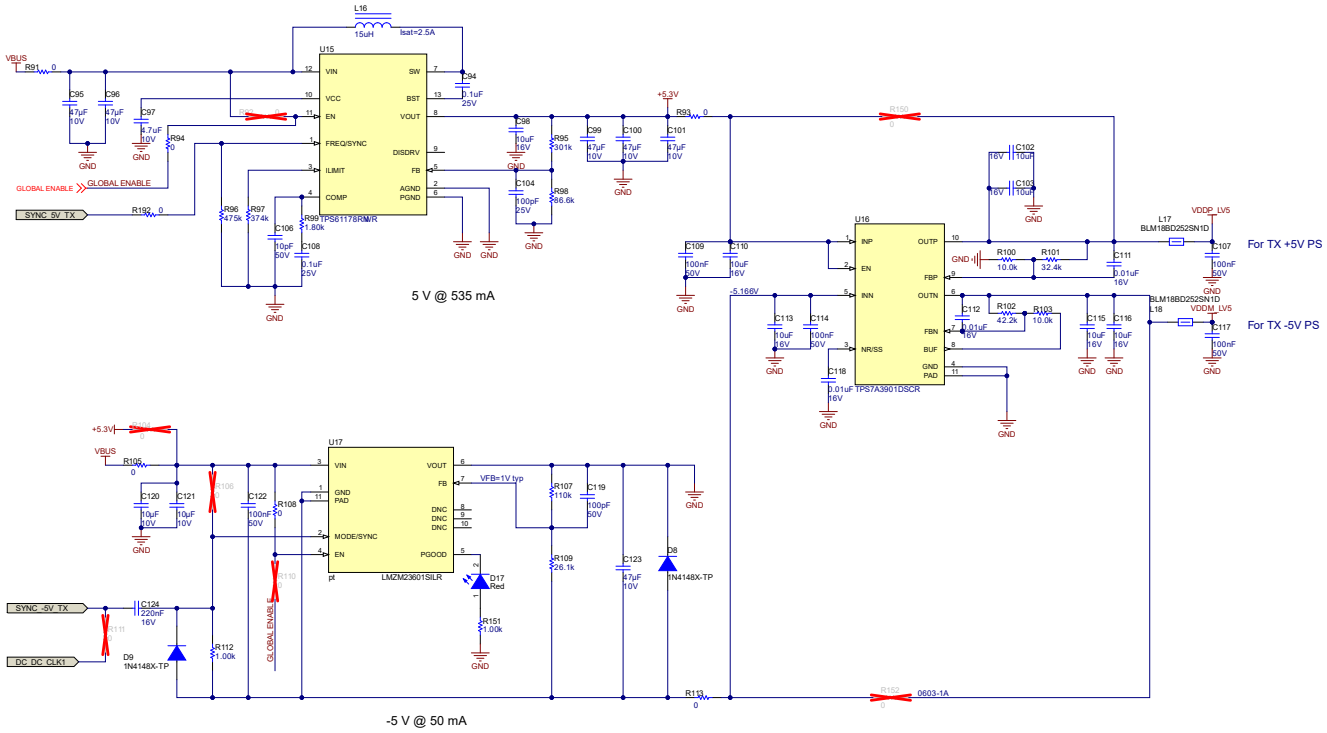


Figure 3-16. ±5V Transmit Circuit Schematic

The TPS61178 device also has a true load-disconnect feature (not implemented in the existing design). Placing an external P-FET between the output and the point of load, the device has a DISDRV pin which can be used to turn off the FET in case of any short conditions. This feature is particularly useful when using an intermediate boost stage to power the high-voltage circuit. The input to the high-voltage circuit can be completely cut off in case any output short occurs; therefore, protecting the circuitry. The user can implement the same in a design providing a more robust system. Figure 3-17 shows the implementation of the load disconnect in TPS61178. For detailed information on the FET selection and other aspects, see the *application and implementation* section of the device data sheet.

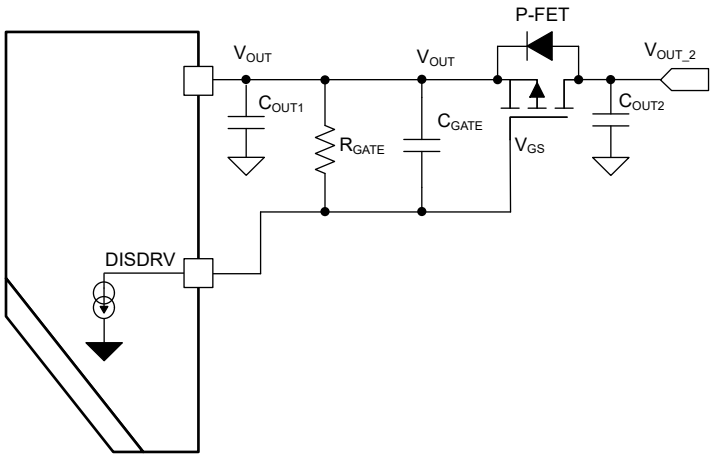


Figure 3-17. Load Disconnect FET Connected in TPS61178

3.4 System Clock Synchronization

The schematic shown in Figure 3-11 can be synchronized to an external clock signal only if the duty cycle of the latter is larger than the duty cycle of the controller (larger than 93%). This design can be synchronized to an external clock with 50% duty cycle by implementing the design shown in Figure 3-18. The various point-of-load supplies can be synchronized to the external clock which is available on the power connector discussed in Section 3.5. The signal from the clock source pin DC_DC_CLK_1 is further is divided and distributed to respective supplies and the switching frequencies. Figure 3-18 shows the schematic of the implementation. The source clock is first given as an input to the 9-channel integrated clock buffer and divider device CDCE949. The eight outputs are 500kHz for the seven TPS54218 buck devices and one TPS61178 for the 5V rail, the 9th output is 250kHz for the high-voltage circuit. The configuration of the device CDCE949 can be stored in the integrated EEPROM CDCEL9XXPROGEVM or over the I^2C bus. If CDCEL9XXPROGEVM is used, the configuration file is found in the design files.

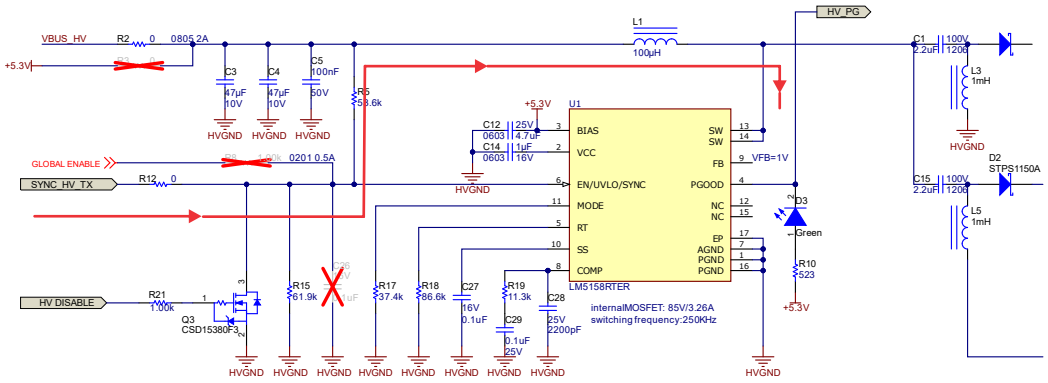


Figure 3-18. External Clock Synchronization Implementation Schematic

The high-voltage circuit can be synchronized to an external clock with 50% duty cycle. The boost regulator (LM5158) imposes a limit on the duty cycle clock pulse width to be larger than the duty cycle of the supply which is very high in the current implementation. Figure 3-18 shows the schematic of the implementation.

3.5 Power and Data Output Connector

Figure 3-19 shows the schematic of the data and power connector placed on the board. Two sets of connectors are placed on the board to connect to the TX + RX AFE board. Multiple signals are also coming from the FPGA to communicate with the FX3 device. A clock signal named DC_DC_CLK 1 of 1MHz frequency comes from the FPGA to be the source clock for the power supply clock synchronization. Different power rails are distributed among the connectors for ease of layout and keeping the routing length short. The high-voltage rails are put separately on two connectors providing equal lengths and separation. The connectors are also routed along the edge of the board to keep the connectors away from sensitive circuitry. The connector used is the Panasonic AXK5S80347YG.

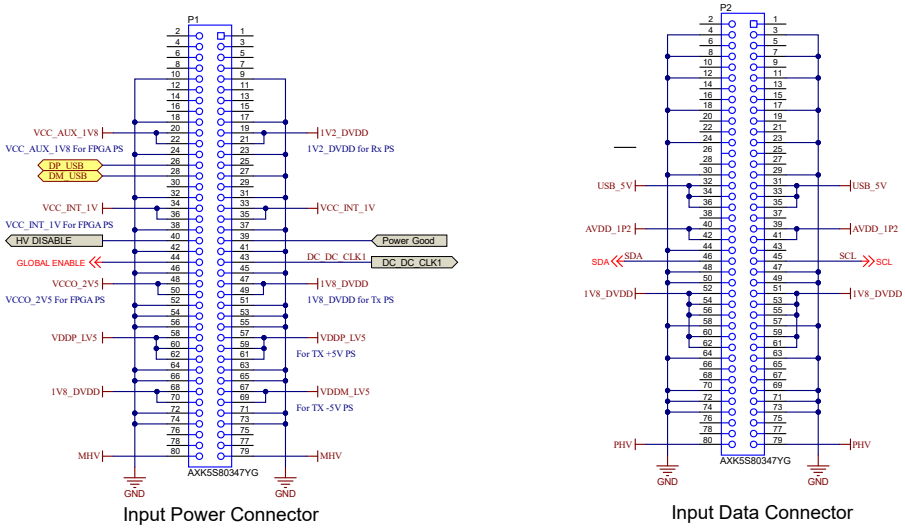


Figure 3-19. Schematic of the Connector Between TIDA-010269 and TX + RX AFE Board

3.6 System Current and Power Monitoring

The TIDA-010269 reference design provides a provision for users to monitor system current, bus-voltage, and power consumption. TI's INA231 28V, 16-bit, I^2C output current, voltage and power monitor is used to monitor various sections of the design similar to TIDA-010057 reference design. Figure 2-3 shows the circuit schematic. Three INA devices are implemented in the schematic. One INA measures the total current and power consumed in the system. The other two INA devices monitor the current and power of the transmitter (TX) and FPGA units respectively. The communication is done through the I^2C interface. The measured voltage, current, and power values can be dynamically plotted against time.

4 Hardware, Testing Requirements, and Test Results

This reference design is built to power an ultrasonic smart probe with a one cell Li-ion battery. The input voltage is in the range of 3V to 5V since the Li-ion battery output voltage is in range of 2.7V to 4.2V with a general stop discharge under 3.0V. The Li-ion battery is charged by an external USB power supply once the voltage drops below 3.0V. The input voltage is in range of 3V to 5V. The power supply board powers the FPGA, transmitter, receiver, and other supporting circuits located in the main board. Figure 2-3 shows the system block diagram of the power supply board. Voltages of 2.5V, 1.0V, and 1.8V were used for the FPGA power supply. A ±5V and adjustable high-voltage was used for the transmitter. The voltages for the receiver circuit were 1.2V and 1.8V. The system also adds a hot-swap and supporting circuits for a power on and power off system. The BQ25790 was used to charge the Li-ion battery. The INA231 device was used to monitor the power and current of the associated subsystem. The LM3880 was used for the power sequence since the receiver has power on sequence requirements. The CDCE949 was used for synchronous with external system clock.

4.1 Hardware Requirements

System performance was tested for efficiency, line regulation, noise, and so forth. The following instruments were used to test power supply performance.

- Digital multimeter
- Electronic load
- Table power supply
- Oscillography

Figure 4-1 shows the test scheme.

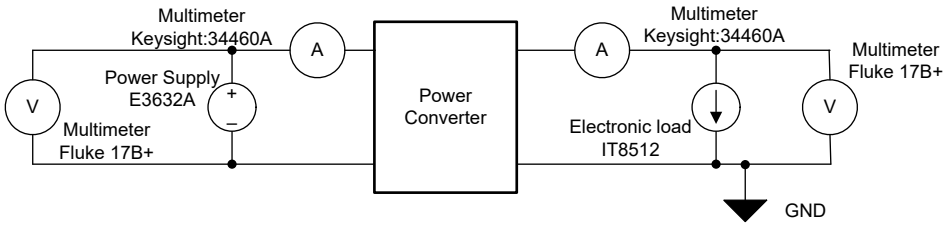


Figure 4-1. Test Scheme

4.2 Test Setup

Figure 4-2 shows the front and back images of the TIDA-010269 board. The EMI shield placed between the AFE and TIDA-010269 board provide EMI reduction. The two connectors dock into the TX + RX board. The TIDA-10269 reference design was evaluated and characterized by using blue wire. There are many 0Ω resistors in every input and output of the power rail. The 0Ω resistor can be removed and a test instrument with blue wires can be inserted.

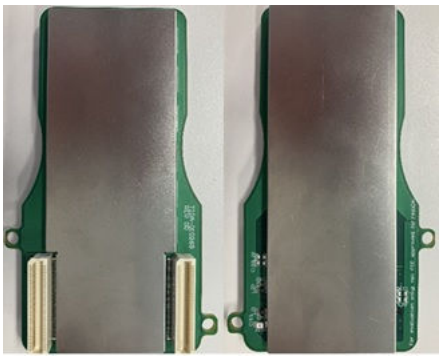


Figure 4-2. Front (Left) and Back (Right) Images of the TIDA-010269 Board

4.3 Test Results

4.3.1 Efficiency Test Result

Efficiency is important for this handheld device. The graphs in Figure 4-3 through Figure 4-10 show the efficiency of the power rails under different load currents.

Figure 4-3. FPGA 2.5V Efficiency

Figure 4-4. FPGA 1.0V Efficiency

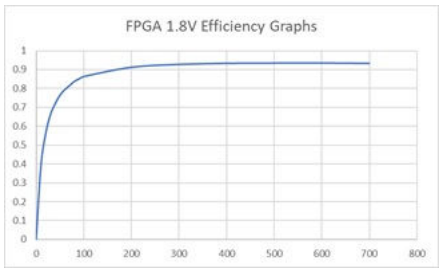


Figure 4-5. FPGA 1.8V Efficiency

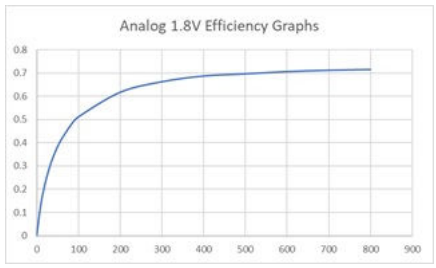


Figure 4-6. AVDD 1.8V Efficiency

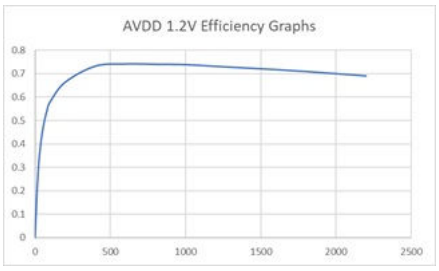


Figure 4-7. AVDD 1.2V Efficiency

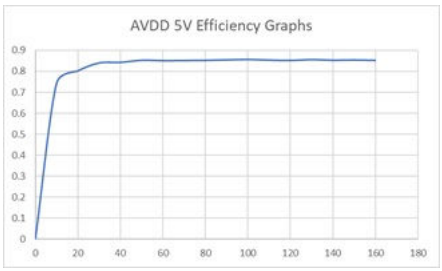


Figure 4-8. AVDD 5V Efficiency

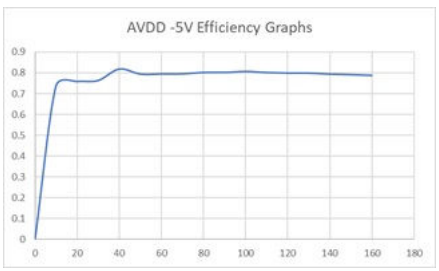


Figure 4-9. AVDD –5V Efficiency

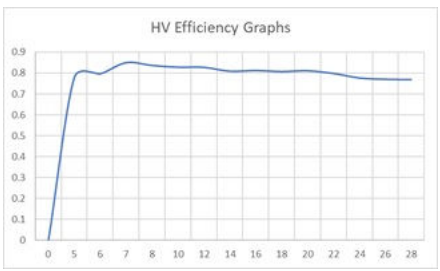


Figure 4-10. High-Voltage Efficiency

4.3.2 Line Regulation Testing Result

The line regulation test is mainly used to test the response of the power supply under different loads. Figure 4-11 through Figure 4-18 show the test results.

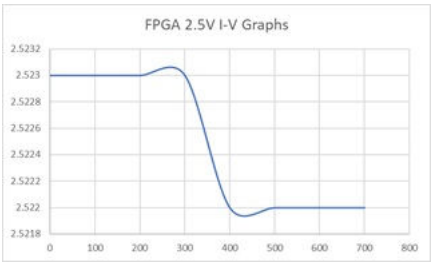


Figure 4-11. FPGA 2.5V Line Regulation Test Result

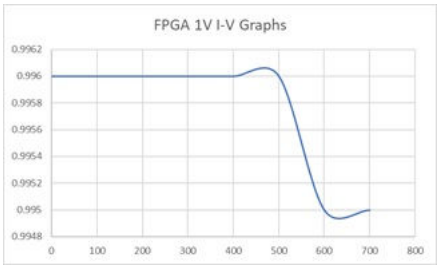


Figure 4-12. FPGA 1.0V Line Regulation Test Result

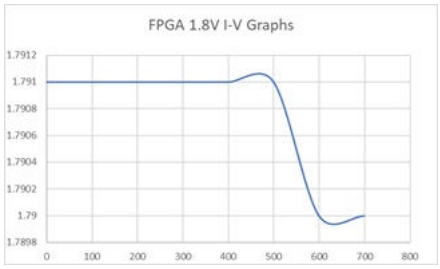


Figure 4-13. FPGA 1.8V Line Regulation Test Result

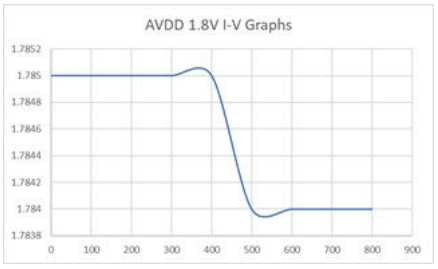


Figure 4-14. AVDD 1.8V Line Regulation Test Result

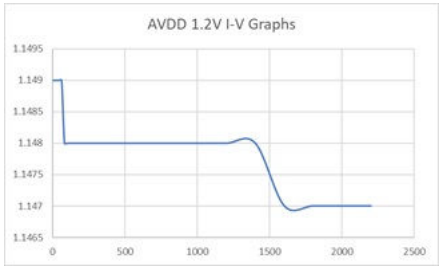


Figure 4-15. AVDD 1.2V Line Regulation Test Result

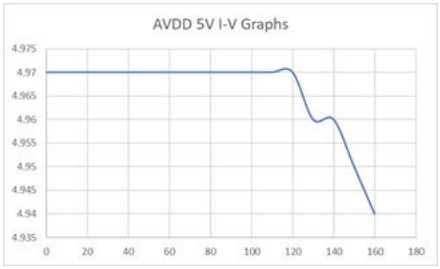


Figure 4-16. AVDD 5V Line Regulation Test Result

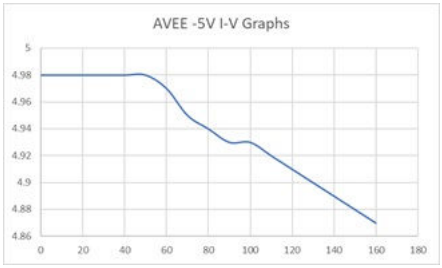


Figure 4-17. AVDD –5V Line Regulation Test Result

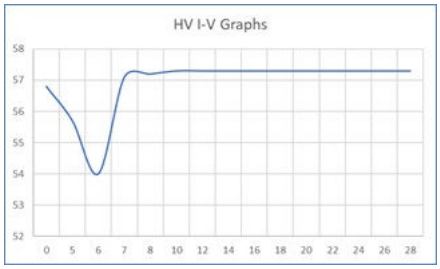


Figure 4-18. High-Voltage Line Regulation Test Result

4.3.3 Spectrum Test Result

Spectrum analysis can help a designer to evaluate the harmonic of the output power supply and then evaluate the noise performance. Figure 4-19 through Figure 4-37 show the testing results.

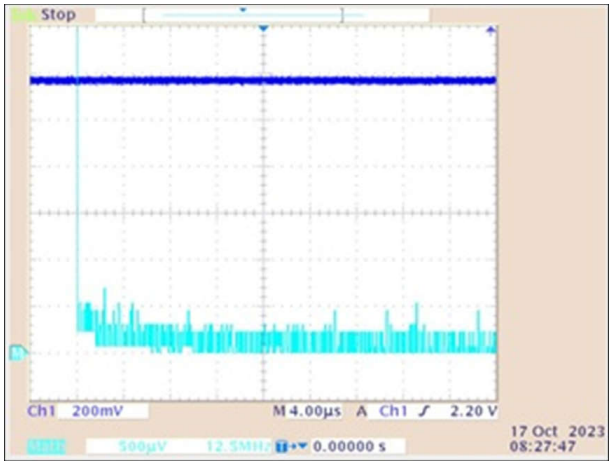


Figure 4-19. AVDD 1.2V Output and Spectrum Under DC Mode

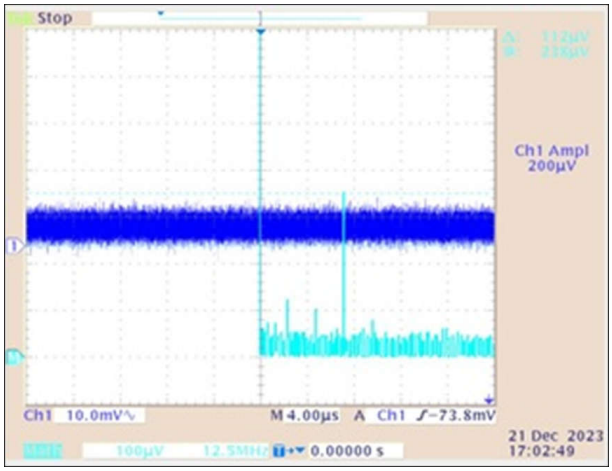


Figure 4-20. AVDD 1.2V Output and Spectrum Under AC Mode With Full Load

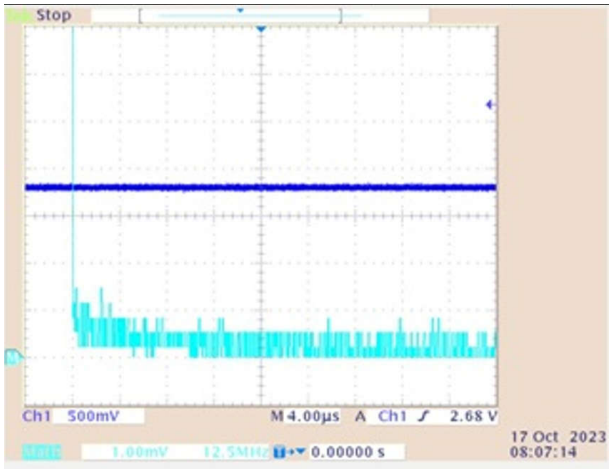


Figure 4-21. AVDD 1.8V and Spectrum Under DC Mode

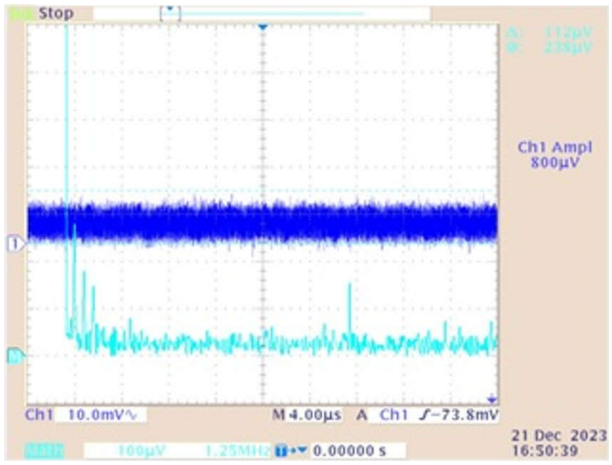


Figure 4-22. AVDD 1.8V and Spectrum Under AC Mode With Full Load

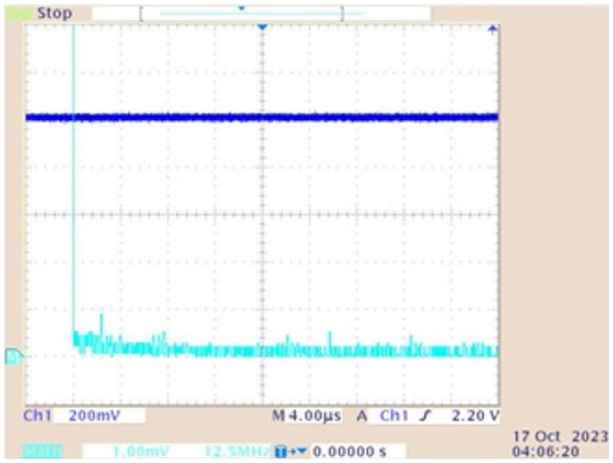


Figure 4-23. FPGA-1.8V Output and Spectrum Under DC Mode

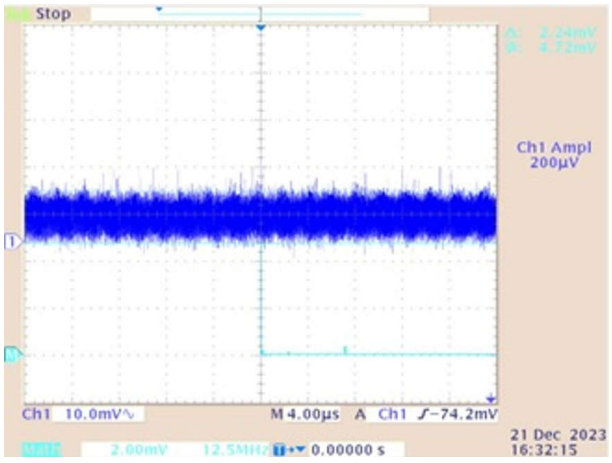


Figure 4-24. FPGA-1.8V Output and Spectrum Under AC Mode and Full Load

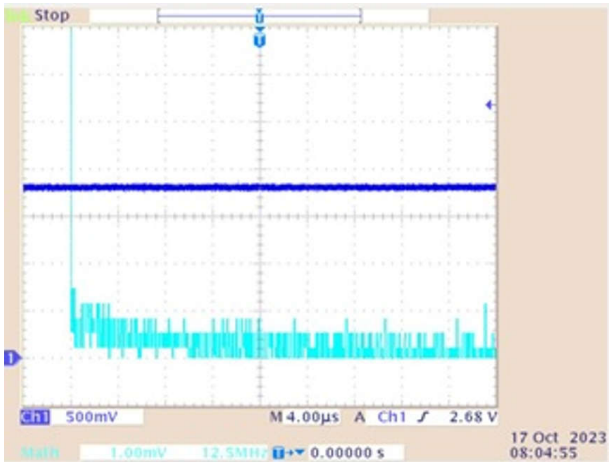


Figure 4-25. FPGA-1.0V Output and Spectrum Under DC Mode

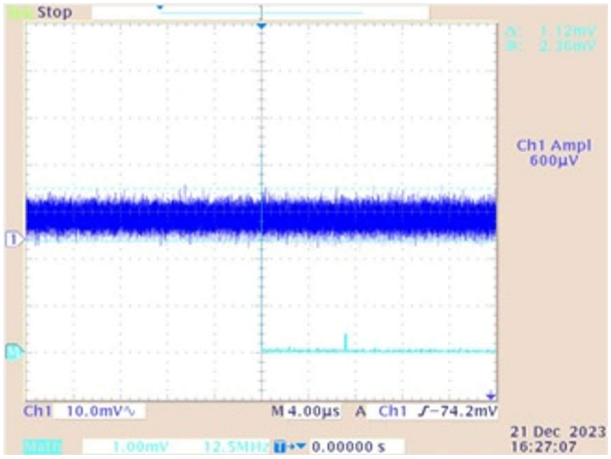


Figure 4-26. FPGA-1.0V Output and Spectrum Under AC Mode and Full Load

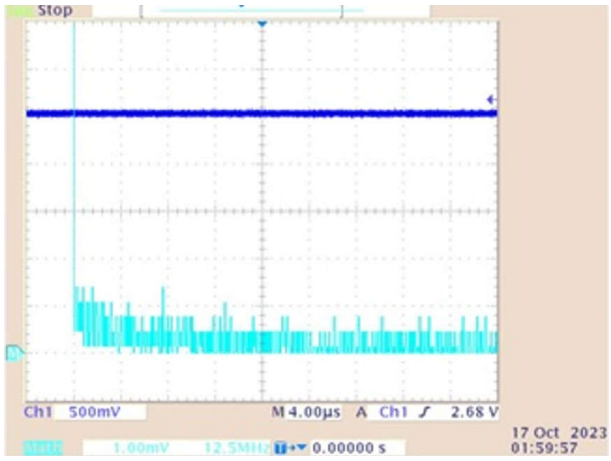


Figure 4-27. FPGA-2.5V Output and Spectrum Under DC Mode

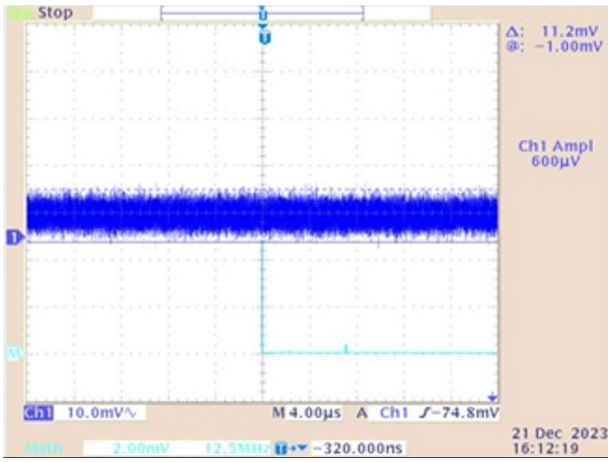


Figure 4-28. FPGA-2.5V Output and Spectrum Under AC Mode and Full Load

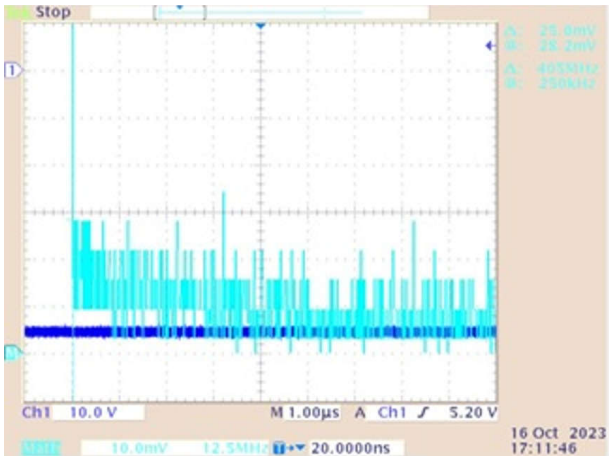


Figure 4-29. MHV Output and Spectrum Under DC Mode

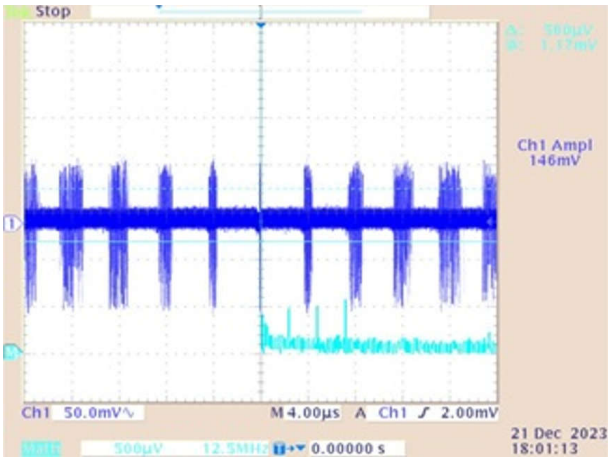


Figure 4-30. MHV Output and Spectrum Under AC Mode and Full Load

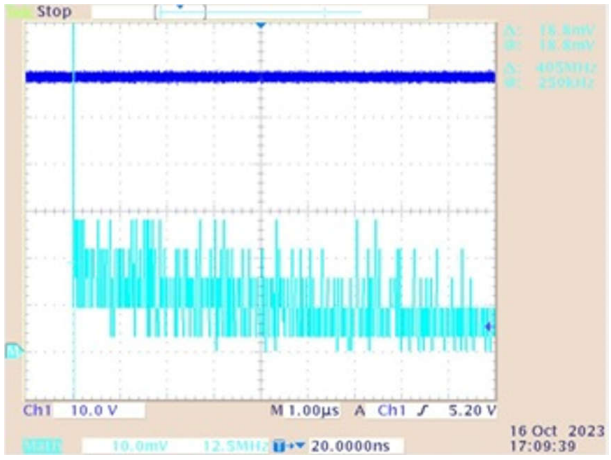


Figure 4-31. P_{HV} Output and Spectrum Under DC Mode

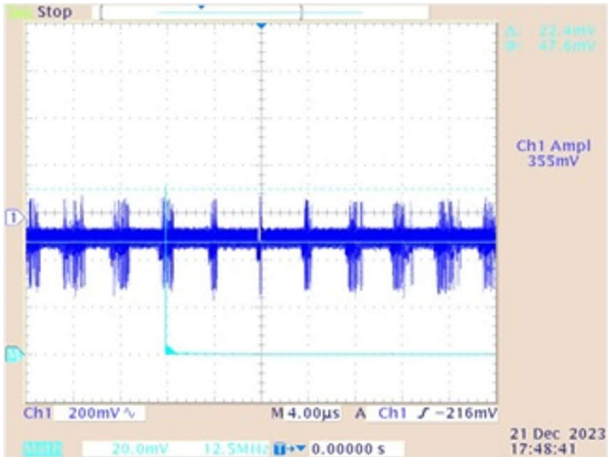


Figure 4-32. P_{HV} Output and Spectrum Under AC Mode and Full Load

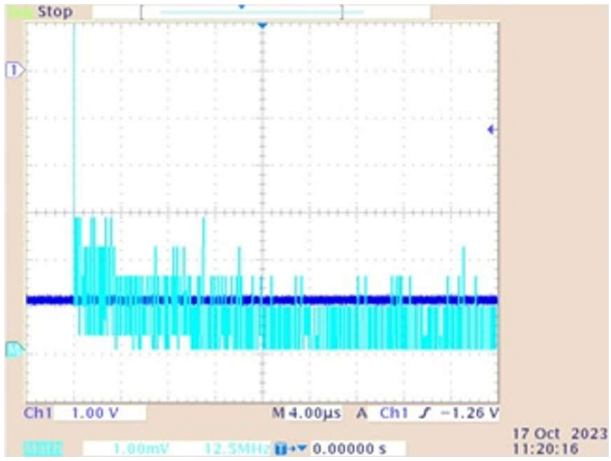


Figure 4-33. AVEE -5V Output and Spectrum Under DC Mode

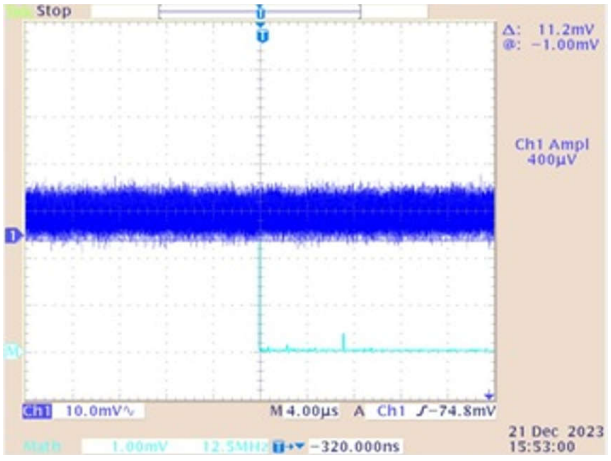


Figure 4-34. AVEE -5V Output Spectrum Under AC Mode and Full Load

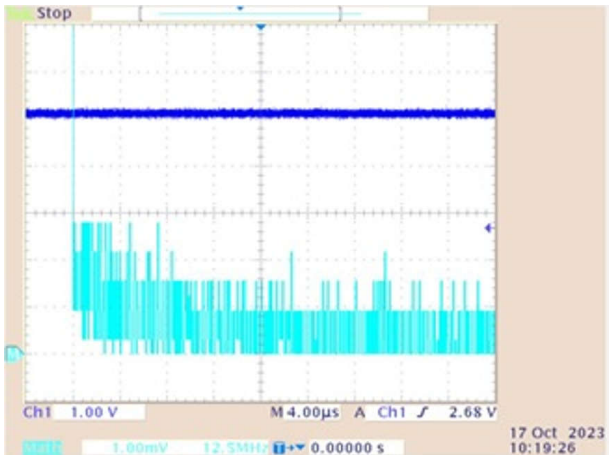


Figure 4-35. AVDD 5V Output and Spectrum

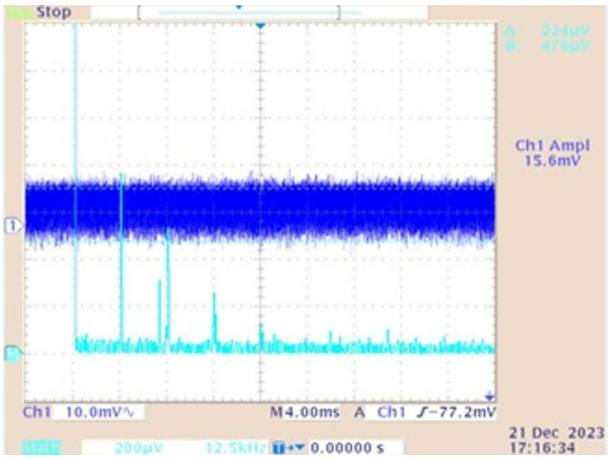


Figure 4-36. AVDD 5V Output Spectrum Under AC Mode and Full Load

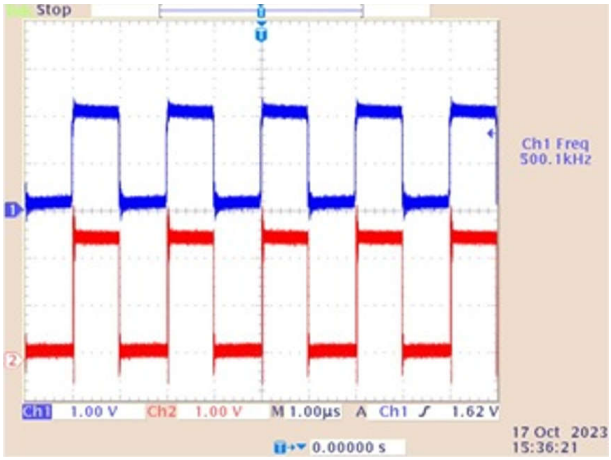


Figure 4-37. Synchronous Clock—Yellow: Input, Blue: Output

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010269.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010269.

5.1.3 PCB Layout Recommendations

Layout is an important factor for imaging quality in ultrasonic applications since the reflect signal is small. This reference design is made on an 8-layer board for better noise performance. Figure 5-1 shows the stack up of the board. The board has two ground layers, two power layers, and four signal layers.

#	Name	Material	Type	Weight	Thickness	Dk	GlassTransTemp
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.0254mm	3.5	
1	Top Layer		Signal	2oz	0.07mm		
	Dielectric1	FR-4	Core		0.2mm	4.2	
2	GND1	CF-004	Signal	1/2oz	0.0175mm		
	Dielectric 2	PP-006	Prepreg		0.2mm	4.1	180°C
3	Signal 1	CF-004	Signal	1/2oz	0.0175mm		
	Dielectric 3	PP-006	Prepreg		0.2mm	4.1	180°C
4	Power 1	CF-004	Signal	1/2oz	0.0175mm		
	Dielectric 4	PP-006	Prepreg		0.2mm	4.1	180°C
5	Power 2	CF-004	Signal	1/2oz	0.0175mm		
	Dielectric 5	PP-006	Prepreg		0.2mm	4.1	180°C
6	Signal 2	CF-004	Signal	1/2oz	0.0175mm		
	Dielectric 6	PP-006	Prepreg		0.2mm	4.1	180°C
7	GND2	CF-004	Signal	1/2oz	0.0175mm		
	Dielectric 1	FR-4	Prepreg		0.2mm	4.1	180°C
8	Bottom Layer		Signal	2oz	0.07mm		
	Bottom Solder	Solder Resist	Solder Mask		0.0254mm	3.5	
	Bottom Overlay		Overlay				

Figure 5-1. TIDA-010269 Layer Stack-Up

5.1.3.1 High-Voltage Supply Layout

Layout in SEPIC and Cuk is critical. While designing, the most important rule is to reduce the noise in the high-current switching loop, shown in Figure 5-2. The current flows from the input supply to the primary inductor and through the MOSFET. To minimize induced EMF due to switching currents, it is desirable to keep parasitic inductance of this loop as low as possible. Components (primary inductors, input electrolytic capacitors, and FET) must be placed as close as possible to each other. In this layout, a single ground plane was used, and all the signals return onto this low-impedance plane, as shown in Figure 5-3. In case the high-voltage circuit is placed in proximity to the transducer, shielding can be necessary to minimize the effects of radiated interference from the high-voltage section.

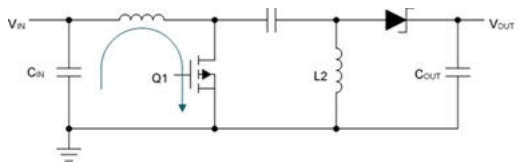


Figure 5-2. Hot Loop in SEPIC Configuration

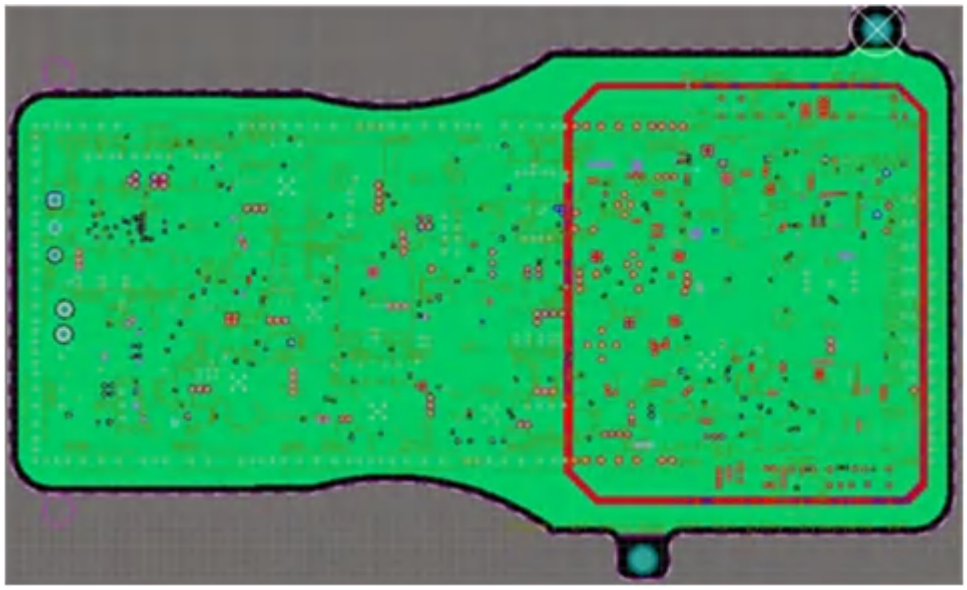


Figure 5-3. High Voltage Layout Section

5.2 Tools and Software

Tools

Radar Toolbox for mmWave Sensors	The Radar toolbox is a collection of demonstrations, software tools, and documentation designed to assist in the evaluation of TI Radar devices.

Software

UNIFLASH	UniFlash is a software tool for programming on-chip flash on TI microcontrollers and wireless connectivity devices and onboard flash for TI processors. UniFlash provides both graphical and command-line interfaces.

5.3 Documentation Support

1. Texas Instruments, TIDA-010057: Ultrasound smart probe power supply reference design
2. Texas Instruments, LM5158: *3A, 85V 2.2MHz wide V_{IN} boost, flyback, and SEPIC converter with dual random spread spectrum*
3. Seven design challenges for ultrasound smart probes
4. Texas Instruments, *Designing Bipolar High-Voltage SEPIC Supply for Ultrasound Smart Probe Application Note*
5. Texas Instruments, *AN-1484 Designing A SEPIC Converter Application Note*
6. Texas Instruments, BQ25790: *Integrated, NVDC, 5A 1-cell to 4-cell switch-mode buck-boost battery charger*
7. Texas Instrument, *Highly Integrated Signal Chain Solutions TX7332 and AFE5832LP for Smart Ultrasound Probes Application Note*
8. Texas Instrument, *Power Topologies Quick Reference Guide*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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