Design Guide: TIDA-010955

Analog Front End Reference Design for Machine Learning Arc Detection in Solar Applications

Description

This reference design features a analog front end for DC arc detection in solar applications based on artificial intelligence (AI). The string current is measured, filtered and fed into an AI-based arc detection algorithm running on the TMDSCNCD28P55X, controlCARD of C2000™ F28P55x devices, to detect DC series arcs. AI-based arc detection offers improved accuracy and robustness compared to traditional algorithms. A complete tool chain for collecting arc data, training an embedded AI model, and validating the system is available. This reference deign is available to order through the part number TIEVM-ARC-AFE.

Resources

TIEVM-ARC-AFE	Tool Folder
TIDA-010955	Design Folder
TMS320F28P550SJ, TMDSCNCD28P55X	Tool Folder
AMC3330, AMC23C11	Product Folder
OPA4323, TPS562203, TPS7A20	Product Folder

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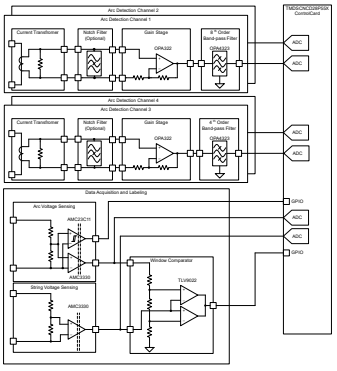
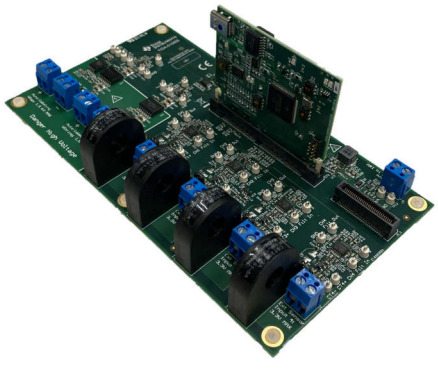
Features

- 4-channel analog front end for AI-based arc detection
- Configurable analog front end with band-pass and notch filter
- String voltage and arc gap voltage measurement inputs for training data acquisition
- Auto-labeling circuits to generate labeled arcing data
- Works with TMDSCNCD28P55X, controlCARD of C2000™ F28P55x devices, as well as other C2000 controlCARDs in 180-pin connector
- Selected embedded AI models for a quick start into AI-based arc detection

Applications

- Solar arc protection
- String inverter
- Central inverter





1 System Description

With the increasing amount of solar installations, safety concerns become ever more important. Arcing on high-voltage lines must be detected and the solar string must be de-energized to prevent hazards like electrical shock or fire. Therefore, standards like UL 1699B demand arc-fault protection circuits for all solar systems with rated voltages below 1500V. This reference design is intended to show an implementation for an analog front end for such arc detection purposes. The design does not fulfill the UL 1699B standard by itself.

DC arcing causes an AC noise current in the cabling of a PV string, which is present in a wide spectrum up to several MHz. The challenge for DC arc detection in solar is to detect this increase in noise within the PV cables in a reliable way, while not causing false alarms and shutdowns. To achieve this capability, a low-noise, high-performance, analog front end is required, since the injected AC noise of an arc can be in the range of a few mA sitting on top of the DC string current which is in the range of 20A in residential applications and even higher for commercial solar applications. Additionally, there a several other sources of noise within a solar system which cannot be falsely interpreted as an arc. Examples for these other noise sources are the switching frequency of the inverter or power line communication on the PV cabling. Traditionally, algorithms were used to identify arcing signatures in the measured current. To achieve a reliable arc detection, these algorithms often need to be fine-tuned to each system, since the arcing signatures are highly system-dependent.

A recent approach is to use embedded Artificial Intelligence (AI) models to identify arcs. If trained correctly, this AI-based approach can achieve better accuracy and is more robust against false alarms.

To train these AI models, training data must be acquired. For this purpose this reference design has an arc-labeling circuit implemented. The design uses the fact that there is a measurable voltage drop across the arc, to label the current data as an arc or as a normal operating condition. This can be done, since in a laboratory environment this arc voltage is accessible.

1.1 Key System Specifications

Table 1-1 shows the key specifications fro this reference design.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATION	COMMENT
Number of arc detection channels	4	—
Maximum String current	16A (onboard CT)	If higher DC currents are needed a external current sensor can be interfaced via connectors J1, J2 ,J3, or J4
Analog-to-Digital Conversion (ADC) Resolution	12 bit	Internal C2000 ADC. Other C2000 support higher resolution ADCs
Auxiliary power supply	8V to 16V	J7, Lab bench supply recommended
Number of labeling channels	1	Auto-labeling channel for training data acquisition
Maximum input voltage of string voltage and gap voltage measurement	1500	Voltage measurements used for generating and labeling arc training data

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board*. Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider it to be a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board*** . The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the high-level TIDA-010955 block diagram.

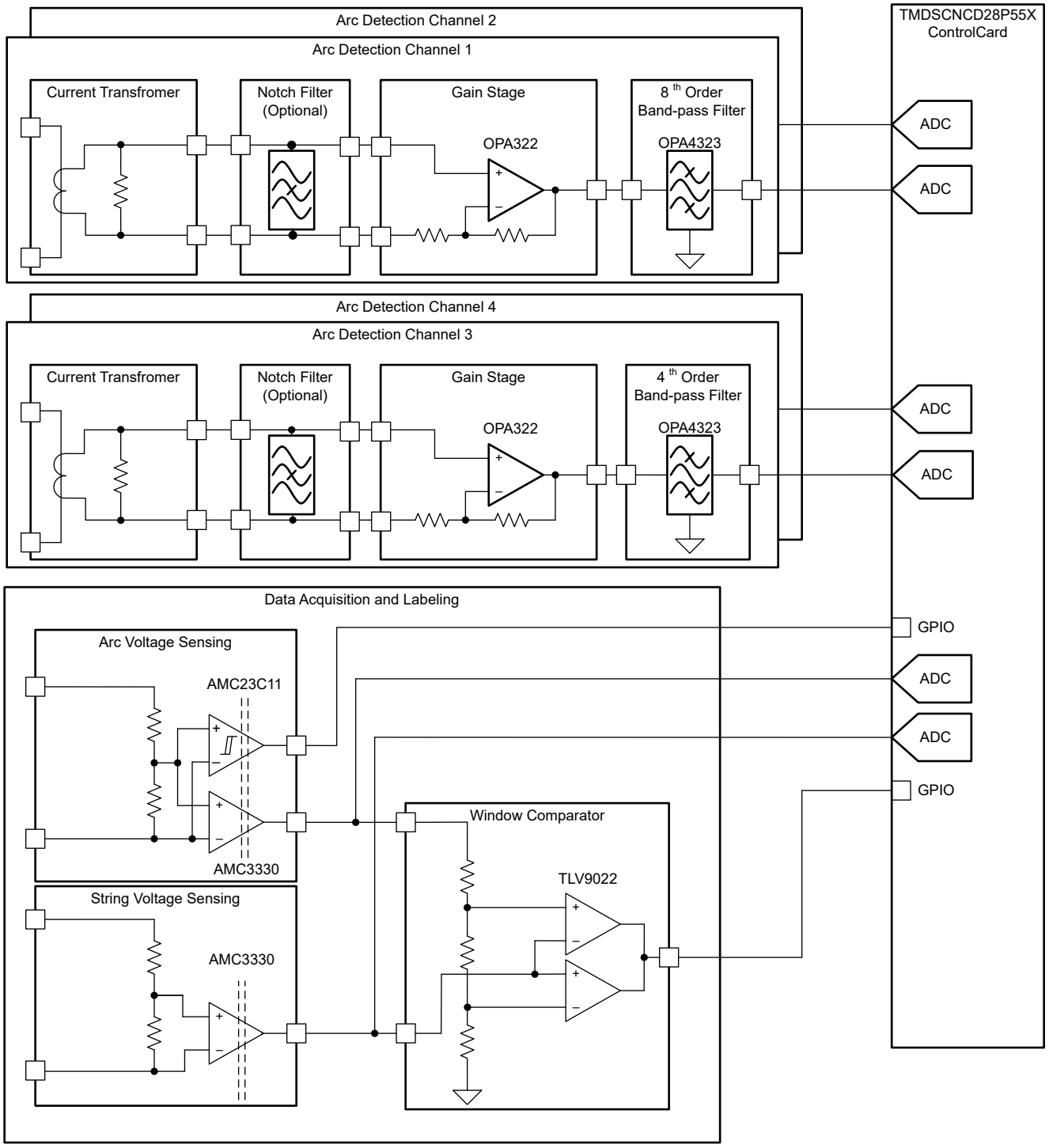


Figure 2-1. TIDA-010955 Block Diagram

2.1.1 Subsystems

The design consists of two main subsystems:

- Four independent analog front-end channels for arc detection
- Arc labeling circuit, which can be used to acquire labeled training data from the AI model training

2.1.1.1 Arc Detection Channels

The signal chain of the arc detection channels used in this reference design consist of four major blocks:

- Isolated current measurement
- Band-pass filter
- Analog-to-digital conversion
- Arc detection using embedded AI models

2.1.1.1.1 Isolated Current Measurement

For the isolated current measurement, there are two input options for each channel.

1. Onboard current transformer (CT)
2. Connector for external current sensor (J1, J2, J3, or J4)

Using a current transformer has two advantages. First, the current transformer provides the necessary isolation from the high DC link voltages and second, the current transformer filters out the DC component of the current, which is not of interest for the arc detection. An important point is to consider the saturation behavior of the CT for the high DC current. The selected transformer performs well up to 16A DC. To interface the voltage drop on the burden resistor to the voltage level of the filter stage and ADC, a first gain stage with a gain of 10 is implemented, which also introduces a bias to signal to convert the CT output into a unipolar signal.

When using an external current sensor, the designer must remember to account for isolation. The signal must be isolated from any high-voltage potentials, since the rest of the signal chain on the board is non-isolated. Also, the maximum supported input voltage for the external current sensor is 3.3V, but it can be necessary to adjust the gain of the first gain stage to avoid saturation of the signal chain. The gain stage implements a gain of 10 by default and the maximum voltage supported by the signal chain after the gain stage is 3.3V. So if the maximum input voltage of the external current sensor is higher than 300mV, the gain stage must be modified.

2.1.1.1.2 Band-Pass Filter

A band-pass filter is implemented to limit the spectrum of the acquired signal. Since a solar inverter system can be a noisy environment, a 4^{th} order low-pass filter and a 4^{th} order high-pass filter is selected. The separate structure is chosen, to easily adjust upper and lower boundaries of the frequency range. Design this filter in a way to filter out the switching frequency as well other noise sources. In this design, a frequency band of 30kHz to 100kHz is selected, but the frequency band can be specifically adjusted for each application.

2.1.1.1.3 Analog-to-Digital Conversion

This design uses an internal 12-bit ADC of the C2000 MCU. To gather data from up to 4 arc-detection channels. A sampling frequency of 250kHz is used to fulfill the sampling theorem for the selected frequency band of up to 100kHz.

2.1.1.1.4 Arc Detection Using Embedded AI Models

The acquired data is fed into a preprocessing block followed by an embedded AI model. More details regarding the process of detecting arcs using AI models are found in the software users guide, which is included in the software download folder.

2.1.1.2 Arc Labeling Circuit

The labeling circuit is not part of the arc detection system. The circuit is an additional subsystem meant for acquiring data during the AI model training and validation phase. The labeling circuit is not part of the actual end-application circuit.

This circuit can be used to label data in a laboratory environment. The circuit makes use of the fact that during arcing there is a voltage drop across the arc. In a laboratory environment with a discrete arc generator, this voltage is accessible and can be used to indicate if an arc is happening. To collect training data for the AI

model, arcs are generated in a laboratory environment and both the arc current and the labeling circuit are sampled. Using these procedures, a dataset is acquired which contains a sequence of current samples and the information, when during this sequence the arcing started. In short, information is collected of how the current looks during arcing and how the current looks in normal operation.

Section 3.2 has more details on the setup.

This labeled data can be used to train an AI model. Tools and software for this data acquisition and model training process are available. Links are found in the TIDA-010955 tool folder.

The circuit consist of the following blocks:

- Isolated string-voltage measurement
- Isolated arc gap voltage measurement with isolated comparator
- Window comparator for advanced labeling

2.1.1.2.1 Isolated String Voltage Measurement

An isolated amplifier is used to measure the string voltage. The output of the isolated amplifier is used for the advanced labeling circuit with the window comparator.

2.1.1.2.2 Isolated Arc Voltage Measurement With Isolated Comparator

The arc voltage is monitored in two ways. First with an isolated amplifier and second with an isolated comparator. The comparator indicates the start of an arc if the arc gap voltage rises above the comparator threshold. The output of the isolated amplifier is used for the advanced labeling circuit with the window comparator.

2.1.1.2.3 Window Comparator for Advanced Labeling

If the arc gap is increase too much during arc testing, the arc extinguishes and the full string voltage is applied across the arc gap. This means the voltage is still above the threshold of the isolated comparator, but arcing is no longer present. The window comparator circuit can be also be used to catch these cases, to set a lower threshold for when arcing is starting and an upper threshold for when the arc is stopping.

2.2 Design Considerations

The key design considerations are described in this chapter.

2.2.1 Current Sensor and Input Stage

In this reference design, the string current is used to detect an arc fault. Typically, only the AC content is analyzed which allows use of an AC coupled current sensor like a current transformer. Figure 2-2 shows the schematics for the input circuitry of this reference design. There are two input options. Either the onboard CT can be used or a external sensor can be connected to J1 (J2, J3, or J4 for channels 2, 3, or 4). To select the onboard CT, place a jumper on connector J8 between pins 1 and 2. To select the external sensor input place a jumper on J8 between pin 2 and 3.

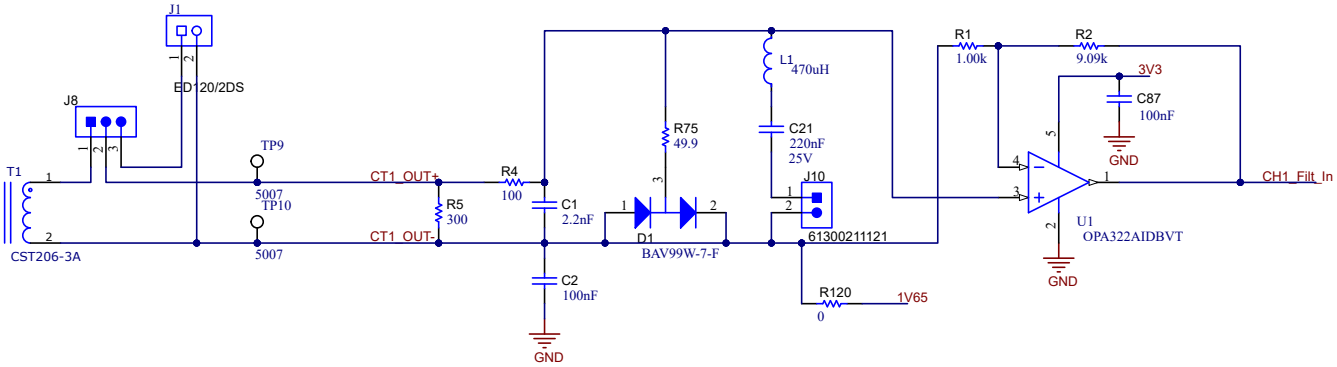


Figure 2-2. Schematics Current Sensing Circuit

The CST206-3A was selected as an onboard CT, since this device offers a high saturation limit and allows feed trough of the PV cable without cutting the cable. See Figure 3-2 for saturation testing. The output of the CT is connected to a 300Ω burden resistor R5, which results in a sensitivity of 1V/A. This signal is connected first to RC filter R4 and C1. R75 and D1 implement an overvoltage protection for the gain stage. Footprints for a notch filter are provided with L1 and C21. This notch filter can be used to filter out the inverter switching frequency to prevent saturation of the gain stage. U1 implements a simple gain stage. A gain of 10 is selected since typical arcing signatures have amplitudes up to 100mA or 200mA. These settings result in a voltage of 100mV to 200mV of voltage drop across the R1. The amplified signal is the connected to the filter stage.

For other input voltages or if a external current sensor with a different sensitivity is used the gain can be adjusted by changing R1 and R2.

2.2.2 Analog Band-Pass Filter

Figure 2-3 shows the filter stage consisting of an OPA4323, a 4-channel operational amplifier. U5A and U5B form a low-pass filter with a cutoff frequency at 100kHz. U5C and U5D form a high-pass filter with a cutoff frequency of 30kHz. In combination, this forms a band-pass filter with a pass band of 30kHz to 100kHz. The split topology of low-pass plus high-pass filters is selected to make it easy to adjust upper and lower levels of the band-pass filter separately. U5D also allows for an additional gain by adjusting R153 and R154. This can be used to introduce further gain after the filtering.

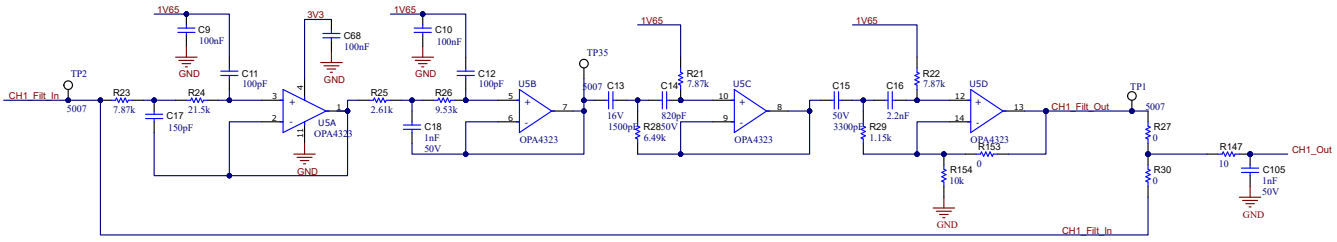


Figure 2-3. Schematics 8th Order Analog Band-Pass Filter

The two most important specifications of an amplifier in an active filter application are Gain-Bandwidth-Product (GBW) and slew rate (SR).The minimum requirements for GBW and SR are given in Equation 1 and Equation 2.

$$\mathrm{GBW_{min}} = 100 \times \mathrm{G} \times \mathrm{f_c} \quad (1)$$

$$\mathrm{SR_{min}} = 2 \times \pi \times \mathrm{f_c} \times \mathrm{V_{P-P}} \quad (2)$$

where

- G = closed-loop gain
- f_c= cutoff frequency of the low-pass filter
- V_{P-P}= peak-to-peak output voltage

With the values of G = 1, f_c = 100kHz, and V_{P-P} = 5V; a minimum GBW of 10MHz and a minimum slew rate of 3.14V/µs are calculated. With a GBW of 20MHz and a slew rate of 10V/µs, the OPA4323 fulfills these criteria and allows for some head room if a higher frequency band is desired. The transfer function is validated in the test results LINK. The output of the filter stage is connected to an internal ADC of the C2000 MCU. Populating R30 and removing R27 allows bypass of the analog filter stage.

For channel 3 and channel 4, only a 2nd order low-pass and 2nd order high-pass is implemented, as shown in Figure 2-4.

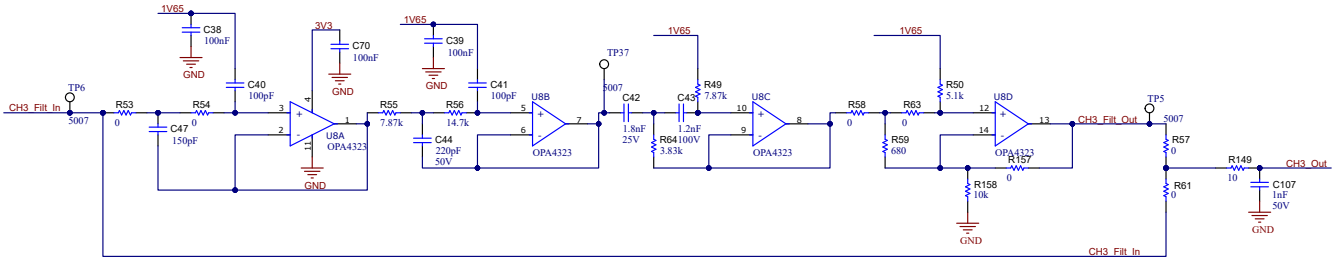


Figure 2-4. Schematics 4th Order Analog Band-Pass Filter

Therefore, U8A and U8D are just implementing a voltage follower and are not required. This is done to allow comparison between a 4th order band-pass on channels 3 and 4 and an 8th order band-pass on channels 1 and 2. In case 4 similar channels are desired, the resistors and capacitors can be adjusted.

2.2.3 Arc-Labeling Circuit

The arc-labeling circuit consists of two isolated amplifiers, an isolated comparator, and an analog implemented window comparator. The arc-labeling circuit is design to gather and automatically label arc signatures in a controlled lab environment. The design uses the fact that in a lab environment, the string voltage and the arc gap voltage are available, which is not the case in the field. Figure 2-5 shows the typical arc test setup in the lab. An arc generator is used to generate reproducible arcs at different operating conditions. The relation between the arc gap voltage, which can be measured across the arc generator and string voltage is used as an indicator for an arc. This information is then used to label the data sampled by standard arc-detection signal chain. The labeled data then can be used to train an embedded AI model.

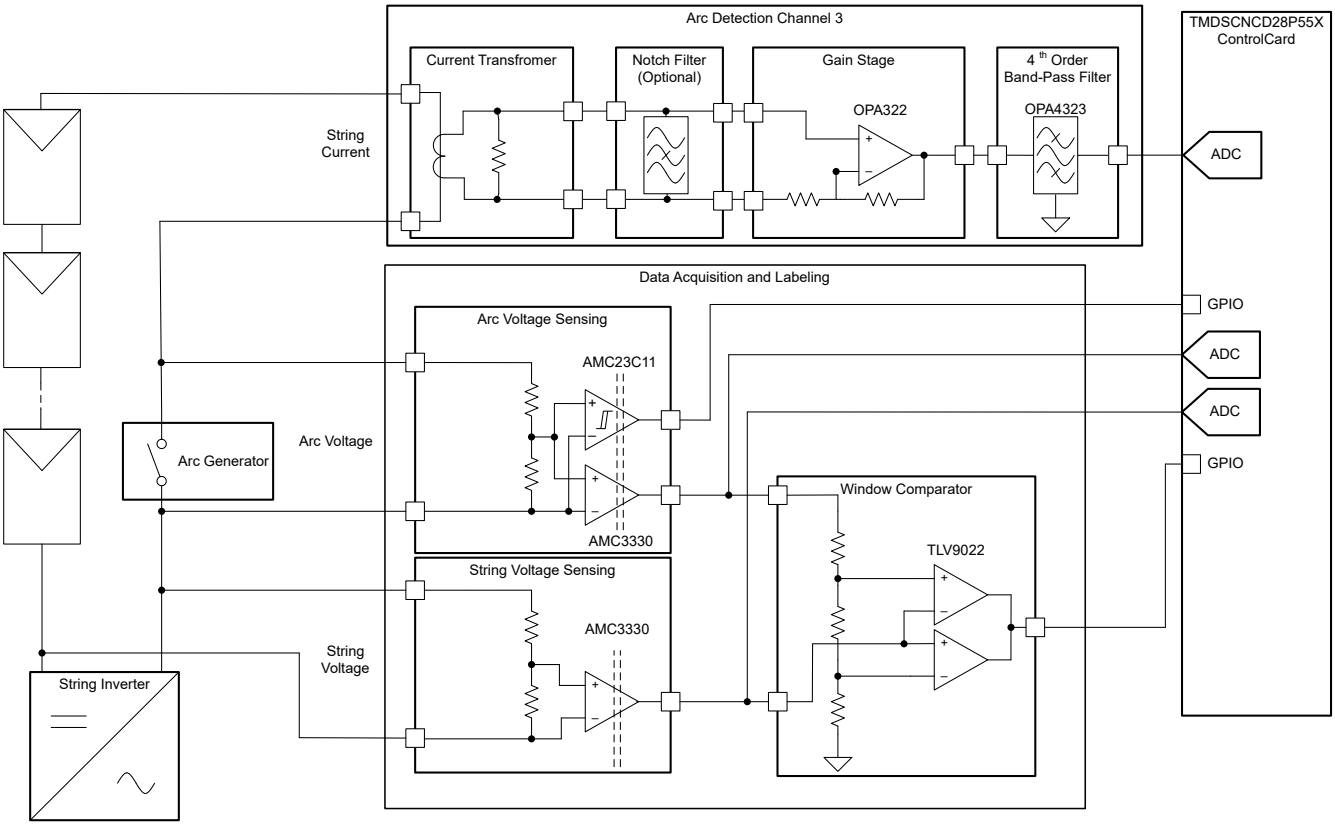


Figure 2-5. Block Diagram Arc Test Setup

2.2.3.1 String Voltage Sensing

Figure 2-6 shows the string voltage sensing circuit. The circuit consists of a resistor divider connected to AMC3330, which is a reinforced isolated amplifier with a fixed gain of 2.0V/V. The differential output of the AMC3330 is connected to the circuit described in Section 2.2.3.3. This differential to single-ended conversion introduces a gain of 1.65V/V. The output of the conversion is then connected to an internal ADC of the MCU.

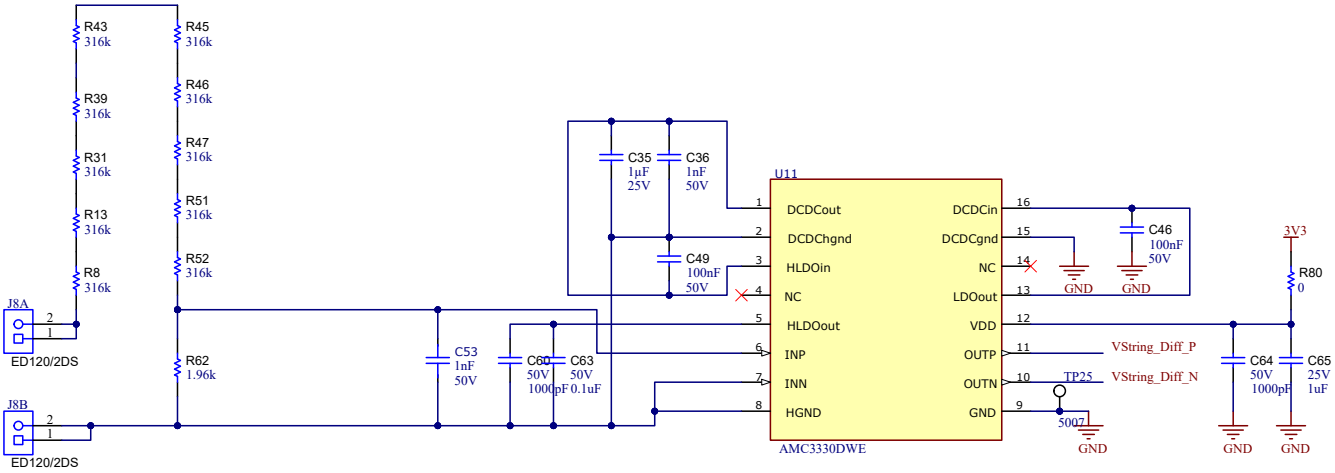


Figure 2-6. Schematics String Voltage Sensing

Equation 3 describes the relation of input voltage between J8A and J8B to output voltage of the differential to single-ended conversion.

$$V_{out} = V_{in} \times \frac{1960\Omega}{(10 \times 316000\Omega + 1960\Omega)} \approx V_{in} \times 0.00062 \quad (3)$$

2.2.3.2 Arc Gap Voltage Sensing

To sense the arc gap voltage, a similar circuit as for the string voltage sensing is used. The sense resistor R110 is increased; however, to increase sensitivity for lower voltage and allow a lower threshold for AMC23C11.

$$V_{out} = V_{in} \times \frac{6490\Omega}{(10 \times 316000\Omega + 6490\Omega)} \approx V_{in} \times 0.00205 \quad (4)$$

Typical arc gap voltages are in a range from 10V to 50V depending on the string current. It is important to not exceed the maximum allowed input voltage of AMC3330. This is the maximum string voltage. In case the gap is to wide and the arc extinguishes the full string voltage is applied to this voltage divider. Assuming this scenario 1500V is applied, which leads to a input voltage of 3.1V across R110. This is far outside the linear range, but still within the absolute maximum rating.

In addition a isolated comparator AMC23C11 is used to indicate when the arc gap voltage is above a threshold. This threshold is programmed using R128. A 100µA current source is implemented int the REF pin off AMC23C11 to generate the threshold voltage. R128 is selected to the minimum of 200Ω, resulting in a voltage of 20mV at the REF pin. This equals an input voltage of 9.75V. Figure 2-7 shows the schematic.

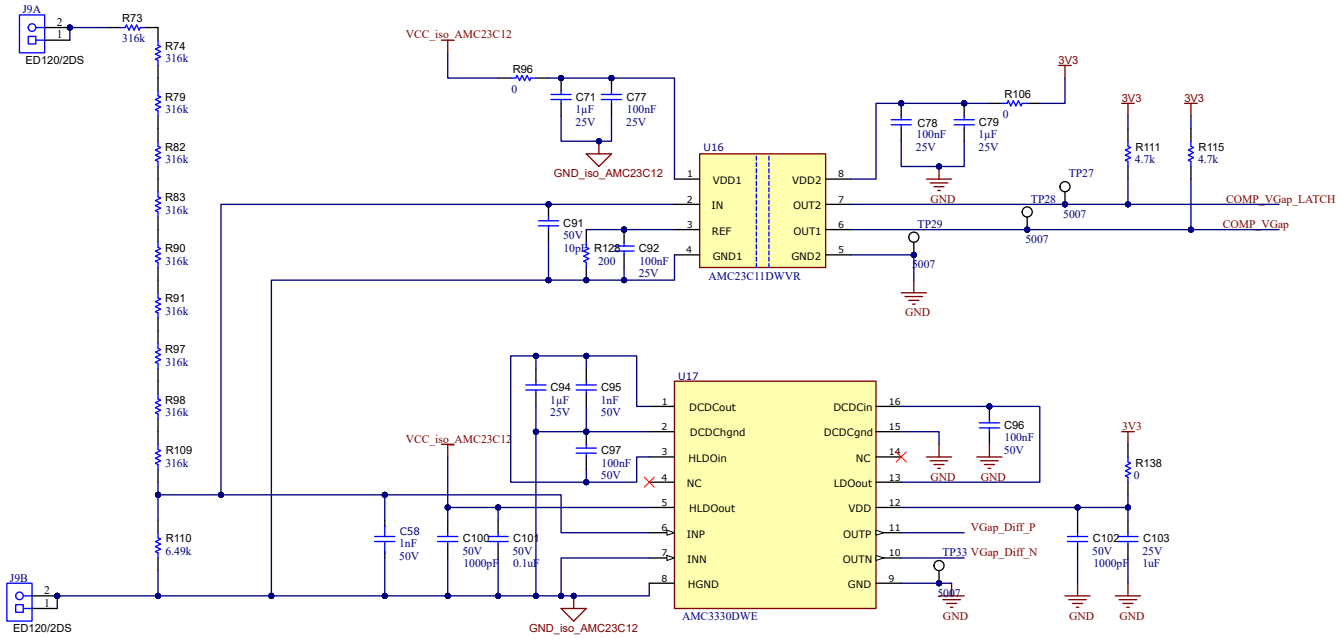


Figure 2-7. Schematics Arc Voltage Sensing

2.2.3.3 Differential to Single-Ended Conversion

AMC3330 used for both voltage sensing paths has a differential signal output. To interface this signal to the single-ended ADC of the C2000 MCU a conversion stage is implemented using TLV6001. See also the *Interfacing a Differential-Output (Isolated) Amp to a Single-Ended Input ADC* application brief. R92 is not populated, since the input voltage is always positive, which means no biasing is required. The gain of this conversion stage is set by the relation between R60 and R84 and R87 and R86. A gain of 1.65 is used, since the maximum output of AMC3330 is 2V and the maximum input of the ADC is 3.3V.

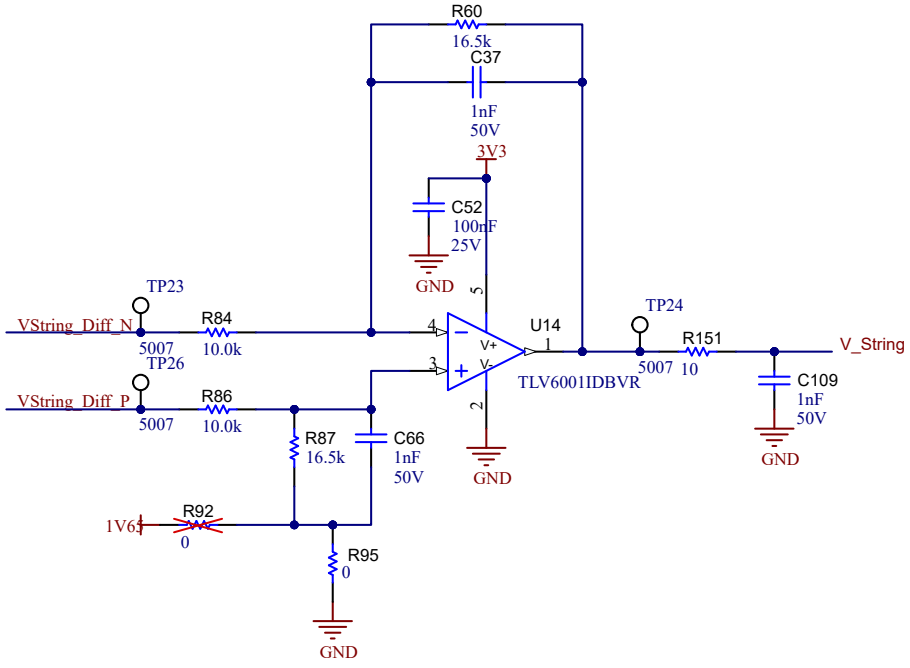


Figure 2-8. Schematics Differential to Single-Ended Conversion

2.2.3.4 Window Comparator for Arc Labeling

A window comparator is implemented using the dual-channel TLV9022 amplifier. This circuit is used for arc labeling in addition with AMC23C11. While AMC23C11 provides a very fast response for when the arc starts, the device cannot detect when the arcing stops, since after the arcing the arc gap voltage is still higher than the threshold. Here the window comparator circuit comes into play. The comparator allows indication of the start of an arc, as soon as the arc voltage rises above the lower threshold and the end of an arc as soon as the arc rises above the upper threshold. Both thresholds are set with relative to the string voltage using R3, R42 and R48. The lower threshold is described in Equation 5.

$$V_{TH\_L} = V_{String} \times \frac{3k\Omega}{(43k\Omega + 27k\Omega + 3k\Omega)} \approx V_{String} \times 0.041 \quad (5)$$

The upper threshold is described inEquation 6.

$$V_{TH\_H} = V_{String} \times \frac{(27k\Omega + 3k\Omega)}{(43k\Omega + 27k\Omega + 3k\Omega)} \approx V_{String} \times 0.41 \quad (6)$$

Note

V_{String} is the output of the differential to single-ended conversion circuit and not the input voltage.

When applying these formulas to the actual input voltages for the string voltage V_{String_IN} and arc gap voltage V_{Arc_IN} we need to take the different voltage gains of the two sensing circuits into account.

$$V_{ARC\_TH\_L} = V_{String\_IN} \times \frac{0.0062}{0.0205} \times \frac{3k\Omega}{(43k\Omega + 27k\Omega + 3k\Omega)} \approx V_{String\_IN} \times 0.0124 \quad (7)$$

$$V_{ARC\_TH\_H} = V_{String\_IN} \times \frac{0.0062}{0.0205} \times \frac{(27k\Omega + 3k\Omega)}{(43k\Omega + 27k\Omega + 3k\Omega)} \approx V_{String\_IN} \times 0.124 \quad (8)$$

As an example, for a string voltage V_{String_IN} of 800V, the lower threshold $V_{ARC\_TH\_L}$ is about 10V and the higher threshold $V_{ARC\_TH\_H}$ is about 100V. This means if the arc gap voltage V_{Arc_IN} is between 10V and 100V the window comparator indicates that an arc is present.

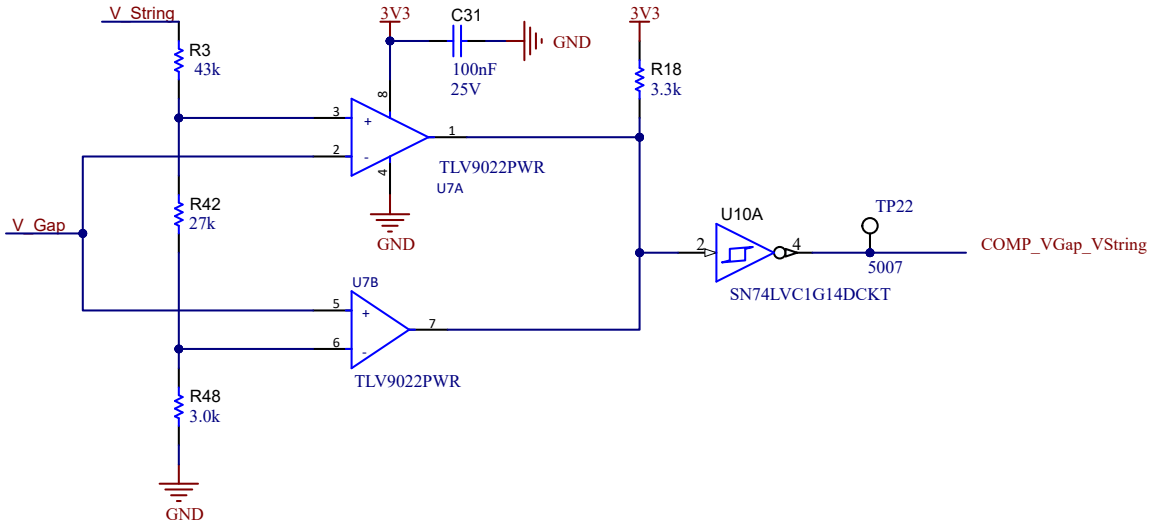


Figure 2-9. Schematics Window Comparator Circuit for Arc Labeling

2.2.4 Auxiliary Power Supply

Figure 2-10 shows how this reference design is powered by an auxiliary power supply. A voltage between 8V and 16V can be applied to connector J7. The eFuse TPS25947 is implemented to limit the input current and provide protection again reverse polarity. The current limit is set to 0.6A by R113. The undervoltage and overvoltage lockout is set to 6V and 16.3V by the resistors R104, R105, and R112. For a detailed description and formulas, see the data sheet.

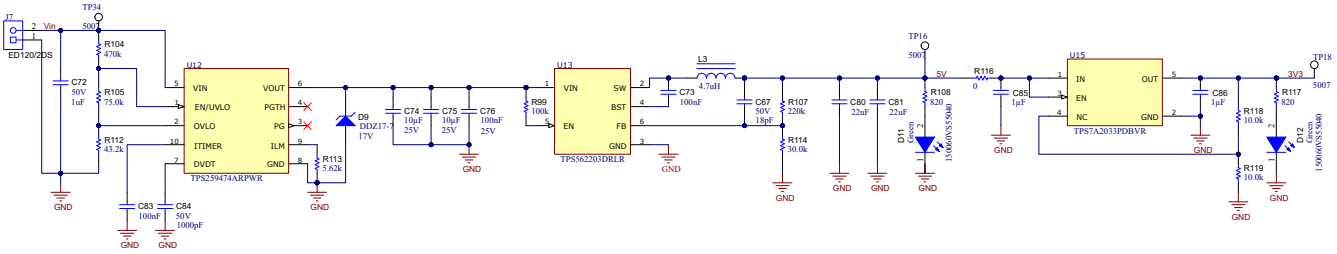


Figure 2-10. Schematics Auxiliary Power Supply

TPS562203 is used to step-down the input voltage to 5V. This 5V is used to supply the C2000 control card. The 5V rail is stepped down by TPS7A2033 to 3.3V. Here a low dropout (LDO) regulator is used to generate a low noise 3.3V rail. This rail is used for the analog signal chain.

2.2.5 controlCard and Debug Interface

Figure 2-11 shows the controlCard and debug interfaces of this reference design. The controlCard is connected to connector J5. The controlCARD provides connection to the ADCs of the MCU for the analog signals as well as several GPIO connections for the comparator outputs. Additionally four LEDs can be controlled by the MCU. This can be used for status indication or debug purposes.

J6 is an additional debug header. This header provides an serial-peripheral interface (SPI) to the controlCard, three additional GPIOs and supply rails.

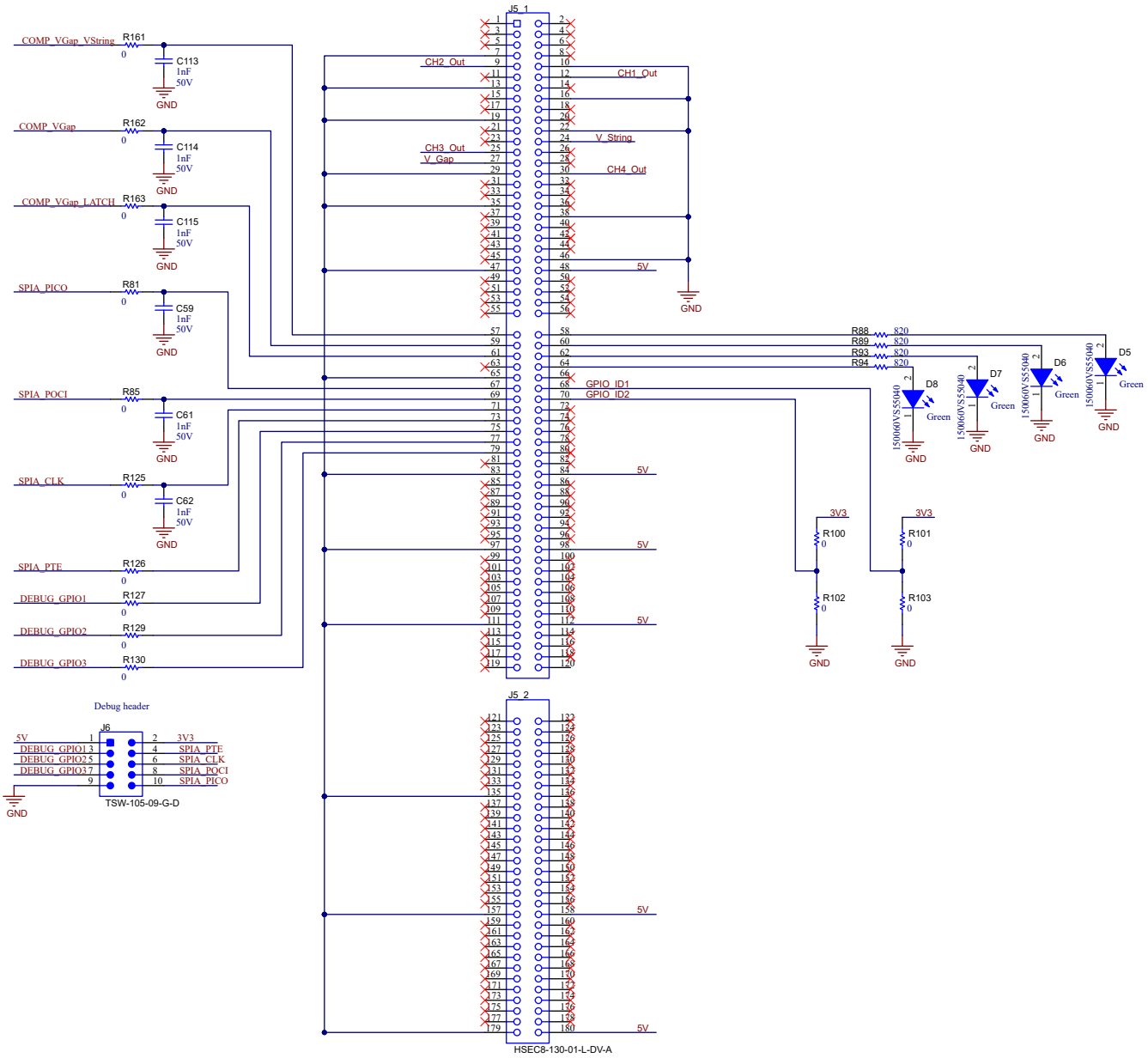


Figure 2-11. Schematics Off-Board Connectors

2.3 Highlighted Products

2.3.1 TIEVM-ARC-AFE

The TIEVM-ARC-AFE is an analog front end for the C2000™ MCU based machine learning arc detection in solar applications.

2.3.2 TMDSCNCD28P55X – TMDSCNCD28P55X controlCARD Evaluation Module

TMDSCNCD28P55X is a low-cost evaluation and development board for TI C2000™ MCU series of F28P55x devices. The board comes with a HSEC180 (180-pin high-speed edge connector) and, as a controlCARD, is an excellent choice for initial evaluation and prototyping. For evaluation of TMDSCNCD28P55X, a 180-pin docking station TMDSHSECDOCK is required and can be purchased separately or as a bundled kit.

2.3.2.1 Hardware Features

- Isolated onboard XDS110 USB-to-JTAG debug probe enables real-time in-system programming and debugging
- Standard 180-pin controlCARD high-speed edge card (HSEC) interface
- Analog I/O, digital I/O, and JTAG signals at card interface
- Hardware Files are in C2000Ware at boards\controlCARDs\TMDSCNCD28P55X

The TMS320F28P55x (F28P55x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies. The device features a C28x 32-bit DSP CPU and a programmable Control Law Accelerator (CLA), which operate at 150MHz for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Floating-Point Unit (FPU), Trigonometric Math Unit (TMU), and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems. The device also features a Neural-Network Processing Unit (NPU) that is highly optimized for Deep Convolutional Neural Networks (CNN) and delivers up to 10 × NN inferring performance improvement versus software implementation.

2.3.3 OPA4323 – Quad, 5.5V, 20MHz, Zero-Cross Low-Noise (6nV/√Hz) RRIO Operational Amplifier

The OPAx323 family of op amps includes single (OPA323), dual (OPA2323), and quad-channel (OPA4323), low-voltage (1.7V to 5.5V), high-bandwidth (20MHz) amplifiers (op amps) with a zero-crossover input stage and a rail-to-rail output stage. The zero-crossover input stage enables OPAx323 to achieve high linearity and low distortion for input signals with rail-to-rail swing that are typical in ADC driver applications. Gain-bandwidth of 20MHz provides a fast settling response for ADC sampling speeds between 0.5MSPS to 5MSPS depending on the settling performance required. The OPAx323 is well-optimized for power savings as the device consumes just 1.6mA typical quiescent current.

The OPAx323 easily supports precision performance in high gain voltage sensing applications such as the Wheatstone bridge, as the device features maximum offset drift of 2µV/°C and thermal noise floor of 5.5nV/rt-Hz with a minimum of 100dB CMRR. This unique combination of higher precision (low offset, drift, noise, distortion, and CMRR) and higher gain-bandwidth (fast settling and slewing) enables use in multiple applications such as the motor rotary encoders, microphone audio pre-amplifiers and ultrasonic transducers.

The OPAx323 achieves a high slew-rate of 33V/µs allowing for fast detection of faults in motor current sensing applications. Unlike traditional amplifiers, the zero-cross over input stage allows for identical precision performance for both low and high-side sensing applications, thus making OPAx323 the best choice for current sensing in a variety of end equipments such as the solar string inverters, power delivery, grid and EV infrastructure. OPAx323S devices provide shutdown functionality for additional power savings and help disable the amplifier when idle. The family features standard and small size as well as leaded and QFN packages across all the channel variants.

2.3.4 OPA323 – Single, 5.5V, 20MHz, Zero-Cross Low-Noise (6nV/√Hz) RRIO Operational Amplifier

The OPAx323 family of op amps includes single (OPA323), dual (OPA2323), and quad-channel (OPA4323), low-voltage (1.7V to 5.5V), high-bandwidth (20MHz) amplifiers (op amps) with a zero-crossover input stage and a rail-to-rail output stage. The zero-crossover input stage enables OPAx323 to achieve high linearity and low distortion for input signals with rail-to-rail swing that are typical in ADC driver applications. Gain-bandwidth of

20MHz provides a fast settling response for ADC sampling speeds between 0.5MSPS to 5MSPS depending on the settling performance required. The OPAx323 is well-optimized for power savings as the device consumes just 1.6mA typical quiescent current.

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The OPAx323 achieves a high slew-rate of 33V/µs allowing for fast detection of faults in motor current sensing applications. Unlike traditional amplifiers, the zero-cross over input stage allows for identical precision performance for both low and high-side sensing applications, thus making OPAx323 the best choice for current sensing in a variety of end equipments such as the solar string inverters, power delivery, grid and EV infrastructure. OPAx323S devices provide shutdown functionality for additional power savings and help disable the amplifier when idle. The family features standard and small size as well as leaded and QFN packages across all the channel variants.

2.3.5 AMC3330 – ±1V Input, Precision Voltage Sensing Reinforced Isolated Amplifier With Integrated DC/DC

The AMC3330 is a precision, isolated amplifier with a fully-integrated, isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and separates sections of the system that operate on different common-mode voltage levels and protects low-voltage domains from damage.

The input of the AMC3330 is optimized for direct connection to high-impedance, voltage-signal sources such as a resistor-divider network to sense high-voltage signals. The integrated isolated DC/DC converter allows measurement of non-ground-referenced signals and makes the device a unique design for noisy, space-constrained applications.

The excellent performance of the device supports accurate voltage monitoring and control. The integrated DC/DC converter fault-detection and diagnostic output pin of the AMC3330 simplify system-level design and diagnostics.

The AMC3330 is specified over the temperature range of –40°C to +125°C.

2.3.6 AMC23C11 – Fast-Response, Reinforced, Isolated Comparator With Adjustable Threshold and Latch Function

The AMC23C11 is an isolated comparator with a short response time. The open-drain output is separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to $5kV_{RMS}$ according to VDE 0884-17 and UL1577, and supports a working voltage of up to $1kV_{PK}$.

The trip threshold is adjustable from 20mV to 450mV in low-hysteresis mode and from 600mV to 2.7V in high-hysteresis mode through a single external resistor.

The open-drain output on the device supports transparent mode (LATCH input tied to GND2) where the output follows the input state, or latch mode, where the output is cleared on the falling edge of the latch input signal.

The AMC23C11 is available in an 8-pin, wide-body SOIC package and is specified over the extended industrial temperature range of –40°C to +125°C.

3 Hardware, Testing Requirements, and Test Results

Table 3-1 describes the TIDA-010955 connection point and Table 3-2 lists the maximum input rating.

Table 3-1. Connector and Test Point Description

DESIGNATOR	DESCRIPTION
T1, T2, T3, T4	Current transformers for channels 1, 2, 3, and 4. Feed through PV cabling.
J1, J2, J3, J4	External current sensor input for channels 1, 2, 3, and 4
J7	Connector for auxiliary power (8V to 16V)
J5_1, J5_2	HSEC Connector for C2000 control card
J6	Debug header (Contains GPIOs, Voltage rails and a SPI)
J8A, J8B	Positive and negative input of string voltage for arc labeling circuit
J9A, J9B	Positive and negative input of arc gap voltage for labeling circuit
TP9, TP11, TP17, TP20	Positive output of CT of channels 1, 2, 3, and 4
TP10, TP12, TP19, TP21	Negative output of CT of channels 1, 2, 3, and 4
TP2, TP4, TP6, TP7	Input of band-pass filter after gain stage for channels 1, 2, 3, and 4
TP35, TP36, TP37, TP38	Output of low pass stage of bandpass filter for channels, 1, 2, 3, and 4
TP1, TP3, TP4, TP8	Output of band-pass filter for channels 1, 2, 3, and 4.
TP16	5V rail
TP18	3.3V rail
TP22	Output of window comparator for arc labeling
TP23, TP26	Positive and negative output of U11 for string voltage sensing (differential output)
TP24	Single-ended output of string voltage sensing
TP30, TP2	Positive and negative output of U17 for arc gap voltage sensing (differential output)
TP31	Single-ended output of arc gap voltage sensing
TP13, TP14, TP15, TP39, TP40, TP25, TP29, TP33	GND

Table 3-2. Maximum Input Rating

CONNECTOR	MAXIMUM VOLTAGE (V)	MAXIMUM CURRENT (A)
J9A, J9B	1500	Limited by resistor divider
J8A, J8B	1500	Limited by resistor divider
J7	16	0.6A (limited by eFuse)
J1, J2, J3, J4	3.3	Limited by burden resistor (R5, R10, R15, or R20)

3.1 Signal Chain Verification

Section 3.1.1,Section 3.1.2 and Section 3.1.3 show how to verify the signal chain. Verify the signal chain before the test with real arcs are done, to make sure the hardware is working as intended.

3.1.1 Hardware Requirements

The following items are required for low-voltage signal chain verification:

- TIDA-010955 board
- TMDSCNCD28P55X controlCARD
- USB Type-C® cable
- Auxiliary power supply (8V to 16V, 250mA)
- Signal generator
- Oscilloscope with voltage and current probes
- Lab bench power supply capable of providing 20A (optional for saturation testing)

3.1.2 Test Setup

Before setting up the test board, complete a visual inspection, to make sure the board is in a good condition.

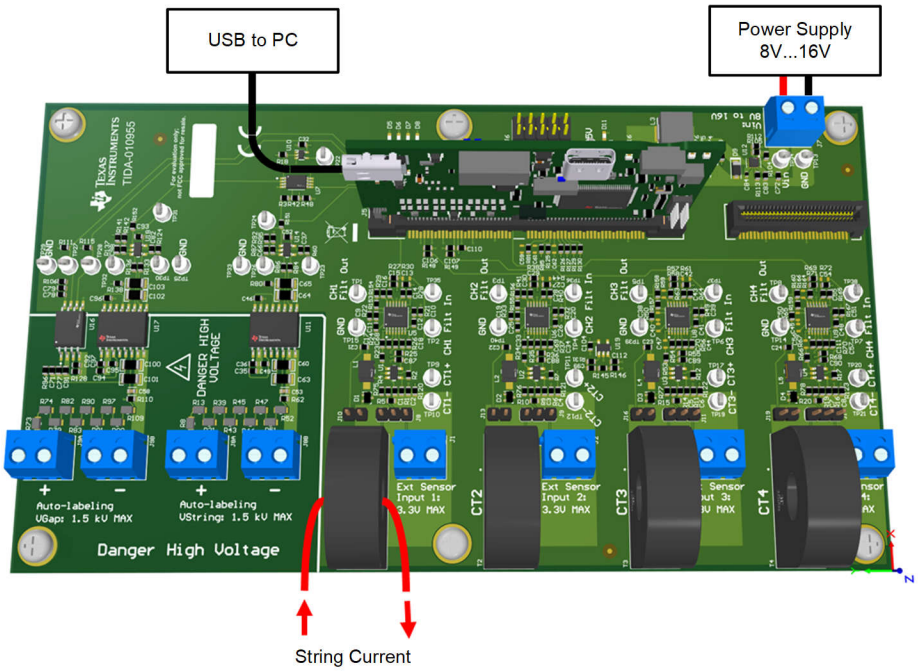

Figure 3-1. Test Setup

Use the following setup for the low-voltage signal chain verification:

1. Connect an auxiliary power supply to J7. The auxiliary supply accepts voltages between 8V and 16V and requires a nominal current below 200mA. An eFuse is implemented to limit the current to a maximum of 600mA.
2. Check that LED D11 and LED D12 for 5V and 3.3V light up.
3. Short circuit the output of the signal generator and feed the cable through one of the current transformers. Select a sinusoidal output. For a 50Ω output and a voltage of 15V this results in 0.3A of current.
4. To verify the saturation behavior of the current transformer, a second cable carrying a DC current can be fed through the current transformer.
5. The debug connection to the PC is not necessary to verify that the analog part of the signal chain is working correctly.
6. Make sure a jumper is placed between pin 1 and pin 2 of J8, J9, J11, and J12 if the onboard CT is used, or between pin 2 and 3 if a external sensor is used.

Now the following test points can be used to observe the signal through the signal chain (example for CH1, see Table 3-1 for test point designators of other channels):

- TP9 (CT1+): Positive output of the current transformer
- TP2 (CH1 Filt In: Signal at the output of the gain stage and input of the band-pass filter
- TP35: Signals after low-pass section of the band-pass filter
- TP1(CH1 Filt Out): Signal at the output of the band-pass filter and input of the ADC

3.1.3 Test Results

Figure 3-2 shows the transfer function of the current transformer circuit with different DC currents applied. This is done by feeding two cables through the current transformer. One is carrying a AC signal with varying frequency for the AC analysis, while the second cable is carrying a DC current. The input current is measured with a high-performance current probe of an oscilloscope. The output voltage is measured on TP9 which is labeled CT+.

High DC currents lead to saturation effects especially for low frequencies. In the band from 30kHz to 100kHz which is used for arc detection the attenuation is around 3dB for a current of 20A which is acceptable. If higher DC currents are present in the system, an external sensor which can handle these currents can be used. The signal chain needs to be adjusted accordingly.

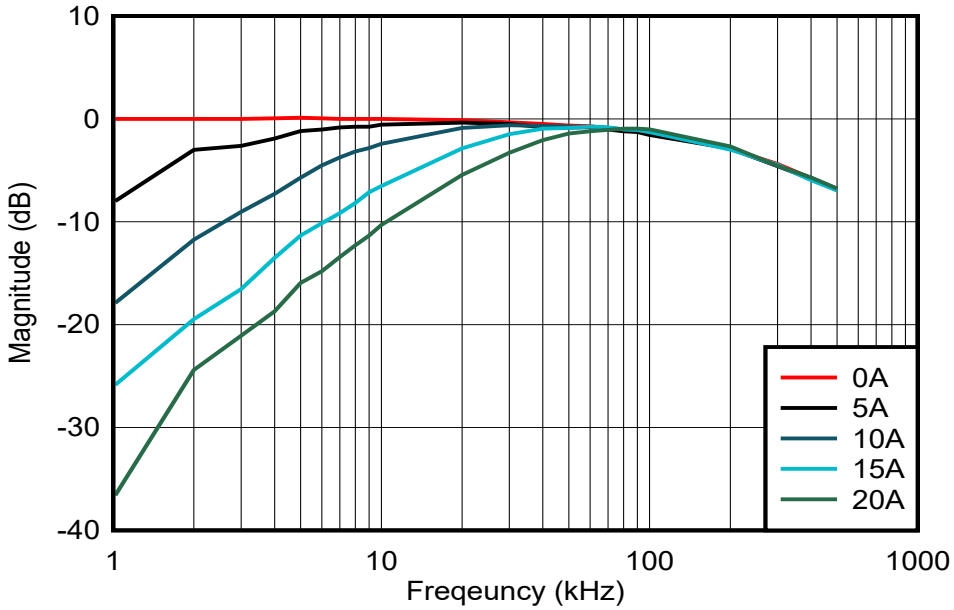

Figure 3-2. Transfer Curve of the Current Transformer for Different DC Currents

Figure 3-3 shows the transfer curve between the output of the CT circuit and the output of the gain stage. A stable gain of 20dB (Gain of 10) is achieved up 100kHz which is the upper limit of the frequency range used for arc detection.

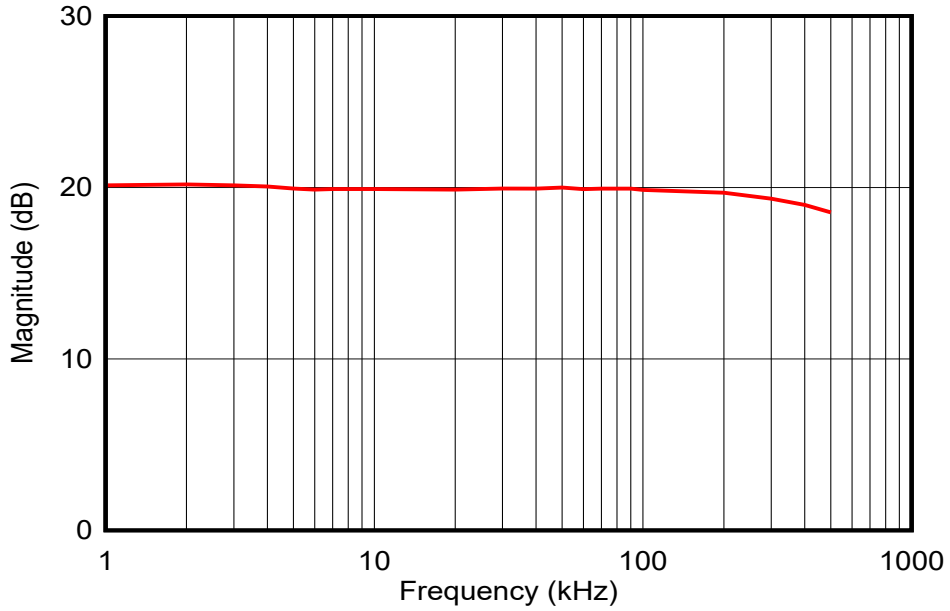

Figure 3-3. Transfer Curve of Gain Stage

Figure 3-4 and Figure 3-5 show the transfer curves of the filter stage. Channel 1 and channel 2 are implemented as a 8th order band-pass filter while channel 3 and channel 4 are implemented as a 4th order band-pass filter. These transfer curves are measured between TP2 (output of the gain stage) and TP1 (output of the band-pass filter stage).

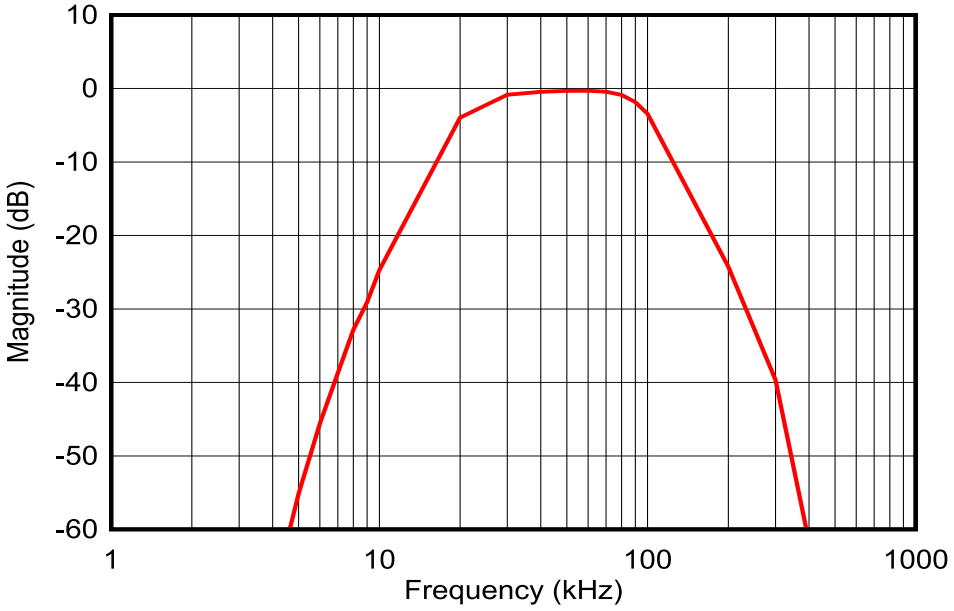

Figure 3-4. Transfer Curve of 8th Order Band-Pass Filter Stage (CH1 and CH2)

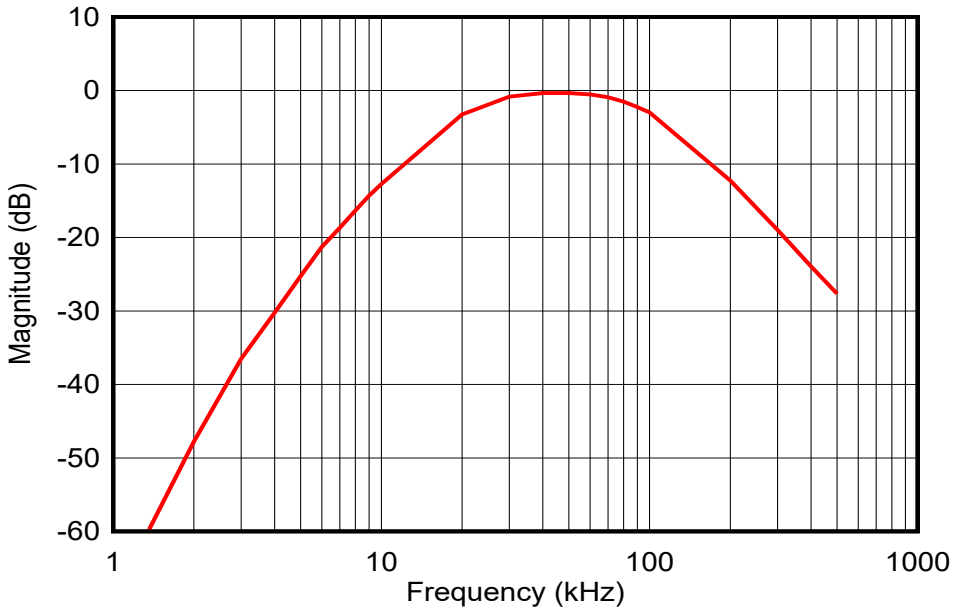

Figure 3-5. Transfer Curve of 4th Order Band-Pass Filter Stage (CH3 and CH4)

Figure 3-2 and Figure 3-3 show the transfer curves of the complete signal chain for channel 1 with a 8th order band-pass filter and channel 3 with a 4th order band-pass filter.

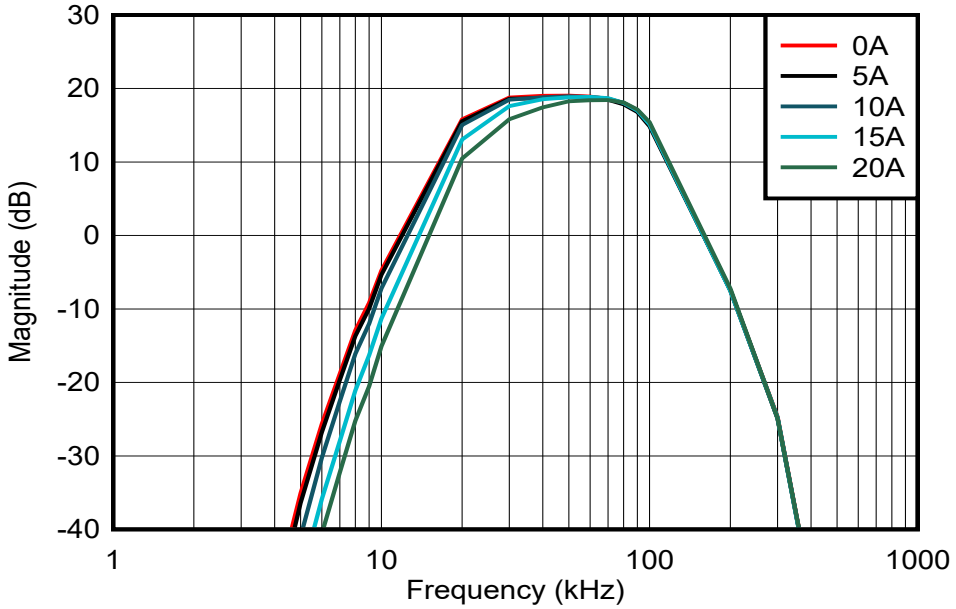

Figure 3-6. Transfer Curve of Analog Signal Chain With 8th Order Band-Pass Filter (CH1 and CH2)

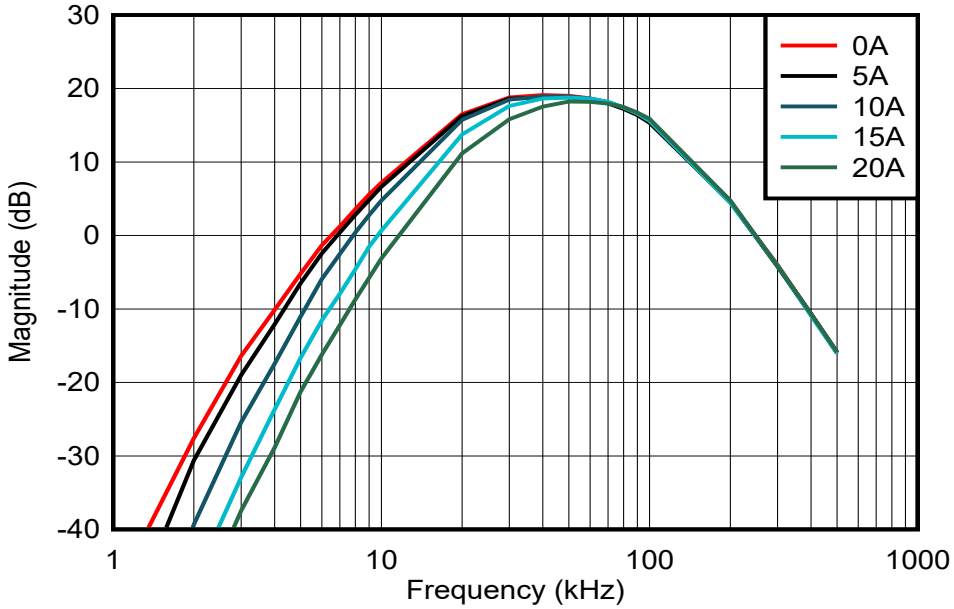

Figure 3-7. Transfer Curve of Analog Signal Chain With 4th Order Band-Pass Filter (CH3 and CH4)

3.2 Arc Testing

Figure 3-8 shows the setup for testing with real arcs. An arc generator is needed to emulate real-world arcs. The string of PV panels can be emulated by a DC current source. In that case, a decoupling and line impedance network is necessary to imitate the impedance of the solar cabling. The exact setup and testing scenarios are described in the relevant norms like UL1699B.

For the arc labeling circuit, it is important to connect the voltage across the arc generator with low impedance to the arc labeling circuit input J9. The string current needs to be feed through the current transformer. Connect the string voltage to connector J8.

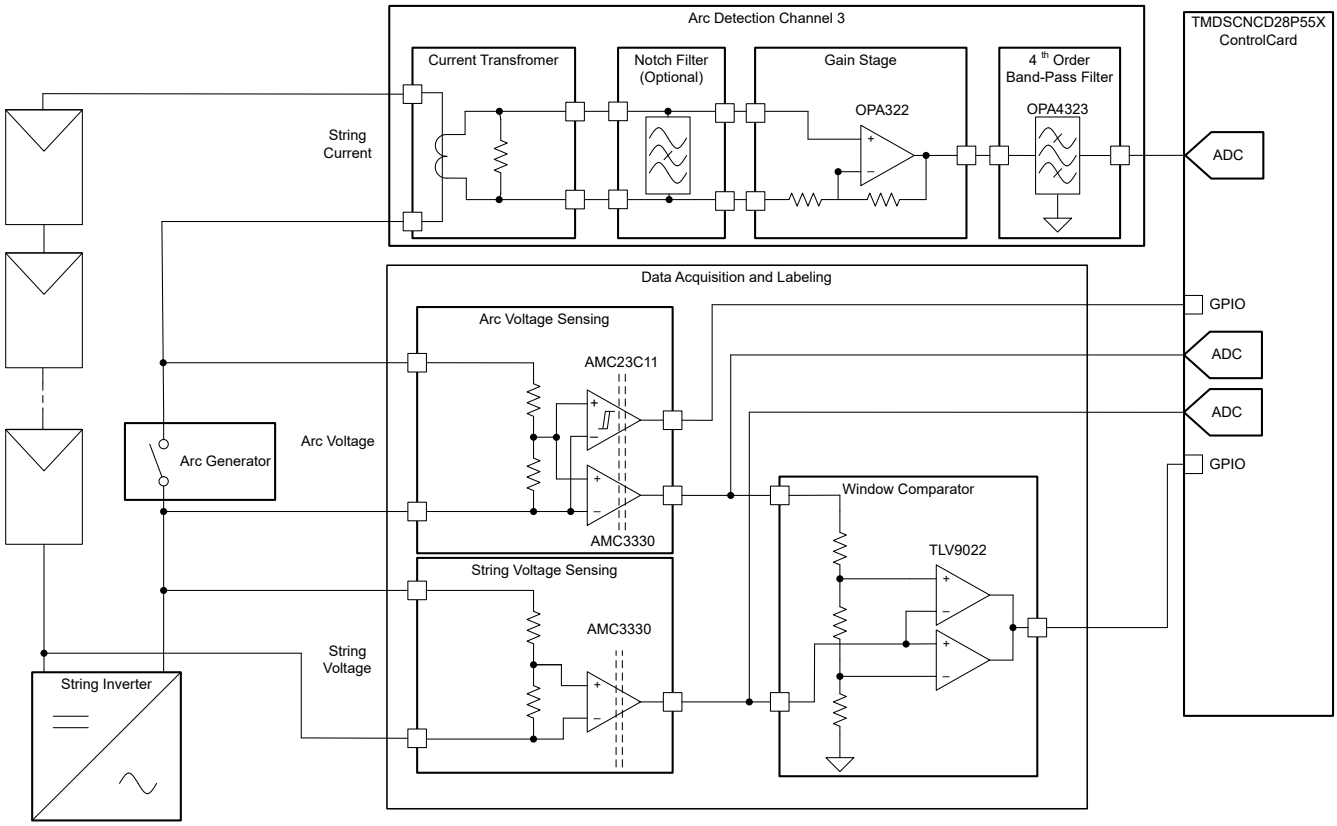

Figure 3-8. Test Setup for Test With Real Arcs

The description of the software tools and workflow on how to gather and label data, train an embedded AI model and validate the model is beyond the scope of this document. Links to detailed descriptions, user guides, tools and other resources are available in the product folder of TIDA-010955 and TIEVM-ARC-AFE. The required software is part of the C2000WARE-DIGITALPOWER-SDK.

4 Design and Documentation Support

4.1 Design Files

To download the design files, see the design files at TIDA-010955.

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010955.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010955.

4.2 Tools and Software

Tools

TMDSCNCD28P55X	TMDSCNCD28P55X controlCARD evaluation module
TIEVM-ARC-AFE	Orderable part number for this reference design
Filter Design Tool	Filter Design Tool used for band-pass design

Software

Code Composer Studio™	Integrated development environment (IDE)
C2000WARE-DIGITALPOWER-SDK	SDK including test software for this reference design
TI Resource Explorer	Software package in TI Resource explorer
Edge-AI-Studio	Landing Page for Edge AI Projects

4.3 Documentation Support

1. Texas Instruments, *TMDSCNCD28P55X controlCARD EVM User's Guide*
2. Texas Instruments, *OPAx323 20MHz High-Bandwidth, 114dB CMRR, Low Voltage (1.7V to 5.5V), RRIO Zero-Cross Operational Amplifier Data Sheet*
3. Texas Instruments, *AMC3330 Precision, ±1V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter Data Sheet*
4. Texas Instruments, *AMC23C11 Fast Response, Reinforced Isolated Comparator With Adjustable Threshold and Latch Function Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2024) to Revision A (December 2024)	Page
• Add context about the TIEVM-ARC-AFE throughout the document	1

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