Design Guide: TIDA-020072

100/1000Base-T1 Automotive Ethernet Expansion Reference Design for Jacinto™ 7 Processors

Description

This reference design interfaces with Jacinto™ 7 processor EVM boards through the Serial Ethernet Expansion Connector. Automotive Ethernet connectivity is added through TI's automotive Ethernet PHYs. The design is implemented with TI's DP83TC817S-Q1 100MBit/s single pair Ethernet (SPE) PHY with the option to switch to the DP83TG720S-Q1 SPE PHY for 1000MBit/s operation. A coupling network is used to couple in 12V to the data line.

Resources

TIDA-020072	Design Folder
DP83TC817S-Q1, DP83TC818S-Q1	Product Folder
DP83TG720S-Q1, DP83TG721S-Q1	Product Folder
TPS629210-Q1, TPS7B82-Q1	Product Folder
TPS74701-Q1	Product Folder

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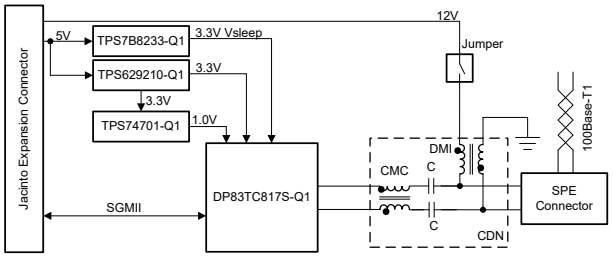
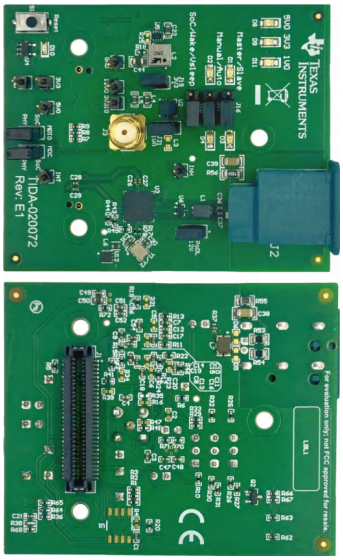
Features

- 100Base-T1 automotive Ethernet connected through SGMII to Jacinto™ 7 processors
- Footprint compatible to TI's 1000Base-T1 SPE PHYs
- Automotive qualified filter network for 12V power coupling
- Option to populate TI's BAW oscillator CDC6CEx-Q1
- Board ID EEPROM for identification

Applications

- Advanced driver assistance systems (ADAS)
- Body electronics and lighting
- Infotainment and cluster
- Software-defined vehicle





1 System Description

The Jacinto™ 7 EVMs are development and evaluation platforms that enable developers to write software and develop hardware around the Jacinto™ 7 family of processors. The main elements of the system are available on the EVM. This gives developers the basic resources needed for most general-purpose type projects that encompass the Jacinto™ 7 processor. Beyond the basic resources provided, additional functionality can be added through expansion cards.

This reference design adds automotive Ethernet connectivity through TI's automotive Ethernet PHYs. The DP83TC817S-Q1 automotive Ethernet PHY support 100Mbps link speed, is IEEE 802.3bw compliant and OA 100BASE-T1 compliant, and supports IEEE 802.1AS time synchronization as well as IEEE 802.1AE MACsec.

1.1 Key System Specifications

The key features of the TIDA-020072 reference design include:

- 100Base-T1 automotive Ethernet
- Default PHY address is configured to 15
- 12V can be coupled on the automotive Ethernet cable
- DP83TC817S-Q1 1.0V supplied by the internal LDO of the PHY
- Option to populate TI's BAW oscillator
- Footprint compatible to TI's 1000Base-T1 SPE PHYs
- Board ID EEPROM for board identification

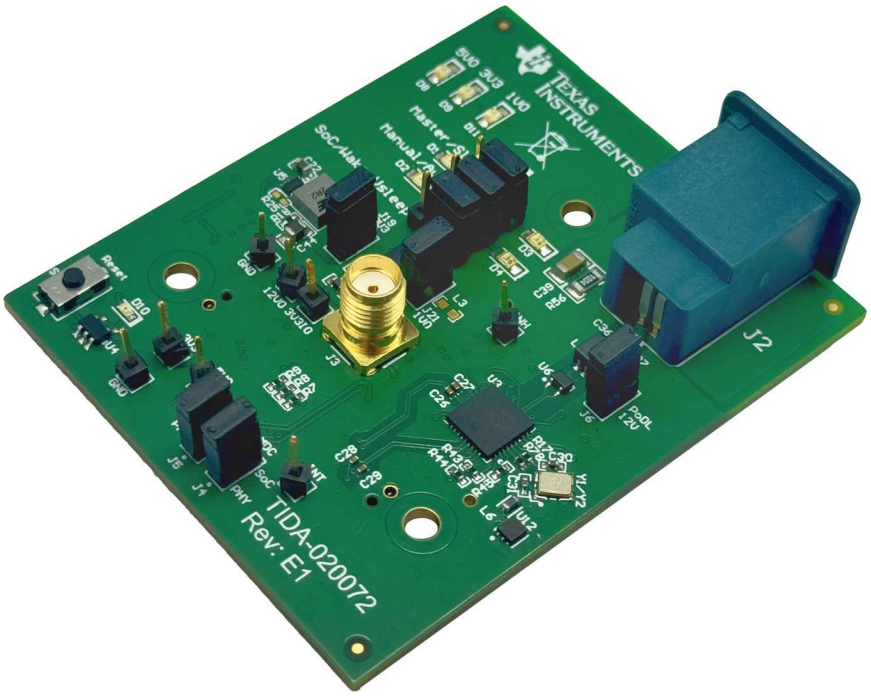


Figure 1-1. TIDA-020072 Board Image

2 System Overview

The system consists of this reference design, connected on one side through the expansion connector to a Jacinto 7 processor EVM and on the other side through one twisted-pair cable to a link partner as shown in Figure 2-1.

The Jacinto 7 EVM provides 5V power through the expansion connector to the buck converter and the LDO for 3.3V V_{SLEEP}. The device also provides 12V through Jumper J6 to the differential mode inductor L7 to couple in power to the automotive Ethernet cable.

2.1 Block Diagram

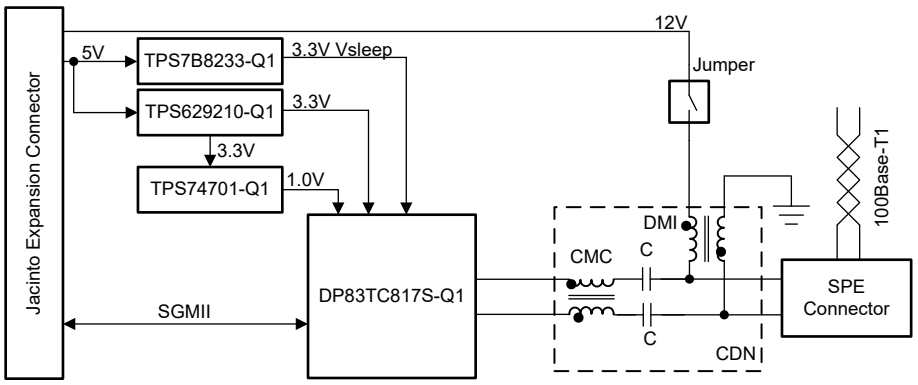


Figure 2-1. TIDA-020072 Block Diagram

2.2 Design Considerations

This reference design shows the implementation of an Ethernet interface consisting of a single-pair Ethernet (SPE) PHY with the option for powering a link partner through the same cable. This is part of Power over Data Lines (PoDL). Although PoDL is standardized in IEEE802.3bu for 100/1000Base-T1, this reference design is not compliant to IEEE802.3bu to address the automotive requirements. In the automotive sector the car OEM defines which ECUs and sensor modules are used in the system and therefore a detection and classification is not required. This assumption is based on the fact that the network does not change over the lifetime of the vehicle. The boards are designed to fulfill the automotive requirements for a cost- and weight-efficient implementation.

With transmitting the power over the same cable as the data, the use of the classic fuse is no longer applicable, which is why the integration of a high-side switch (HSS) is strongly recommended to protect the link partner from any damage. The 12V supply for power coupling to the data line is generated on the Jacinto 7 EVM by a LM5175 buck-boost converter. This device already supports protection features including cycle-by-cycle current limiting, output overvoltage protection (OVP), and thermal shutdown.

2.3 Highlighted Products

This section introduces the key devices in this reference design. For comprehensive details, see the product page and data sheet of each respective device.

2.3.1 DP83TC817S-Q1 (Automotive SPE PHY)

The DP83TC817-Q1 device is an IEEE 802.3bw automotive Ethernet physical layer transceiver. The device provides all physical layer functions needed to transmit and receive data, and xMII interface flexibility. DP83TC817-Q1 is compliant to Open Alliance EMC and interoperable specifications over unshielded single twisted-pair cable. DP83TC817-Q1 supports OA TC-10 low power sleep feature with wake forwarding for reduced system power consumption when communication is not required.

The DP83TC817-Q1 integrates IEEE 802.1AE line rate security with authentication and optional encryption support, to secure communication over the network. The PHY supports up to 16 secure association (SA) channels with automatic SAK rollover and extended packet numbering support. DP83TC817-Q1 offers ingress classification to filter the unwanted packets and supports WAN MACsec for end-to-end security.

DP83TC817-Q1 also integrates 1588v2 (802.1AS) to enable highly accurate time synchronization and hardware timestamping for ADAS applications. DP83TC817-Q1 also offers precise time stamping and synchronization with encrypted PTP packets.

DP83TC817-Q1 is footprint compatible to TI's 100BASE-T1 PHYs and 1000BASE-T1 PHYs enabling design scalability with a single board for different speeds and features.

2.3.2 TPS629210-Q1 (3.3V Rail Buck Converter)

The automotive-qualified TPS6292xx-Q1 family of devices are highly efficient, small, and highly flexible synchronous step-down DC-DC converters that are easy to use. A wide 3V to 17V input voltage range supports a wide variety of systems powered from either 12V, 5V, or 3.3V supply rails, or single-cell or multicell Li-Ion batteries. The TPS629210-Q1 can be configured to run at either 2.5MHz or 1MHz in a forced PWM mode or a variable frequency (auto PFM) mode. In auto PFM mode, the device automatically transitions to power save mode at light loads to maintain high efficiency. The low 4µA typical quiescent current also provides high efficiency down to the smallest loads. TI's automatic efficiency enhancement (AEE) mode holds a high conversion efficiency through the whole operation range without the need of using different inductors by automatically adjusting the switching frequency based on input and output voltages. In addition to selecting the switching frequency behavior, the MODE/S-CONF input pin can also be used to select between different combinations of external and internal feedback dividers and enabling and disabling the output voltage discharge capability. In the internal feedback configuration, a resistor between the FB/VSET pin and GND can be used to select between 18 different output voltage options.

2.3.3 TPS7B8233-Q1 (3.3V V_{SLEEP} Ultra-Low-I_Q Low-Dropout Regulator)

In automotive battery-connected applications, low quiescent current (I_Q) is important to save power and extend battery lifetime. Ultra-low I_Q must be included for always-on systems.

The TPS7B82-Q1 is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3V to 40V (45V load dump protection). Operation down to 3V allows the TPS7B82-Q1 to continue operating during cold-crank and start and stop conditions. With only 2.7µA typical quiescent current at light load, this device is an excellent choice for powering microcontrollers (MCUs) and CAN or LIN transceivers in standby systems.

The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to +125°C and with junction temperatures from –40°C to +150°C. Additionally, this device uses a thermally conductive package to enable sustained operation despite significant dissipation across the device. Because of these features, the device is designed as a power supply for various automotive applications.

2.3.4 TPS74701-Q1 (1.0V Rail Low-Dropout Regulator)

The TPS74701-Q1 low-dropout (LDO) linear regulator provides an easy-to-use, robust power management design for a wide variety of applications. The user-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current and the monotonic start-up is designed for powering many different types of processors and application-specific integrated circuits (ASIC). The enable input and power-good output allow easy sequencing with external regulators, allowing a design to be configured that meets the sequencing requirements for a wide range of applications with special start-up requirements.

A precision reference and error amplifier deliver 0.95% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2µF, and is fully specified per AEC-Q100.

2.3.5 CDC6CE025000-Q1 (BAW Oscillator)

Texas Instruments' Bulk-Acoustic Wave (BAW) is a micro-resonator technology that enables integration of high-precision BAW resonator directly into packages with ultra-low jitter clock circuitry. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

The CDC6x device is an ultra-low jitter, fixed-frequency oscillator which incorporates the BAW as the resonator source. The device is factory-programmed per specific operation mode, including frequency, voltage, output type, and function pin. With a high-performance fractional frequency divider, the CDC6x is capable of producing any frequency within the specified range providing a single device family for all frequency needs.

The high-performance clocking, mechanical stability, flexibility, and small package options for this device are designed for reference and core clocks in high-speed SERDES used in telecommunications, data and enterprise network, and industrial applications.

3 System Design Theory

This section provides details about different sections on the reference design.

3.1 Ethernet PHY

This board supports a broad range of TI's automotive SPE PHYs. The board supports both 100Base-T1 and 1000Base-T1. By default the board uses 100Base-T1 with DP83TC817S-Q1. To use this board with 1000Base-T1, the PHY can be replaced with the DP83TG720S-Q1 SPE PHY. When replacing the DP83TC817S-Q1 with the DP83TG720S-Q1, populate L3, C2, C5, C6, C15 and C16. Additionally, see the design requirements and power supply recommendations of the DP83TG720S-Q1 data sheet.

3.1.1 Ethernet PHY Power Supply

The DP83TC817S-Q1 is capable of operating with a wide range of I/O supply voltages (3.3V, 2.5V, or 1.8V). This board features an IO supply voltage of 3.3V to interface with various baseboards capable of 3.3V I/O voltage. The DP83TC817S-Q1 also requires a 1.0V rail. Figure 3-1 shows the implemented schematic that allows use of the DP83TC817S-Q1 integrated LDO to generate the required 1.0V. No power supply sequencing is required. Check and follow the *DP83TC817-Q1 Precise and Secure 100BASE-T1 Automotive Ethernet with TC10, IEEE802.1AS and IEEE802.1AE MACsec* data sheet for the latest power supply device recommendations.

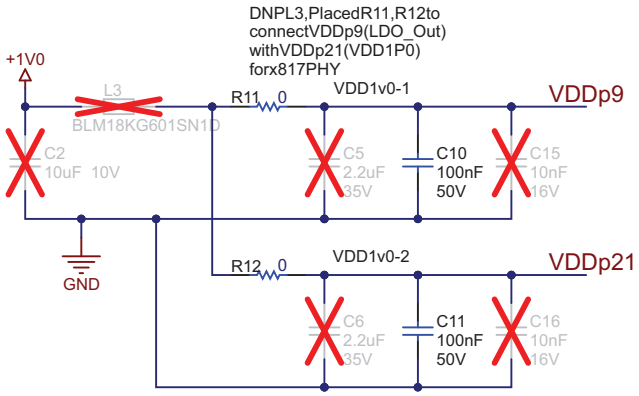


Figure 3-1. Ethernet PHY 1.0V Rail Schematic

3.1.2 Ethernet PHY Clock Source

Figure 3-2 shows the reference design schematic and the layout allowing population of TI's BAW oscillator to replace the crystal. To populate the BAW oscillator Y2, remove Y1, R19, R78, C30, and C31 and populate Y2, R21, and C56.

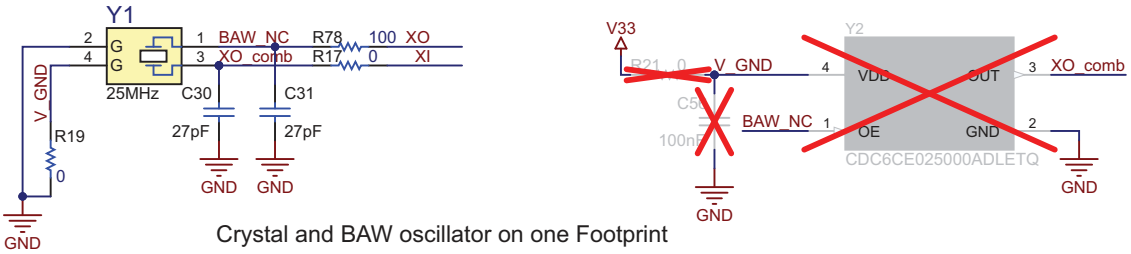


Figure 3-2. Ethernet PHY Clocking Schematic

3.2 Power Coupling Network

There are two main factors to consider when selecting a coupling network: Ethernet data rate and power consumption of the link partner. Table 3-1 shows each Ethernet PHY with the corresponding Ethernet standard and data frequency.

Table 3-1. Ethernet Signal Frequencies

Ethernet PHY	IEEE STANDARD	DATA RATE	SYMBOL RATE
—	10Base-T1S	10MBit/s	12.5MHz
DP83TC812-Q1	100Base-T1	100MBit/s	66.6MHz
DP83TC813-Q1			
DP83TC814-Q1			
DP83TC817-Q1			
DP83TG720-Q1	1000Base-T1	1000MBit/s	750MHz
DP83TG721-Q1			

Each coupling network has a maximum current that the network can support while maintaining the required impedance based on the saturation characteristics of the components. Inductors do not behave in an manner, the inductors dissipate heat, pass very high frequencies, and saturate when too much current is passed through. All components and cables have parasitic capacities and inductance throughout the entire circuit. Knowing the maximum power, the link partner draws from the power line and selecting a component design that can deliver that power for a given voltage is important. Calculate the maximum power as the worst-case scenario of power consumption on the link partner side.

Table 3-2 provides coupling network design suggestions. TI recommends selecting one of the networks based on the desired frequency range, current rating, and temperature.

Table 3-2. CDN Filter Design for PoDL

VENDOR	Ethernet SPEED	COMPONENTS	CURRENT RATING	TEMPERATURE RATING
TDK	1000Base-T1	CMC: ACT1210G-800 DMI: ADL32VHR-3R9M	540mA	150°C
TDK	100Base-T1	CMC: ACT1210L-201 DMI: ADL32VHR-180M	370mA	150°C

4 Hardware, Software, Testing Requirements, and Test Results

This section describes the fundamental hardware and software requirements to demonstrate the automotive Ethernet functionality in a minimal setup. The setup allows measurement of the maximum achievable bandwidth on IP networks.

4.1 Hardware Requirements

Table 4-1 lists the required hardware.

Table 4-1. Hardware Required for Minimal Setup

QUANTITY	DEVICE DESCRIPTION	DEVICE NUMBER
1 ×	DP83TC813S-Q1 100Base-T1 Automotive Ethernet Expansion Reference Design	TIDA-020073
1 ×	Jacinto™ 7 system on module (SoM) board	J721EXSOMXEVM
1 ×	Common processor board for Jacinto™ 7 processors	J721EXCPXEVM
1 ×	Automotive to standard Ethernet media converter for 100MBit/s	DP83TC812EVM-MC
1 ×	TE Connectivity MATEnet SPE cable	—
1 ×	RJ45 Cable	—
1 ×	12V, 5A power supply	—

4.2 Software Requirements

This section describes the software requirements for the minimal setup. The Software development kit (SDK) for Jacinto™ 7 processors is used to control and monitor the Ethernet PHY on this reference design (shown in Figure 4-1) during testing.

The automotive Ethernet PHY driver needs to be added to the Linux SDK for the Jacinto™ 7 processor to be able to identify the Ethernet PHY. See the *How to Integrate Linux Driver Into Your System* application note.

The Linux Device Tree overlay for this specific board with the PHY configured for PHY address 15 is shown in the following code block for Jacinto™ 7 SDK v10. For other SDK versions, see the SDK documentation.

```
/dts-v1/;
/plugin/;

#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/phy/phy.h>
#include <dt-bindings/phy/phy-cadence.h>
#include "k3-pinctrl.h"
#include "k3-serdes.h"

&{/} {
    aliases {
        ethernet2 = "/bus@100000/ethernet@c000000/ethernet-ports/port@2";
    };
};

&cpsw0 {
    status = "okay";
};

&cpsw0_port2 {
    status = "okay";
    phy-handle = <&cpsw9g_phy15>;
    phy-mode = "sgmii";
    mac-address = [00 00 00 00 00 00];
    phys = <&cpsw0_phy_gmii_sel 2>;
};

&cpsw9g_mdio {
    status = "okay";
    pinctrl-names = "default";
    pinctrl-0 = <&mdio0_pins_default>;
    reset-gpios = <&exp2 17 GPIO_ACTIVE_LOW>;
    reset-post-delay-us = <120000>;
```

```
    #address-cells = <1>;
    #size-cells = <0>;

    cpsw9g_phy15: ethernet-phy@15 {
        reg = <15>;
    };
};

&exp2 {
    qsgmii-line-hog {
        gpio-hog;
        gpios = <16 GPIO_ACTIVE_HIGH>;
        output-low;
        line-name = "qsgmii-pwrdn-line";
    };
};

&main_pmx0 {
    mdio0_pins_default: mdio0-pins-default {
        pinctrl-single,pins = <
            J721E_IOPAD(0x1bc, PIN_OUTPUT, 0) /* (V24) MDIO0_MDC */
            J721E_IOPAD(0x1b8, PIN_INPUT, 0) /* (V26) MDIO0_MDIO */
        >;
    };
};

&serdes_ln_ctrl {
    idle-states = <J721E_SERDES0_LANE0_PCIE0_LANE0>, <J721E_SERDES0_LANE1_QSGMII_LANE2>,
              <J721E_SERDES1_LANE0_PCIE1_LANE0>, <J721E_SERDES1_LANE1_PCIE1_LANE1>,
              <J721E_SERDES2_LANE0_PCIE2_LANE0>, <J721E_SERDES2_LANE1_PCIE2_LANE1>,
              <J721E_SERDES3_LANE0_USB3_0_SWAP>, <J721E_SERDES3_LANE1_USB3_0>,
              <J721E_SERDES4_LANE0_EDP_LANE0>, <J721E_SERDES4_LANE1_EDP_LANE1>,
              <J721E_SERDES4_LANE2_EDP_LANE2>, <J721E_SERDES4_LANE3_EDP_LANE3>;
};

&serdes_wiz0 {
    status = "okay";
};

&serdes0 {
    status = "okay";

    assigned-clocks = <&serdes0 CDNS_SIERRA_PLL_CMNLC>, <&serdes0 CDNS_SIERRA_PLL_CMNLC1>;
    assigned-clock-parents = <&wiz0_pll1_refclk>, <&wiz0_pll1_refclk>;
    #address-cells = <1>;
    #size-cells = <0>;

    serdes0_qsgmii_link: phy@1 {
        reg = <1>;
        cdns,num-lanes = <1>;
        #phy-cells = <0>;
        cdns,phy-type = <PHY_TYPE_SGMII>;
        resets = <&serdes_wiz0 2>;
    };
};
```

In addition to adding the PHY driver, adjusting the Device Tree, the following needs to be done, to enable the SGMII interface:

Inside the file: `SDK_Install_Directory/board-support/ti-u-boot-<version>/configs/j721e_evm_a72_defconfig`

Comment out the following two lines with “#” as shown below:

```
# CONFIG_PHY_CADENCE_SIERRA=y
# CONFIG_PHY_J721E_WIZ=y
```

After that, build `u-boot` using the top level make command:

```
make u-boot
```

Copy the build binaries `u-boot.img` and `tispl.bin` to the boot partition of the SD-card.

```
sudo cp SDK_Install_Directory/board-support/ti-u-boot-x/build/a72/u-boot.img /media/$USER/boot
sudo cp SDK_Install_Directory/board-support/ti-u-boot-x/build/a72/tispl.bin /media/$USER/boot
```

Change the linked firmware of `r5f0_0-fw` with the following command:

```
ln -sfn /usr/lib/firmware/ti-ipc/j721e/ipc_echo_test_mcu2_0_release_strip.xer5f /lib/firmware/j7-main-r5f0_0-fw
```

With the board powered up, use the following terminal command to confirm the PHY address (`phy[x]`) and `eth` port (`eth[y]`).:

```
dmesg | grep mdio
```

```
davinci_mdio c000f00.mdio: phy[15]: device c000f00.mdio:0f, driver TI DP83TC817CS2.0
am65-cpsw-nuss c000000.ethernet eth1: PHY [c000f00.mdio:0f] driver [TI DP83TC817CS2.0] (irq=POLL)
```

4.3 Test Setup

Figure 4-1 shows the block diagram of the test setup. The setup consists of a Jacinto™ 7 processor EVM, TIDA-020072, DP83TC812EVM-MC, a standard PC, and cable assemblies.

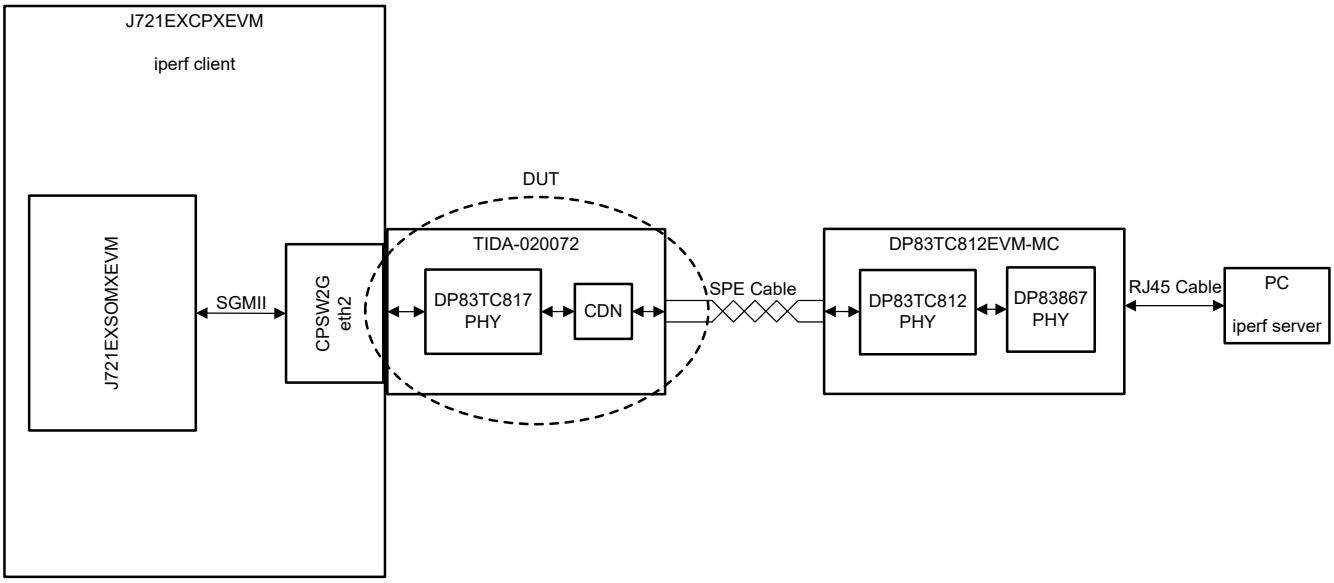


Figure 4-1. IP Network Bandwidth Test Setup

iPerf3, an open-source tool used to measure network performance and bandwidth, is already integrated in TI's SDK, and can be used with following commands after an IP address is assigned to the Ethernet port.

Run the following command on the PC (server):

```
iperf3 -s
```

Additionally, run the following command on the Jacinto™ 7 (client):

```
iperf3 -c 192.168.1.1 (the IP address of the server)
```

4.4 Test Results

The following terminal message is captured from the Jacinto™ 7 EVM. With the 100Mbit/sec connection, observe that 114 MBytes (112 MBytes) of data successfully transferred and the bandwidth is very close to the advertised speed of the network port (100Mbit/sec).

```
root@j721e-evm:~# iperf3 -c 192.168.1.1
Connecting to host 192.168.1.1, port 5201
[  5] local 192.168.1.237 port 32836 connected to 192.168.1.1 port 5201
[ ID] Interval           Transfer     Bitrate         Retr  Cwnd
[  5]   0.00-1.00   sec  12.6 MBytes   106 Mbits/sec    0    249 KBytes
[  5]   1.00-2.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   2.00-3.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   3.00-4.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   4.00-5.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   5.00-6.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   6.00-7.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   7.00-8.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   8.00-9.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   9.00-10.00  sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
- - - - - - - - - - - - - - - - - - - - - - - - -
[ ID] Interval           Transfer     Bitrate         Retr
[  5]   0.00-10.00  sec   114 MBytes  95.2 Mbits/sec    0             sender
[  5]   0.00-10.05  sec   112 MBytes  93.8 Mbits/sec                  receiver

iperf Done.
```

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-020072.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-020072.

5.2 Tools and Software

Tools

ETHERNET-SW	Ethernet PHY Linux drivers and tools
J721EXCPXEVM	Common processor board for Jacinto™ 7 processors
J721EXSOMXEVM	TDA4VM and DRA829V system on module (SoM)

Software

PROCESSOR-SDK-J721E	Software development kit for DRA829 and TDA4VM Jacinto™ processors

5.3 Documentation Support

1. Texas Instruments, *How to Integrate Linux Driver Into Your System Application Note*
2. Texas Instruments, *DP83TC817-Q1 Precise and Secure 100BASE-T1 Automotive Ethernet with TC10, IEEE802.1AS and IEEE802.1AE MACsec Data Sheet*
3. Texas Instruments, *DP83TC811, DP83TC812, DP83TC814, DP83TG720 Hardware Rollover Document Application Note*
4. Texas Instruments, *TDA4: Custom Board Bring Up Guide Application Note*
5. Texas Instruments, *High-Speed Interface Layout Guidelines Application Note*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

YANNIK MUENDLER is a systems engineer at Texas Instruments contributing to the Automotive ADAS Systems Engineering team. In this role, he plays a pivotal part in the development of reference designs within the automotive sector. With a wealth of expertise in areas such as high-performance compute with TI's Jacinto™ 7 processors and communication interfaces such as single-pair Ethernet and FPD-Link™ technology, Yannik brings a depth of knowledge and experience to his responsibilities.

He holds a Master of Engineering degree in Electrical Engineering from the Landshut University of Applied Science in Germany.

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