Design Guide: TIDA-010956

48V, 85A Small Form-Factor Three-Phase Inverter Reference Design for Integrated Motor Drives

TEXAS INSTRUMENTS

Description

This reference design demonstrates a 48V DC input, 85A$_{RMS}$ output, three-phase motor drive inverter. The 100V intelligent half-bridge gate driver DRV8162L enables a small size, robust, and high-efficiency power stage. Multichannel shutdown paths are proposed, utilizing the split power supply architecture of DRV8162L, for the Safe Torque Off (STO) function. Internal V$_{DS}$ monitor and protection features of the DRV8162L protect against overcurrent failures. Precision motor current sensing is achieved in phases A and B using INA241A, and in phase C using the AMC0106M05 functional isolated delta-sigma modulator. A 3.3V I/O interface to connect a host controller, like a C2000™ MCU, is provided for quick and easy evaluation.

Resources

|	
TIDA-010956	Design Folder
DRV8162, AMC0106M05, INA241A	Product Folder
TMP6131, TPSM861253	Product Folder
ISOM8710, LMR38010	Product Folder
LAUNCHXL-F280039C	Tool Folder

Ask the TI E2E™ support experts

Features

- Three-phase inverter with 24V to 60V DC input and 85A$_{RMS}$ continuous output
- Smart half-bridge gate driver DRV8162L with on-chip hardware protection
- Fully-protected against: shoot-through, over current, short circuit, under voltage, over temperature
- Programmable gate driver source, sink currents from 16mA, 32mA to 1A, 2A eases optimization of efficiency and EMI performance
- Configurable dead-time insertion to avoid shoot-through
- In-phase shunt-based current sensing with INA241A high-common mode rejection, zero-drift current-sense amplifier and AMC0106M05 function isolated modulator
- Multichannel shutdown paths to enable flexible design of STO function

Applications

- Single and multiaxis servo drives
- Robotics
- AC inverter and VF drives
- Industrial and collaborative robot
- Mobile robot
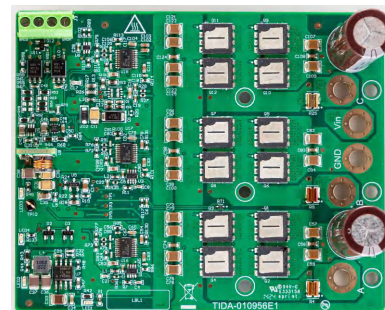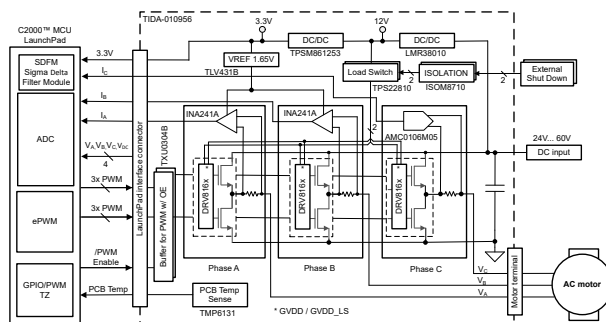
1 System Description

Many low-voltage, three-phase inverters for DC-fed motor drives are powered by a 24V to 60V DC rail. When looking at robotics systems, the motors often have different power ratings typically at 200W, 400W, 750W, 1.5kW, and 2.5kW, or even higher occasionally, depending on the functions to implement. These motors have different requirements on the current rating of the motor drives.

This design supports motors from 1.5kW to 4kW with a 48V DC input. The rated output current can be about $32A_{RMS}$ to $85A_{RMS}$; and in some occasions can reach up to around $100A_{RMS}$.

In designing this kind of power stage, high efficiency is a key target. With high efficiency, a small PCB size can be achieved, and the driver can be fit into the shell of an integrated motor drive system, where the power stage can only use the shell as heat sink for thermal dissipation.

To achieve a small PCB size in this design, the smart gate driver DRV8162L helps a lot with the integrated protection functions against power stage shoot-through, over current, and short circuit faults. A V_{GS} handshake with dead time insertion can be enabled to prevent shoot-through from happening.

To optimize system efficiency and EMI performance, the DRV8162L adds the ability to program output source and sink currents without adding any external circuitry.

To enable the drive to control motor at the highest efficiency, in-phase shunt-based current sensing is adopted in phase A and phase B using the INA241A, a high common-mode rejection, zero-drift featured current sense amplifier. Due to the high gain of the amplifier, a 0.2mΩ shunt is used to support a linear sense range of ±165A. The low resistance shunt selection also contributes to the high efficiency of the system. In phase C, a functional isolated delta-sigma modulator AMC0106M05 is used with a 0.3mΩ shunt resistor to sense the current. Working with a digital sinc three decimation filter in the MCU, the linear current measurement range reaches ±167A.

Additional feedback includes the DC-bus voltage and the pulse width modulation (PWM) filtered three-phase voltages to allow validation of advanced sensorless control like the InstaSPIN-FOC™ motor.

Designing the system to be able to stop the motor safely and prevent any unexpected start-ups are critical requirements for robotics and factory automation applications. To assist these system level requirements and achieve the so-called Safe Torque Off (STO) function, this reference design proposes various combinations of shutdown paths for the gate drivers to prevent the motor from unexpected power up.

1.1 Reference Design Overview

This reference design implements a typical 48V three-phase inverter with smart half-bridge gate drivers for low-voltage motors. The major building blocks are six different subsystems:

1. Three-phase power stage including gate drivers and field-effect transistors (FET)
2. Voltage and current sensing
3. Host processor interface
4. Diagnostic measurements
5. System power supply
6. Multilevel shutdown options of the gate driver

Figure 2-1 shows the block diagram of this reference design. The host processor to control the motor is not part of this design.

The focus of this design is to test on the three-phase power stage, including the gate drivers and the FETs. Functional tests on the in-phase current sensing is also done. The diagnostic measurements and the shutdown options are not fully tested yet.

1.2 Key System Specifications

Table 1-1. TIDA-010956 Specifications

PARAMETER	VALUE (TYPICAL)	COMMENT
DC input voltage	24V to 60V	Absolute maximum 80V DC.
Output phase current	85A$_{RMS}$	Continuous current. A heat sink is possibly needed and airflow for the FETs is important.
In-phase current sense range	±165A (Phase A and B)	Phase A and B scaled to 0V to 3.3V range, inverted, with a 1.65V bias
	±167A (Phase C)	Phase C scaled to ±50mV range
In-phase current sense shunt	0.2mΩ (Phase A and B)	Phase A and B use two pieces of differential, non-isolated amplifier INA241A3, with enhanced pulse-width modulation (PWM) rejection
	0.3mΩ (Phase C)	Phase C uses a functional isolated delta-sigma modulator AMC0106M05
PWM switching frequency	16kHz	Up to 40kHz
PWM dead time	User defined	Default 370ns with the hardware R$_{DT}$ setting
Temperature range	–40°C to 85°C	Possibly need a proper heat sink and airflow for thermal dissipation of the FETs
Protections	Short-circuit protection	With the default R$_{VDSLVL}$ setting. See also Table 2-1
	Shoot-through protection	Automatic dead-time insertion handshake
	Temperature protection	Temperature sensor mounted on PCB to indicate overtemperature
	UVLO	Integrated at 4.8V
PCB temperature sense range and accuracy	–40°C to 150°C	Using a TMP6131, ±1%, 10kΩ linear thermistor
Controller interface signals	3.3V I/O for PWM, I-V sensing, PWM buffer and gate driver enables, fault	TI BoosterPack™ Plug-in Module compatible; supporting 3.3V signal levels. See pin assignments in Section 3.1.2.
Indicator LEDs	Power rails and user-defined	3.3V, 12V, V$_{IN}$ input and one for user software control.
PCB layer stack	Eight-layer, 70µm copper	2oz copper
Form Factor	80mm × 98mm	3150mil × 3860mil

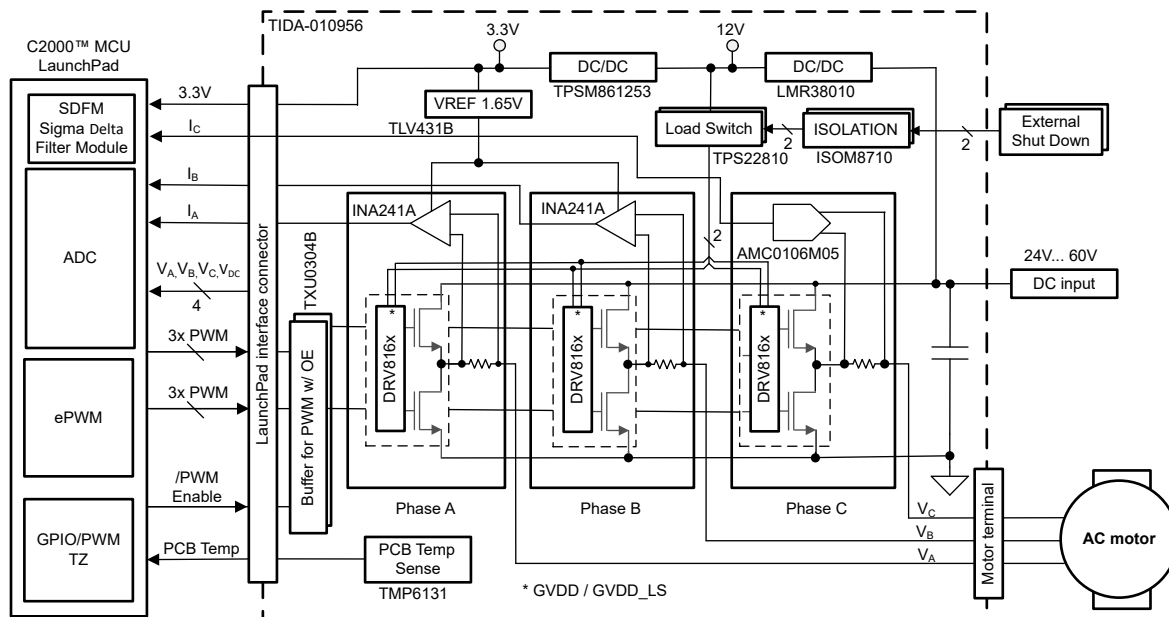# 2 System Overview

2.1 Block Diagram

Figure 2-1. TIDA-010956 System Block Diagram

2.2 Design Considerations

2.2.1 Hardware Design

2.2.1.1 Power Stage Gate Driver

2.2.1.1.1 Gate Driver

The DRV8162L is used to drive two N-Channel power MOSFETs in half-bridge configuration. The device supports 16-level output peak currents up to 1A source and 2A sink. This reference design optimized the gate drive currents for the best switching performance of the power stage.

2.2.1.1.2 Protection Features

The overcurrent event of the power stage is detected with the DRV8162L by measuring the drain-source voltage drop V_{DS} of the FET. The overcurrent trip threshold of the DRV8162L can be set using strap resistors with 13-level options. These values can be found in the *protection circuits* section of the *electrical characteristics* chapter of the *DRV8162L* data sheet, by the parameters of $V_{DS\_LVLx\_y}$. The minimum is 0.1V and the maximum is 2.0V.

With this feature, a blanking time is also adopted to make sure no overshoots are being detected during the switching of the FETs.

For more information on the protection features, see *gate driver protective circuits* section in the *DRV8162L* data sheet.

2.2.1.1.3 V_{GVDD} Definition

The DRV8162L has two power-supply pins, GVDD and GVDD_LS, for the high-side and low-side operations, respectively. The high-side power supply V_{GVDD} can be in 5V to 20V range. The low-side power supply V_{GVDD_LS} can be even lower to a minimum 3.5V. These values are found in the *electrical characteristics* section of the DRV8162L data sheet by the V_{GVDD} parameter.
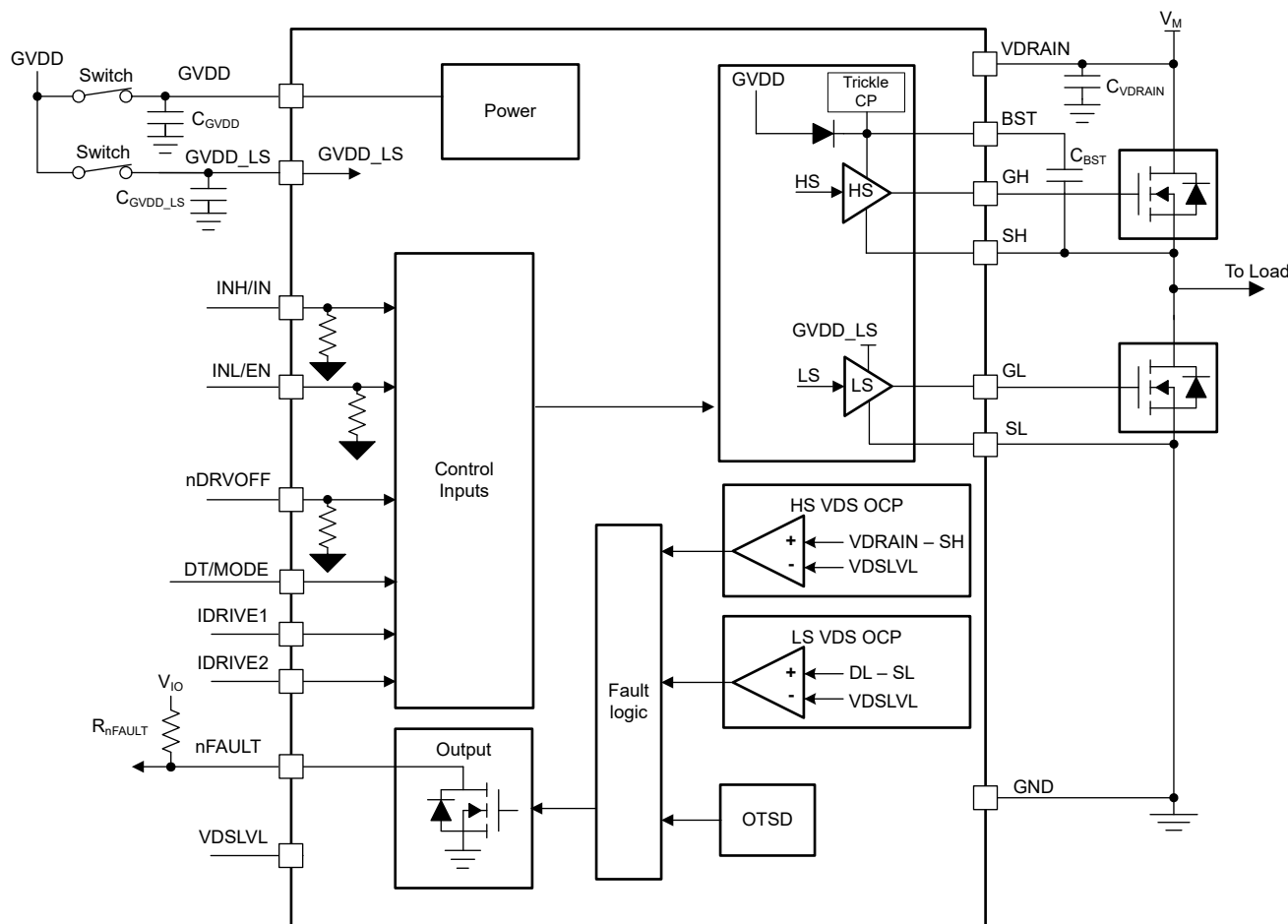

Figure 2-2. DRV8162L Split Power Supply Architecture

Typically, in this design, the V_{GVDD} and the V_{GVDD_LS} are set to 12V for the best performance of the FETs selected.

When picking the FETs, knowing the values of V_{GS} and $R_{DS(ON)}$ is important. These parameters have significant impacts on the efficiency of the overall system.

2.2.1.1.4 Strap Functions

When designing application circuits with DRV8162L, the following parameters can be adjusted using strap resistors:

- Drive strength
- Dead time
- Control mode
- V_{DS} overcurrent threshold

2.2.1.2 Power Stage FETs

With the targeted power rating of this system, choosing a FET which can meet the system needs is important. In this design, a choice of paralleling two FETs is made to meet the high current requirements.

2.2.1.2.1 V_{GS} versus $R_{DS(ON)}$

The V_{GVDD} and V_{GVDD_SL} voltages can define the ON state V_{GS}, or the actual high level gate voltage of the FETs in an application.

This value can be used to find the $R_{DS(ON)}$ of the FET at the given voltage. The $R_{DS(ON)}$ is needed in defining the overcurrent trip level of the DRV8162L.

With these considerations, calculation of the FET chosen is made and the results are shown in Table 2-1. This design implements two parallel FETs to achieve lower $R_{DS(ON)}$ and enable high-current output. The calculation is done using Ohm's law.

Table 2-1. Overcurrent Trip Level of DRV8162L with Regards to NTMTSC1D6N10 V_{DS}

PARAMETER	NTMTSC1D6N10		2 × NTMTSC1D6N10	
I_D	267A		534A	
I_{DM}	900A		1800A	
Q_G	106nC		212nC	
Junction Temperature	25°C	125°C	25°C	125°C
$R_{DS(ON)}$ at V_{GS} = 10V	1.42mΩ	2.50mΩ	0.71mΩ	0.88mΩ
TRIP LEVEL1-0: 0.15V	106A	60A	211A	120A
TRIP LEVEL1-1: 0.2V	141A	80A	282A	160A

When using fast switching FETs, RC snubber networks can be necessary for each half bridge to suppress ringing of the circuit. This design reserves an RC snubber for every half bridge as an option for test and debug, although these are not needed for the test cases.

2.2.1.3 Phase Current and Voltage Sensing

For technology comparison, this design offers two different cases of shunt-based precision phase-current sensing. The A and B phases employ the differential current sense amplifier INA241A. The C phase employs a functional isolated modulator AMC0106M05.

2.2.1.3.1 Phase A and Phase B Current Sensing

For A and B phase current sensing, as the ADC module of the controller MCU selected for testing the system accepts a maximum input voltage of 3.3V, the measured voltages are scaled into the 0V to 3.3V range. When using a different MCU, a voltage scale of 3.0V can be used, if necessary.
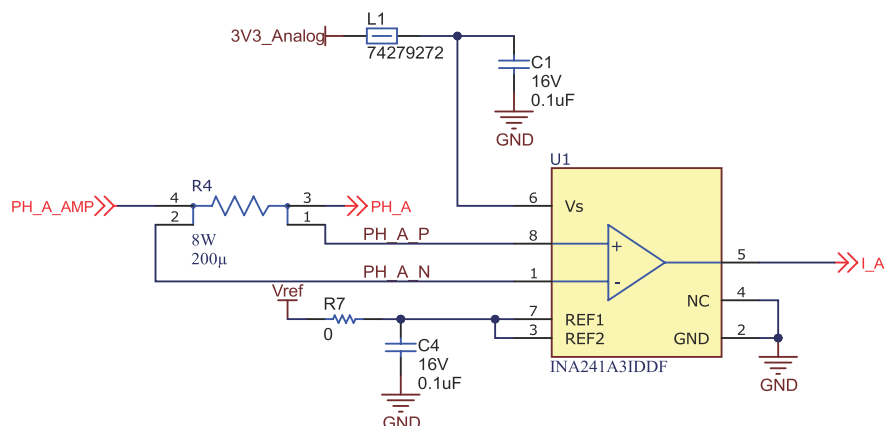

Figure 2-3. Inline Phase Current Sense With INA241 for Phase A

This design supports a rated motor current of 85A$_{RMS}$ or 120A at peak. Allowing for some margin, the maximum current sense range is set to 165A. With this specification, a 0.2mΩ, 8W shunt resistor is chosen and an amplifier with a fixed 50 gain is selected.

The in-phase currents measured are bidirectional, so the voltage range calculated is further scaled by 2.

Now, we can use Equation 1 to calculate the voltage range of the amplifier output.

$$V_{scale} \quad = \quad I_{ph} \quad \times R_{shunt} \times G_{amp} \times 2 = 165A \times 0.2mΩ \times 50 \times 2 = 3.3V \tag{1}$$

With the scale set to 3.3V, the voltage reference of the amplifier is also set to make sure that 0A corresponds to the center point of the voltage scale. Figure 2-4 shows the 1.65V bias voltage reference, using a TLV431, that is adopted in this design.
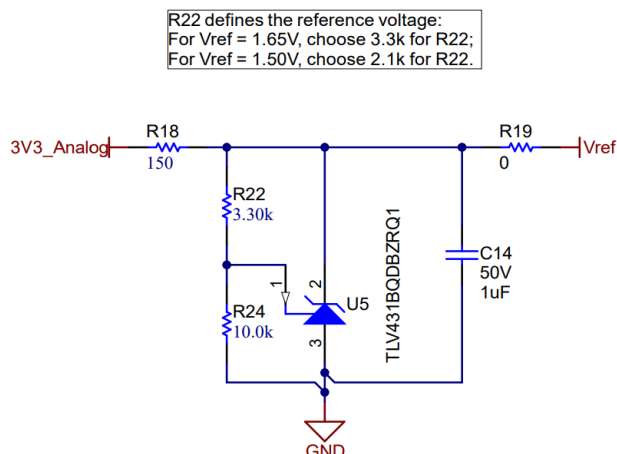
Figure 2-4. TLV431 Schematic From TIDA-010956

Resistor R18 limits the maximum current flow into the circuit. A 150Ω resistor is chosen. R22 and R24 determines the output voltage of the bias reference circuit. Fix R24 to 10.0kΩ, then R22 can be chosen as 3.3kΩ for the 1.65V bias reference of INA241A.

Make sure that the power dissipation rating of the current sense shunt resistor can sustain the current of the system.

$$P_{loss} = I_{RMS}^2 \times R_{shunt} = 165A^2 \times 0.2mΩ = 5.445W \tag{2}$$

The 165A is only possible in case of a fault condition. The nominal current rating is 85A$_{RMS}$, and then the power loss is merely 1.445W. The 8W shunt resistor has enough margin.

2.2.1.3.2 Phase C Current Sensing

Phase C current sensing is using the functionally isolated modulator AMC0106M05 (U4) with a ±50mV linear input voltage range, and a 300µΩ, 8W shunt resistor. The 300µΩ shunt value determines that the linear input range is ±167A. The AMC0106M05 has a ±64mV input clipping range; therefore, the maximum current range can be ±213A. The power dissipation in the shunt at 160A is 7.68W.
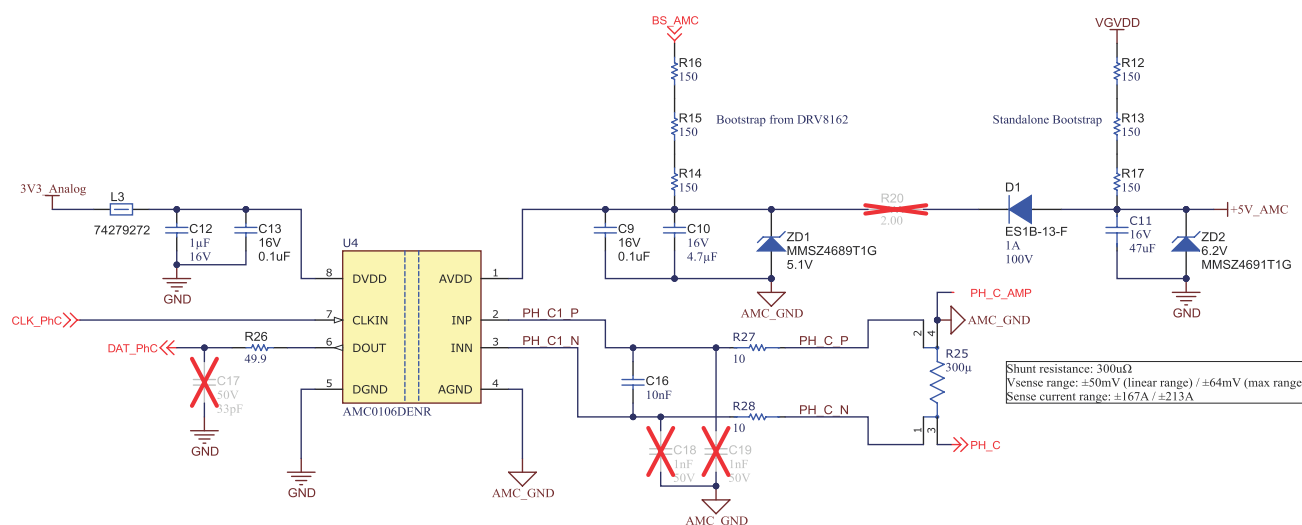
Figure 2-5. Inline Phase Current Sense With ACM0306M05 for Phase C

The application circuit here follows the recommended pattern in the data sheet. For the high-side power supply, two channels of boot-strap circuits are available to choose. One channel comes from the bootstrap voltage BS_AMC of the phase C gate driver, through R14, R15, R16, and then clamps at 5.1V by ZD1; another channel comes from a standalone bootstrap circuit by R20, D1, C11, ZD2 and R12, R13, R17. By default, the R20 is not populated and the standalone bootstrap circuit is not active.

For more details about the AMC0106M05 application and performance, see the *High Resolution, Small Form Factor Phase Current Sense for 48V Robotics and Servo Drives* application note.

See also the *Achieving Better Signal Integrity With Isolated Delta-Sigma Modulators in Motor Drives* and *Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs* application notes for more design tips.

2.2.1.3.3 Voltage Sensing

The DC input voltage V_{IN} and the three phase output voltages of the drive are measured in this design. The maximum input voltage can be up to 80V and is limited by the LMR38010 buck converter, which is used to generate the 12V voltage rail for the gate drivers.

In this design, the voltage sense dividers are set to support a maximum sense voltage of 80V, which is enough for the rated V_{IN} of 48V for the system.

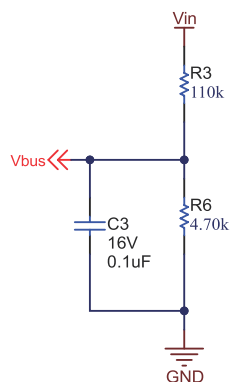Figure 2-6 shows a schematic view of the V_{IN} voltage measurement.

Figure 2-6. TIDA-010956 V_{IN} Voltage Sense Circuit

Equation 3 is used for the calculation.

Copyright © 2025 Texas Instruments Incorporated

$$R_6 = \frac{R_3 \times V_{OUT}}{V_{IN} - V_{OUT}} = \frac{110k\Omega \times 3.3V}{80V - 3.3V} = 4{,}733\Omega \tag{3}$$

where

- R3 is chosen as 110kΩ

For each voltage divider, a low-pass filter is adopted; such as in this specific channel with C3.

For the phase voltages and the V_{IN} voltage measurements, put these values into Equation 3: V_{IN} = 80V, V_{out} = 3.3V, R_3 = 110kΩ. This makes R_6 = 4733Ω. A 4.7kΩ, 1% resistor is chosen.

2.2.1.4 Host Processor Interface

The processor interface is designed to work with a LAUNCHXL-F280039C or a LAUNCHXL-F28P65X through the J1 and J2 headers. In this design, all the tests are done using a LAUNCHXL-F280039C controller board. More details on the pins and signals are available in Section 3.1.2.3.

2.2.1.5 Gate Drive Shutdown Path

Due to the V_{GVDD} and V_{GVDD_LS} split-supply feature of the half-bridge gate driver DRV8162L, there is an option to shut down the high-side outputs and the low-side outputs of the gate drivers of the three phases with independent paths. An example circuit is implemented in this design.

There are two load switches (U12 and U14, TPS22810DRVR) built into the system for the V_{GVDD} and the V_{GVDD_LS} supplies, respectively. Inside the DRV8162L, the V_{GVDD_LS} is used to supply the low-side driver circuits and the V_{GVDD} is used to supply the high-side bootstrap circuit.

There is a third shutdown path built into the system with a specific load switch (U9, TPS22948DCKT) for the 3.3V power supply of the two PWM buffers and level translator chips (U13 and U15, TXU0304BQA). The output-enable (OE) pins of both devices can be configured to be fed with either an GPIO output of the system control MCU (J2-Pin18 of the host processor interface) or an external input signal through an opto-emulator isolator (U10 or U11, ISOM8710DFF).

2.2.1.6 System Diagnostic Measurements

2.2.1.6.1 Temperature Measurement

A temperature sensor (RT1, TMP6131DYAR) is used in this design to provide an option for the host controller to either simply turn off the three phases outputs or perform some comprehensive output control in case of the temperature of the PCB, sensed at a point just beside the C-phase low-side FET of Q3, is too high.

2.2.1.7 System Power Supply

As mentioned in previous chapters, the DRV8162L smart gate driver has two split power supplies for the high-side (V_{GVDD}) and the low-side (V_{GVDD_LS}), respectively. Both are fed with an intermediate supply rail of 12V, through the U12 or U14 load switches. So, the actual V_{GS} voltage applied to the power MOSFETs can be affected by the 12V supply rail.

2.2.1.7.1 12V Rail

To generate the 12V intermediate supply rail for the DRV8162L gate drivers of the three phases, a 4.2V to 80V input synchronous buck converter LMR38010 (U7) is used, and configured to run at 1MHz which is set by using R47 = 25.5kΩ.

The buck converter (U7) can provide a maximum output current of 1A. To make sure the system consumption is below this 1A power budget, a calculation is made for the loads.

Table 2-2. Current Budget of the Buck Converter at 12V

PART NUMBER	VOLTAGE RAIL	CURRENT CONSUMPTION BY DATA SHEET	WATT	CURRENT ON 12V WITH 80% EFFICIENCY
DRV8162L (Need 3 ×)	12V	18mA (V_{GVDD})	0.648W	67.5mA
F280039C	3.3V	108mA	0.356W	37mA
Total				**104.5mA**

This indicates that there is still an output current capacity of 895.5mA in the 12V rail left for additional circuitry to use.

2.2.1.7.2 3.3V Rail

In this design, the 3.3V rail needs to supply a load current of around 0.5A maximum for both the C2000 host control LaunchPad™ development kit and the onboard components of system control circuits, including the sensing, diagnostic, and the shutdown control sections.

As for the input voltage range of the 3.3V rail supply circuit, since the GVDD of the DRV8162L is supplied with the 12V rail, select a scheme that has enough margin, so that the 3.3V rail supply circuit can directly use the V_{GVDD} as the input.

This design uses a simple, easy-to-use, high-efficiency, high-power density, synchronous buck module, TPSM861253, to supply the 3.3V rail. This device has a 3V to 17V input range, a 3.3V, 1A maximum output and is in a QFN package.

2.2.2 Software Design

The software used to test this reference design is modified from the *servo_drive_with_can* example project in the C2000Ware_MotorControl_SDK. The example project is tuned to work with the hardware following the instructions in the related documentation found in the installation folder.

If not previously installed, download and install *C2000WARE-MOTORCONTROL-SDK* using the default settings. Locate the *servo_drive_with_can* example code at this path:

```
c:\ti\c2000\C2000Ware_MotorControl_SDK_x_xx_xx_xx\solutions\servo_drive_with_can
```

There are multiple subfolders for different MCUs in this path, and the documentation is also available in the *doc* subfolder in this path.

The tuning work is done in the *Code Composer Studio™ integrated development environment (IDE)*. If not previously installed, download and install *Code Composer Studio* using the default settings. For more instructions on *Code Composer Studio*, see also the resources on the installation path.

To tune the example project for this reference design and run a three-phase motor, import the project in the *f28003x* subfolder to Code Composer Studio and then make these changes:

First, modify the analog and digital I/O port settings. Make sure the PWM signals from the C2000™ MCU are configured correctly for the high-side and low-side FETs. Make sure the control outputs, the fault feedback inputs, and the ADC channels are all configured correctly for the LaunchPad development kit I/O ports used.

Second, tune the related parameters and codes for the reference design hardware and system control. The reference design is tested using build level 2, which means the system is run in an open loop configuration.

For questions on the software, C2000Ware_MotorControl_SDK, or Code Composer Studio, see also the C2000 microcontrollers forum E2E design support forum.

2.3 Highlighted Products

2.3.1 DRV8162L

The DRV816x devices are integrated half-bridge gate drivers capable of driving high-side and low-side N-channel power FETs. The device generates the gate drive voltages from the GVDD supply pin and uses a bootstrap circuit to drive the high-side FET. A trickle charge pump supports 100% duty cycle operation. The gate drive architecture supports peak gate drive currents up to 1A source and 2A sink. These devices can be used to drive various types of loads including brushless or brushed DC motors, Permanent Magnet Synchronous Motors (PMSM), stepper motors, switched reluctance motors (SRM), and solenoids.

The 1-pin PWM, 2-pin PWM, and independent FET PWM modes allow for simple interfacing to controller circuits and flexible FET power stage configurations. The hardware pins help configure device settings including current sense amplifier gain, gate drive current, and VDS overcurrent protection. The DRV8161 device integrates a low-side current sense amplifier to provide current measurement information back to the controller. The DRV8162L variant offers separate GVDD and GVDD_LS pins to help system design of safe torque off (STO) function.

Internal protection functions are provided for under-voltage lockout, FET over-current, and over-temperature. The nFAULT pin indicates fault events detected by the protection features.

2.3.2 INA241A

The INA241x is an ultra-precise, bidirectional current sense amplifier that can measure voltage drops on shunt resistors over a wide common-mode voltage range from –5V to 110V, independent of the supply voltage. High-precision current measurement is achieved through a combination of low offset voltage (±10µV, maximum), small gain error (±0.01%, maximum) and high DC CMRR (typical 166dB). The INA241x is designed for high-voltage, bidirectional measurements in switching systems that see large common-mode voltage transients at the device inputs. The enhanced PWM rejection circuitry inside the INA241x maintains minimal signal disturbance at the output despite the common-mode voltage transitions at the input.

The INA241x operates from a single 2.7V to 20V supply, drawing 2.5mA of supply current. The INA241x is available in five gain options of 10V/V, 20V/V, 50V/V, 100V/V, and 200V/V. Multiple gain options allow for optimization between available shunt resistor values and wide output dynamic range requirements.

The INA241x is specified over an operating temperature range of −40°C to +125°C.

2.3.3 AMC0106M05

The AMC0106Mxx devices are precision, functionally isolated, second-order delta-sigma modulators for shunt-based high accuracy, isolated current sensing. The AMC0106M05 supports a linear input range of ±50mV and the AMC0106M25 supports ±250mV.

The isolation barrier separates the two parts of the device that operate on different common-mode voltage levels, and supports a working voltage up to 200V$_{RMS}$ / 280V$_{DC}$ and transient overvoltages up to 570V$_{RMS}$ / 800V$_{DC}$. The galvanic isolation barrier supports high common-mode transients and allows for isolating sensitive control circuitry from the switching noise of the power stage.

The AMC0106Mxx devices are in a small, 2.7mm × 3.5mm leadless package with 1mm creepage and clearance. This small package size enables small PCB layouts that are essential for small form-factor motor-drive applications.

To reduce the power dissipation on the current sense shunt, a 300µΩ, 8W shunt resistor is selected to work with an AMC0106M05 in phase C current sense in this design. This leads to a linear full sense range of ±167A.

The output bitstream of the AMC0106M05 is synchronized to an external clock. Combined with a sinc3, OSR 256 filter, the device can achieve 16-bit resolution with 82.5dB dynamic range and 78kSPS data rate.

2.3.4 TPSM861253

The TPSM861253 is a simple, easy-to-use, high-efficiency, high-power density, synchronous buck module with input voltage ranging from 3V to 17V and supports up to 1A continuous current. The device has a fixed 3.3V output voltage and supports FCCM mode. The device also integrates the divider resistors and a feedforward capacitor inside the module. Complete protections including OVP, OCP, UVLO, OTP, and UVP with hiccup are also integrated.

2.3.5 LMR38010

The LMR38010 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. The LMR38010 operates during input voltage dips as low as 4.2V, at nearly 100% duty cycle if needed, making the device an excellent choice for wide input industrial applications and MHEV or EV systems.

The LMR38010 uses precision enable to provide flexibility by enabling a direct connection to the wide input voltage or precise control over device start-up and shutdown. The power-good flag, with built-in filtering and delay, offers a true indication of system status, eliminating the need for an external supervisor. The device incorporates pseudo random spread spectrum for minimal EMI and switching frequency and can be configured between 200kHz and 2.2MHz to avoid noise sensitive frequency bands. In addition, the frequency can be selected for improved efficiency at low operating frequency or smaller design size at high operating frequency.

The device has built-in protection features such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The LMR38010 is available in an 8-pin HSOIC PowerPAD integrated circuit package.

2.3.6 TMP6131

The TMP61 linear thermistor offers linearity and consistent sensitivity across temperature to enable simple and accurate methods for temperature conversion. The low power consumption and a small thermal mass of the device minimize self-heating.

With built-in fail-safe behaviors at high temperatures and powerful immunity to environmental variation, these devices are designed for a long lifetime of high performance. The small size of the TMP6 series also allows for close placement to heat sources and quick response times.

Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory.

The TMP61 is currently available in a 0402 X1SON package, a 0603 SOT-5X3 package, and a 2-pin through-hole TO-92S package.

2.3.7 ISOM8710

The ISOM871x family of devices are opto-emulators that provide isolation for digital signals of data rates up to 25Mbps and are single-channel, pin-compatible, drop-in replacements for optocouplers. While standard optocouplers use an LED as the input stage, ISOM871x uses an emulated diode as the input stage. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO2) isolation barrier, which not only provides robust isolation, but also offers best-in-class common mode transient immunity. Ordering options include CMOS output and open collector output options.

ISOM871x devices isolate high-speed digital signals and offer performance, reliability, and flexibility advantages not available with traditional optocouplers. The devices are based on CMOS isolation technology for low-power and high-speed operation, therefore the devices are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age.

3 Hardware, Software Test Requirements and Test Results

3.1 Hardware Requirements

3.1.1 PCB Overview

Figure 3-1 shows a photo of the top side of the TIDA-010956 PCB with the LAUNCHXL-F280039C.
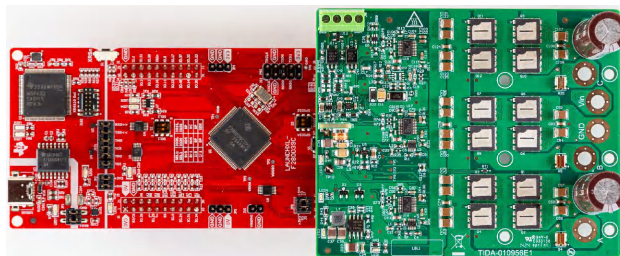

Figure 3-1. Board Picture (Top View)

3.1.2 Hardware Configuration

3.1.2.1 Prerequisites

The following hardware equipment and software are required for the evaluation tests of the TIDA-010956 design guide.

Table 3-1. Prerequisites

EQUIPMENT	COMMENT
TIDA-010956	Available from the *Design Folder*
TMS320F280039C LaunchPad™ development kit for C2000™ real-time MCU	Available from *LAUNCHXL-F280039C*
Code Composer Studio™ integrated development environment (IDE) version 12	Download from *CCSTUDIO*
C2000Ware_MotorControl_SDK	Download from *C2000WARE-MOTORCONTROL-SDK*.
Motor	Needs to support voltage and current level of the design
Power supply	Needs to support voltage and current level of the design

3.1.2.2 Default Resistor and Jumper Configuration

Prior to working with the TIDA-010956 board, make sure that the correct resistor settings are applied. Table 3-2 shows the default resistor settings. As for the jumpers on the LAUNCHXL-F280039C, remove the JP1 to disconnect the 5V power supply from the PC USB port; since this reference has supplied the MCU controller board with a 3.3V power rail directly by the default setting of R29..

Table 3-2. Default Resistor and Jumper Settings

HEADER and RESISTOR	JUMPER SETTING
R51 and R58	Resistor to disable the isolator for the external shutdown input signal
R54 and R56	Resistor defining which shutdown path drives the load switch for PWM disable function
R61 and R63	Resistor defining which shutdown path can drive the load switch for high-side gate driver disable function
R67 and R69	Resistor defining which shutdown path can drive the load switch for low-side gate driver disable function
R29	0Ω resistor to supply the LAUNCHXL-F280039C with the 3.3V onboard. Remove JP1 on the LaunchPad before use.
R83, R86; R98, R101; R111, R114	Resistors to configure the gate drive current of the DRV8162L in the three phases. *The default setting is LEVEL0 for both IDRIVE1 and IDRIVE2.*
R84, R99, R112	Resistors to configure the V_{DS} monitor threshold level of DRV8162L. *The default setting is LEVEL1.*
R85, R100, R113	Resistor outside the DT/MODE pin to set the dead time. *The default setting is LEVEL3.*

3.1.2.3 Connector

3.1.2.3.1 Host Processor Interface

Table 3-3 shows the signals that the TIDA-010956 reference design uses to communicate with a C2000 LaunchPad of LAUNCHXL-F280039C.

Table 3-3. Pinout of J1 and J2 Host Processor Interface

LAUNCHXL-F280039C				TIDA-010956			
J5	**J7**	**J8**	**J6**	**J1**		**J2**	
3.3V	5V[2]	PWM7A	GND	3.3V	NC[2]	PWM_CH	GND
ADCINC1[2]	GND	PWM7B	GPIO27[2]	NC[2]	GND	PWM_CL	NC[2]
GPIO15	ADCINB11	PWM4A	GPIO47	LED4	*Vbus* [1]	PWM_BH	FAULT
GPIO56[2]	ADCINA10, ADCINB1, ADCINC10	PWM4B	GPIO57[2]	NC[2]	*V_C* [1]	PWM_BL	NC[2]
GPIO56[2]	ADCINA5	PWM5A	XRSn[2]	NC[2]	*V_B* [1]	PWM_AH	NC[2]
ADCINA9[2]	ADCINA4, ADCINB8	PWM5B	SD2_D3	NC[2]	*V_A* [1]	PWM_AL	*DAT_PhC*
GPIO58[2]	ADCINB4, ADCINC8[2]	GPIO21[2]	SD2_C3	NC[2]	NC[2]	NC[2]	*SD_CLK*
GPIO4	ADCINB5	EPWM1B	GPIO20	VDSLVLCC	*I_B* [1]	*SD_CLK* [1]	EN_DRV
GPIO18	ADCINA12, ADCINC5	EPWM2A	GPIO26	VDSLVLCB	*I_A* [1]	*CLK_PhC* [1]	PWM_EN
GPIO19	ADCINA0, ADCINB15, ADCINC15	GPIO40[2]	GPIO25[2]	VDSLVLCA	*Temperature* [1]	NC[2]	NC[2]

(1) The signals shown in italic font are not tested in this design yet.
(2) The gray color code shows the pins which are *Not Connected* or reserved in the TIDA-010956 design.

Connections to the J5, J7 and J6, J8 are tested using a LAUNCHXL-F280039C as shown in Table 3-3. The TIDA-010956 can also be able to work with the J1, J3 and J2, J4 connectors of a LAUNCHXL-F280039C, or a LAUNCHXL-F28P65X LaunchPad.

3.2 Test Setup

The equipment listed in Table 3-4 is used for the TIDA-010956 testing session.

Table 3-4. DRV8162L Settings

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix DPO3054
Probes	Tektronix TPP0200
Current probe	CYBERTEK CP8500A
PMSM Motor	GLOBE6440
Power supply	Agilent 6030A, ITECH IT6724H

For the different tests some of the equipment is used as described in Table 3-4. Figure 3-2 shows a test setup used for the system.
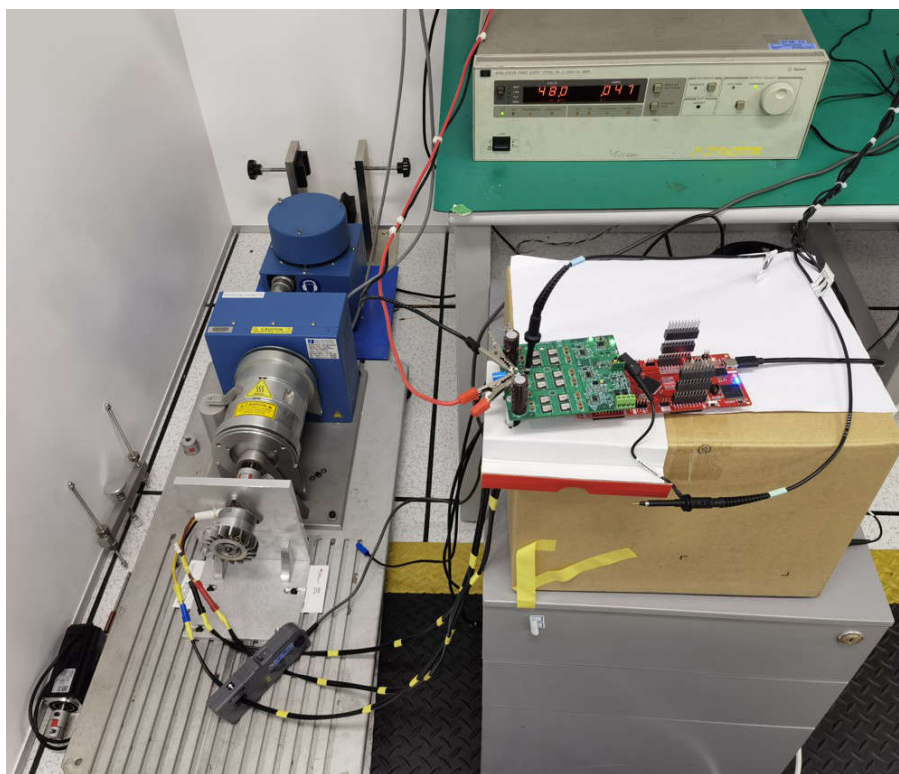
Figure 3-2. TIDA-010956 System Test Setup

The DRV8162L chips are setup in a way shown in Table 3-5 during the tests, if not otherwise specified.

Table 3-5. DRV8162L Settings

IDRIVEP	1024mA	IDRIVE1 = LEVEL0 ($V_{IDRIVE1}$ = 0kΩ) and
IDRIVEN	2048mA	IDRIVE2 = LEVEL0 ($V_{IDRIVE2}$ = 0kΩ)
VDSLVL	LEVEL1-0: 0.15V or LEVEL1-1: 0.2V	LEVEL1 (R_{VDSLVL} = 2kΩ)
DEAD_TIME	370ns dead time	LEVEL3 (R_{DT} = 3.3kΩ)

In the tests, a C2000™ LaunchPad of LAUNCHXL-F280039C is used to control the system. The related MCU software settings are shown in Table 3-6.

Table 3-6. C2000 MCU Settings

PWM	16kHz	Dead time	200ns

Different setups are used in the tests and are described in the related test section.

3.3 Test Results

Tests are done to characterize each individual functional block, as well as the entire board. In particular, the following tests are conducted:

- Power management
- Three-phase power stage tests
- Voltage and Current Sensing Tests
- System thermal performance

Tests are done at room temperature around 28 degrees Celsius.

3.3.1 Power Management

This section shows the power up and power down sequence of the TIDA-010956. The measurements are done in the process shown in Figure 3-3.
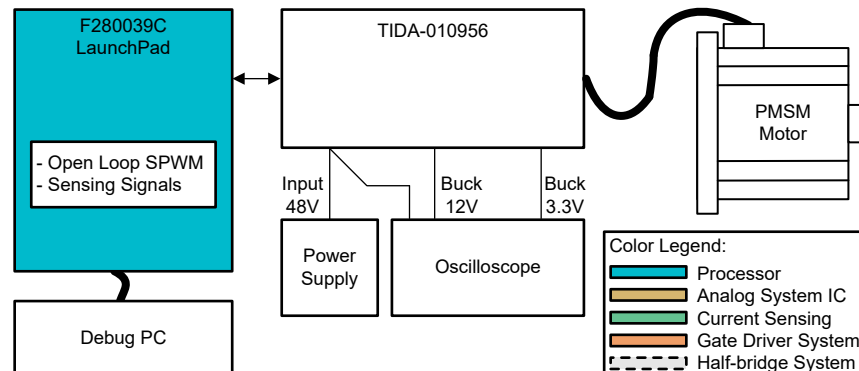
Figure 3-3. TIDA-010956 Diagram of Test Setup for the Voltage Rails

3.3.1.1 Power Up

Figure 3-4 illustrates the TIDA-010956 power-up sequence.
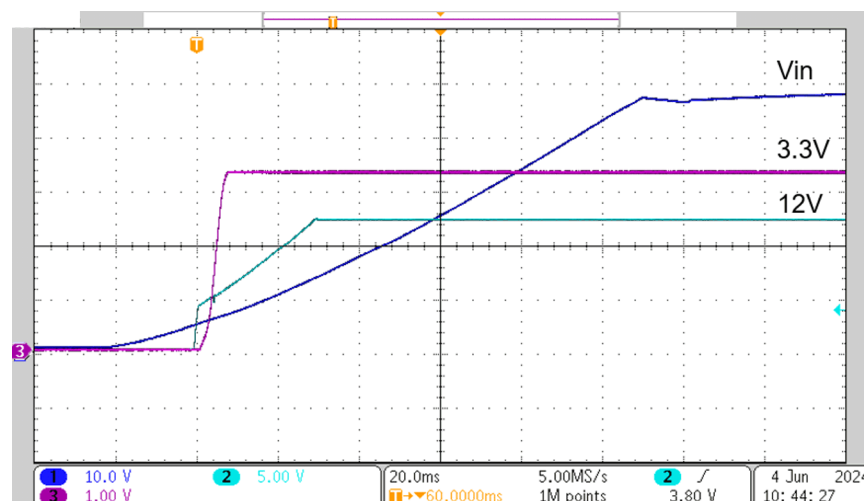
Figure 3-4. TIDA-010956 Power-Up Sequence

The power up sequence of the system is as follows: 48V V_{IN} (CH1 in dark blue) goes above approximately 5V first, then LMR38010FDDAR starts providing the 12V rail (CH2 in light blue). When this 12V rail is approximately 5V, the 3.3V rail (CH3 in purple) is enabled.

The V_{IN} has a slow ramp up while charging the VDC bus capacitors which are mainly of 330µF × 2 + 2.2µF × 20 and sum up to over 700µF. Another 180µF × 20 = 3.6mF needs to be added if a capacitor board is adopted.

3.3.1.2 Power Down

During the power-down process, the V_{IN} ramp down is also slow because the V_{IN} has to discharge the > 700μF capacitance (see Figure 3-5).

As the V_{IN} drops to approximately 7V, the 12V rail starts to power down. When this 12V rail gets to approximately 4V, the V_{IN} shuts down the 3.3V rail. Then the remaining charge of the capacitors dissipates slowly.
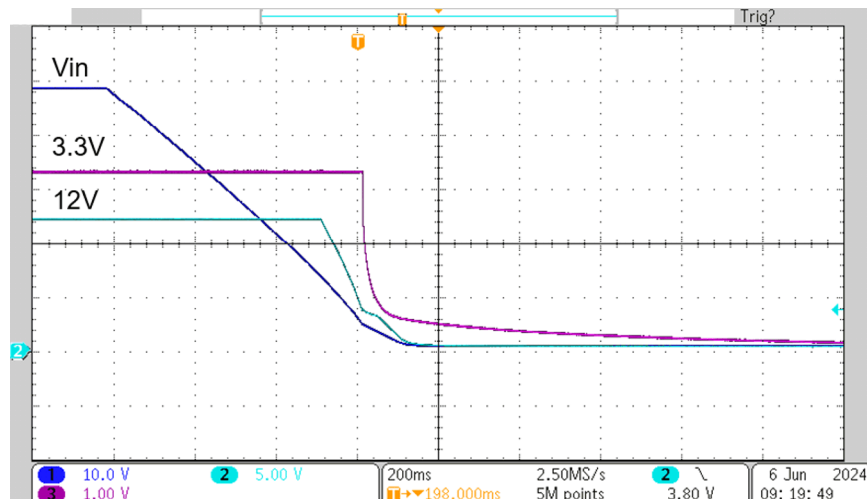
Figure 3-5. TIDA-010956 Power-Down Sequence

Table 3-7 shows the system status when the current is a 12V rail.

Table 3-7. 12V Rail Current in Various System Status

MEASUREMENT	SYSTEM STATUS	12V RAIL CURRENT
Current (mA)	Idle (Gate driver disabled)	73.5
Current (mA)	16kHz PWM	125.4

Note

By default, in this design the C2000 LaunchPad is supposed to be powered up by the TIDA-010956 with the 3.3V supply through a 0Ω resistor (R29). Remove the JP1 (5V power supply from the PC USB) on the LAUNCHXL-F280039C before applying V_{IN}.

3.3.2 Gate Voltage and Phase Voltage

To measure the gate voltage and the phase voltage on the switch node, the following measurements are performed. Figure 3-6 shows the test setup.
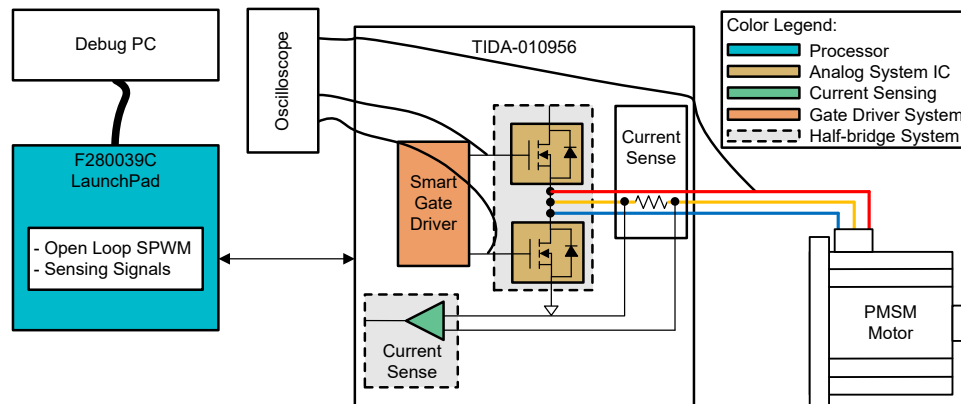
Figure 3-6. Test Setup for the Gate Voltage and Switch Node Voltage Measurements

In these tests the VDC applied is 48V and the motor is set to a fixed angle with open loop vector control. The signals are measured in phase B, including the gate voltage (CH1, in dark blue) of the low-side MOSFET, the switch node voltage (CH2, in light blue) of the phase, and the output current (CH4, in green). Both voltages are referenced to GND and the positive direction of the phase current is from the drive to the motor.

The measurements in Section 3.3.2.1, Section 3.3.2.2, and Section 3.3.2.3 show the shifts of the phase in the conditions when the current is set to both positive and negative values. All four configurations of soft switching and hard switching of the low-side MOSFET are measured.

3.3.2.1 20 VDC
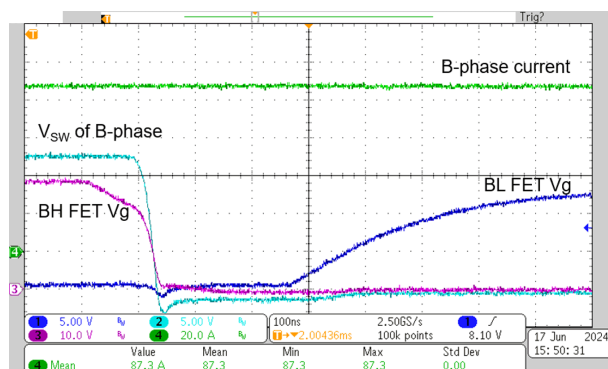
Figure 3-7. Hard Switching, Phase Current at 20V, 87.3A
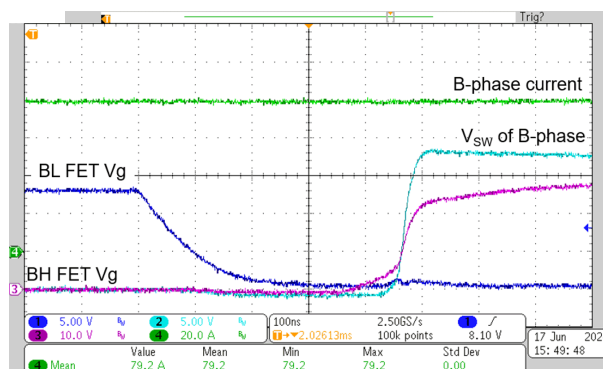
Figure 3-8. Soft Switching, Phase Current at 20V, 79.2A
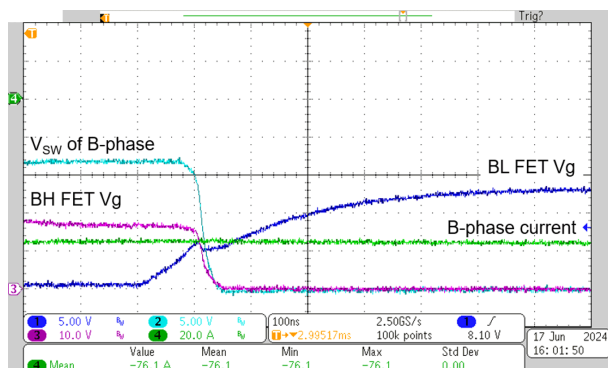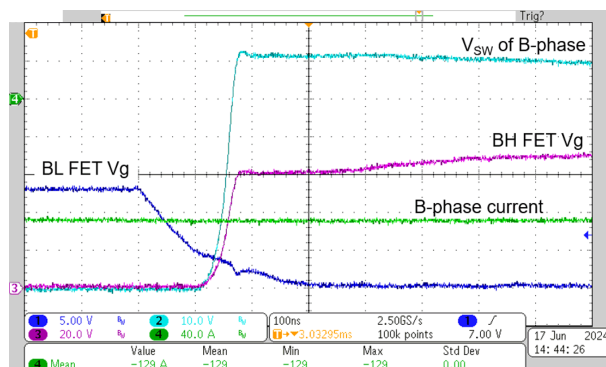
Figure 3-9. Soft Switching, Phase Current at 20V, −76.1A
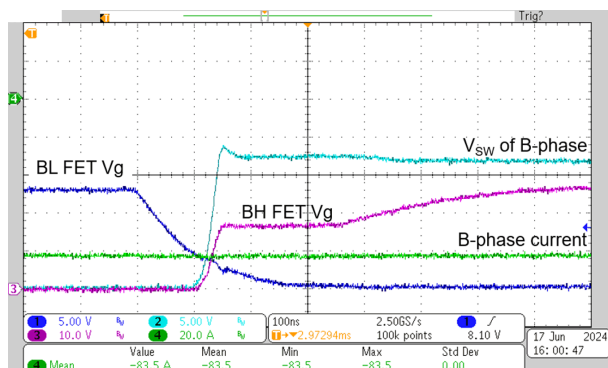
Figure 3-10. Hard Switching, Phase Current at 48V, −83.5A

3.3.2.2 48 VDC
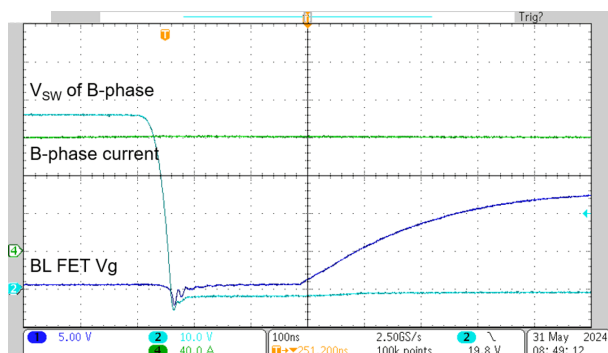
Figure 3-11. Hard Switching, Phase Current at 48V, 120A
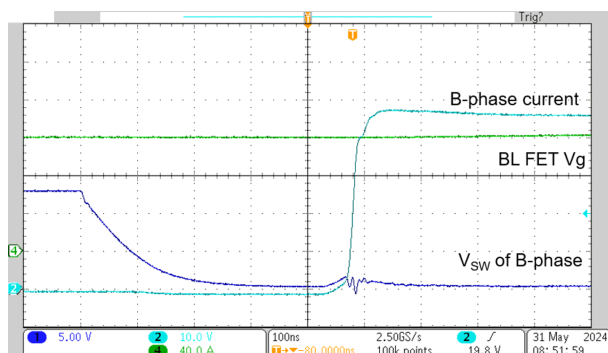
Figure 3-12. Soft Switching, Phase Current at 48V, 120A
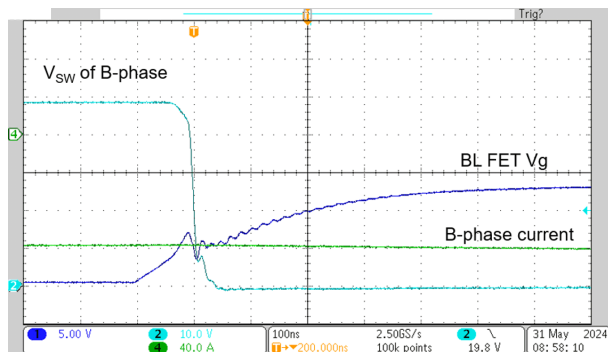
Figure 3-13. Soft Switching, Phase Current at 48V, −120A
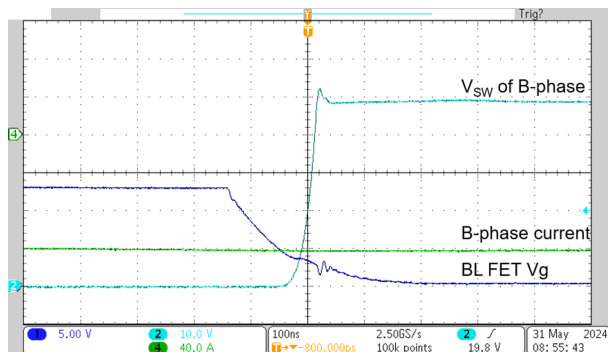
Figure 3-14. Hard Switching, Phase Current at 48V, −120A

3.3.2.3 60 VDC
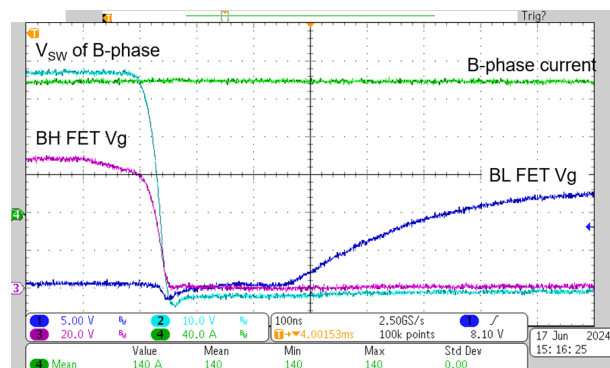
Figure 3-15. Hard Switching, Phase Current at 60V, 140A
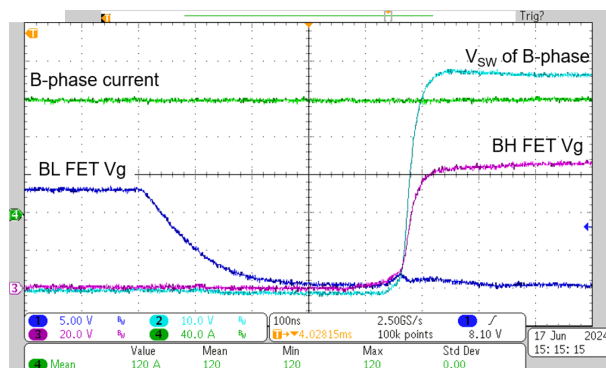
Figure 3-16. Soft Switching, Phase Current at 60V, 120A
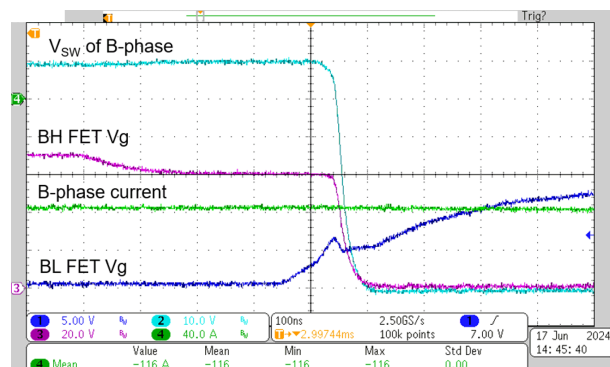
Figure 3-17. Soft Switching, Phase Current at 60V, –116A

Figure 3-18. Hard Switching, Phase Current at 60V, –129A

3.3.3 Digital PWM and Gate Voltage

In these tests, the propagation delay between the PWM signal and the MOSFET gate voltage is measured in a low-side channel first; and then the dead time between the high-side and low-side digital PWMs as well as the gate voltages of the MOSFETs are measured. Figure 3-19 shows the test setup.
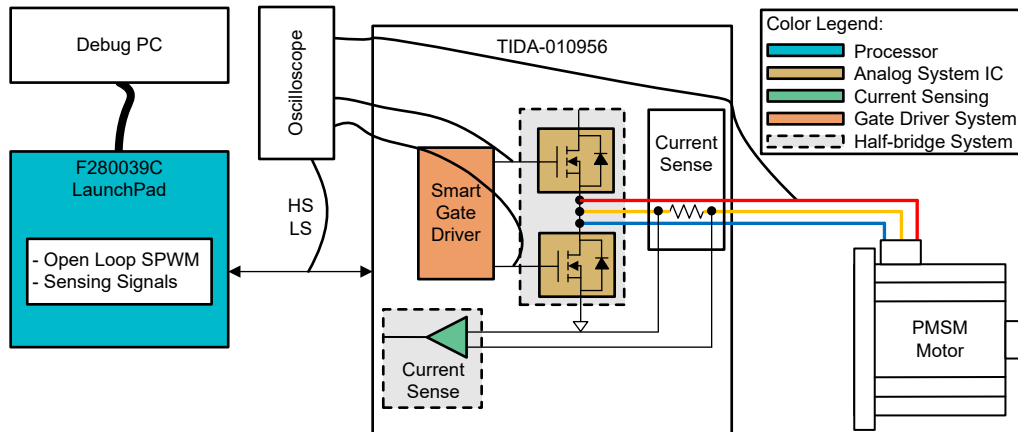
Figure 3-19. Test Setup for the Digital PWM and Gate Voltage Measurements

The system uses a 48V V_{IN} in these tests and the motor is set to a fixed angle with open loop control. The signals are measured in Phase C and all signals are referenced to GND.

The propagation delay in turn-on and turn-off appear in Figure 3-20 and Figure 3-21.
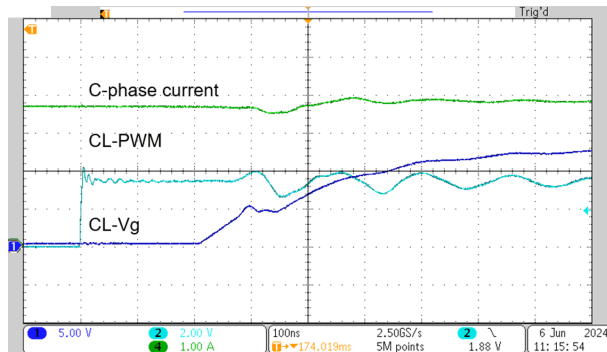
Figure 3-20. Propagation Delay in Turn-On
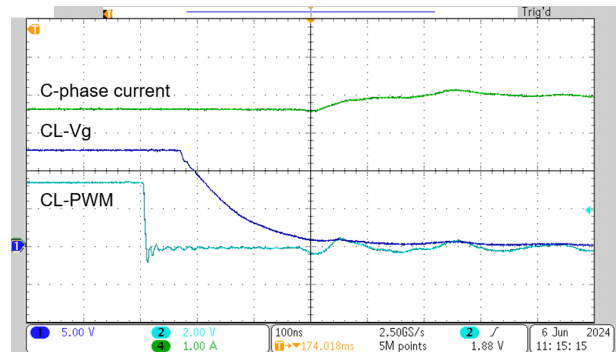
Figure 3-21. Propagation Delay in Turn-off

The turn-on delay is measured at about 200ns and the turn-off delay is measured at about 70ns. The turn-on is postponed by about 130ns due to an extra dead time that is introduced with the DRV8162L, following the DT pin setting of a 3.3kΩ R_{DT} connecting to GND.

Figure 3-22 and Figure 3-23 show the 200ns dead time of the PWM signals and the corresponding gate voltages when the half bridge is switching from low to high (CH2 for CL and CH3 for CH).
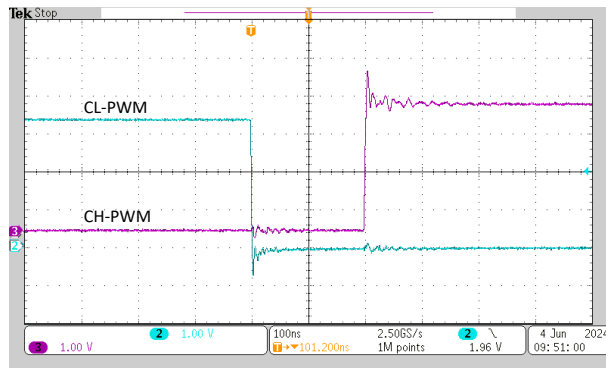
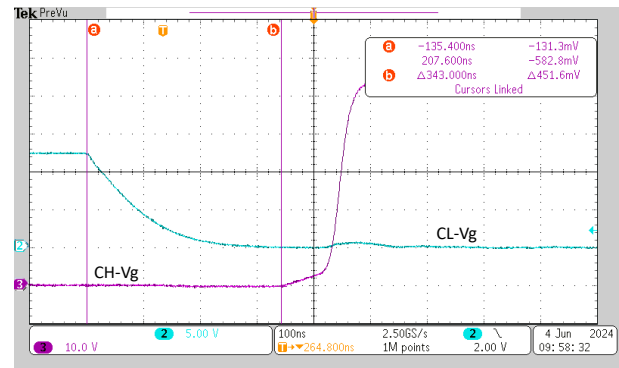**Figure 3-22. PWM Inputs in Positive Shift, DT = 200ns**

Figure 3-23. Gate Voltages in Positive Shift, DT = 343ns

The dead time between the high-side and the low-side gate voltages is expanded to about 340ns with the DRV8162L.

Figure 3-24 and Figure 3-25 show the half bridge is switching from high to low. The dead time is also expanded to about 340ns with the R_{DT} setting.
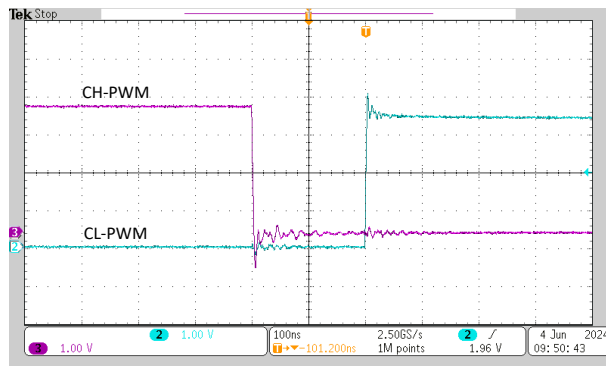
Figure 3-24. PWM Inputs in Negative Shift, DT = 200ns
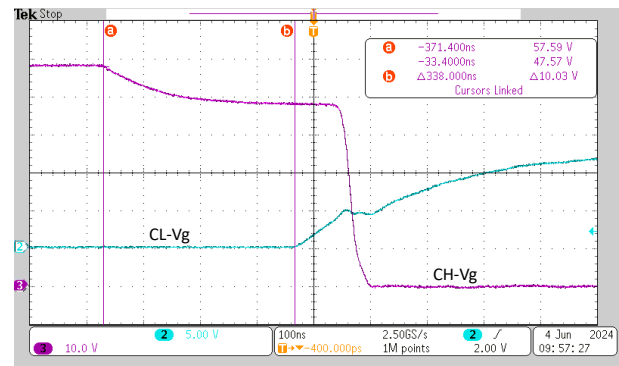
Figure 3-25. Gate Voltages in Negative Shift, DT = 338ns

This DRV8162L automatically inserts dead time and can vary between 20ns to 370ns, depending on the R_{DT} value. See the data sheet for the details.

3.3.4 Phase-Current Measurements

This section shows the phase-current measurement performance generating an open loop rotating field for the motor control.
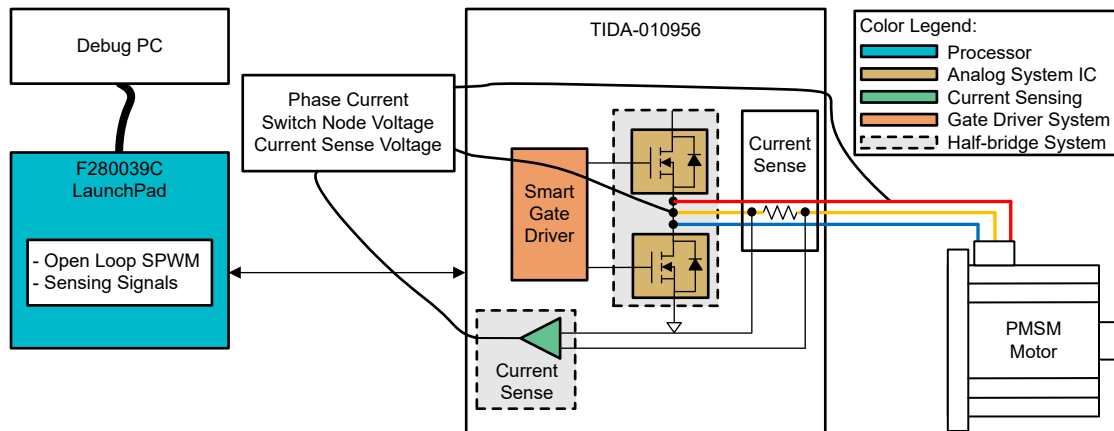

Figure 3-26. TIDA-010956 Diagram of the Test Setup for the Current Measurements

Figure 3-27 shows the motor current (CH4 in green) and the current-sense amplifier output voltage (CH1 in deep blue) of the INA241 measurements in B-phase. The switching node voltage is also shown (CH2 in light blue).

Figure 3-28 shows the sinusoidal-like waveform output of the INA241. Obvious distortions of the sine wave are displayed as the system is running in open loop. Figure 3-28 shows the common-mode performance of the INA241.
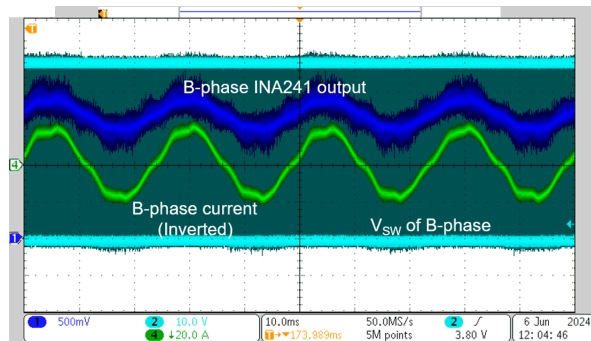
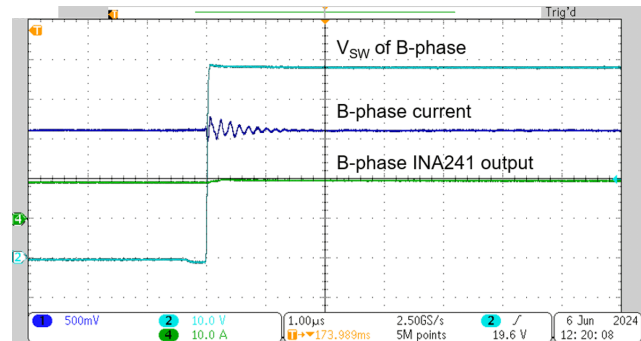**Figure 3-27. Rotating Current Measured on the INA241 Output**

Figure 3-28. INA241 Output Measured During Switch Point

This measurement captures the worst-case scenario of the settling time of the amplifier. Observe that a maximum settling time of around 1.0µs can be expected.

3.3.5 System Test Results

3.3.5.1 Thermal Analysis

Thermal analysis of the design is performed at a 28°C lab temperature with a 48V V_{IN} and 16kHz PWM. A low-voltage PMSM is driven with sinusoidal phase currents at a load current of 26.2A_{RMS}, (37.0A peak). This test did not use a heat sink or fan. Figure 3-29 shows the thermal picture of the board.
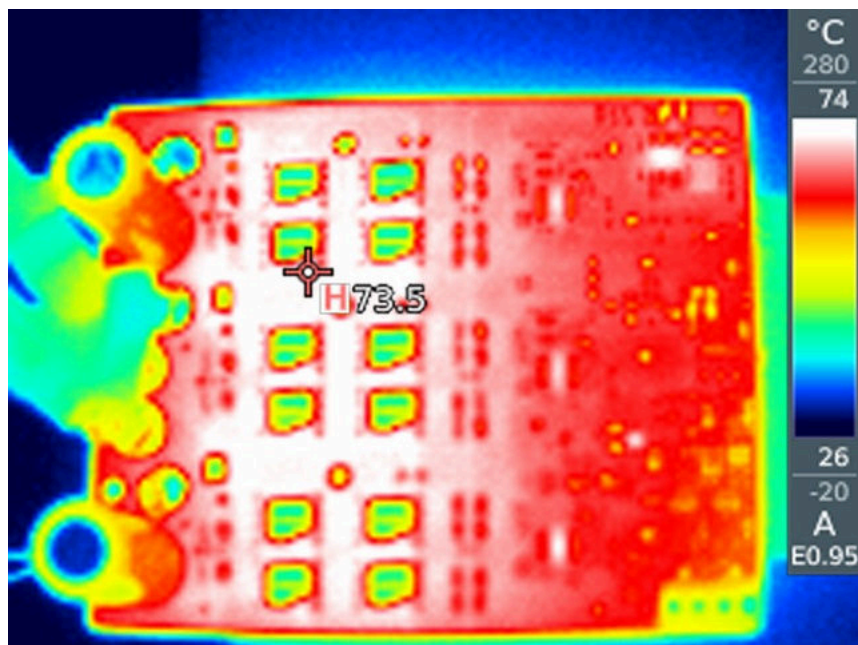

Figure 3-29. TIDA-010956 Thermal Picture at 26.2A_{RMS} Output

This measurement shows that at 26.2A_{RMS}, the MOSFETs have a temperature rise of 45.5°C. Consider keeping the junction temperature of the MOSFET at less than 125°C, the current design can work up to 79.5°C ambient at 26.2A_{RMS} without a heat sink. It is possible that a heat sink and cooling fan are needed for higher current or higher ambient temperature conditions.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010956.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010956.

4.2 Tools and Software

Tools

LAUNCHXL-F280039C   C2000™ real-time MCU F280039C LaunchPad™ development kit

Software

C2000WARE-MOTORCONTROL-SDK   MotorControl software development kit (SDK) for C2000™ MCUs

4.3 Documentation Support

1. Texas Instruments, *DRV816x 100V Half-Bridge Smart Gate Driver with Integrated Protection and Current Sense Amplifier Data Sheet*
2. Texas Instruments, *INA241x–5V to 110V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection Data Sheet*
3. Texas Instruments, *AMC0106M05 Precision, ±50mV Input, Functionally Isolated, Delta-Sigma Modulator With External Clock Data Sheet*
4. Texas Instruments, *TMP61 ±1%, 10kΩ Linear Thermistor With 0402 and 0603 Package Options Data Sheet*
5. Texas Instruments, *LMR38010 4.2V to 80V, 1A, Synchronous SIMPLE SWITCHER Power Converter With 40µA I_Q Data Sheet*
6. Texas Instruments, *TPSM86125x 3V to 17V Input, 1A, Synchronous Buck Module in QFN Package Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.5 Trademarks

C2000™, E2E™, InstaSPIN-FOC™, BoosterPack™, LaunchPad™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

5 About the Authors

KRISTEN MOGENSEN is a system engineer in the Industrial Systems-Robotics team at Texas Instruments responsible for developing technical collateral for robotics systems with a main focus on functional safety, communication, and motor drives.

JEROME SHAN is a system engineer in the Industrial Systems-Motor Drive team at Texas Instruments responsible for developing technical collateral for industrial motor drives.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.