Design Guide: TIDA-050077

4kW, 12V Input Power Path Protection Reference Design Using Stackable eFuse

Description

This reference design illustrates a 12V, 4kW input power path protection system for data center servers, utilizing six TPS25985 eFuse devices in parallel. The TPS25985x is a compact, package-integrated, parallelizable, high-current circuit protection and power management device. The primary goal of this reference design is to demonstrate the thermal performance of the TPS25985 eFuse when two devices are positioned in the same area: one at the top and another at the bottom of the PCB. In this configuration, four devices are located on the top layer, while the other two are placed on the bottom layer, directly aligning with the second and third devices on the top layer.

Resources

TIDA-050077	Design Folder
TPS25985, LM94022	Product Folder
SN74LVC1G123, INA241A	Product Folder
UCC27511, TLV760	Product Folder
CSD18510Q5B	Product Folder

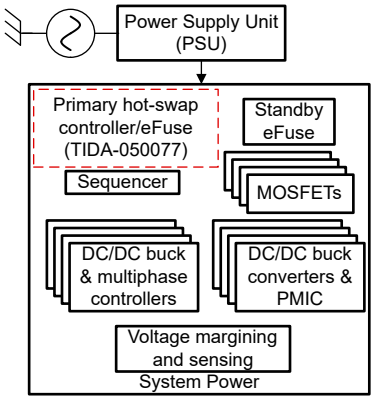
Ask our TI E2E™ support experts

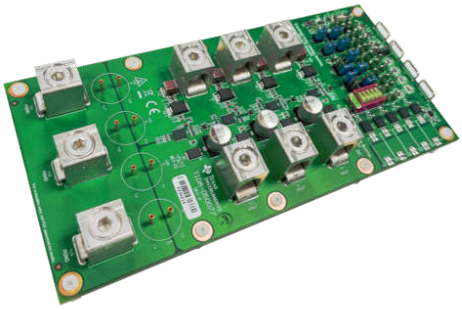
Features

- Capable of carrying $350A_{RMS}$ current at an elevated ambient temperature of 55°C without any external airflow
- 220A and 330A programmable circuit breaker threshold using onboard jumpers
- LED status for power good and fault indications
- Options to engage the enable power cycle and the quick output discharge (QOD)
- Option to apply custom load transients using onboard metal-oxide semiconductor field-effect transistors (MOSFET), gate-drive circuits, and load resistors
- Option to perform output hot-short using onboard MOSFETs, gate-drive circuits, and five 1mΩ resistors in parallel
- Monitoring PCB temperature at different locations using onboard analog temperature sensors

Applications

- Rack server motherboard
- High performance computing
- Network interface card (NIC)
- Hardware accelerator and GPU card or module
- Fixed data center switch
- Edge router





1 System Description

Figure 1-1 depicts a typical power distribution architecture in a 12V enterprise server motherboard. The image also indicates the location in the power tree at which the TIDA-050077 reference design can be used in a server motherboard.

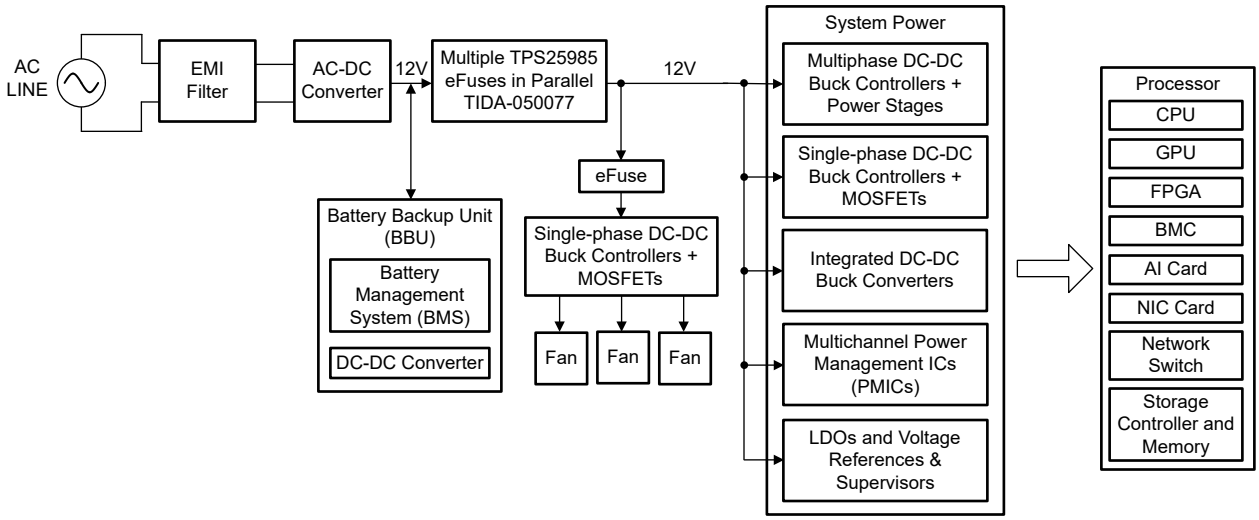


Figure 1-1. System Block Diagram

1.1 Key System Specifications

Table 1-1 shows the design parameters for this reference design.

Table 1-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	10
Maximum DC load current ($I_{OUT(max)}$)	300A
Peak current	500A
Maximum output capacitance (C_{LOAD})	95mF
Are all the loads off until the PG is asserted?	No
Load at start-up ($R_{LOAD(Start-up)}$)	0.15Ω (equivalent to approximately 12% of the maximum steady-state load)
Maximum ambient temperature	55°C
Transient overload blanking timer	15ms
Output voltage slew rate	1.2V/ms
Need to survive a hot-short on output condition?	Yes
Need to survive a power-up into short condition?	Yes
Can a board be hot-plugged in or power-cycled?	Yes
Load current monitoring needed?	Yes
Fault response	Latch-off

2 System Overview

The TIDA-050077 reference design showcases a 12V, 4kW input power path protection system in data center servers, utilizing six TPS25985 eFuse devices arranged in parallel. The TPS25985x is a compact, package-integrated, parallelizable design for high-current circuit protection and power management. This device offers multiple protection modes with minimal external components, providing robust defense against overloads, short circuits, and excessive inrush current. The main purpose of this reference design is to demonstrate the thermal performance of the TPS25985 eFuse when two devices are positioned in the same location—one at the top and the other at the bottom of the PCB. In this configuration, four devices are placed on the top layer, while the other two are located on the bottom layer, precisely corresponding to the second and third devices on the top layer.

This reference design incorporates additional circuitry to safely perform output hot-short experiments using the SN74LVC1G123 monostable multivibrator and a low-side MOSFET gate driver, UCC27511. The design also includes an ultra-precise current sense amplifier, INA241A, to monitor the short-circuit current. Four analog temperature sensors, LM94022, are utilized to monitor the PCB temperature at various locations.

2.1 System Block Diagram

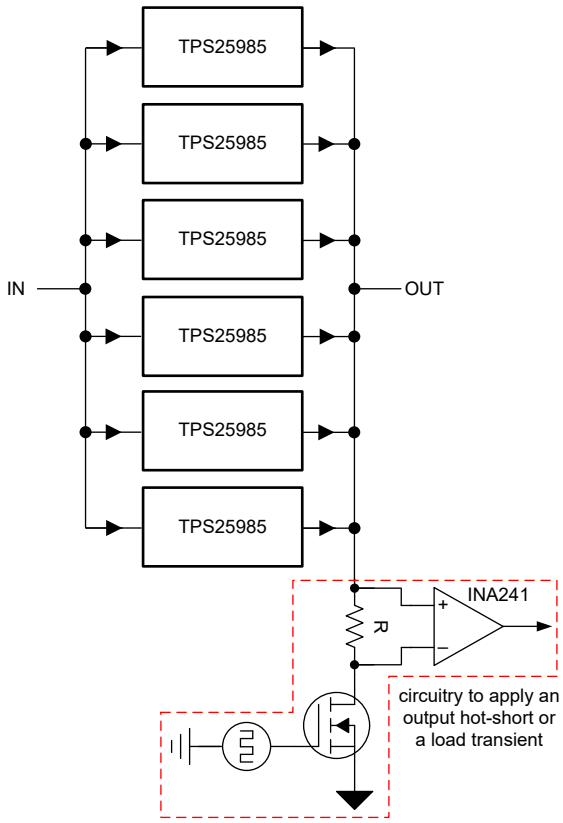


Figure 2-1. TIDA-050077 Block Diagram

2.2 Design Considerations

2.2.1 Determining the Number of eFuse Devices to use in Parallel

By factoring in a small variation in the junction-to-ambient thermal resistance ($R_{\theta JA}$), a single TPS25985x eFuse is rated at a maximum steady state DC current of 60A with a maximum junction temperature of less than 125°C. Considering further degradation of $R_{\theta JA}$ of each eFuse due to the placement of multiple devices connected in parallel, each device is assumed to be rated for a thermal design current (TDC) of 50A at an elevated ambient temperature of 70°C.

Therefore, Equation 1 can be used to calculate the number of parallel devices (N) to support the maximum steady-state DC load current ($I_{LOAD(max)}$), for which to model the design.

$$N \geq \frac{I_{OUT(max)}\,(A)}{50A} \tag{1}$$

According to Table 1-1, $I_{OUT(max)}$ is 300A. Therefore, six (6) TPS25985 eFuses are connected in parallel in the TIDA-050077.

2.2.2 Setting up the Primary and Secondary Devices in a Parallel Configuration

The MODE pin is used to configure one TPS25985x eFuse as the primary device in a parallel chain along with the other TPS25985x eFuses as the secondary devices. As a result, some of the TPS25985 pin functionalities can be changed to facilitate primary and secondary configuration as described in the *multiple devices, parallel connection* of the *TPS25985x 4.5V–16V, 0.59mΩ, 80A Stackable eFuse With Accurate and Fast Current Monitor* data sheet.

Leaving the pin open configures the corresponding device as the primary one. For the secondary devices, this pin must be connected to GND.

2.2.3 Selecting the C_{DVDT} Capacitor to Control the Output Slew Rate and Start-Up Time

For a robust design, the junction temperature of the device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Typically, dynamic power stresses are orders of magnitude greater than static stresses. Therefore, establishing the right start-up time and inrush current limit for the capacitance in the system and the associated loads to avoid thermal shutdown during start-up is crucial.

Table 2-1 summarizes the formulas for calculating the average inrush power loss on the eFuses in the presence of different loads during start-up if the power-good (PG) signal is not used to turn on all the downstream loads.

Table 2-1. Calculation of Average Power Loss During Inrush

Type of Loads During Start-Up	Expressions to Calculate the Average Inrush Power Loss
Only output capacitor of C_{LOAD} (µF)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}}$ (2)
Output capacitor of C_{LOAD} (µF) and constant resistance of $R_{LOAD(Startup)}$ (Ω) with turn-on threshold of V_{RTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + \frac{V_{IN}^2}{R_{LOAD(Startup)}}\left[\frac{1}{6} - \left\{\frac{1}{2}\left(\frac{V_{RTH}}{V_{IN}}\right)^2\right\} + \left\{\frac{1}{3}\left(\frac{V_{RTH}}{V_{IN}}\right)^3\right\}\right]$ (3)
Output capacitor of C_{LOAD} (µF) and constant current of $I_{LOAD(Startup)}$ (A) with turn-on threshold of V_{CTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + V_{IN} I_{LOAD(Startup)}\left[\frac{1}{2} - \left(\frac{V_{CTH}}{V_{IN}}\right) + \left\{\frac{1}{2}\left(\frac{V_{CTH}}{V_{IN}}\right)^2\right\}\right]$ (4)
Output capacitor of C_{LOAD} (µF) and constant power of $P_{LOAD(Startup)}$ (W) with turn-ON threshold of V_{PTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + P_{LOAD(Startup)}\left[\ln\left(\frac{V_{PTH}}{V_{IN}}\right) + \left(\frac{V_{PTH}}{V_{IN}}\right) - 1\right]$ (5)

where

- V_{IN} is the input voltage
- T_{ss} is the start-up time

With the different combinations of loads during start-up, the total average inrush power loss (P_{INRUSH}) can be calculated using the formulas described in Table 2-1. For a successful start-up, the system must satisfy the condition stated in Equation 6.

$$P_{INRUSH}(W)\sqrt{T_{ss}(s)} < 12 \times N \quad (6)$$

where

- N denotes the number of eFuses in parallel
- 12 W$\sqrt{s}$ is the SOA limit of a single TPS25985x eFuse

Use Equation 7 to obtain the maximum allowed T_{ss}.

Note

TI recommends using a T_{ss} in the range of 5ms to 120ms to prevent start-up issues.

A capacitor (C_{DVDT}) must be added at the DVDT pin to GND to set the required value of T_{ss} as previously calculated. Equation 7 is used to compute the value of C_{DVDT}. The DVDT pins of all the eFuses in a parallel chain must be connected together.

$$C_{DVDT}(pF) = \frac{42000}{V_{IN}(V)/T_{ss}(ms)} \quad (7)$$

Using V_{IN} = 12V, T_{ss} = 10ms, and Equation 7, the required C_{DVDT} value can be calculated to be 35nF. The closest standard value of C_{DVDT} is 33nF with 10% tolerance and a DC voltage rating of 25V.

Note

In some systems, there can be active load circuits (for example, DC-DC converters) with low turn-on threshold voltages which can start drawing power before the eFuse has completed the inrush sequence. This action can cause additional power dissipation inside the eFuse during start-up and can lead to thermal shutdown. TI recommends using the Power Good (PG) pin of the eFuse to enable and disable the load circuit. This action makes sure that the load is turned on only when the eFuse has completed start-up and is ready to deliver full power without the risk of hitting thermal shutdown.

2.2.4 Selecting the R_{IREF} Resistor to set the Reference Voltage for Overcurrent Protection and Active Current Sharing

In this parallel configuration, the IREF internal current source (I_{IREF}) of the primary eFuse interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage (V_{IREF}) for the overcurrent protection and active current sharing blocks. When the voltage at the IMON pin (V_{IMON}) is used as an input to an ADC to monitor the system current or to implement the Platform Power Control (Intel® PSYS) functionality inside the VR controller, V_{IREF} must be set to half of the maximum voltage range of the ISYS_IN input of the controller. This action provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the fast-trip threshold (2 × I_{OCP}). Equation 8 is used to calculate the value of R_{IREF}.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (8)$$

In the TIDA-050077, V_{IREF} is set at 1V. With I_{IREF} = 25µA (typical), the target R_{IREF} is calculated to be 40kΩ. The closest standard value of R_{IREF} is 40.2kΩ with 0.1% tolerance and a power rating of 100mW. For improved noise immunity, place a 1nF ceramic capacitor from the IREF pin to GND.

Note

Maintain V_{IREF} within the recommended voltage to provide proper operation of the overcurrent detection circuit.

2.2.5 Selecting the R_{IMON} Resistor to set the Overcurrent (Circuit Breaker) and Fast-Trip Thresholds During Steady-State

TPS25985x eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a user-adjustable transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{IMON}) on the IMON pin. This generates a voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) in response to the load current, which is defined as Equation 9.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (9)$$

G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 18.18µA/A. The overcurrent condition is detected by comparing the V_{IMON} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using Equation 10.

$$I_{OCP(TOTAL)} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (10)$$

In the TIDA-050077, $I_{OCP(TOTAL)}$ is considered to be 1.1 times $I_{OUT(max)}$. Hence, $I_{OCP(TOTAL)}$ is set at 330A, and R_{IMON} can be calculated to be 166.67Ω with G_{IMON} as 18.18µA/A and V_{IREF} as 1V. The nearest value of R_{IMON} is 167Ω with 0.1% tolerance and a power rating of 100mW. For noise reduction, place a 22pF ceramic capacitor across the IMON pin and GND.

Note

A system output current (I_{OUT}) must be considered when selecting R_{IMON}, not the current carried by each device.

2.2.6 Selecting the R_{ILIM} Resistor to set the Current Limit and Fast-Trip Thresholds During Start-Up and the Active Sharing Threshold During Steady-State

R_{ILIM} is used in setting up the active current sharing threshold during steady-state and the overcurrent limit during start-up among the devices in a parallel chain. Each device continuously monitors the current flowing through (I_{DEVICE}) and outputs a proportional analog output current on the ILIM pin. This, in turn, produces a proportional voltage (V_{ILIM}) across the respective ILIM pin resistor (R_{ILIM}), which is expressed as Equation 11.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (11)$$

G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE}), with a typical value of 18.18µA/A.

- *Active current sharing during steady-state*: This mechanism operates only after the device reaches steady-state and acts independently by comparing the load current information (V_{ILIM}) with the Active Current Sharing reference ($CLREF_{LIN}$) threshold, defined as Equation 12.

$$CLREF_{LIN} = \frac{1.1 \times V_{IREF}}{3} \quad (12)$$

  Therefore, R_{ILIM} must be calculated using Equation 13 to define the active current sharing threshold as $I_{OCP(TOTAL)}$ / N, where N is the number of devices in parallel. Using N = 6, R_{IMON} = 167Ω, and Equation 13, R_{ILIM} can be calculated to be 367.4Ω. The closest standard value of 365Ω with 0.1% tolerance and power rating of 100mW resistances are selected as R_{ILIM} for each device.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (13)$$

Note

To determine the value of R_{ILIM}, Equation 14 must be used if a different threshold for active current sharing ($I_{LIM(ACS)}$) than I_{OCP} / N is desired.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (14)$$

When computing the current limit threshold during start-up in the next subsection, be sure to use this R_{ILIM} value.

- *overcurrent limit during start-up*: During inrush, the overcurrent condition for each device is detected by comparing the load current information (V_{ILIM}) with a scaled reference voltage as depicted in Equation 15.

$$CLREF_{SAT} = \frac{0.7 \times V_{IREF}}{3} \quad (15)$$

The current limit threshold during start-up can be calculated using Equation 16.

$$I_{ILIM(Startup)} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \quad (16)$$

By using a R_{ILIM} value of 365Ω for each device, the start-up current is limited to about 35A for each device and the $I_{LIM(ACS)}$ is set at about 55A.

Note

The active current limit block employs a fold-back mechanism during start-up based on V_{OUT}. When V_{OUT} is below the fold-back threshold (V_{FB}) of 1.99V, the current limit threshold is further lowered.

2.2.7 Selecting the C_{ITIMER} Capacitor to Set the Overcurrent Blanking Timer

An appropriate capacitor must be connected at the ITIMER pin to ground of the primary or standalone device to adjust the duration for which the load transients above the circuit-breaker threshold are allowed. The transient overcurrent blanking interval can be calculated using Equation 17.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (17)$$

where

- t_{ITIMER} = the transient overcurrent blanking timer
- C_{ITIMER} is the capacitor connected between the ITIMER pin of the primary device and GND
- I_{ITIMER} = 2.07µA (typical)
- ΔV_{ITIMER} = 1.5V (typical)

A 22nF capacitor with 10% tolerance and DC voltage rating of 25V is used as the C_{ITIMER} for the primary device in this design, which results in 16.5ms of t_{ITIMER}. Leave the ITIMER pin for all the secondary devices open.

2.2.8 Selecting the Resistors to set the Under-voltage Lockout Threshold

The under-voltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R_1 and R_2 connected between IN, EN/UVLO, and GND pins of the device as described in the *under-voltage protection* section of the *TPS25985x* data sheet. The resistor values required for setting up the UVLO threshold are calculated using Equation 18.

$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \quad (18)$$

To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_1 and R_2. The current drawn by R_1 and R_2 from the power supply is $I_{R12} = V_{IN} / (R_1 + R_2)$. However, the leakage currents due to external active components connected to the resistor string can add errors to these calculations. So, the resistor string current, I_{R12} must be 20 times greater than the leakage current at the

EN/UVLO pin (I_{ENLKG}). From the device electrical specifications, I_{ENLKG} is 0.1µA (maximum) and UVLO rising threshold $V_{UVLO(R)}$ = 1.2V. From the design requirements, V_{INUVLO} = 10.8V. First choose the value of R_1 = 1MΩ and use Equation 18 to calculate R_2 = 125kΩ. Use the closest standard 1% resistor values: R_1 = 1MΩ and R_2 = 124kΩ. For noise reduction, place a 1nF ceramic capacitor across the EN/UVLO pin and GND.

2.2.9 Selecting the R-C Filter Between V_{IN} and V_{DD}

The VDD pin is intended to power the internal control circuitry of the eFuse with a filtered and stable supply, not affected by system transients. Therefore, use an R (10Ω) – C (2.2µF) filter from the input supply (IN pin) to the VDD pin. This helps to filter out the supply noises and to hold up the controller supply during severe faults such as short circuit at the output. In a parallel chain, this R-C filter must be employed for each device.

2.2.10 Selecting the Pullup Resistors and Power Supplies for SWEN, PG, $\overline{FLT}$, and CMPOUT Pins

$\overline{FLT}$, PG, and CMPOUT are the open drain outputs. If these logic signals are used, the corresponding pins must be pulled up to an appropriate supply rail voltage through 10kΩ pull-up resistances.

Note

The SWEN pin must be pulled up to a voltage in the range of 2.5V to 5V through a 100kΩ resistance. This pull-up power supply must be generated from the input (V_{IN}) to the eFuse and available before the eFuse is enabled, without which the eFuse cannot start up.

2.2.11 TVS Diode Selection at Input and Schottky Diode Selection at Output

When the device interrupts a large amount of current instantaneously causing a short circuit and overload current limit, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical over-stress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

1. Minimize lead length and inductance into and out of the device.
2. Use a large PCB GND plane.
3. Add TVS diodes to clamp the positive transient spike at the input.
4. Use Schottky diodes across the output to absorb negative spikes.

See also *TVS Clamping in Hot-Swap Circuits* and *Selecting TVS Diodes in Hot-Swap and ORing Applications* for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (20V). These TVS diodes also help to limit the transient voltage at the IN pin during the Hot Plug event. Five (5) 5.0SMDJ12A are used in parallel in the TIDA-050077.

Note

Maximum Clamping Voltage (V_C) specification of the selected TVS diode at I_{pp} (10/1000µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

Select Schottky diodes based on the following criteria:

- The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. Equation 19 calculates the number of Schottky diodes ($N_{Schottky}$) that must be in parallel.

$$N_{Schottky} > \frac{2 \times I_{OCP(TOTAL)}}{I_{FSM}} \quad (19)$$

- Forward Voltage Drop (V_F) at or near to I_{FSM} must be as small as possible. For the best outcome, clamp the negative transient voltage at the OUT pin within the absolute maximum rating of the OUT pin (–1V).
- DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
- Leakage current (I_R) must be as small as possible.

Five (5) PMEG045V100EPE-QZ devices are used in parallel in the TIDA-050077.

2.2.12 Selecting C_{IN} and C_{OUT}

TI recommends adding ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.1µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 2.2µF can be used at the OUT pin of each device.

2.3 Highlighted Products

2.3.1 TPS25985

The TPS25985x is an integrated, high-current circuit protection and power management design in a small package. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short-circuits, and excessive inrush current.

Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Output current limit levels can be set by the user as per system needs. A user-adjustable overcurrent blanking timer allows systems to support transient peaks in the load current without tripping the eFuse.

2.3.2 LM94022 and LM94022-Q1

The LM94022 and LM94022-Q1 (LM94022x) devices are precision analog output CMOS integrated-circuit temperature sensors with selectable linear negative temperature coefficient (NTC). A class-AB output structure gives the LM94022x strong output source and sink current capability for driving heavy transient loads such as that presented by the input of a sample-and-hold analog-to-digital converter (ADC). The low 5.4µA supply current and 1.5V operating voltage of the LM94022x make the device an excellent choice for battery-powered systems as well as general temperature-sensing applications.

2.3.3 INA241x

The INA241x is an ultra-precise, bidirectional current-sense amplifier than can measure voltage drops across shunt resistors over a wide common-mode range from –5V to 110V, independent of the supply voltage. The high-precision current measurement is achieved through a combination of low offset voltage (±10µV, maximum), small gain error (±0.01%, maximum) and a high DC CMRR (typical 166dB). The INA241x is designed for high-voltage, bidirectional measurements in switching systems that encounter large common-mode voltage transients at the inputs of the device. The enhanced PWM rejection circuitry inside the INA241x makes sure minimal signal disturbance at the output due to the common-mode voltage transitions at the input.

2.3.4 TLV760

The TLV760 is an integrated linear-voltage regulator featuring operation from an input as high as 30V. The TLV760 has a maximum dropout of 1.2V at the full 100mA load across operating temperature. Standard packaging for the TLV760 is the 3-pin SOT-23 package.

The TLV760 is available in 3.3V, 5V, 12V, and 15V. The SOT-23 packaging of the TLV760 series allows the device to be used in space-constrained applications. The TLV760 is a small size alternative to LM78Lxx series and similar devices.

2.3.5 SN74LVC1G123

The SN74LVC1G123 device is a single retriggerable monostable multivibrator designed for 1.65V to 5.5V, VCC operation.

This monostable multivibrator features output pulse-duration control using three methods. In the first method, the A input is low, and the B input goes high. In the second method, the B input is high, and the A input goes low. In the third method, the A input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

2.3.6 UCC27511A

The UCC27511A device is a compact gate driver that offers best-in-class replacement of NPN and PNP discrete driver (buffer circuit) designs. The UCC27511A device is a single-channel, low-side, high-speed gate driver rated for MOSFETs, IGBTs, and emerging wide-band-gap power devices such as GaN. The device features fast rise times, fall times, and propagation delays, making the UCC27511A device an excellent choice for high-speed applications. The asymmetrical 4A peak source and 8A peak sink currents of this device boost immunity against the parasitic Miller turn-on effect. The split output configuration enables easy and independent adjustment of rise and fall times using only two resistors and eliminating the need for an external diode. Features including wide input hysteresis and negative input voltage handling enhance transient immunity.

2.3.7 CSD18510Q5B

This 40V, 0.79mΩ, SON 5mm × 6mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

- TIDA-050077 reference design board
- DC power supply: N8951A, auto-ranging system DC power-supply, 80V, 510A, 15kW
- DC electronic load: 63210A-150-1000, high-power DC electronic load, 150V, 1000A, 10kW
- Digital multimeters
- Fluke® Ti480 PRO infrared camera
- MDO4000C mixed domain oscilloscope

Figure 3-1 through Figure 3-4 show the reference design schematics.

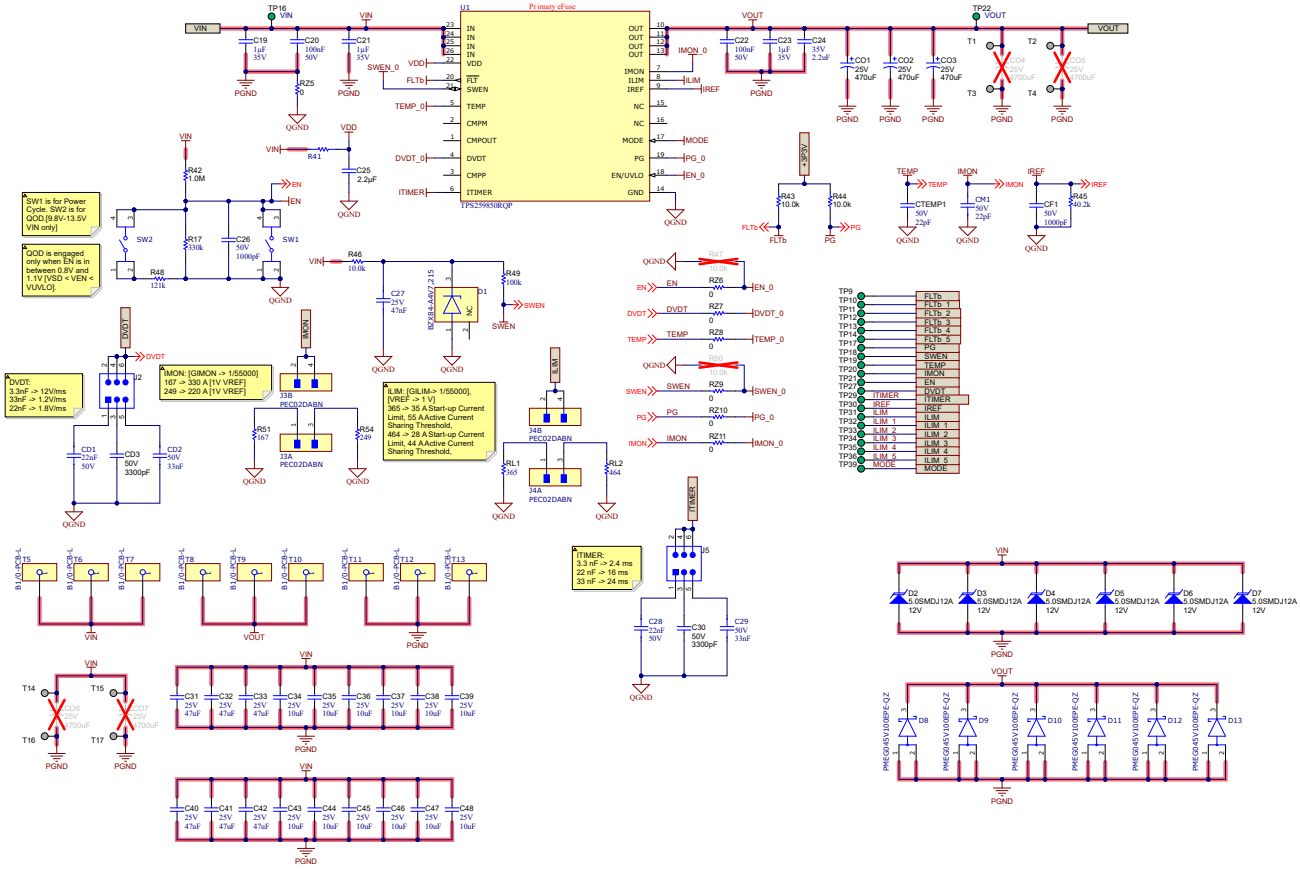


Figure 3-1. TIDA-050077 Reference Design (Schematic Image 1)

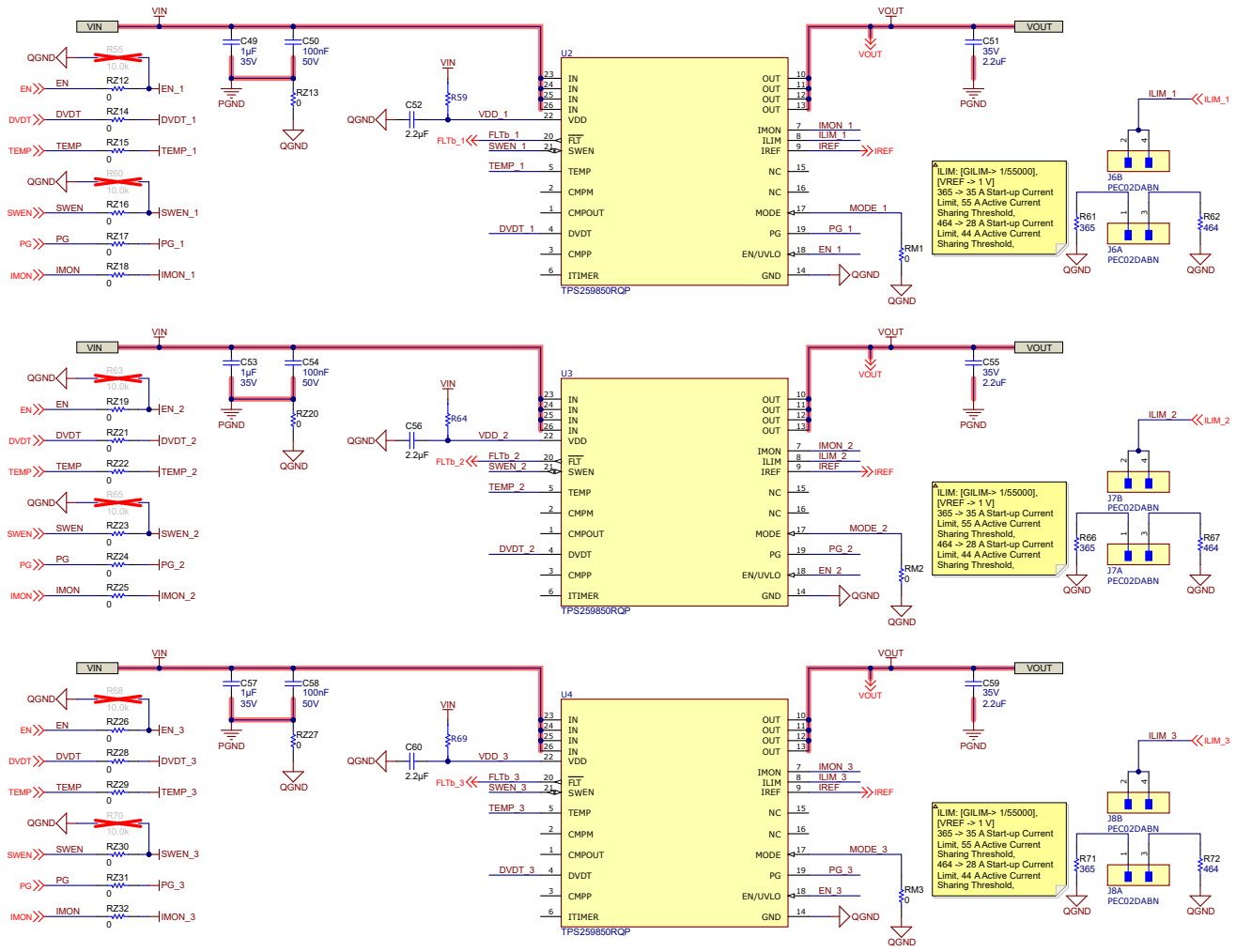


Figure 3-2. TIDA-050077 Reference Design (Schematic Image 2)

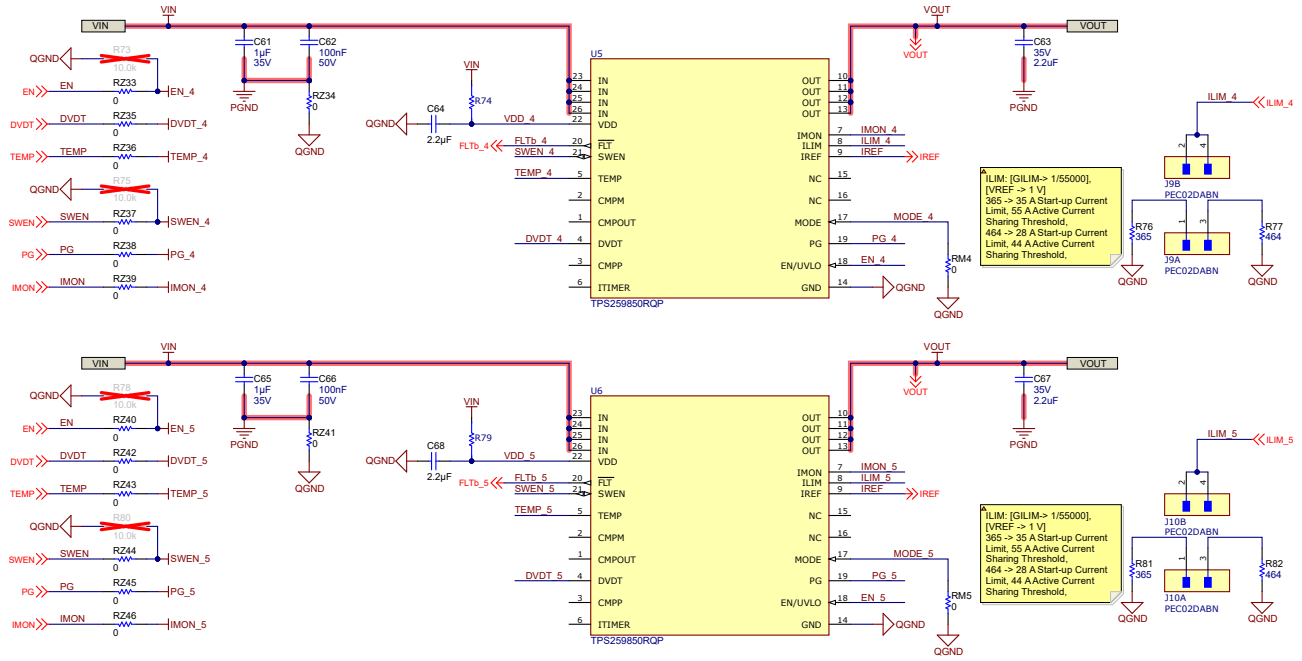


Figure 3-3. TIDA-050077 Reference Design (Schematic Image 3)

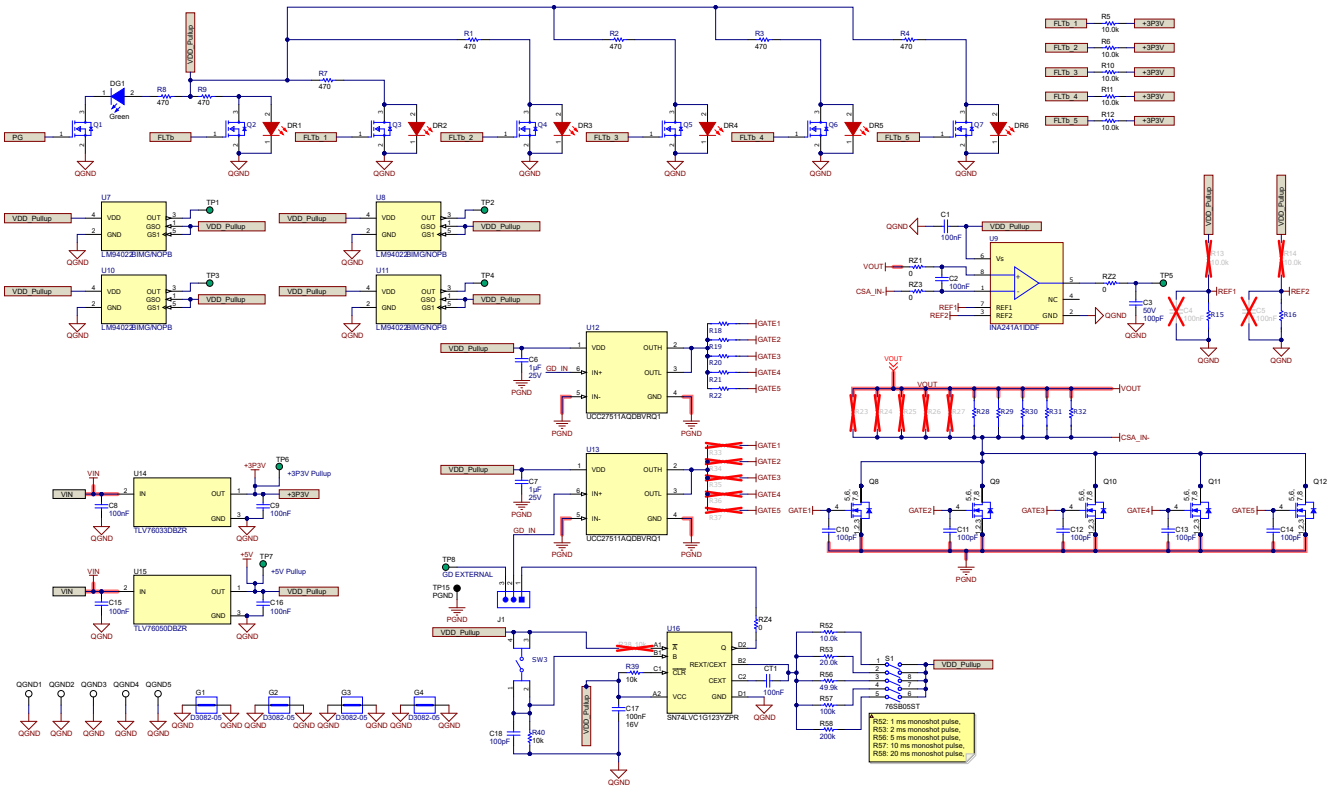


Figure 3-4. TIDA-050077 Reference Design (Schematic Image 4)

Figure 3-5 through Figure 3-7 show the reference design board images.

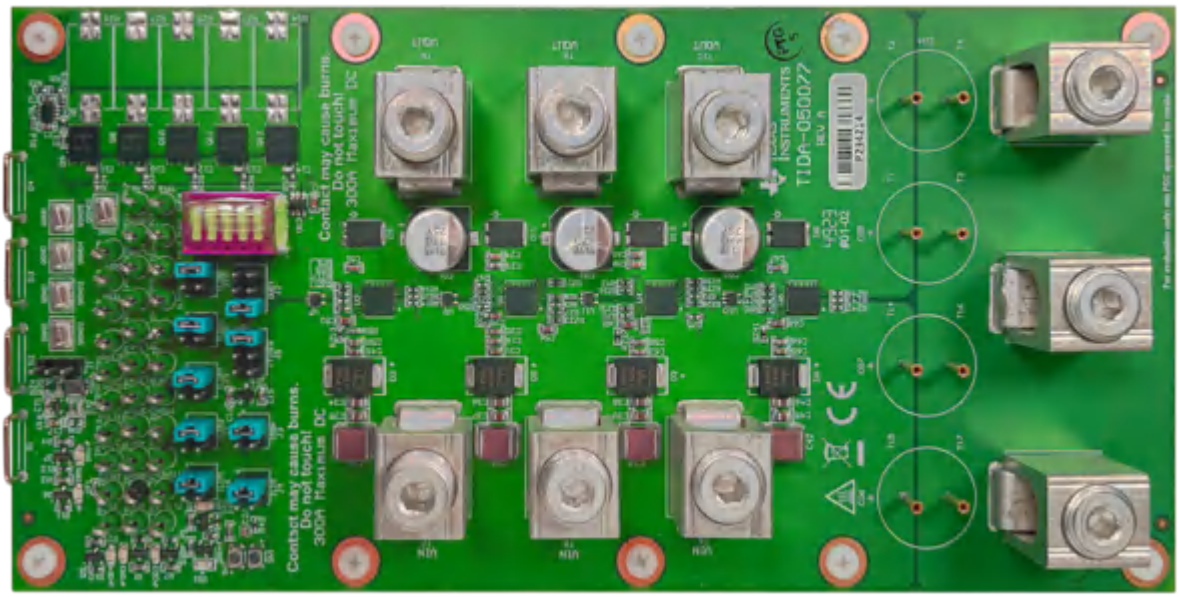


Figure 3-5. TIDA-050077 Reference Design: Top View

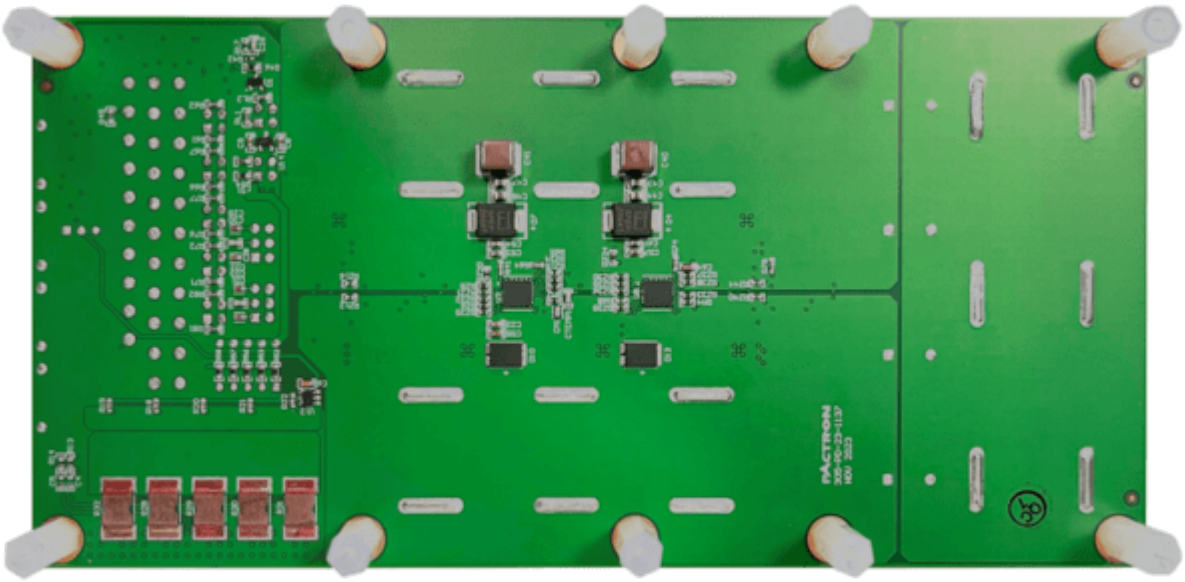


Figure 3-6. TIDA-050077 Reference Design: Bottom View

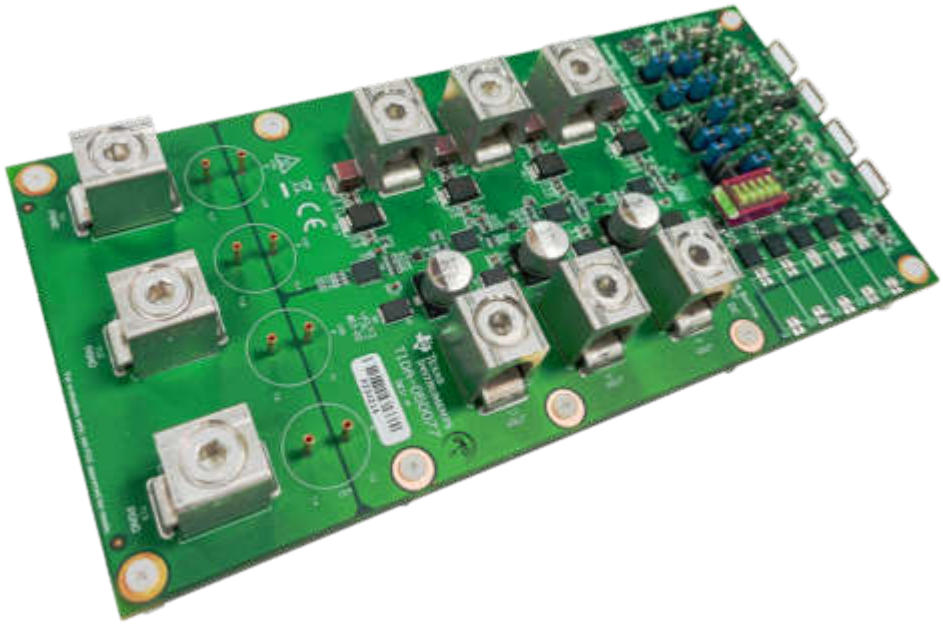


Figure 3-7. TIDA-050077 Reference Design: Angle View

3.2 Test Setup

Figure 3-8 shows a block diagram of the test setup.

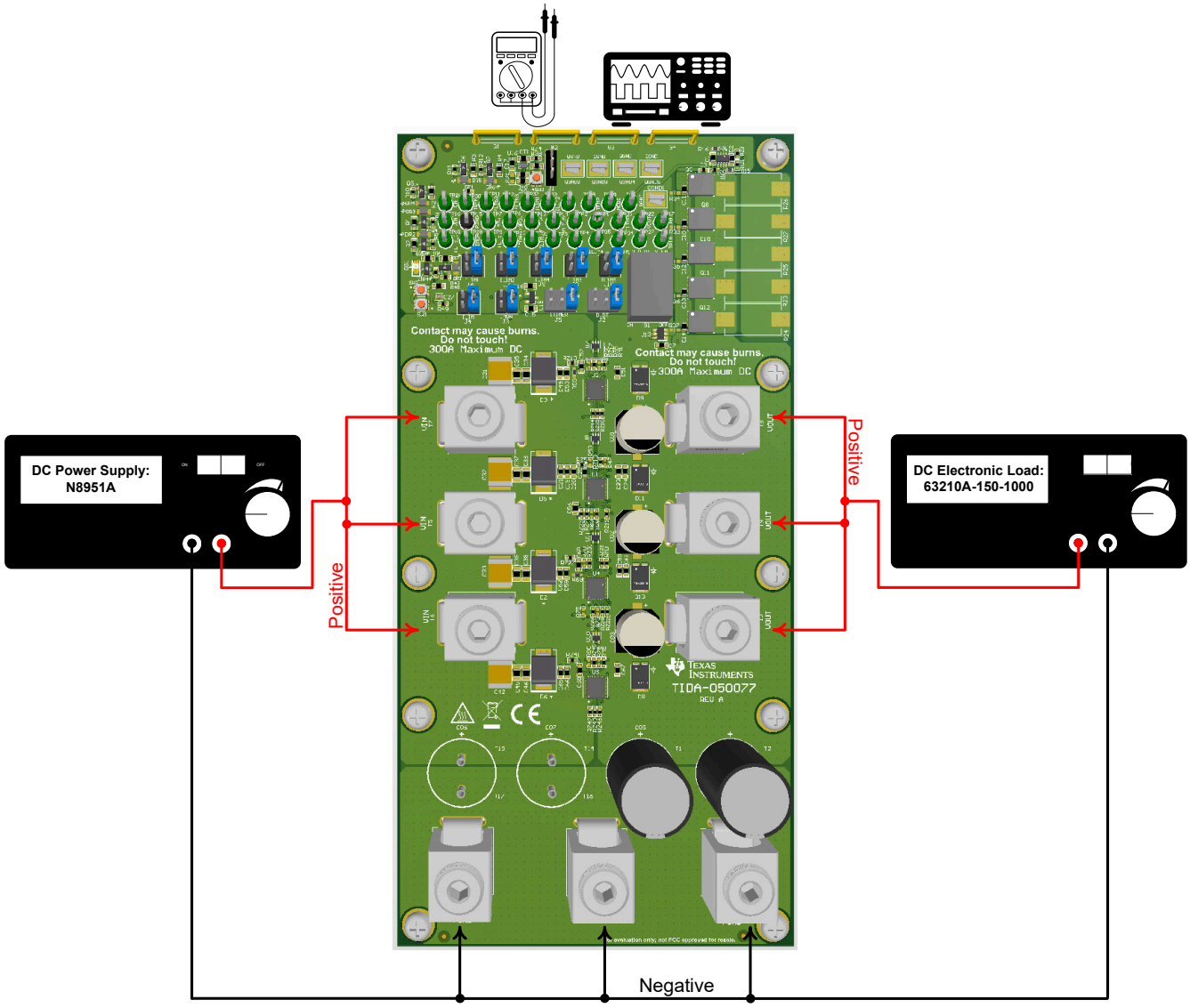


Figure 3-8. TIDA-050077 Test Setup

3.3 Test Results

Table 3-1 and Table 3-2 summarize the experimental results.

Table 3-1. Experimental Results Captured on TIDA-050077

BOARD CONFIGURATION	NAME OF THE EXPERIMENT	TEST CONDITIONS	FIGURE NUMBER
Four Devices in Parallel: Two devices on the top layer and two devices on the bottom layer	Input hot-plug	V_{IN} stepped up from 0V to 12V, C_{OUT} = 26mF, C_{DVDT} = 33nF, R_{ILIM} (each device)= 365Ω, R_{IREF} = 40.2kΩ, and R_{LOAD} = 1Ω	Figure 3-9
	Power-up using ENABLE	V_{IN} = 12V, EN stepped up from 0V to 3V, C_{OUT} = 58mF, C_{DVDT} = 33nF, R_{ILIM} (each device)= 365Ω, R_{IREF} = 40.2kΩ, and R_{LOAD} = 0.2Ω	Figure 3-10
	Current sharing among the devices during power-up	V_{IN} = 12V, EN stepped up from 0V to 3V, C_{OUT} = 58mF, C_{DVDT} = 33nF, R_{ILIM} (each device)= 365Ω, R_{IREF} = 40.2kΩ, and R_{LOAD} = 0.15Ω	Figure 3-11
	Power-up into output short to ground	V_{IN} = 12V, EN stepped up from 0V to 3V, R_{ILIM} (each device)= 464Ω, R_{IREF} = 40.2kΩ, and OUT shorted to PGND	Figure 3-12
	Current sharing among the devices during power-up into output short to ground	V_{IN} = 12V, EN stepped up from 0V to 3V, R_{ILIM} (each device)= 464Ω, R_{IREF} = 40.2kΩ, and OUT shorted to PGND	Figure 3-13
	Persistent overcurrent protection	V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 200A to 350A for 100ms then 200A Captured signals: VIN, VOUT, ITIMER, and IIN	Figure 3-14
		V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 200A to 350A for 100ms then 200A Captured signals: VIREF, VIMON, ITIMER, and IIN	Figure 3-15
	Transient overcurrent blanking	V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 200A for 10ms to 350A for 10ms then 200A for 10ms Captured signals: VIN, VOUT, ITIMER, and IIN	Figure 3-16
		V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 200A for 10ms to 350A for 10ms then 200A for 10ms Captured signals: VIREF, VIMON, ITIMER, and IIN	Figure 3-17
	Current sharing among the devices during persistent over-load	V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 200A to 350A for 100ms then 200A	Figure 3-18
	Current sharing among the devices during transient overload	V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 200A for 10ms to 350A for 10ms then 200A for 10ms	Figure 3-19
	Active current sharing during load transients	V_{IN} = 12V, C_{OUT} = 58mF, R_{IMON} = 167Ω, R_{IREF} = 40.2kΩ, R_{ILIM} (each device)= 365Ω, and I_{OUT} ramped from 0A to 200A in 100ms then ramped to 330A in 100ms and then ramped down to 200A in 100ms	Figure 3-20
	Active current sharing during steady-state	V_{IN} = 12V, C_{OUT} = 58mF, R_{IMON} = 167Ω, R_{IREF} = 40.2kΩ, R_{ILIM} (each device)= 365Ω, and I_{OUT} = 260A	Figure 3-21
	Output hot-short	V_{IN} = 12V, C_{OUT} = 58mF, R_{IMON} = 249Ω, R_{IREF} = 40.2kΩ, and OUT is connected to PGND under steady-state.	Figure 3-22

Table 3-1. Experimental Results Captured on TIDA-050077 (continued)

BOARD CONFIGURATION	NAME OF THE EXPERIMENT	TEST CONDITIONS	FIGURE NUMBER
Six Devices In Parallel: Four devices on the top layer and two devices on the bottom layer	Power-up using ENABLE	V_{IN} = 12V, EN stepped up from 0V to 3V, C_{OUT} = 95mF, C_{DVDT} = 33nF, R_{ILIM} (each device)= 365Ω, R_{IREF} = 40.2kΩ, and R_{LOAD} = 0.15Ω	Figure 3-23
	Power-up into output short to ground	V_{IN} = 12V, EN stepped up from 0V to 3V, R_{ILIM} (each device)= 365Ω, R_{IREF} = 40.2kΩ, and OUT shorted to PGND	Figure 3-24
	Transient overcurrent blanking	V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 95mF, R_{IMON} = 167Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 300A for 10ms to 500A for 10ms then 300A for 10ms	Figure 3-25
	Persistent overcurrent protection	V_{IN} = 12V, t_{ITIMER} = 16ms, C_{OUT} = 95mF, R_{IMON} = 167Ω, R_{IREF} = 40.2kΩ, and I_{OUT} ramped from 300A to 500A for 100ms then 300A	Figure 3-26

Table 3-2. Thermal Performance of the TIDA-050077 Reference Design

BOARD CONFIGURATION	TEST CONDITIONS	THERMAL IMAGE CAPTURED	FIGURE NUMBER
Four Devices in Parallel: All devices on the top layer.	V_{IN} = 12V, I_{OUT} = 200A, and no external airflow	Top Layer	Figure 3-27
Four Devices in Parallel: Two devices on the top layer and the other two devices on the bottom layer at exactly the same location as the top layer devices.	V_{IN} = 12V, I_{OUT} = 200A, and no external airflow	Top Layer	Figure 3-28
		Bottom Layer	Figure 3-29
Six Devices in Parallel: Four devices on the top layer and the other two devices on the bottom layer at exactly the same locations as the second and third devices on the top layer.	V_{IN} = 12V, I_{OUT} = 300A, and no external airflow	Top Layer	Figure 3-30
		Bottom Layer	Figure 3-31

Figure 3-9 through Figure 3-26 show various test results in the TIDA-050077 reference design.

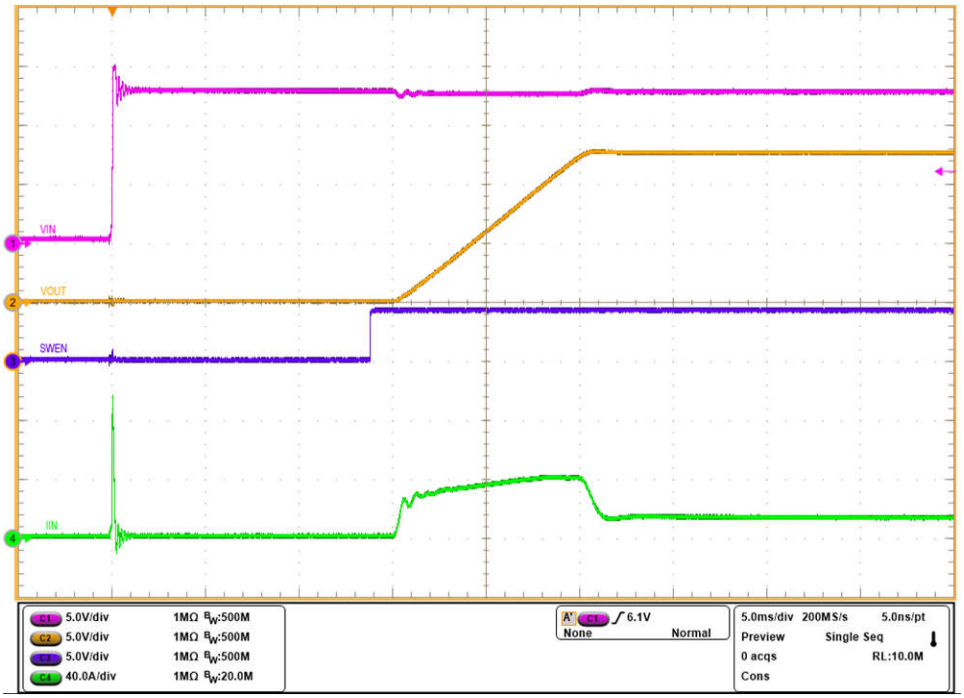


Figure 3-9. Hot-Plug Profile With Two Devices on the Top Layer and Two Devices on the Bottom Layer

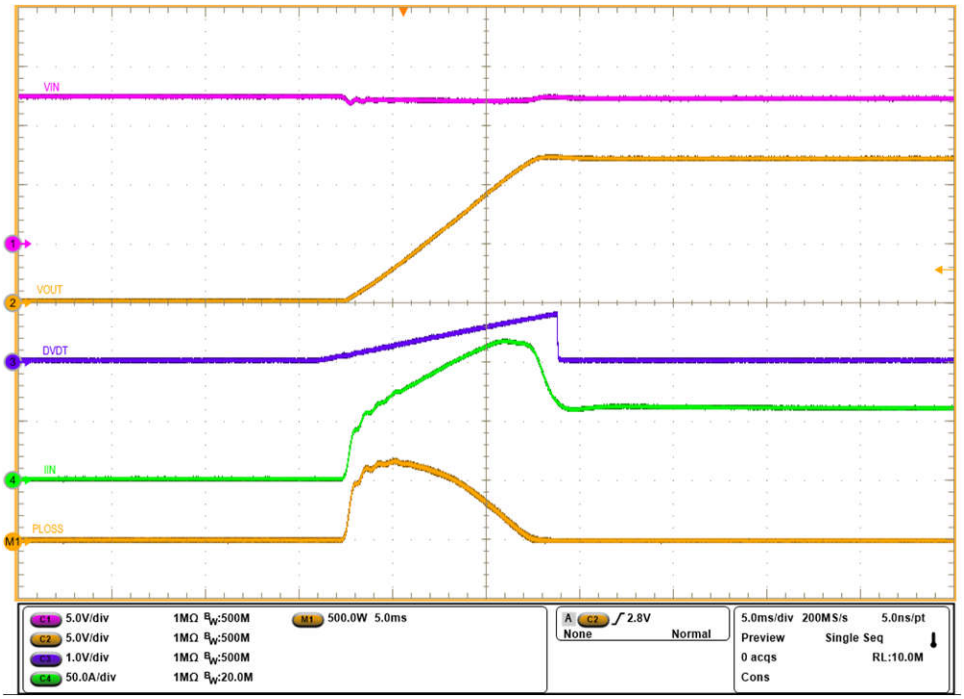


Figure 3-10. Power-Up Using ENABLE With Two Devices on the Top Layer and Two Devices on the Bottom Layer

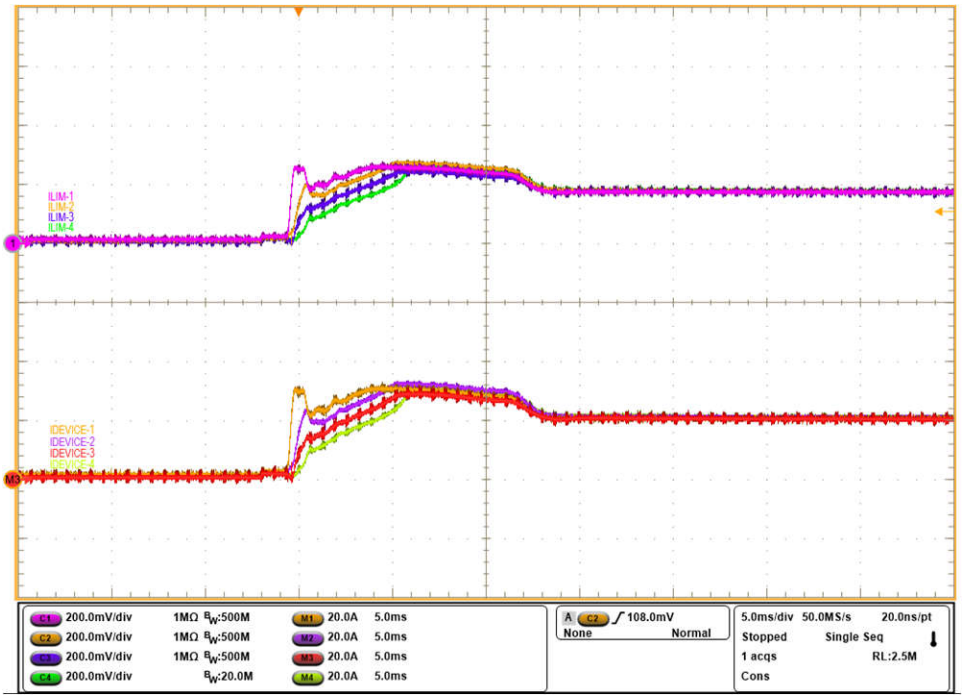


Figure 3-11. Current Sharing Among the Devices During Power-Up With Four Devices in Parallel

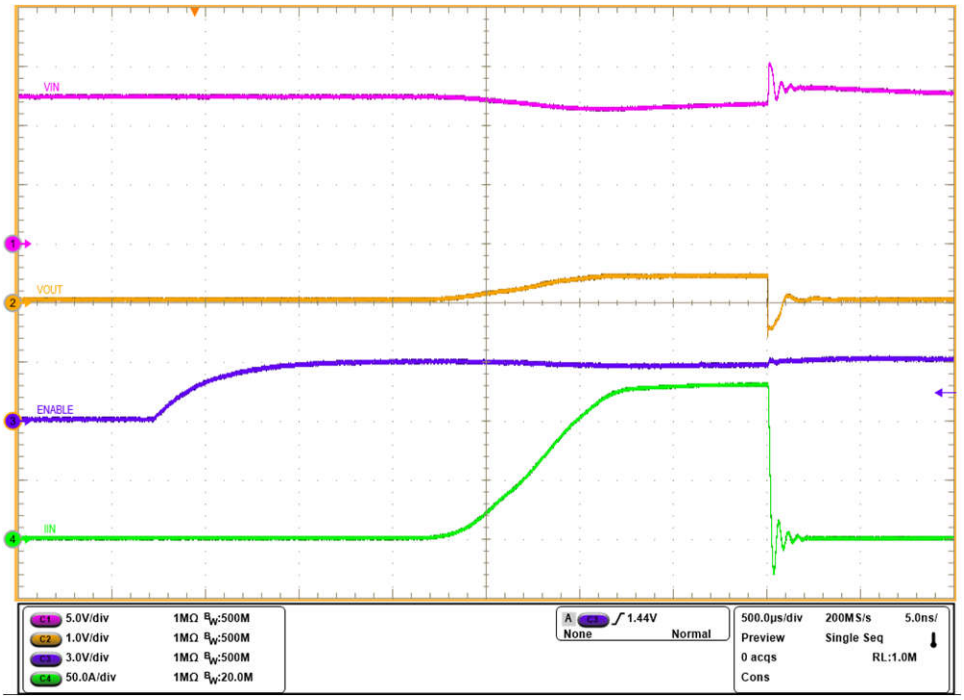


Figure 3-12. Power-Up Into Output Short Response With Four Devices in Parallel

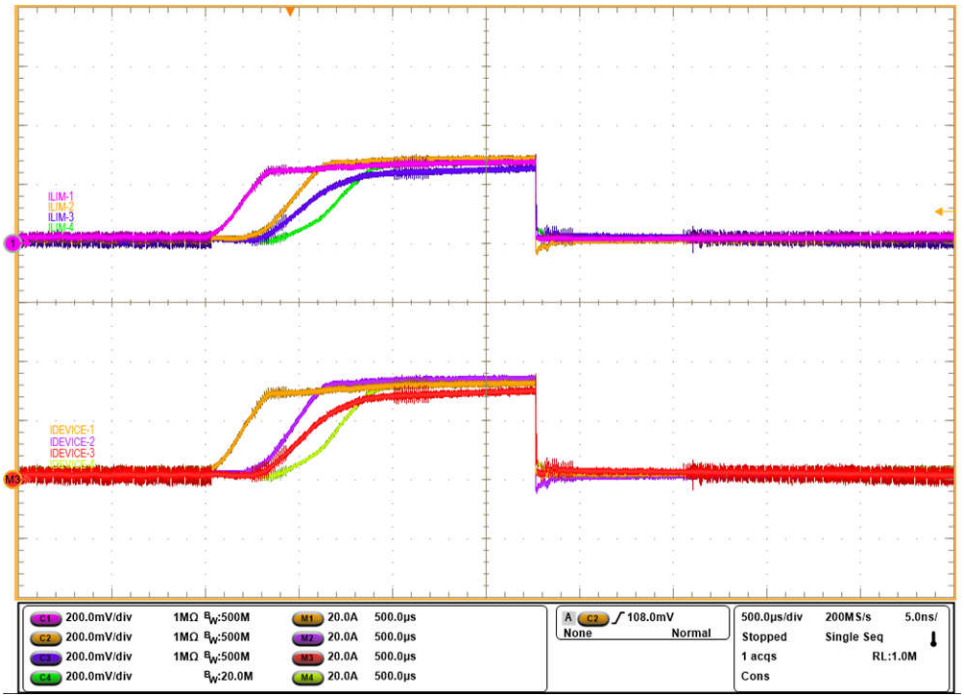


Figure 3-13. Current Sharing Among the Devices During Power-Up Into Short With Four Devices in Parallel

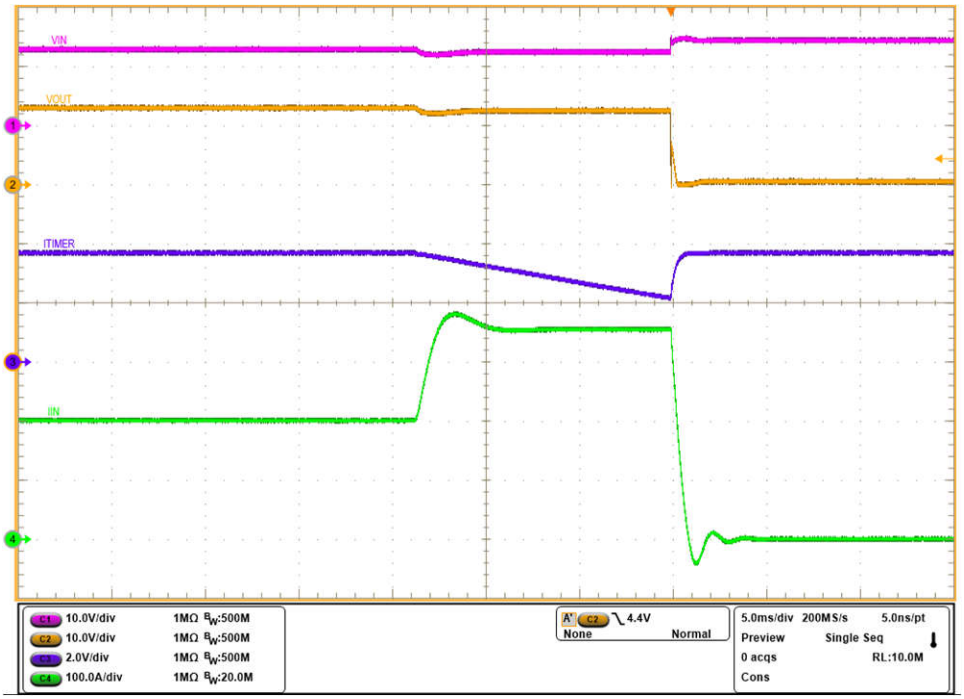


Figure 3-14. Overcurrent Performance With Four Devices in Parallel

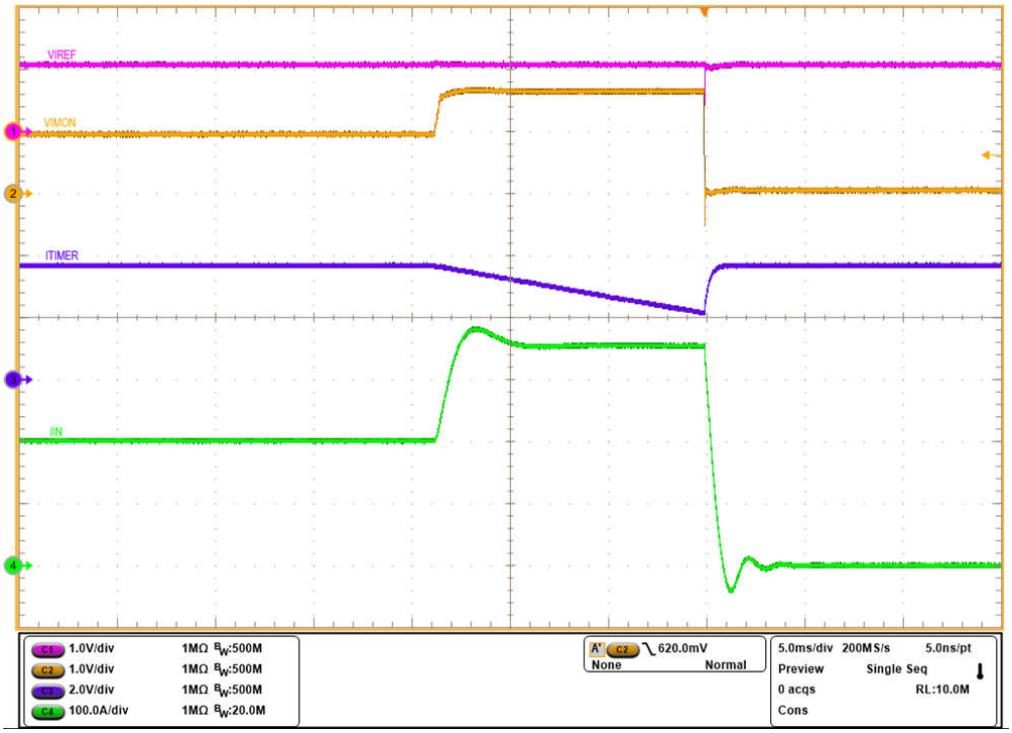


Figure 3-15. Overcurrent Performance With Four Devices in Parallel

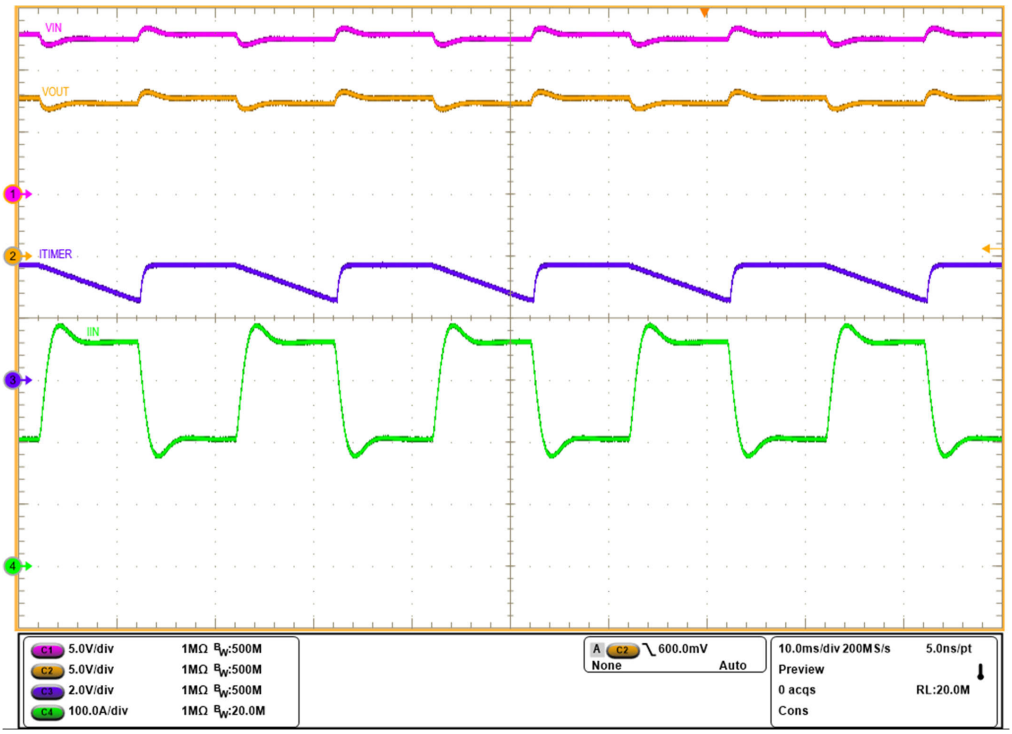


Figure 3-16. Transient Overload Performance With Four Devices in Parallel

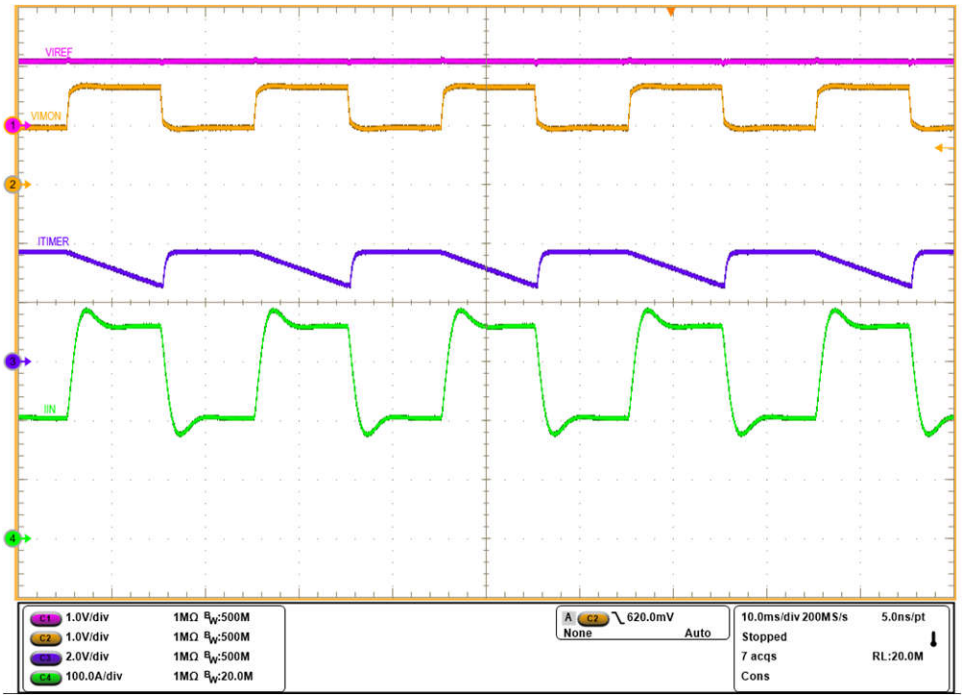


Figure 3-17. Transient Overload Performance With Four Devices in Parallel

Figure 3-18. Current Sharing Among the Devices During an Overcurrent Event With Four Devices in Parallel

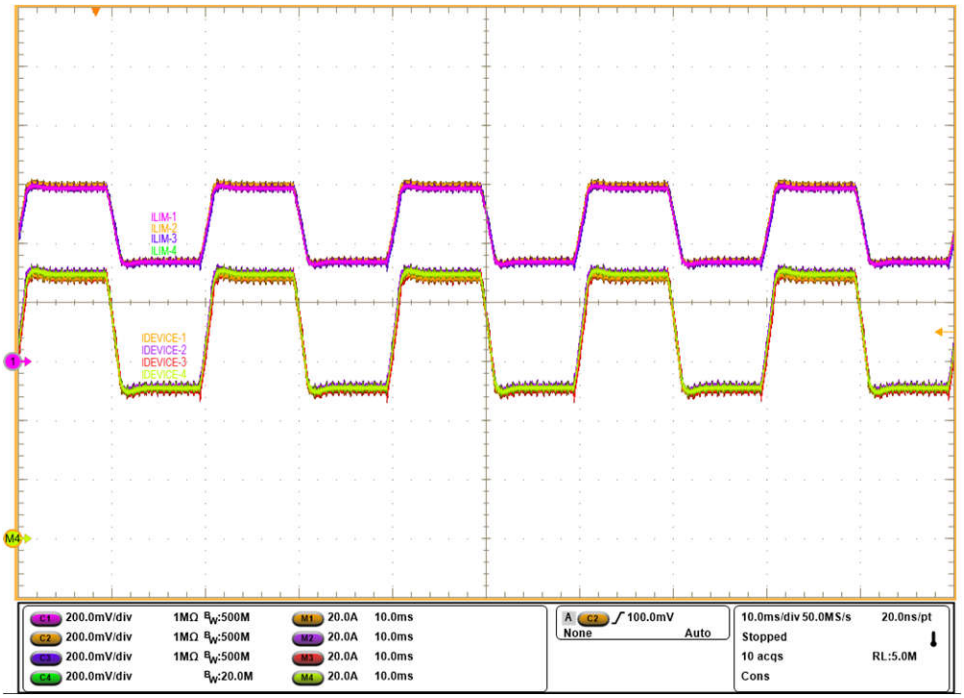


Figure 3-19. Current Sharing Among the Devices During Transient Overload Events With Four Devices in Parallel

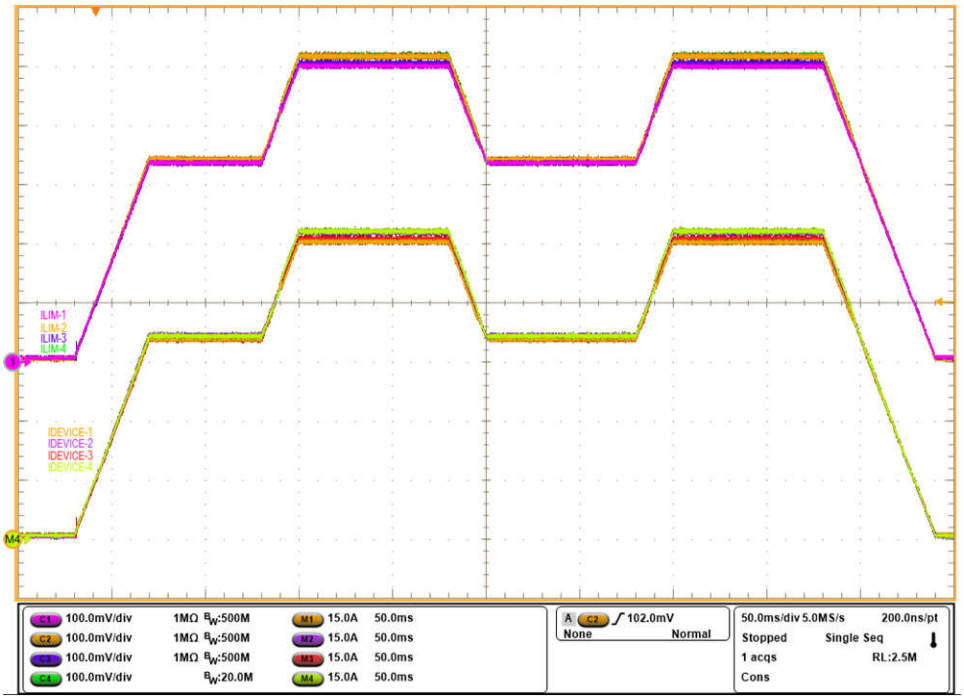


Figure 3-20. Active Current Sharing Among the Devices During Load Transients With Four Devices in Parallel

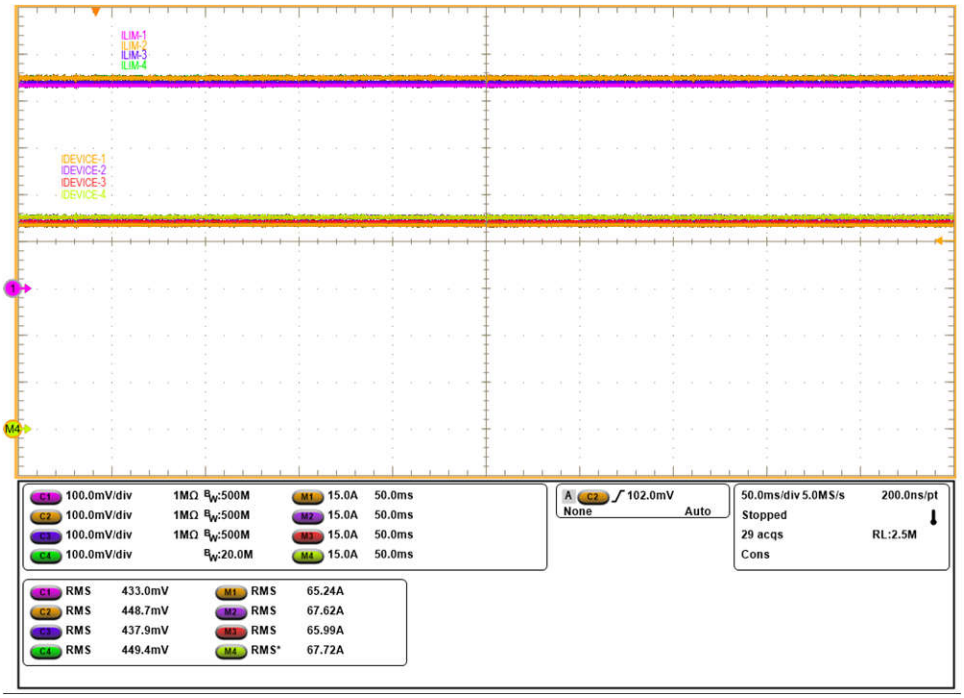


Figure 3-21. Active Current Sharing Among the Devices During Steady-State With Four Devices in Parallel

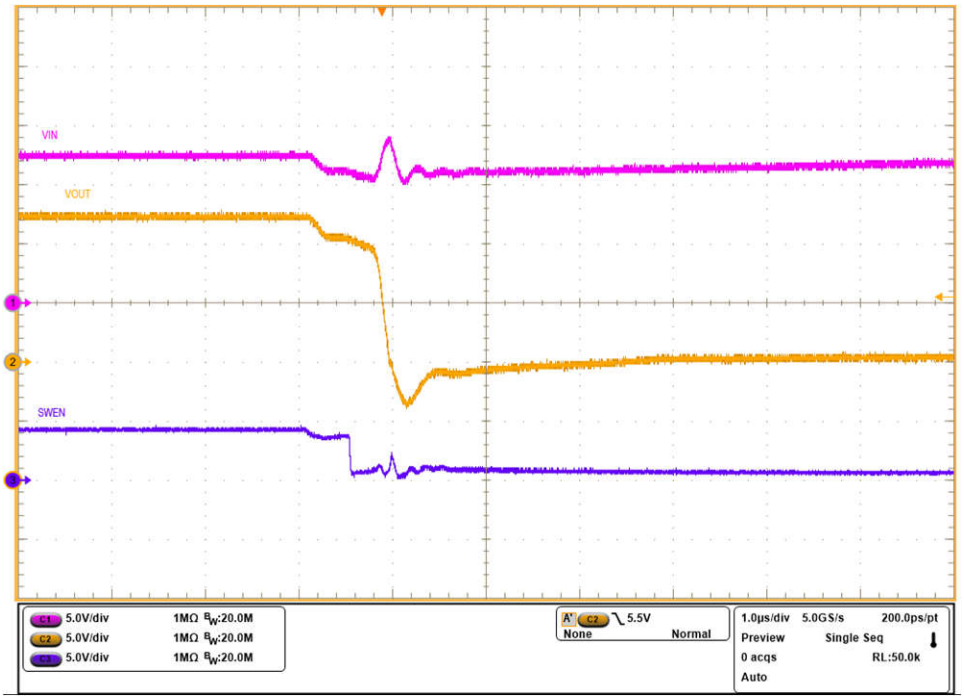


Figure 3-22. Output Hot-Short Response

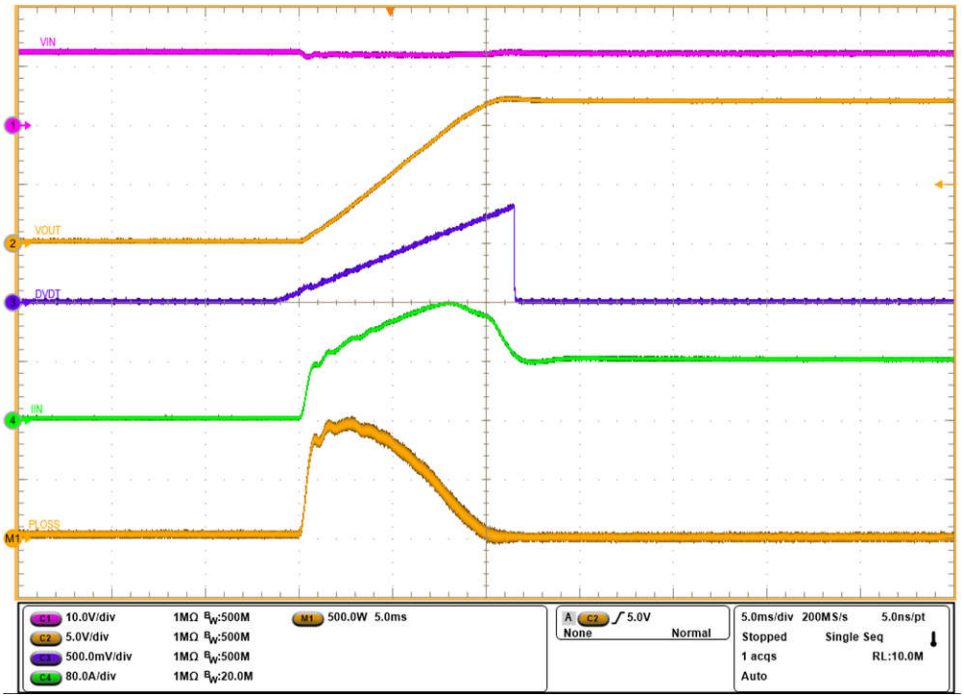


Figure 3-23. Power-Up Using ENABLE With Four Devices on the Top Layer and Two Devices on the Bottom Layer

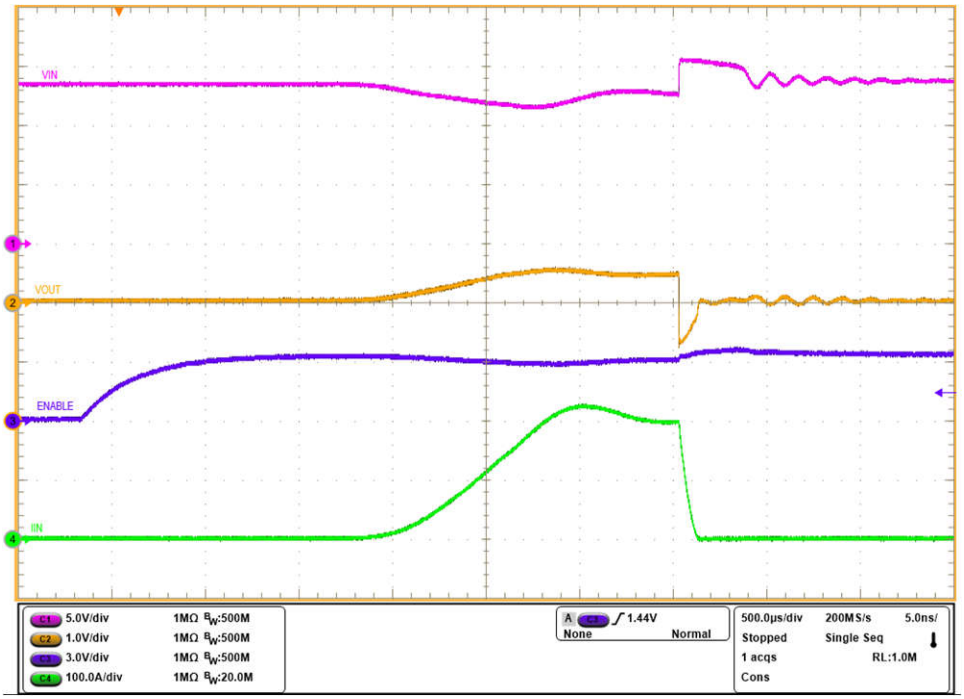


Figure 3-24. Power-Up Into Output Short Response With Six Devices in Parallel

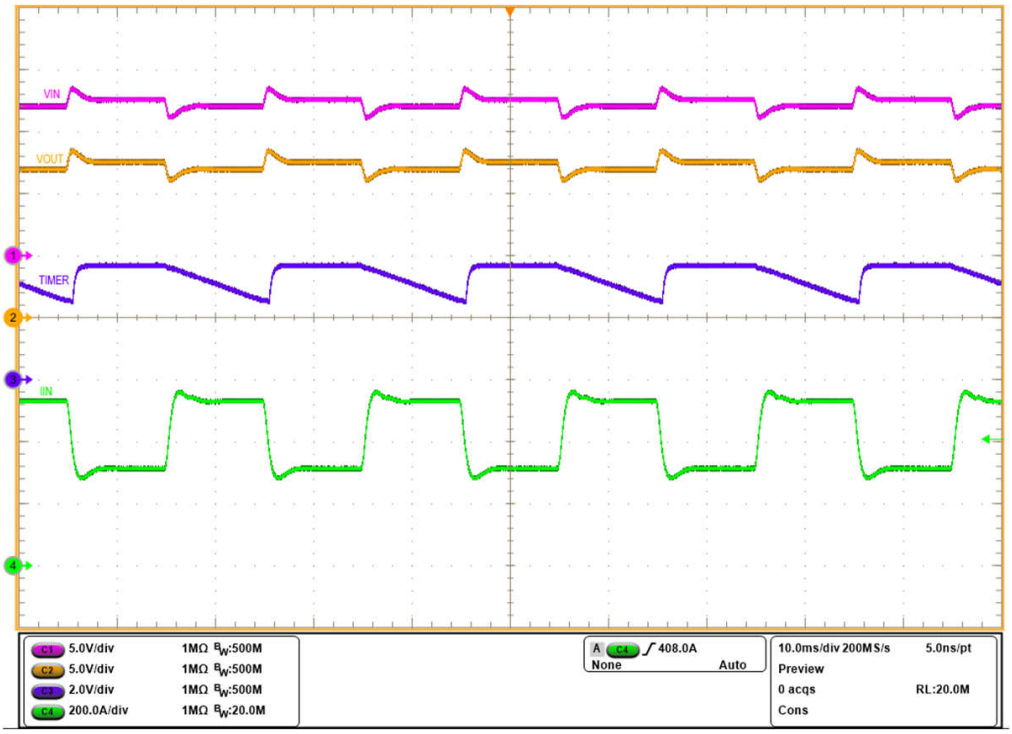


Figure 3-25. Transient Overload Performance With Six Devices in Parallel

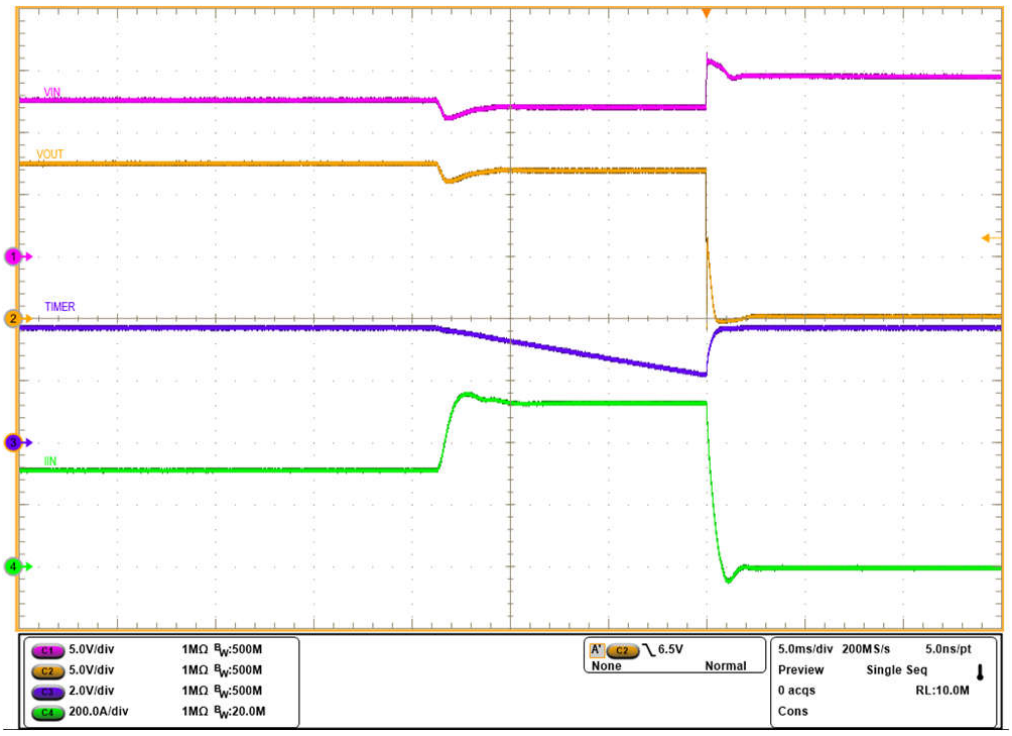
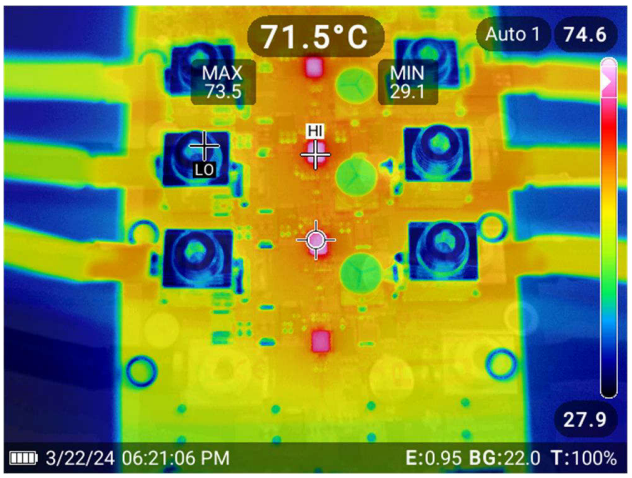


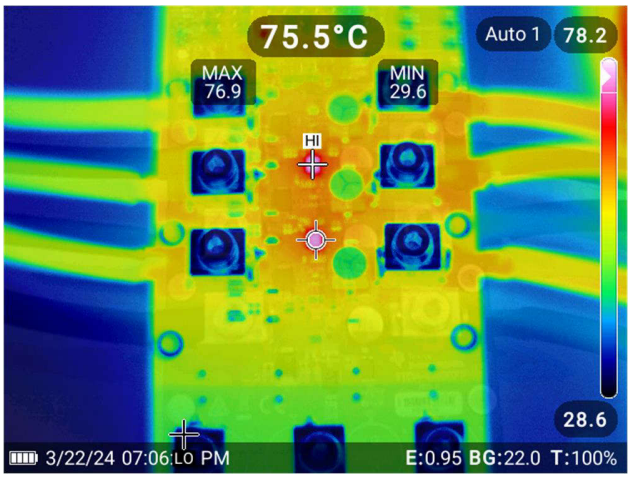
Figure 3-26. Overcurrent Performance With Six Devices in Parallel

Figure 3-27 through Figure 3-29 show the thermal performance of the TIDA-050077 reference design under the given conditions.



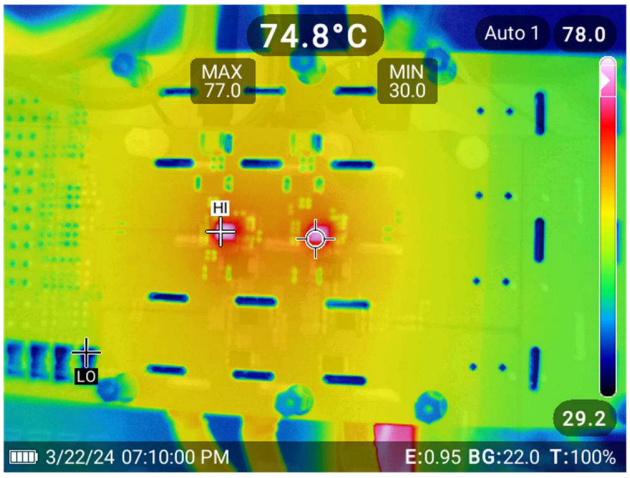
All four devices are on the top layer in parallel.

Figure 3-27. Four Devices



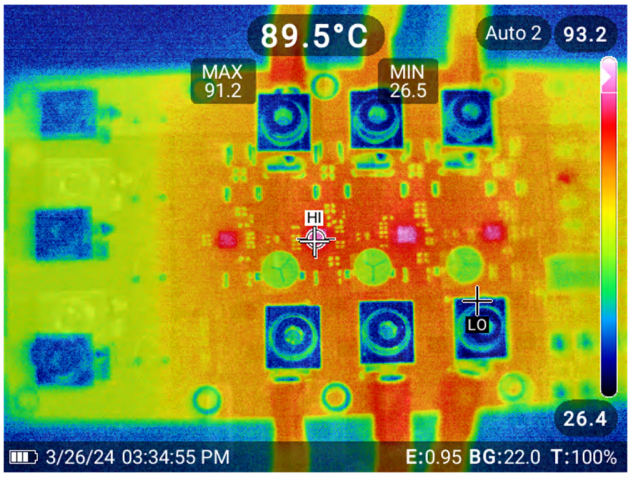
Two devices are on the top layer and the other two devices are on the bottom layer exactly at same location as the top layer devices, in parallel.

Figure 3-28. Top Layer of the Board With Four Devices



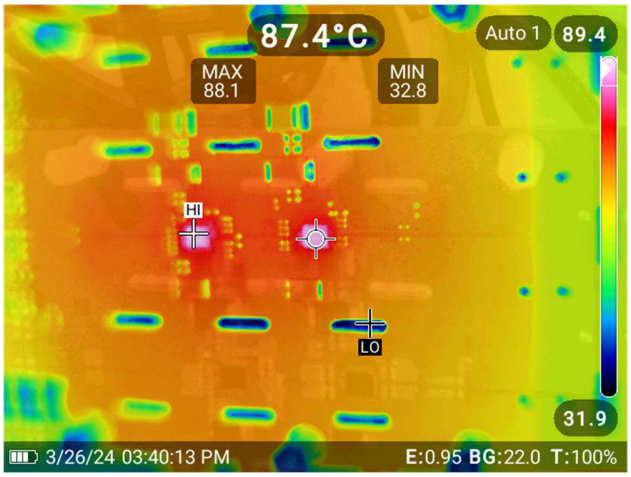
Two devices are on the top layer and the other two devices are on the bottom layer exactly at same location as the top layer devices, in parallel.

Figure 3-29. Bottom Layer of the Board With Four devices



V_{IN} = 12V, I_{OUT} = 300A, and no external air flow

Figure 3-30. Top Layer of the Board With Six Devices in Parallel



V_{IN} = 12V, I_{OUT} = 300A, and no external air flow

Figure 3-31. Bottom Layer of the Board With Six Devices in Parallel

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050077.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050077.

4.1.3 Altium Project

To download the Altium project files, see the design files at TIDA-050077.

4.1.4 Gerber Files

To download the Gerber files, see the design files at TIDA-050077.

4.2 Tools

Tools

Design Calculator	TPS25985 Design Calculator
TVS-RECOMMENDATION-CALC	TVS diode recommendation tool
PSPICE-FOR-TI	PSpice® for TI design and simulation tool

4.3 Documentation Support

1. Texas Instruments, *TPS25985x 4.5V – 16V, 0.59mΩ, 80A Stackable eFuse with Accurate and Fast Current Monitor Data Sheet*
2. Texas Instruments, *LM94022, LM94022-Q1 1.5V, SC70, Multi-Gain Analog Temperature Sensor With Class-AB Output Data Sheet*
3. Texas Instruments, *SN74LVC1G123 Single Retriggerable Monostable Multivibrator With Schmitt-Trigger Inputs Data Sheet*
4. Texas Instruments, *INA241x –5V to 110V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection Data Sheet*
5. Texas Instruments, *UCC2751x Single-Channel, High-Speed, Low-Side Gate Driver (With 4A Peak Source and 8A Peak Sink) Data Sheet*
6. Texas Instruments, *TLV760 100mA, 30V, Fixed-Output, Linear-Voltage Regulator Data Sheet*
7. Texas Instruments, *CSD18510Q5B N-Channel NexFET™ Power MOSFET Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.5 Trademarks

TI E2E™ and NexFET™ are trademarks of Texas Instruments.
Intel® is a registered trademark of Intel Corporation.
Fluke® is a registered trademark of Fluke Corporation.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

5 About the Author

AVISHEK PAL is a Product Application Engineer at Texas Instruments, responsible for supporting hot-swap controllers and high-current eFuse devices. He earned his Master of Science (MS by Research) from the Indian Institute of Technology, Kharagpur, and his Bachelor of Engineering (BE) from the Indian Institute of Engineering Science and Technology, Shibpur (IIEST).

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265