*Design Guide: TIDA-050080*

# *High-Voltage Passive Precharge With Overcurrent Protection Reference Design*

## Description

This reference design implements a common circuit in high-voltage DC buses – precharge – with newer, smaller, and more cost-efficient components. This design features the TPSI3100-Q1 isolated switch driver, which provides reinforced isolation between voltage domains and does not require a secondary side bias supply for driving field-effect transistors (FET). TPSI3100-Q1 also offers integrated digital comparators for fault detection which, in this design, is used for overcurrent protection. This design is rated for an 800V battery management system (BMS) but can also be implemented in 400V systems.

## Features

- 5kV$_{RMS}$ reinforced isolation
- Integrated isolated bias supply
- Supports 800V power train architectures
- Provides low-cost overcurrent detection scheme
- Capable of charging 2mF capacitor to 800V in 500ms

## Applications

- High-voltage battery system
- Traction inverter
- Battery energy storage system

## Resources

| | |
|---|---|
| TIDA-050080 | Design Folder |
| TPSI3100-Q1. TPSI2140-Q1 | Product Folder |
| INA180-Q1 | Product Folder |

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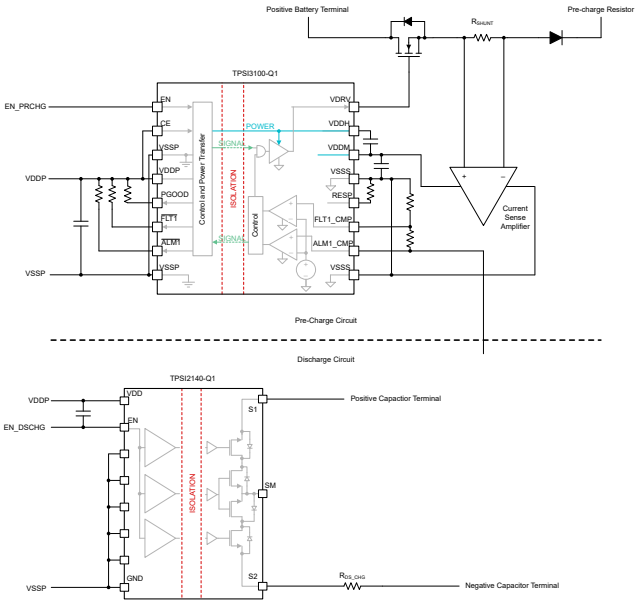


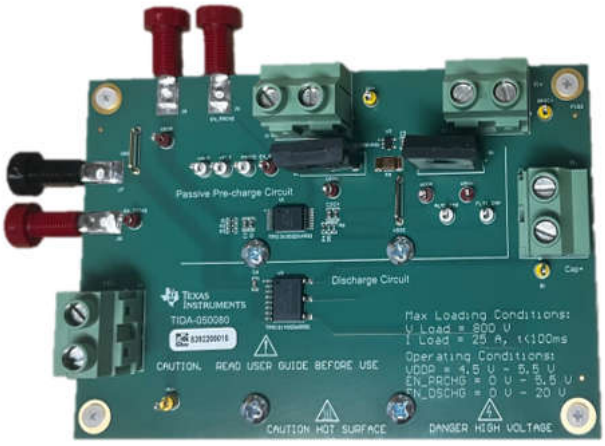

# 1 System Description

Precharge is a common circuit in Electric and Hybrid Electric Vehicles (EVs and HEVs) that prepares the high-voltage DC rails before the rails are connected to the battery. The positive and negative high-voltage rails are connected by the DC-Link capacitor, which helps stabilize the rails as loads are connected and disconnected during the vehicle operation. A precharge circuit charges the DC-link capacitor to the battery voltage, minimizing the inrush current caused when the main contactors close. For the health of the main contactors the inrush is minimized as too high of inrush can cause the contacts to weld together, rendering them defective.

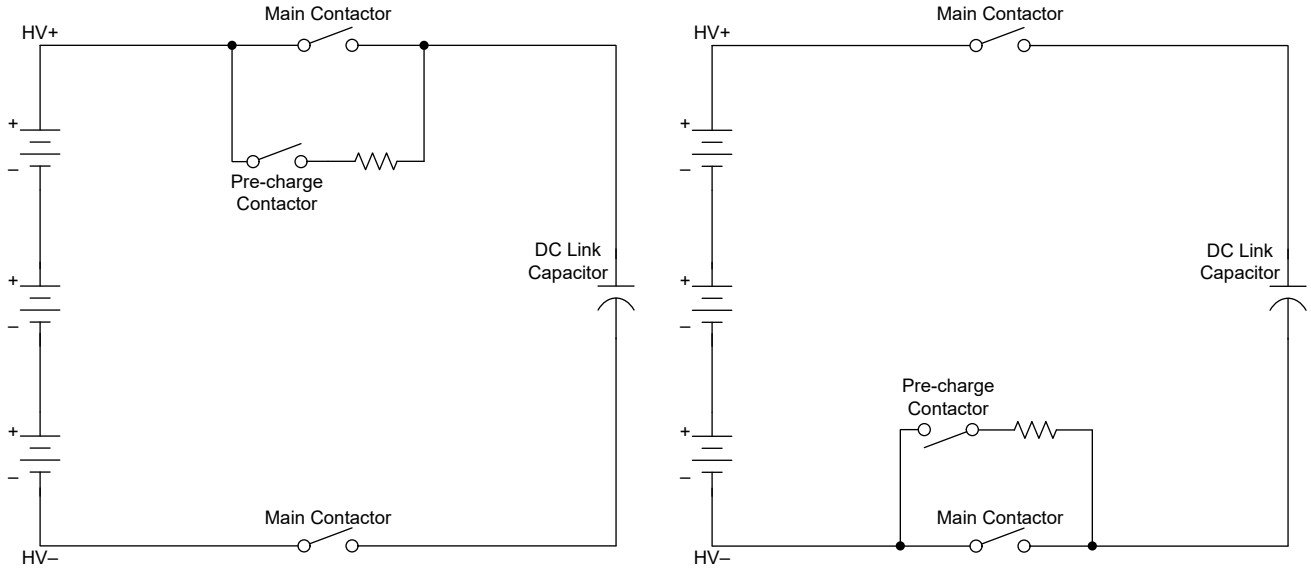


**Figure 1-1. Precharge Configurations**

This design features passive precharge with solid-state relays. In passive precharge, the switch closes statically until the capacitor is charged. Figure 1-1 shows how precharge is often achieved with mechanical contractors or relays. The goal of this design is to replace the mechanical contactor with a solid-state relay, providing a more reliable design. The benefits of passive precharge are the low complexity and low switching noise emissions. This is a very common method of precharge in the industry because of the simplicity and the widespread availability and options of power resistors. However, as this design has less control logic, sizing components to withstand the power and protecting them from overcurrent is foremost of the design considerations.

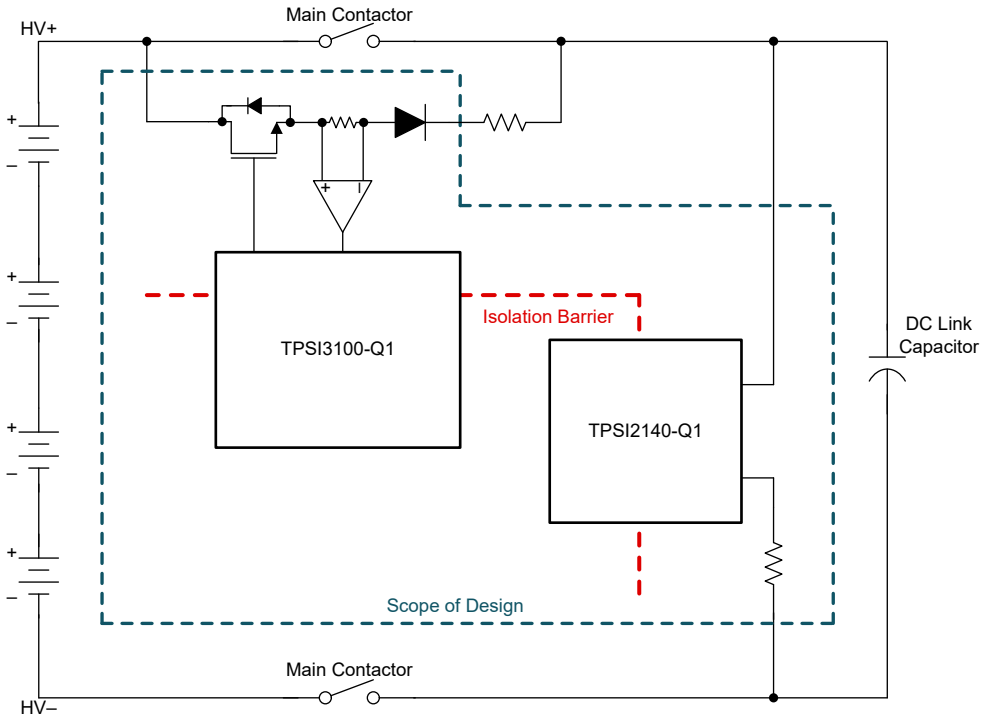


**Figure 1-2. Scope of Design**

Outside of the high-power path, the control circuitry of this design is comprised of a FET driver and an overcurrent detection circuit. This design uses the TPSI3100-Q1 isolated switch driver which, when paired with a FET, creates a seamless solid-state relay design that replaces contactors such as the precharge contactor. Additionally, integrated in the TPSI3100-Q1 are fault and alarm comparators. The fault comparator disables the driver when tripped and sends a signal back across the barrier. The alarm comparator only sends a signal when tripped. Along with an INA180-Q1 current-sense amplifier, these comparators constitute the overcurrent detection circuit. The current-sense amplifier is powered through the internal secondary side supply of the TPSI3100-Q1, a nominal 5V rail generated from the VDDM pin.

The final element of this design is a discharge path for the voltage that is stored on the capacitor. In EVs, there are different types of discharge requirements. For safety-critical events, such as a crash, the capacitor must be discharged in under a few seconds, the exact time varying between manufacturers. For non-emergency cases, the discharge can be on the order of minutes. This design features a non-emergency discharge that is comprised of the isolated switch TPSI2140-Q1 and a power resistor. Once activated, the capacitor is discharged to below 60V in about 2 minutes from 1000V. This discharge circuit is also necessary for safe handling and testing of the design.

# 2 System Overview

## 2.1 Block Diagram

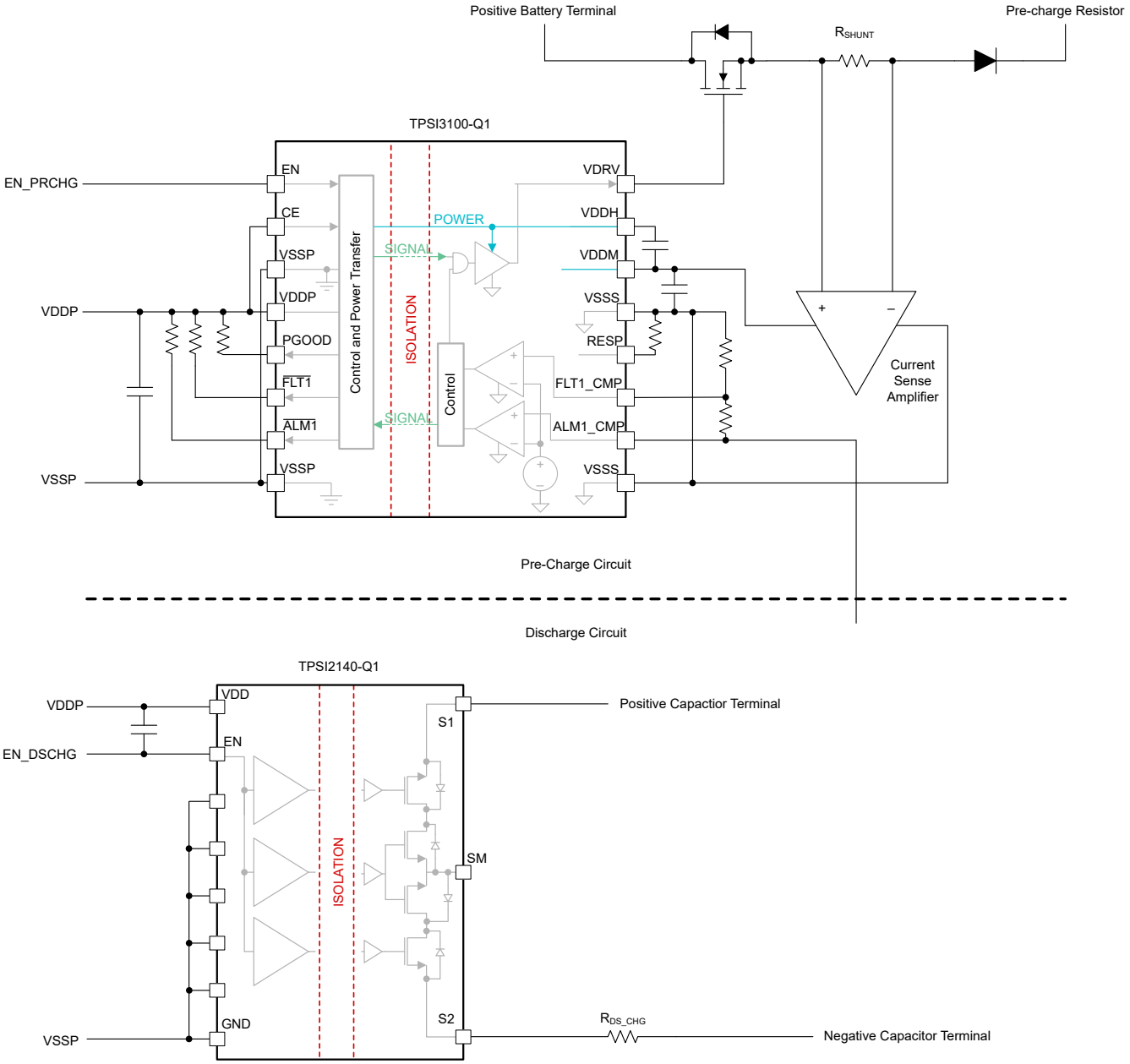


**Figure 2-1. Block Diagram**

## 2.2 Design Considerations

The precharge design process begins with the requirements as the requirements are the most consequential aspect in the choice of components. Table 2-1 lists the requirements.

**Table 2-1. Precharge Design Requirements**

| REQUIREMENT NAME | VALUE |
|---|---|
| Precharge Time | 0.5 seconds |
| System Voltage | 800V (1000V) |
| DC-Link Capacitance | 2mF |

This design must charge a 2mF DC-Link capacitor up to the system voltage of 800V in 0.5 seconds. However, 800V EVs can carry as much as 1000V at full charge, so the components in the design must be sized accordingly.

### 2.2.1 Design Theory

At a high level, a passive precharge circuit is a simple RC circuit that can be represented as an exponentially decaying function. The voltage on the capacitor is calculated using Equation 1:

$$V_C = V_S \times \left(1 - e^{\frac{-t}{\tau}}\right) \quad (1)$$

where

- $V_S$ is the system voltage
- The time constant τ, or Tau, determines the rate of charge

For this system, the precharge cycle is considered complete when the 5τ has passed. Some systems can require longer than 5τ to charge to maintain that the voltage drop across the main contactors meets the contactor switching requirements. The desired system resistance is calculated from the time constant equation (Equation 2):

$$5 \times \tau = 5 \times R \times C = 0.5 \text{ seconds} \quad (2)$$

Substituting the DC-Link capacitance and solving for R, the system resistance is 50Ω. Of all the components in the power path, the precharge power resistor dissipates the most power. This component is not sized with the peak or average power in mind, however. To size the resistor, the pulse energy and length are the most important. The energy can be calculated through two ways: as an integral of power over time (Equation 3) and as a function of the capacitor (Equation 4):

$$E = \int_0^{0.5} 20{,}000 \times e^{\frac{-2 \times t}{0.1}} dt \approx 1000 \text{ J} \quad (3)$$

$$E = \frac{1}{2}CV^2 = 1000 \text{ J} \quad (4)$$

### 2.2.2 Resistor Selection

The correct resistor is most reliably selected through an understanding of the pulse energy. The standard resistor power rating is the limit of continuous power that the resistor can handle if held at a specific ambient temperature, very often 25°C. Since precharge is not a uniform or continuous type power cycle, choosing a 20kW resistor is wrong. Moreover, a resistor of this size is tremendously expensive, heavy, and possibly does not even exist. The characteristics of the resistor that are relevant to this design are the pulse energy handling capabilities, which are a determined by the thermal robustness of the resistive element and the ability to sink heat. For this design, a wire-wound resistor is the best option because these resistors have additional mass placed within, known as the core, and often around the coil, which is known as the housing. This additional mass sinks the heat generated from the high-power pulse.

There are several ways to determine if a resistor is capable of the handling the precharge pulse, typically through charts that are included in the data sheet. The first way is through the short-term overload rating. This rating means that for a specified period of time, the resistor can withstand some multiple of the regular power rating. Wire-wound resistors typically have a short-term overload of 5 × or 10 × the rated power for 5 seconds. This can sometimes be extrapolated further and presented as a chart: if a resistor has an overload of 5 × for 5 seconds then the resistor can also be able to handle 25 × for 1 second if the data sheet explicitly says. If the power rating of the resistor is 100W, the overload pulse energy in this scenario is 2500J. This does not mean the resistor can handle 2500J of any pulse length. Too short of a pulse length does not allow the coil enough time to distribute the heat throughout the core and housing, causing the wire to fail.

The second way to confirm the ability of a resistor is through a pulse energy chart. This chart is typically presented with resistance on the x-axis, linear or logarithmic, and pulse energy on the y-axis. The chart relatively straightforward visual that shows the pulse energy limit of each resistor within a family. A third chart to reference is often labeled pulse performance. This chart shows pulse duration on the x-axis and maximum power on the y-axis, both of which are in the logarithmic form.

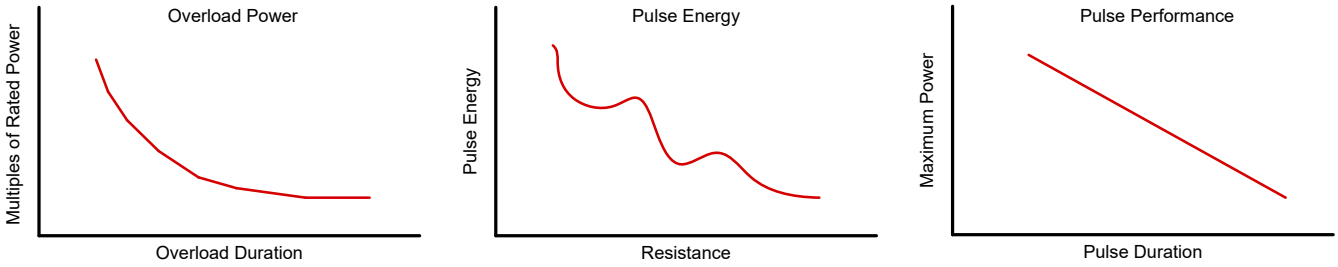


**Figure 2-2. Power and Energy Plot Variants**

In the interest of cutting costs, a designer can pursue the smallest possible resistor available that can handle the precharge pulse. In this event, or if none of the pulse information is published, confirm with the manufacturer what the energy limits are for a particular resistor. As the energy limit can change depending on the type of pulse, a designer must confirm the resistor based on a capacitive pulse.

#### 2.2.2.1 Transistor and Diode Selection

For this design, the first thing to consider in both the transistor and the diode is the breakdown and blocking voltage. Since this is for an 800V BMS, the blocking voltage must be higher. Note that EV batteries are often charged to a higher voltage than the system voltage; an 800V EV can hold as much as 1000V on a full charge. Select a breakdown that gives additional margin above the full charge voltage of the EV. For this design, the breakdown for the FET and the diode must be 1200V.

The next consideration for these components, particularly the transistor, is the power, heat, and time. Similar to the resistor, a continuous characteristic such as the rated continuous drain current of a FET is not useful for two reasons: a characteristic like this is determined under an exceptional thermal scenario with no temporal consideration and the precharge cycle is a pulse, not continuous. Use the Safe Operating Area chart on the FET data sheet to determine if a FET is good. In an RC circuit like precharge, the power dissipation in the resistor is nearly one-third of the initial magnitude after one time constant. Relating that to this design, the pulse length worth considering for component sizing is 100ms. FETs sized for 1200V automotive systems often show a 100ms curve on the Safe Operating Area chart and a FET is likely to be large enough if the peak expected current through the design is beneath both the 100ms curve and the on-resistance limit curve.

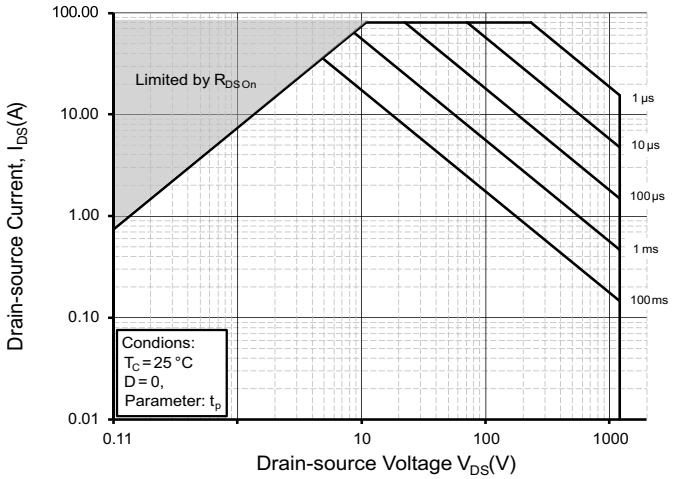


**Figure 2-3. Safe Operating Area of a Wolfspeed E3M0075120D SiC MOSFET**

The final component that requires additional scrutiny is the diode. As mentioned, a reverse blocking voltage of 1200V is needed and the diode must withstand the maximum forward current of the design. The forward current capabilities are confirmed through the continuous forward current rating. For this design, this current rating does not have to be larger than the peak current of the circuit, since the diodes non-repetitive peak forward surge current rating is likely orders of magnitude larger than this peak current. To be safe, the diode chosen for this design was chosen with a continuous forward current that is no more 60%–80% of the peak forward current. This maintains that the diode can withstand a soft short that is too low to trip the overcurrent protection. Additionally, if a design with a lower $R_{DS(on)}$ and lower voltage drop is needed, a second blocking FET can be used, however this is higher cost.

### *2.2.3 Overcurrent Detection – Short-Circuit Protection*

The TPSI3100-Q1 includes two high-speed comparators on the secondary side. The information from both comparators is transmitted to the primary side; however, the fault comparator, when tripped, de-asserts the drive pin. At a system-level perspective, these signals can be sent to a microcontroller to provide current, voltage, or temperature monitoring. Although the fault comparator does not need a monitor to disable the driver, the information can still be useful. In this design, these comparators are used in an overcurrent protection circuit. This circuit is comprised of the unidirectional current sense amplifier INA180-Q1 which outputs into a resistor divider that feeds the fault and alarm comparators of the TPSI3100-Q1. The fault current is 25A because at a full 1000V charge the initial current can reach 20A. To reduce the risk of false positives throughout the life of the design, add some margin.

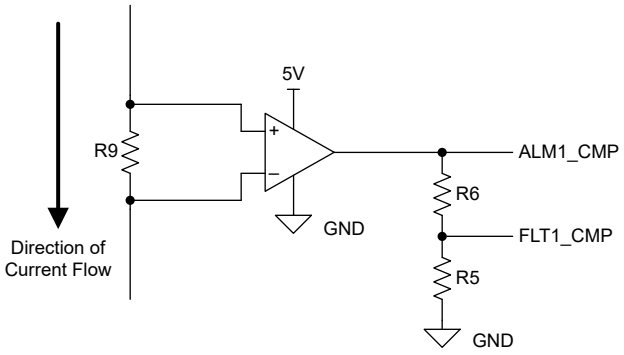


**Figure 2-4. Current-Sense Scheme**

There are several different ways an ALM1_CMP comparator can be configured. Since this comparator cannot disable the driver, there is more flexibility in the precise meaning of the signal. Table 2-2 shows three examples of the ALM configuration.

**Table 2-2. ALM Configuration Examples**

| CONFIGURATION | FLT CURRENT | ALM CURRENT | R9 | R6 | R5 | ALM PURPOSE |
|---|---|---|---|---|---|---|
| 1 | 2A | 20A | 0.75mΩ | 2.5kΩ | 10kΩ | ALM must deassert in less than 10ms to 50ms |
| 2 | 25A | 12.5A | 1.2mΩ | 10kΩ | 10kΩ | ALM must deassert in less than 50ms to 70ms |
| 3 | 25A | 2A | 7.5mΩ | 115kΩ | 10kΩ | ALM must deassert in less than 300ms |

In configuration 1, the alarm signal is not tripped on a regular basis as the circumstance requires a 1000V charge. Therefore, the alarm signal serves as a warning that the current has reached a level that can prove harmful to the components in the power path if not addressed quickly. Since the driver is disabled at 25A, the range of currents expected is between 20A and 25A. A reasonable time period for the alarm to be active under this operation is from 10ms to 50ms. The alarm information is transmitted across the isolation barrier in 30µs, which gives a microcontroller the ability to act if the alarm signal remains active.

In configurations 2 and 3, expect for the alarm signal to trip and remain tripped for a longer time. Similar to configuration 1, a microcontroller can be tasked with timekeeping and given authority to disable the device if the time limit is exceeded. Configuration 2 gives some more breathing room for the alarm signal to deactivate and configuration 3 is the temporal halfway point of the typical precharge cycle.

Beyond current and voltage sensing, the alarm and fault signals can be used for much more such as temperature or humidity. Because of the low latency with which the signals are transmitted to the primary side, more complex operations are possible with a microcontroller.

## 2.3 Highlighted Products

### *2.3.1 TPSI3100-Q1*

The TPSI3100-Q1 is a fully integrated isolated switch driver, which when combined with an external power switch, forms a complete isolated solid-state relay design. With a gate drive voltage of 15.8V with 1.5A, 2.5A peak source current or sink current, a large availability of power switches can be used to meet many application needs. The TPSI3100-Q1 generates a secondary bias supply from power received on the primary side, so no isolated secondary supply bias is required. The TPSI3100-Q1 provides additional power through the nominal 5V rail (VDDM) for use by auxiliary circuits to perform various function such as current and voltage monitoring or remote temperature detection.

The TPSI3100-Q1 also integrates a communication back channel that transfers status information from the secondary side to the primary side. When the comparator input FLT1_CMP exceeds the voltage reference, the driver is immediately asserted low and FLT1 is also driven low, indicating to the system that a fault has occurred. This is useful for disabling the external switch with low latency on critical events, such as overcurrent detection. When the comparator input, ALM1_CMP, exceeds the voltage reference, ALM1 signal is asserted low, but no action is taken by the driver. This can be useful as an alarm or warning indicator for overtemperature or overvoltage events.

In this design, a 5V supply powers the primary side pins VDDP and CE with 1100nF input capacitance. An external 5V signal is tied to the EN pin. The signal pins PGOOD, nFLT, and nALM are tied to a pull-up network. Lastly, the VSSP pins are tied to ground together.

On the secondary side, the capacitors between VDDH and VDDM, VDDM and VSSS, named $C_{DIV1}$ and $C_{DIV2}$, respectively, are chosen to maintain a ratio of 1:3, or in other words $C_{DIV2} = 3 \times C_{DIV1}$. The current-sense amplifier of the overcurrent detection circuit is powered from the VDDM pin. The RESP pin is tied to VSSS with a 100kΩ resistor and FLM1_CMP and ALM1_CMP pins are tied to the resistor divider of the overcurrent detection circuit.

### 2.3.2 INA180-Q1

The INA180-Q1 current-sense amplifier is designed for cost-optimized applications. These devices are part of a family of current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common mode voltages from –0.2V to +26V, independent of the supply voltage. The INA180-Q1 integrates a matched resistor gain network in four, fixed-gain device options: 20V/V, 50V/V, 100V/V, or 200V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

For this design, the selected gain of the INA180-Q1 is 20V/V and is powered from the VDDM pin of the TPSI3100-Q1 with a 100nF input capacitance. The output of this device serves as the alarm signal for the overcurrent detection circuit and feeds the resistor divider for the fault signal. Any comparable current-sense amplifier can be used.

### 2.3.3 TPSI2140-Q1

The TPSI2140-Q1 is an isolated solid-state relay designed for high-voltage automotive and industrial applications. The TPSI2140-Q1 uses TI's high-reliability capacitive isolation technology in combination with internal back-to-back metal-oxide semiconductor field-effect transistors (MOSFET) to form a completely-integrated design requiring no secondary-side power supply.

In this design, the TPSI2140-Q1 is used as an isolated switch for discharging the capacitors after the precharge cycle. The switch is placed in series with a high-ohmic resistor to provide a low-power discharge that takes around two minutes to reach a safe voltage level of less than 60V.

## 3 Hardware, Software, Testing Requirements, and Test Results

### 3.1 Hardware Requirements

Figure 3-1 represents the tested design.

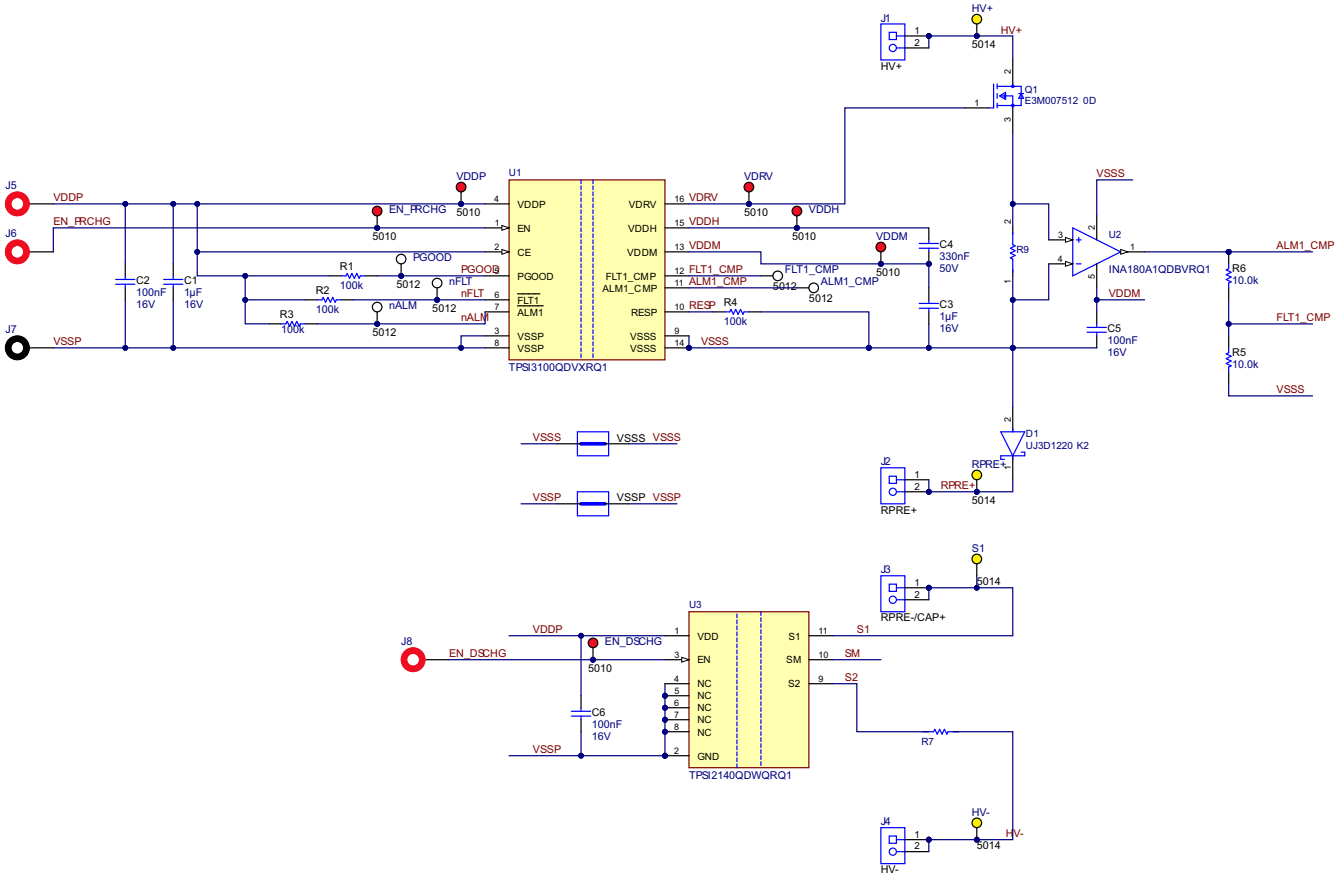


**Figure 3-1. Reference Design Schematic**

Figure 3-2 is the final PCB which measures 140mm × 100mm and is about 55mm in height.

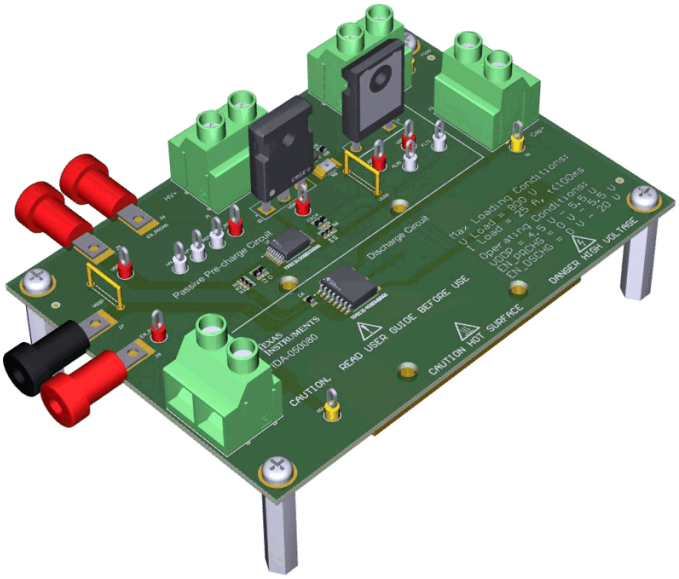


**Figure 3-2. Reference Design Board**

### *3.1.1 External Hardware Requirements*

The list of required external hardware follows:

1. High-voltage enclosure
2. Power supply
   a. 5V DC power source
   b. High-voltage power supply capable of at least 800V, 25A, preferably 1000V, 30A
3. Oscilloscope
4. Isolated probes
5. External load resistor about 50Ω
6. External capacitor bank about 2mF

## 3.2 Test Setup

To test the normal operation of the passive precharge reference design, implement the following steps:

1. Connect a 5V power supply to the banana jacks of the VDDP, EN_PRCHG, and EN_DSCHG, with the negative lead connected to VSSP.
2. Before placing in the enclosure or connecting the high-voltage power supply, power the TPSI3100-Q1 and verify all voltages on the primary and secondary side are as expected.
3. Perform *step 2* with TPSI2140-Q1 verifying the internal FETs are on through measuring the resistance between S1 and S2.
4. Turn off the 5V power supplies leaving the cables attached.
5. Placing the board in the enclosure, attach one lead of the precharge resistor to J2 and the other lead to J3.
6. Attach the positive terminal of the capacitor to J3 and the negative terminal to J4.
7. Attach the high-voltage power supply positive lead to J1 and the negative to J4.
8. Connect an isolated probe to S1-HV_ to measure the voltage across the capacitor as the capacitor charges.
9. Connect an isolated probe to VDRV-VSSS to show the step of the drive pin.
10. Close the enclosure and energize the high-voltage power supply.
11. Power the 5V supply and observe the cycle, powering the supply off after a second.
12. Turn off the high-voltage supply
13. Power the 5V supply again to energize EN_DSCHG to discharge the capacitor
    a. *Wait at least 2 minutes* before opening the high-voltage enclosure.
    b. If the power supply has the ability to show a constant read of the capacitor voltage, this can be used to show the progress of the discharge cycle

## 3.3 Test Results

Figure 3-3 shows a typical precharge cycle and Figure 3-4 a discharge cycle.

- VDRV is the drive pin on the secondary side of TPSI3100-Q1
- VCAP is the voltage across the capacitor bank
- EN_DSHCG is the enable signal for the TPSI2140-Q1

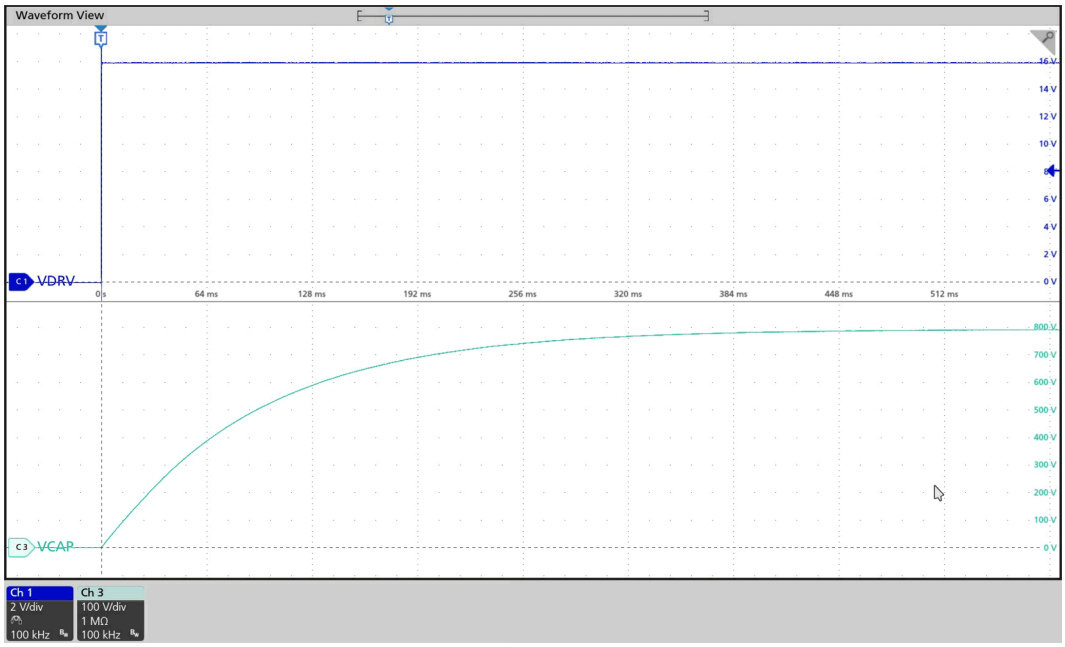


**Figure 3-3. Precharge Cycle**

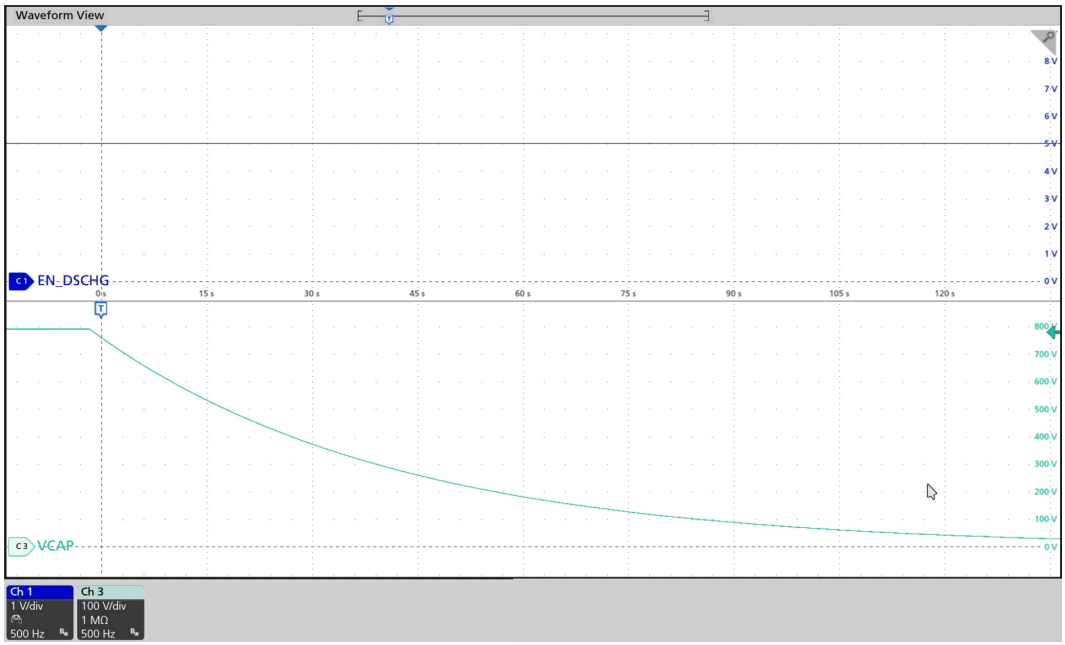


**Figure 3-4. Discharge Cycle**

Figure 3-5 shows the VDRV pin disabling after the current has exceeded the 25A limit. After the auto-recovery period has passed, the drive pin re-asserts. Similarly, in Figure 3-6, the nFLT pin on the primary side reports the fault by pulling down after 30µs passes. This pin is pulled back up after another 30µs passes.

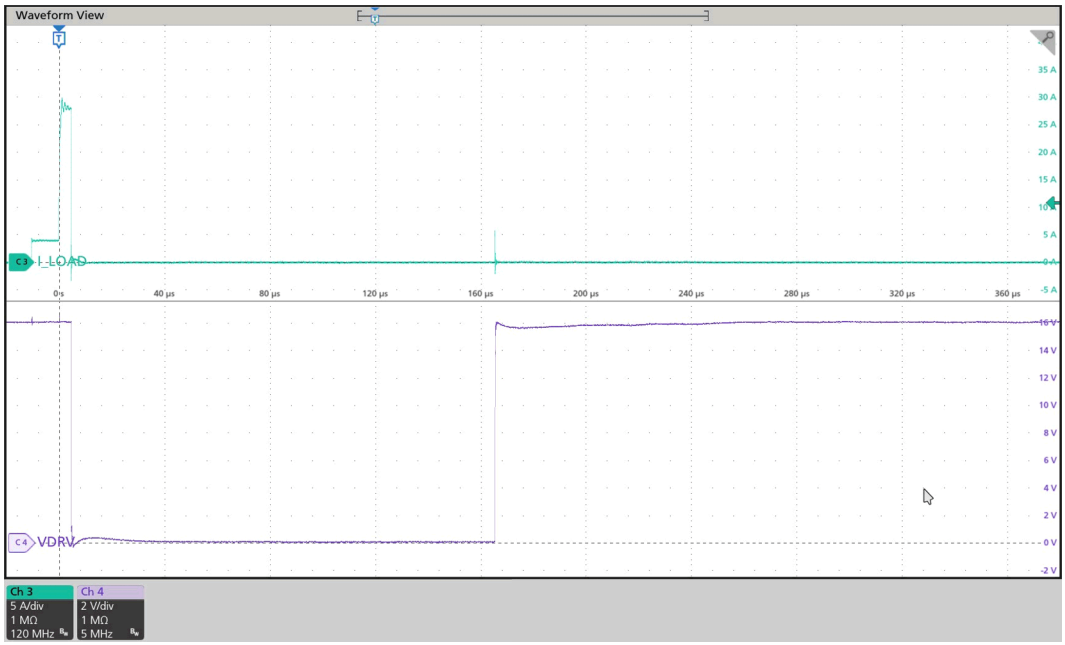


**Figure 3-5. VDRV Disable and Re-enable**

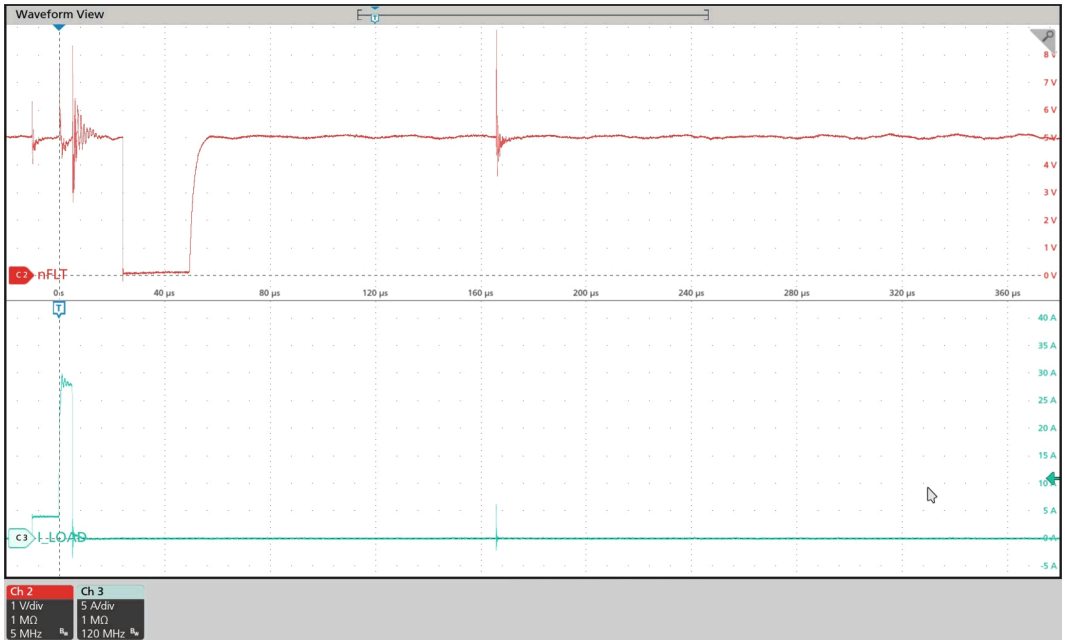


**Figure 3-6. Primary Side Fault Reporting**

# 4 Design and Documentation Support

## 4.1 Design Files

### 4.1.1 Schematics

To download the schematics, see the design files at TIDA-050080.

### 4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050080.

## 4.2 Tools

**Tools**

| | |
|---|---|
| PSPICE-FOR-TI | PSpice® for TI design and simulation tool: PSpice® for TI is a design and simulation environment that helps evaluate functionality of analog circuits. This full-featured, design and simulation suite uses an analog analysis engine from Cadence®. Available at no cost, PSpice for TI includes one of the largest model libraries in the industry, spanning our analog and power portfolio, as well as select analog behavioral models. |

## 4.3 Documentation Support


1. Texas Instruments, *Why Pre-Charge Circuits are Necessary in High-Voltage Systems Application Brief*
2. Texas Instruments, *TPSI2140-Q1 1200-V, 50-mA, Automotive Isolated Switch With 2-mA Avalanche Rating Data Sheet*
3. Texas Instruments, *TPSI3100-Q1 Automotive Reinforced Isolated Switch Driver With 15-V Gate Supply and Dual Isolated Comparators Data Sheet*
4. Texas Instruments, *INAx180-Q1 Automotive, Low- and High-Side Voltage Output, Current-Sense Amplifiers Data Sheet*


## 4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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# 5 About the Author

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