Design Guide: TIDA-020069

Automotive High-Voltage Interlock Loop (HVIL) Reference Design

Description

In hybrid or electric vehicles (HEV, EVs), battery management systems, traction inverters, DC-DC converters, onboard chargers, and other subsystems that operate at high voltages need to have a high-voltage interlock loop (HVIL). HVIL is a low-voltage, low-current loop that monitors the physical state of the connectors. HVIL determines if connectors and wires are in a closed connection, open connection, short-to-battery fault, or short-to-ground fault. This HVIL fault signal is reported to safety logic in the vehicle to put high-voltage circuitry into a safe state. This design covers the generating and monitoring mechanism of the HVIL system.

Resources

TIDA-020069	Design Folder
TLV9002-Q1, TLV9034-Q1	Product Folder
TPS7B69-Q1, SN74HCS08-Q1	Product Folder
SN74HCS86-Q1	Product Folder

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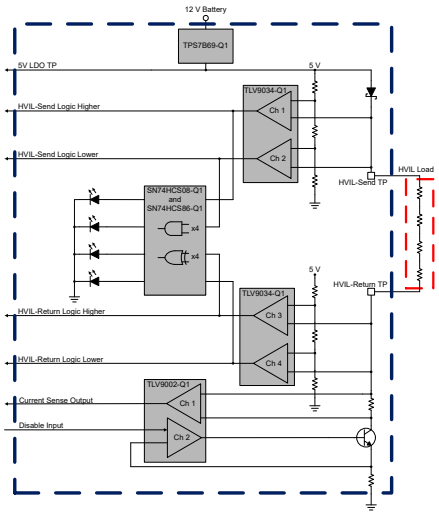
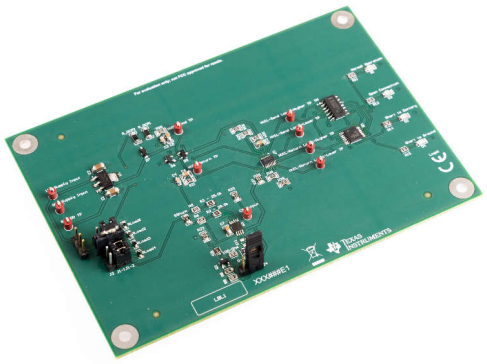
Features

- Wide coverage of interlock loop fault diagnosis with LED indication:
  - Closed connection (normal operation)
  - Open connection
  - Short to battery
  - Short to ground
- Configurable constant current generation
- Analog or digital output signal options
- Adjustable thresholds for fault state monitoring
- Unidirectional interlock system

Applications

- HEV, EV battery-management system (BMS)
- HEV, EV OBC and DC/DC converter
- HEV, EV inverter and motor control





1 System Description

High voltage interlock loop (HVIL) is a safety feature within hybrid or electric vehicles (HEV, EVs) that protects people that come in contact with the connectors to the high voltage battery during normal operation, maintenance, or repair. The HVIL system monitors the integrity of the physical connection of the cables between the high voltage battery and various subsystems throughout the vehicle. The HVIL system indicates which of the following states the high voltage connectors are in: closed connection (normal operation), open connection (an intentional battery disconnect during maintenance or unintentional disconnect due to a faulty connection), short to battery, or short to ground states.

HVIL connectors are designed in a way that keeps the HVIL signal circuit independent of the high voltage power delivery circuit. As the connector is unplugged, the HVIL signal circuit opens before the high voltage power delivery. The HVIL circuitry alerts the battery management system (BMS) of an open connection and allows the BMS to immediately shut off the high voltage power to prevent arcing during disconnect. This also protects against a floating high voltage for a loose wire.

This working principle of an HVIL system consists of a low voltage, constant current signal that independently runs through the cable between the high voltage battery and subsystem. The HVIL design consists of a constant current generator, a current sensing block, the load connectors and clamps, a modified window comparator, and digital logic gates. The design and implementation of each of these blocks is detailed throughout this reference design.

In addition to automotive systems, HVIL is also implemented in various industrial applications that operate with high voltages, such as heavy machinery factory installations, high-voltage smart grids, and relevant applications where there are heavy electrical installations or setups. HVIL is used to avoid damage to a person and equipment when the system is under use.

As Figure 1-1 shows, multiple subsystems can be connected in to the HVIL circuitry in series. In the example image, the traction inverter, DC-DC converters, and onboard charger all operate at a high voltage and need to have an interlock loop. Alternatively, these subsystems can each have a unique HVIL circuitry that is only connected to one subsystem at a time.

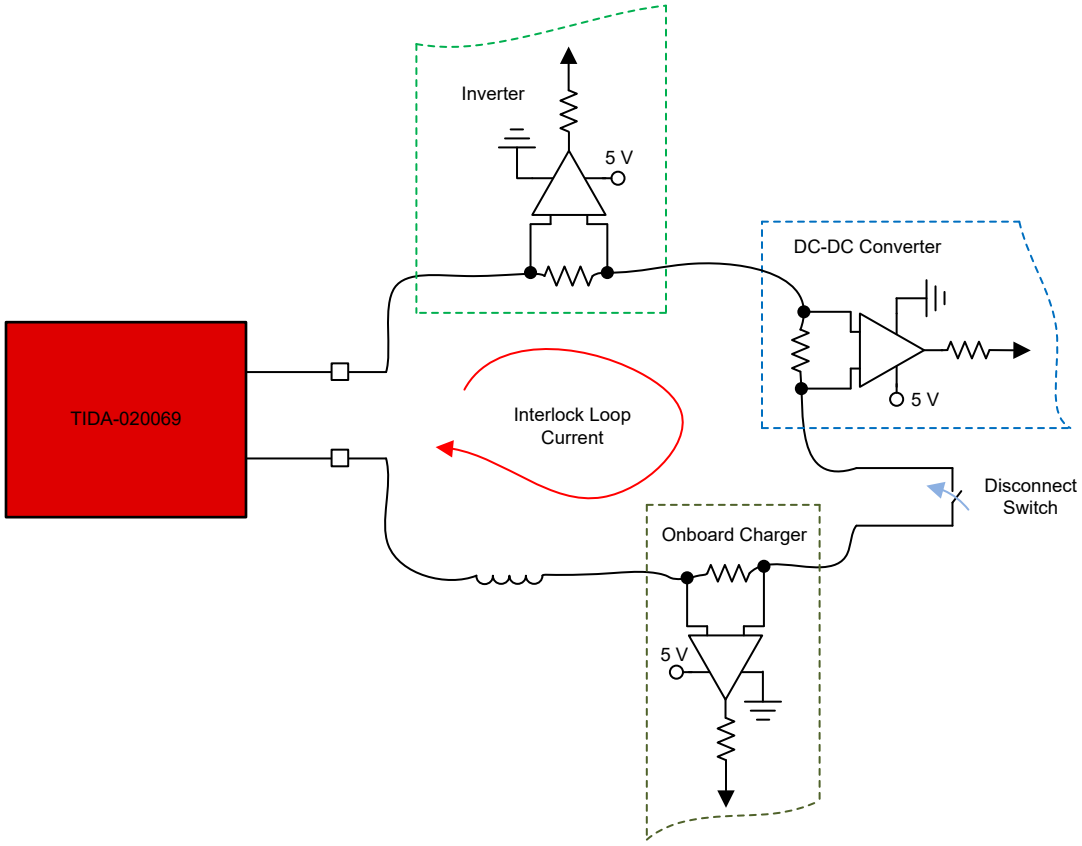


Figure 1-1. Typical Interlock System

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	CONDITIONS	TYP	UNIT
Input voltage	DC battery voltage	12	V
Interlock voltage	LDO voltage output for loop	5	V
Interlock loop current	Constant current generated by HVIL (configurable)	10	mA
Load Resistance	Expected load resistance of four high-voltage connectors	200	Ω
Short to ground current	Expected current for short to ground	15–45	mA
Short to battery current	Expected current for short to battery	15–25	mA
Disable current	Expected current when in DISABLE mode	< 1	mA

2 System Overview

2.1 Block Diagram

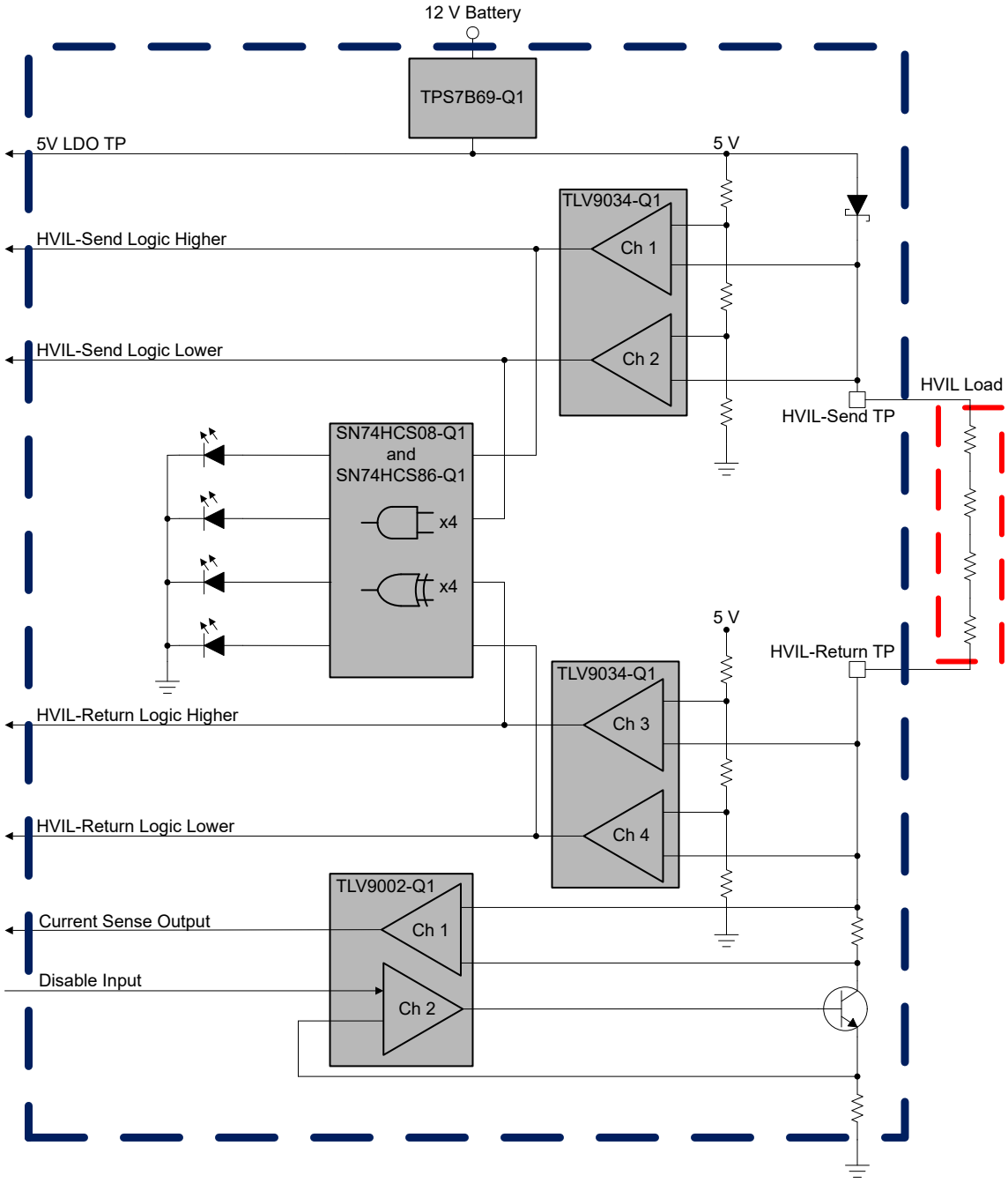


Figure 2-1. TIDA-01445 Block Diagram

2.2 Highlighted Products

2.2.1 TLV9002-Q1

The TLV900x-Q1 family includes single (TLV9001-Q1), dual (TLV9002-Q1), and quad-channel (TLV9004-Q1) low-voltage (1.8V to 5.5V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective answer for space-constrained automotive applications such as Infotainment and lighting where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900x-Q1 family is 500pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8V to 5.5V) with performance specifications similar to the TLV600x-Q1 devices.

The robust design of the TLV900x-Q1 family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

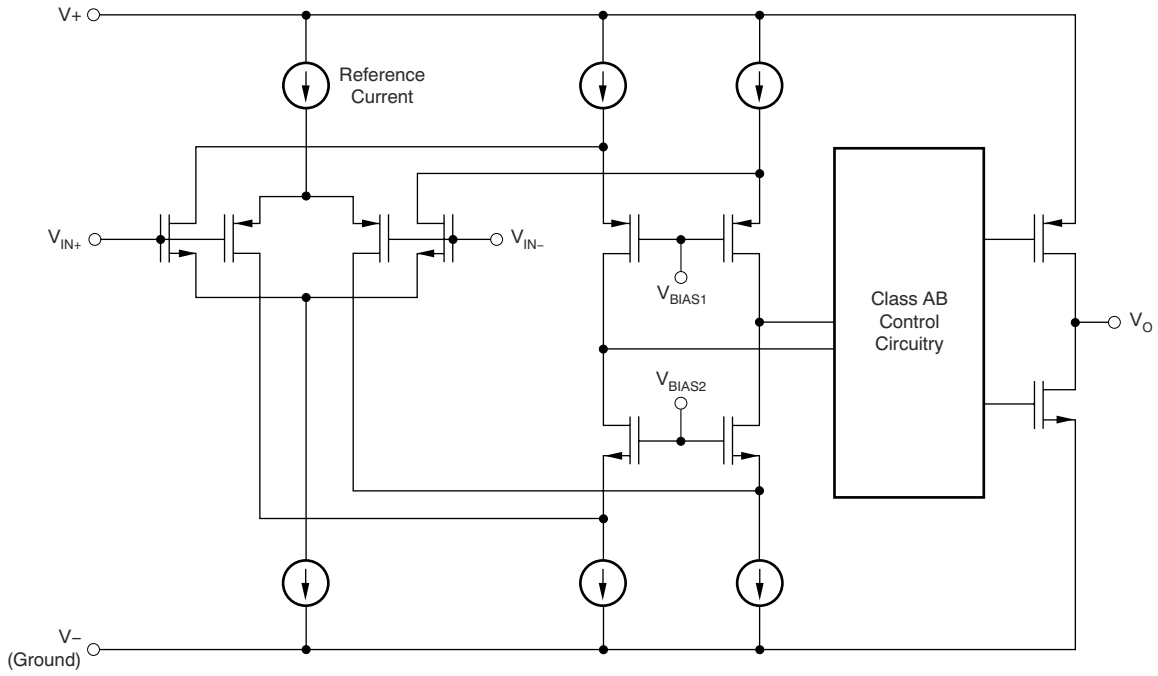


Figure 2-2. TLV9002-Q1 Block Diagram

Key features of the TLV9002-Q1 include:

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to 125°C, T_A
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- Scalable CMOS amplifier for low-cost applications
- Rail-to-rail input and output
- Low input offset voltage: ±0.4mV
- Unity-gain bandwidth: 1MHz
- Low broadband noise: 27nV/$\sqrt{\text{Hz}}$
- Low input bias current: 5pA
- Low quiescent current: 60µA/Ch
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Functional Safety-Capable

2.2.2 TLV9034-Q1

The TLV903x-Q1 are a family of automotive grade dual- and quad-channel comparators. The family offers low input offset voltage, fault-tolerant inputs and a excellent speed-to-power combination with a propagation delay of 100ns with a quiescent supply current of only 18µA per channel.

The family also includes a Power-on Reset (POR) feature that makes sure the output is in a known state until the minimum supply voltage is reached to prevent output transients during system power-up and power-down. These comparators also feature fault-tolerant inputs that can go up to 6V without damage with no output phase inversion. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

The TLV903x-Q1 have a push-pull output stage capable of sinking and sourcing many milliamps of current to drive LEDs or a capacitive load such as a MOSFET gate. The family is specified for the automotive temperature range of –40°C to 125°C and are available in a standard leaded and leadless packages.

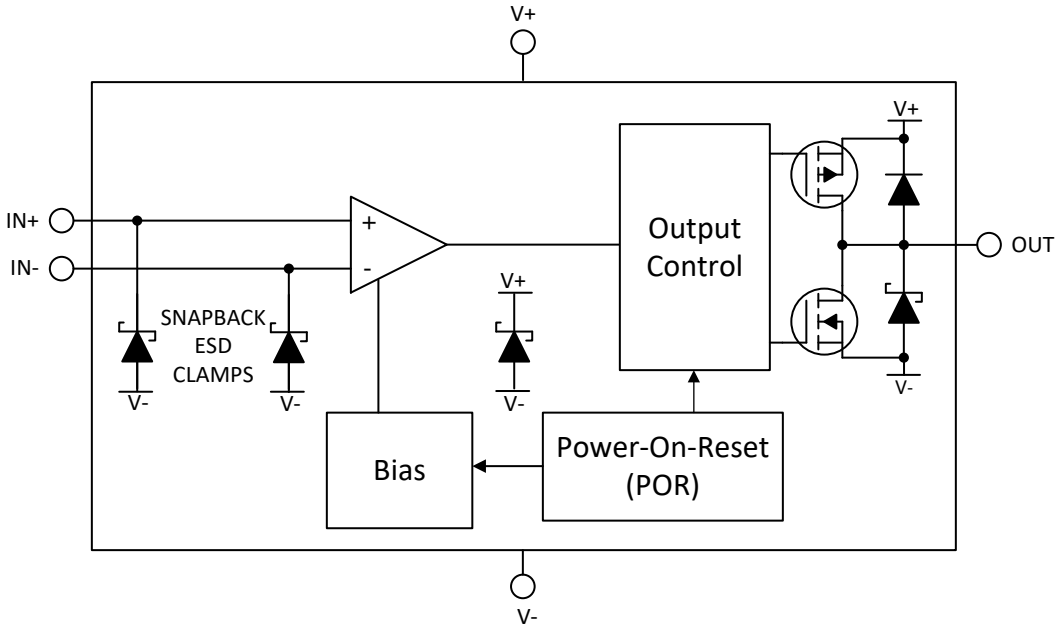


Figure 2-3. TLV9034-Q1 Block Diagram

Key features of the TLV9034-Q1 include:

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- 1.65V to 5.5V supply range
- Power-On Reset (POR) for known start-up
- Precision input offset voltage 300V
- 100ns typical propagation delay
- Low quiescent current 16 per channel
- Rail-to-Rail input voltage range exceeds the rails
- Open-drain output option (TLV902x-Q1)
- Push-pull output option (TLV903x-Q1)
- Alternate single pinout option (TLV90x0)
- 2V ESD protection

2.2.3 TPS7B69-Q1

The TPS7B69xx-Q1 device is a low-dropout linear regulator designed for up to 40V V_I operations. With only 15µA (typical) quiescent current at light load, the device is designed for standby microcontrol-unit systems especially in automotive applications.

The devices feature an integrated short-circuit and overcurrent protection. The TPS7B69xx-Q1 device operates over a –40°C to 125°C temperature range. Because of these features, the TPS7B6925-Q1, TPS7B6933-Q1, and TPS7B6950-Q1 devices are designed for power supplies for various automotive applications.

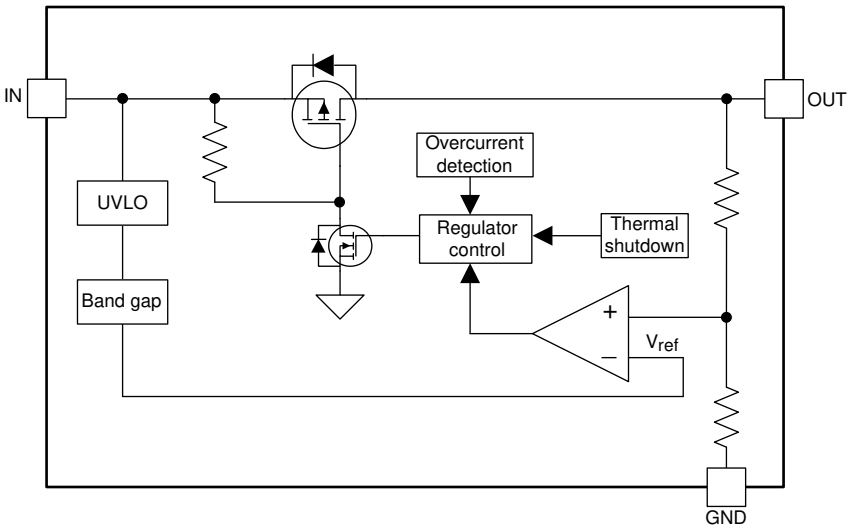


Figure 2-4. TPS7B69-Q1 Block Diagram

Key features of the TPS7B69-Q1 include:

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 4V to 40V wide V_I input voltage range with up to 45V transient
- Maximum output current: 150mA
- Low quiescent current (I_Q):
  - 15µA typical at light loads
  - 25µA maximum under full temperature
- 450mV typical low dropout voltage at 100mA load current
- Stable with low ESR ceramic output capacitor:
  - 2.2µF to 100µF
- Fixed 2.5V, 3.3V, and 5V output voltage options
- Integrated fault protection:
  - Thermal shutdown
  - Short-circuit protection
- Packages
  - 4-pin SOT-223 package
  - 5-pin SOT-23 package

2.2.4 SN74HCS08-Q1

SN74HCS08-Q1 contains four independent 2-input AND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A × B in positive logic.

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. Leave unused push-pull CMOS outputs disconnected.

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance. The Schmitt-trigger input architecture provides hysteresis, which makes this device extremely tolerant to slow or noisy inputs.

The inputs and outputs to this device have both positive and negative clamping diodes.

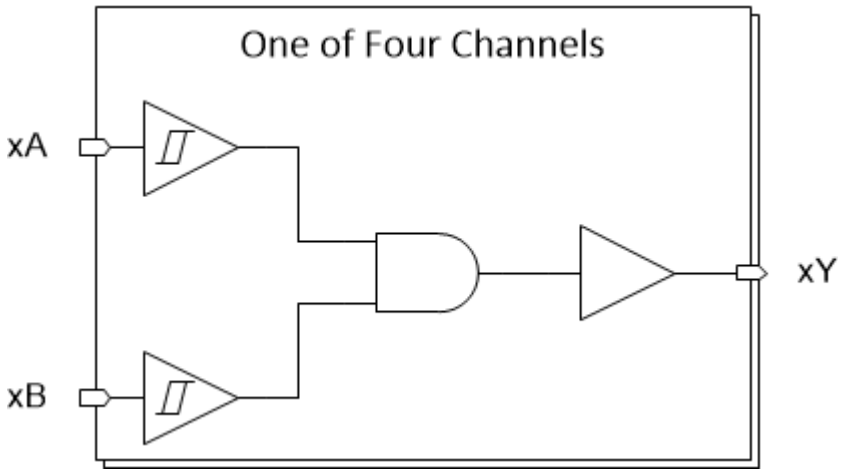


Figure 2-5. SN74HCS08-Q1 Block Diagram

Key features of the SN74HCS08-Q1 include:

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Wide operating voltage range: 2V to 6V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100nA
  - Typical input leakage current of ±100nA
- ±7.8mA output drive at 6V

2.2.5 SN74HCS86-Q1

SN74HCS08-Q1 contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A × B in positive logic.

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. Leave unused push-pull CMOS outputs disconnected.

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance. The Schmitt-trigger input architecture provides hysteresis, which makes this device extremely tolerant to slow or noisy inputs.

The inputs and outputs to this device have both positive and negative clamping diodes.

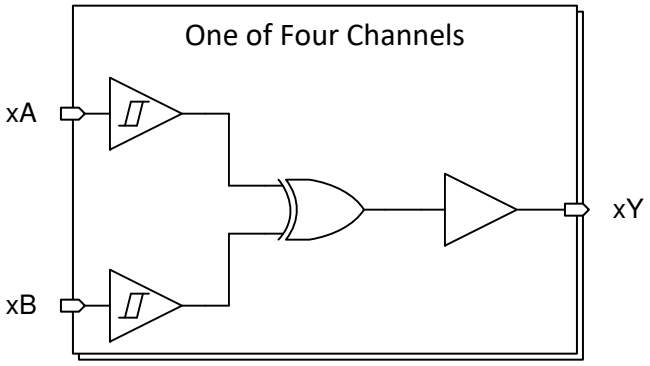


Figure 2-6. SN74HCS86-Q1 Block Diagram

Key features of the SN74HCS86-Q1 include:

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to 125°C, T_A
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- Wide operating voltage range: 2V to 6V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{cc} of 100nA
  - Typical input leakage current of ±100nA
- ±7.8mA output drive at 6V

2.3 System Design Theory

The interlock system design is based on OEM requirements. This reference design can handle most user requirements with the given topology and diagnosis requirements. The topology of the reference design can be easily tweaked to get the required performance of an interlock system. As Figure 1-1 shows, interlock is interfaced to every high-voltage component. The interlock signal is mostly generated and closely monitored by the battery because this source of power can quickly turn off the high-voltage power contactors.

2.3.1 TIDA-0020069 Operation

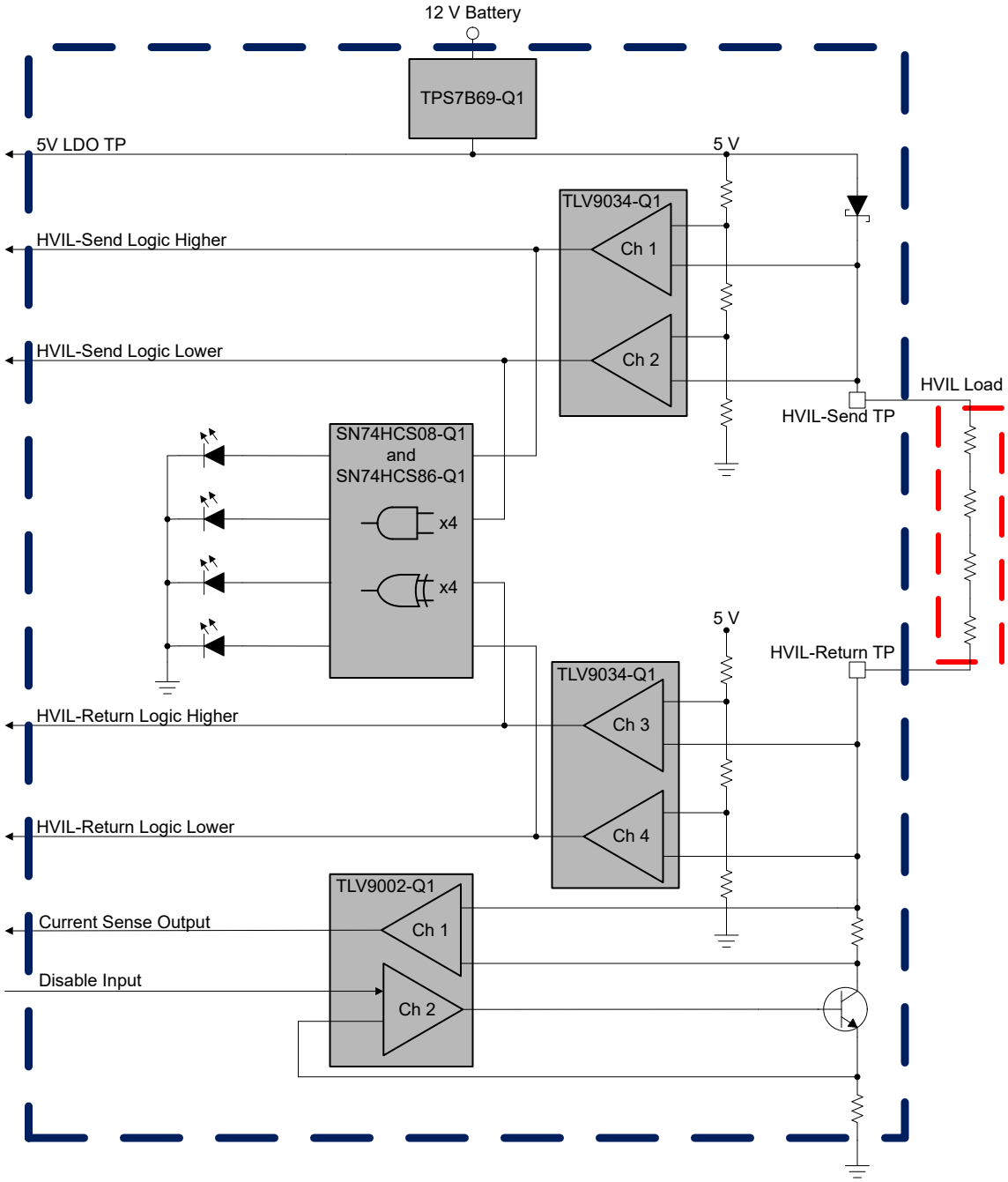


Figure 2-7. Functional Block Diagram

As Figure 2-7 shows, the TPS7B69-Q1 low-dropout (LDO) voltage regulator is used to step down the supply voltage from the 12V battery to 5V. All other components throughout the signal chain, including the HVIL signal, operate from this 5V rail.

The TLV9002-Q1 operational amplifier (op amp) is used to generate a constant current output for the HVIL signal chain. This is shown as the output of Ch 2 in Figure 2-7. The value of this constant current can be configured by varying the passive components, as shown in Section 2.3.1.1. This constant current flows through the HVIL signal cable within the high-voltage connectors. The resistance of the high-voltage connectors and HVIL cable are used to calculate the expected voltage drop between the *HVIL-Send TP* and *HVIL-Return TP* test points.

This constant current output of the amplifier can also be disabled using the *Disable Input* logic signal. When disabled, the output current of the amplifier decreases by a factor of 100. This creates a fault condition similar to the short-to-battery fault, where the voltage difference between the *HVIL-Send TP* and *HVIL-Return TP* is minimal. This disable feature can be used to save on power, and to force an error reading on the output until all other systems are ready for HVIL measurements. Other amplifiers like TLV9061-Q1 and OPA310-Q1, feature integrated shutdown functionality via an extra pin controlled by a logic input, which can also be utilized in place of the TLV9002-Q1.

The other channel of the TLV9002-Q1 op amp is used for current sensing. This channel is configured as a difference amplifier across a shunt resistor placed in series with the load resistors. Under normal operation (closed connection of all high-voltage connectors), the output of this amplifier is set to mid-supply. During open connection (disconnect of high-voltage cables), the current through the shunt resistor is zero and the amplifier outputs 0V. This amplifier also outputs lower voltages during the two fault conditions of short-to-battery and short-to-ground. This current sensing provides feedback and redundancy.

The analog values of *HVIL-Send TP* and *HVIL-Return TP* can be output to a microprocessor with integrated analog-to-digital converters (ADC) to determine the HVIL states. However, this design simplifies computation efforts by converting these two analog values into four binary values. The TLV9034-Q1 is a quad-channel comparator that is used to convert the two analog values, *HVIL-Send TP* and *HVIL-Return TP*, into two 2-bit binary values. A modified window comparator circuit, detailed in Section 2.3.1.4, compares the *HVIL-Send TP* and *HVIL-Return TP* against *Upper Threshold* and *Lower Threshold* to generate 2-bit binary outputs. The four binary outputs from the modified window comparators are called *HVIL-Send Logic-Higher*, *HVIL-Send Logic-Lower*, *HVIL-Return Logic-Higher*, and *HVIL-Return Logic-Lower*. The voltage thresholds for the window comparator are set using resistor dividers and can be configured per design requirements.

The 2-bit binary output of each modified window comparator can be determined using the logic in Table 2-1 and Table 2-2.

Table 2-1. HVIL-Send Binary Output Logic

PARAMETER	HVIL-SEND LOGIC-LOWER TP	HVIL-SEND LOGIC-HIGHER TP
HVIL-Send TP < Lower Threshold	0V	0V
Lower Threshold < HVIL-Send TP < Upper Threshold	5V	0V
HVIL-Send TP > Upper Threshold	5V	5V

Table 2-2. HVIL-Return Binary Output Logic

PARAMETER	HVIL-RETURN LOGIC-LOWER TP	HVIL-RETURN LOGIC-HIGHER TP
HVIL-Return TP < Lower Threshold	0V	0V
Lower Threshold < HVIL-Return TP < Upper Threshold	5V	0V
HVIL-Return TP > Upper Threshold	5V	5V

Figure 2-8 illustrates the expected values for *HVIL-Send* and *HVIL-Return* with respect to the *Upper Threshold* and *Lower Threshold* for each of the four states. Each state has a unique placement for the *HVIL-Send* and *HVIL-Return*.

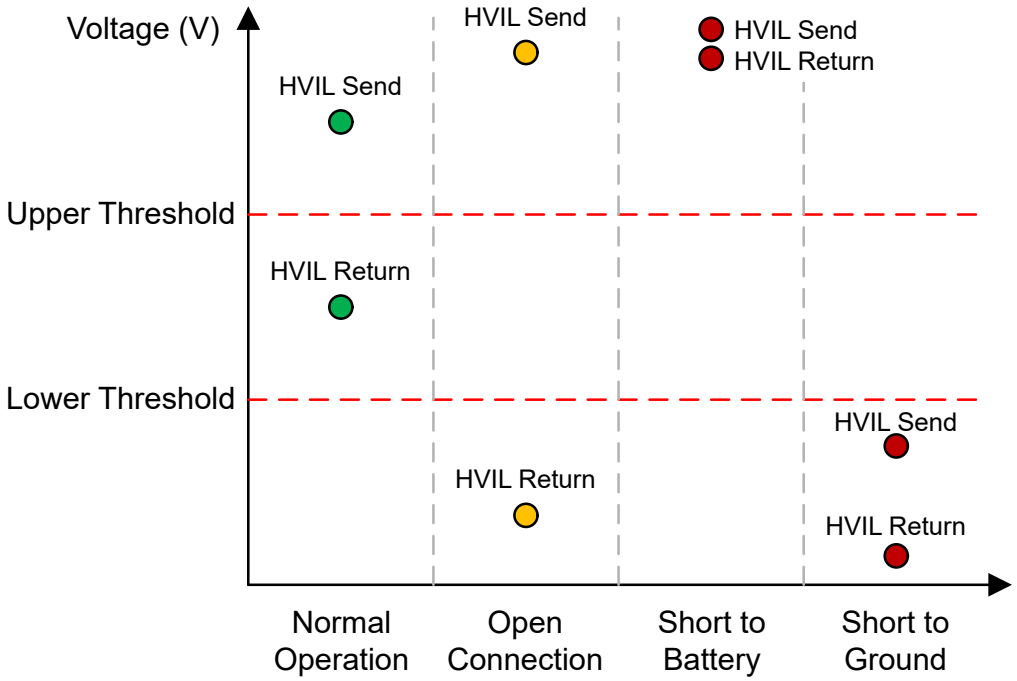


Figure 2-8. TIDA-020069 State Logic Thresholds

The SN74HCS08-Q1 AND gates and SN74HCS86-Q1 XOR gates are used to control the LED status indicators on the board based on the binary outputs from the modified window comparator (*HVIL-Send Logic-Higher*, *HVIL-Send Logic-Lower*, *HVIL-Return Logic-Higher*, and *HVIL-Return Logic-Lower*). Section 2.3.1.5 details the logic tree. Only one status LED indicator is on at a time, and follows Figure 2-8.

2.3.1.1 Constant Current Source

A key criteria of an automotive HVIL design is the generation of a constant current. This current is generated by the HVIL circuitry and flows through the interlock signal cables, through all of the high-voltage connectors, and returns back to the HVIL circuitry. Many automotive OEMs have varying requirements for the HVIL constant current, typically ranging from 5mA–30mA of constant current. A benefit to this reference design is the ability to adjust the current output based on discrete components.

The schematic in Figure 2-9 features the TLV9002-Q1, using one channel to generate a constant HVIL current. This circuit design is based on the Analog Engineer's Circuit: Voltage-to-current (V-I) converter circuit with BJT. Reference this analog circuit design for more details about the circuit, including downloadable simulation models.

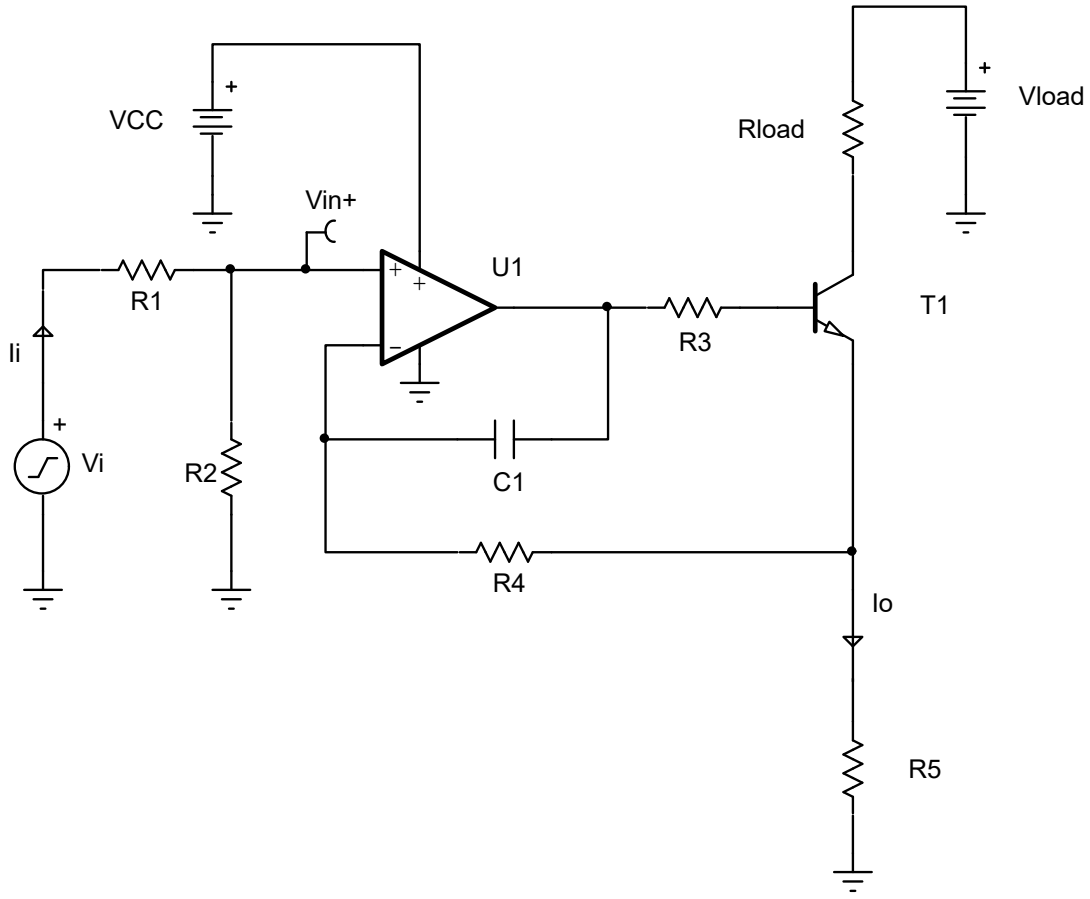


Figure 2-9. Constant Current Source Circuit

2.3.1.1.1 Design Goals

Input	Output	Supply		
V_i	I_o	V_{cc}	V_{ee}	V_{load}
5V	10mA	5V	0V	5V

2.3.1.1.2 Design Description

This low-side voltage-to-current (V-I) converter delivers a well-regulated current to the HVIL load. The circuit uses a resistor divider to step down the 5V supply voltage generated by the TPA7B69-Q1 and converts this voltage to a current of 10mA. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor (R_5) to the op amp. This current is independent of the load resistance or load supply voltage and can be modified to another desired current level by following the *Design Steps*.

2.3.1.1.3 Design Notes

1. Resistor divider (R1 and R2) is implemented to limit the maximum voltage at the non-inverting input, V_{in+}, and sense resistor, R_5, at full-scale.
2. For an op amp that is not rail-to-rail input (RRI), a voltage divider is needed to reduce the input voltage to be within the common-mode voltage of the op amp.
3. Use low resistance values for R_5 to maximize load compliance voltage and reduce the power dissipated at full-scale.
4. Using a high-gain BJT reduces the output current requirement for the op amp.
5. Feedback components R_3, R_4, and C_1 provide compensation to improve stability. R_3 isolates the input capacitance of the bipolar junction transistor (BJT), R_4 provides a DC feedback path directly at the current-setting resistor (R_5), and C_1 provides a high-frequency feedback path that bypasses the BJT.
6. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions in the device data sheet.

2.3.1.1.4 Design Steps

The transfer function of the circuit is:

$$\mathrm{Io} = \frac{\mathrm{R_2}}{\mathrm{R_5} \times (\mathrm{R_1} + \mathrm{R_2})} \times \mathrm{Vi} \tag{1}$$

1. Select resistors, R_1 and R_2, for the voltage divider at the input. These resistors are sized so that the common-mode input voltage seen at the amplifier non-inverting input terminal, V_i is less than the *Lower Threshold* voltage set in the Section 2.3.1.4 section. In the case of this design, the *Lower Threshold* was set to be 1.33V, so the value of V_i is set to 1V.

$$\mathrm{V_{in+}} = \mathrm{V_i} \times \left(\frac{\mathrm{R_2}}{\mathrm{R_1} + \mathrm{R_2}}\right) \tag{2}$$

$$\text{Let } \mathrm{R_1} = 10\mathrm{k\Omega}\left(\text{Standard value}\right),\ \frac{\mathrm{R_2}}{10\mathrm{k\Omega} + \mathrm{R_2}} = \frac{1\mathrm{V}}{5\mathrm{V}} \tag{3}$$

$$\mathrm{R_2} = 4 \times \mathrm{R_1} = 40\mathrm{k\Omega} \tag{4}$$

2. Calculate the sense resistor, R_5. Keeping the sense resistor sized as small as possible maximizes the load compliance voltage and reduces power dissipation. Set the voltage across the sense resistor to 1V. Limiting the voltage drop to 1V limits the power dissipated in the sense resistor to 100mW at full-scale output.

$$\text{Let } \mathrm{V_{in+}} = 1\mathrm{V} \text{ and } \mathrm{I_O} = 10\mathrm{mA}\ \mathrm{R_5} = \frac{\mathrm{V_{in+}}}{\mathrm{I_O}} = \frac{1\mathrm{V}}{10\mathrm{mA}} = 100\Omega \tag{5}$$

3. Refer to TI Precision Labs for the design procedure on how to properly size the compensation components, R_3, R_4, and C_1.

2.3.1.2 Current Sensing

Current sensing is a critical element for automotive HVIL designs. In the past, current sensing was the primary mode of detecting a closed connection in the HVIL loop compared to an open connection. Measuring current across a shunt resistor indicates a closed connection where current is flowing. Conversely, a lack of current indicates an open connection during a battery disconnect scenario. However, a design that only relies on current sensing does not account for fault conditions when a short occurs throughout the load. For example, when the *HVIL-Send* and *HVIL-Return* pins are shorted together, current flows across the current sensing shunt resistor regardless of whether the load is closed (normal operation) or open (battery disconnect). This is why it is important to account for the voltage values of *HVIL-Send* and *HVIL-Return* by measuring these voltages and comparing against predetermined thresholds. For this reference design, the current sensing circuitry provides redundancy to improve the overall safety of the system. The output voltage of the current sensing circuitry can also be used as feedback to the constant current generation for precision designs that require accurate, regulated HVIL currents.

This design features a high-side current sensing circuit with respect to the constant current sink generator. The shunt resistor is placed between the *HVIL-Return* signal and collector of the BJT in the constant current generator circuit. One channel of the TLV9002-Q1 is configured as a difference amplifier across the shunt resistor.

The schematic Figure 2-10 features the TLV9002-Q1, using one channel to measure the HVIL current. The circuit design is based on the Analog Engineer's Circuit: High-Side Current-Sensing Circuit Design. Reference this analog circuit design for more details about the circuit, including downloadable simulation models.

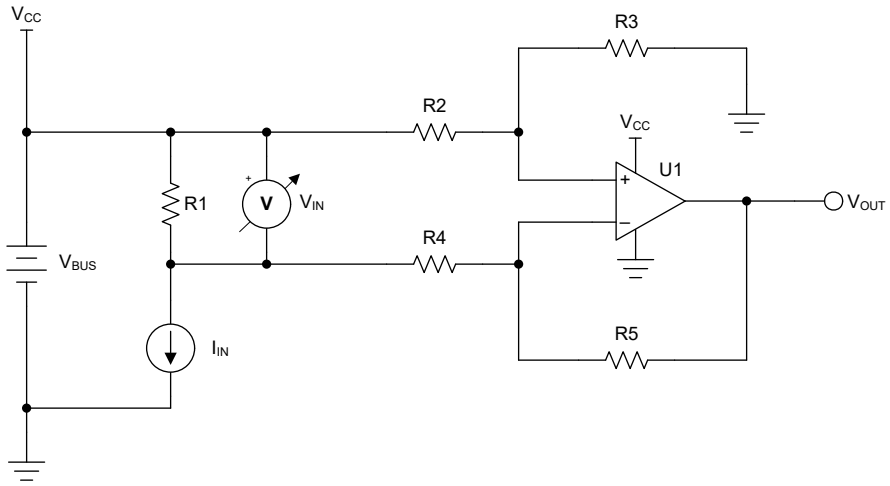


Figure 2-10. High-Side Current Sensing Circuit

2.3.1.2.1 Design Goals

Input	Output	Supply	
I_{IN}	V_{OUT}	V_{CC}	V_{EE}
10mA	2.5V	5V	0V

2.3.1.2.2 Design Description

This single-supply, high-side current sensing circuit detects a load current of 10mA and converts the current to an output voltage of 2.5V. High–side sensing allows for the system to identify ground shorts and does not create a ground disturbance on the load.

2.3.1.2.3 Design Steps

1. The full transfer function of the circuit is provided below.

$$V_o = I_{in} \times R_1 \times \frac{R_5}{R_4}$$

$$\text{Given} \quad R_2 = R_4 \quad \text{and} \quad R_3 = R_5$$

2. Calculate the shunt resistance. Set the voltage across the shunt to 100mV.

$$R_1 = \frac{V_{IN}}{I_{IN}} = \frac{100\text{mV}}{10\text{mA}} = 10\Omega \tag{6}$$

3. Calculate the gain to set the output voltage to 2.5V (mid-supply).

$$\text{Gain} = \frac{V_{OUT}}{I_{IN} \times R_1} = \frac{2.5\text{V}}{10\text{mA} \times 10\Omega} = 25\frac{\text{V}}{\text{V}} \tag{7}$$

4. Calculate the gain setting resistors to set the gain calculated in step 3.

$$\text{Choose } R_2 = R_4 = 1\text{k}\Omega \text{ (Standard value) } R_3 = R_5 = R_2 \times \text{Gain} = 1\text{k}\Omega \times 25\frac{\text{V}}{\text{V}} = 25\text{k}\Omega \tag{8}$$

2.3.1.3 Load Connections and Clamps

The TIDA-020069 utilized clamping diodes to prevent overvoltage and undervoltage conditions, as shown in Figure 2-11. The diodes labeled *D2*, *D3*, *D4*, and *D5* clamp the *HVIL-Send* and *HVIL-Return* voltages to either ground or V_{CC}. In this scenario, V_{CC} is the 5V signal generated by TPS7B69-Q1, not the 12V supply input voltage. These diodes protect the interlock current loop from exceeding 5V or ground in case of a short-to-battery or short-to-ground fault condition. These clamping diodes also protect any downstream devices, like an ADC or microcontroller, that can be connected directly to the *HVIL-Send* and *HVIL-Return* pins.

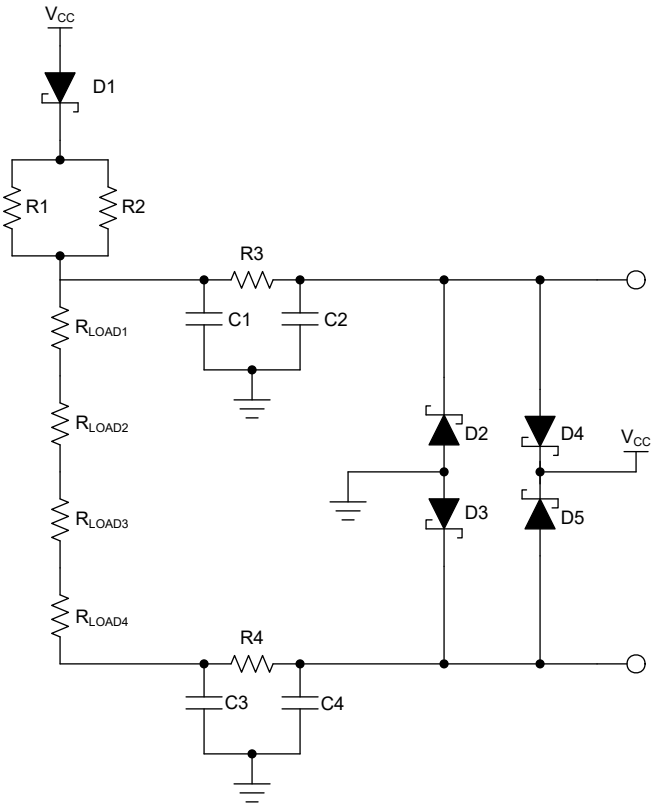


Figure 2-11. Clamping and Load Circuitry

Diode *D1* directs the interlock current from the TPS7B69-Q1 LDO to the *HVIL-Send* terminal, through the load resistors, and to the *HVIL-Return* pin. This creates a unidirectional flow of current that protects the TPS7B69-Q1 LDO. All logic of the different connectors states: normal operation, open connection, short to battery, and short to ground are based on a unidirectional flow of current.

Resistors *R1* and *R2* are larger-sized 1206 shunt resistors that are used to help prevent overcurrent conditions. The resistors labeled R_{LOAD1}, R_{LOAD2}, R_{LOAD3}, and R_{LOAD4} represent the resistance of each high-voltage connector within the vehicle that has the HVIL signal.

2.3.1.4 Modified Window Comparator

The TIDA-020069 converts the analog output voltage of *HVIL-Send* and *HVIL-Return* to binary digital values through the use of a modified window comparator circuit. This simplifies overall system design by converting analog values to digital in hardware, without the use of internal ADCs within a microcontroller. The following output pins of the TIDA-020069 all feature the binary digital outputs of the design: *HVIL-Send Logic-Higher TP*, *HVIL-Send Logic-Lower TP*, *HVIL-Return Logic-Higher TP*, and *HVIL-Return Logic-Lower TP*. The four binary outputs are used as two 2-bit digital representations of analog *HVIL-Send* and *HVIL-Return* analog signals.

The schematic in Figure 2-12 features the TLV9034-Q1, configured in a modified window comparator circuit. The TIDA-020069 features two of these circuits, each requiring two comparators, so the quad-channel TLV9034-Q1 was selected. Push-pull output comparators, like the TLV9034-Q1, are required for this circuit. This prevents the need of an output pullup or pulldown resistor for each channel.

The circuit design is based on the Analog Engineer's Circuit: Window Comparator Circuit. Reference this analog circuit design for more details about the circuit, including downloadable simulation models.

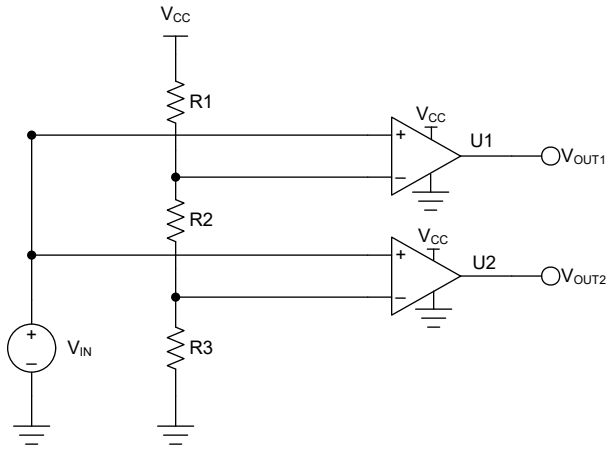


Figure 2-12. Modified Window Comparator Circuit

The expected output voltage, V_{OUT1} and V_{OUT2} is found in Table 2-3 and Table 2-4 below:

Table 2-3. HVIL-Send Binary Output Logic

PARAMETER	HVIL-SEND LOGIC-LOWER TP	HVIL-SEND LOGIC-HIGHER TP
HVIL-Send TP < Lower Threshold	0V	0V
Lower Threshold < HVIL-Send TP < Upper Threshold	5V	0V
HVIL-Send TP > Upper Threshold	5V	5V

Table 2-4. HVIL-Return Binary Output Logic

PARAMETER	HVIL-RETURN LOGIC-LOWER TP	HVIL-RETURN LOGIC-HIGHER TP
HVIL-Return TP < Lower Threshold	0V	0V
Lower Threshold < HVIL-Return TP < Upper Threshold	5V	0V
HVIL-Return TP > Upper Threshold	5V	5V

In this design, resistors *R1*, *R2*, and *R3* are all set to identical values of 10kΩ. This divides the 5V supply voltage, V_{CC} into thirds. This sets the reference voltage of comparator *U2* to 1.67V and the reference voltage of comparator *U1* to 3.33V. These reference voltages correspond to the *Lower Threshold* and *Upper Threshold* of the data in Figure 2-13, respectively. These resistor values were selected to simplify the bill of materials (BOM) by using more similar components. To satisfy the TIDA-020069 State Logic Thresholds, set *Upper Threshold* lower than *HVIL-Send* for the normal operation mode. The state logical also requires that *HVIL-Return (open connection) < Lower Threshold < HVIL-Return (normal operation)*.

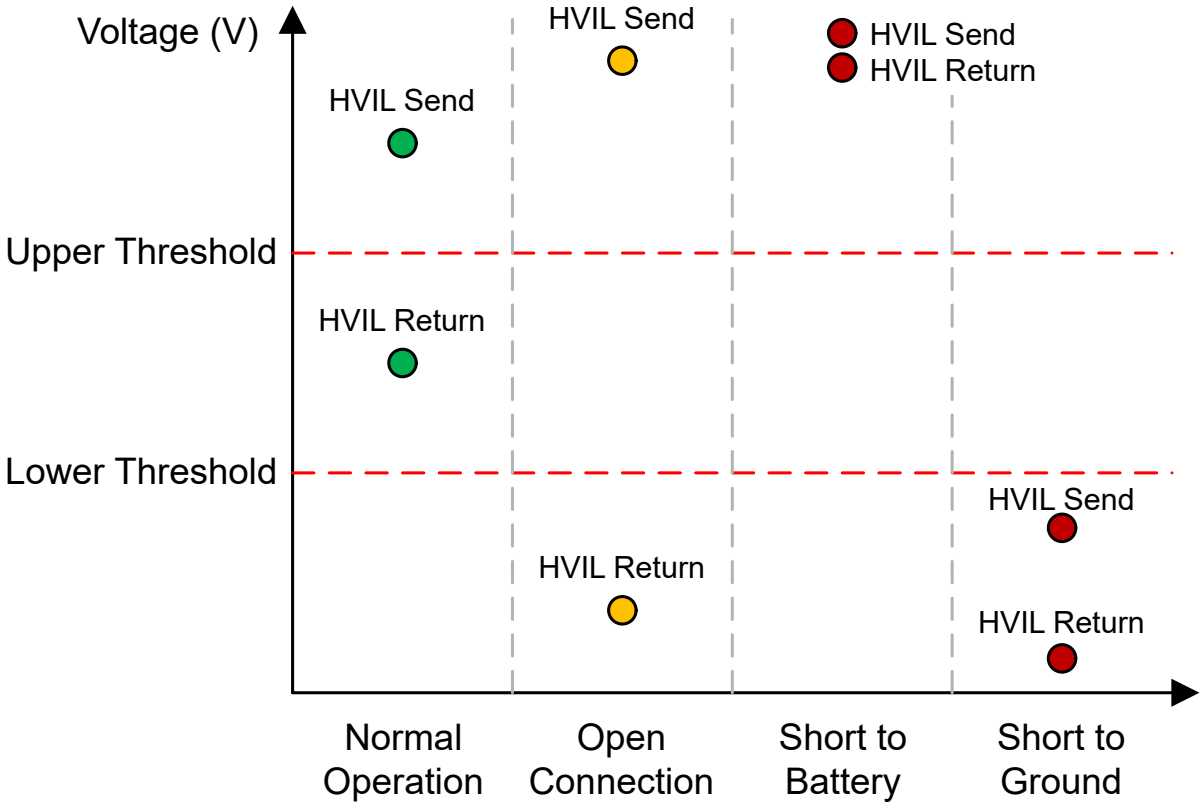


Figure 2-13. TIDA-020069 State Logic Thresholds

2.3.1.5 Digital Logic Gates

The TIDA-020069 converts the binary digital signal output generated by the Section 2.3.1.4 circuit to be four state of the HVIL system: *Normal Operation*, *Open Connection*, *Short to Battery*, or *Short to Ground*. The SN74HCS08-Q1, quad-channel AND gate, and SN74HCS86-Q1, quad-channel XOR gate, translate the two 2-bit binary digital values to output states. These logic gates also control the onboard LEDs to visually indicate each state on the board in real time without the need of external measurement hardware. For even further optimized system integration, these four state values can be translated into a 2-bit binary value, where each combination represents one of the four states. This conversion from the analog *HVIL-Send* and *HVIL-Return* signals to binary and then to state values simplifies system-level design by handling state recognition in hardware, rather than software.

The following circuit shows the logic gate configuration used in the TIDA-020069:

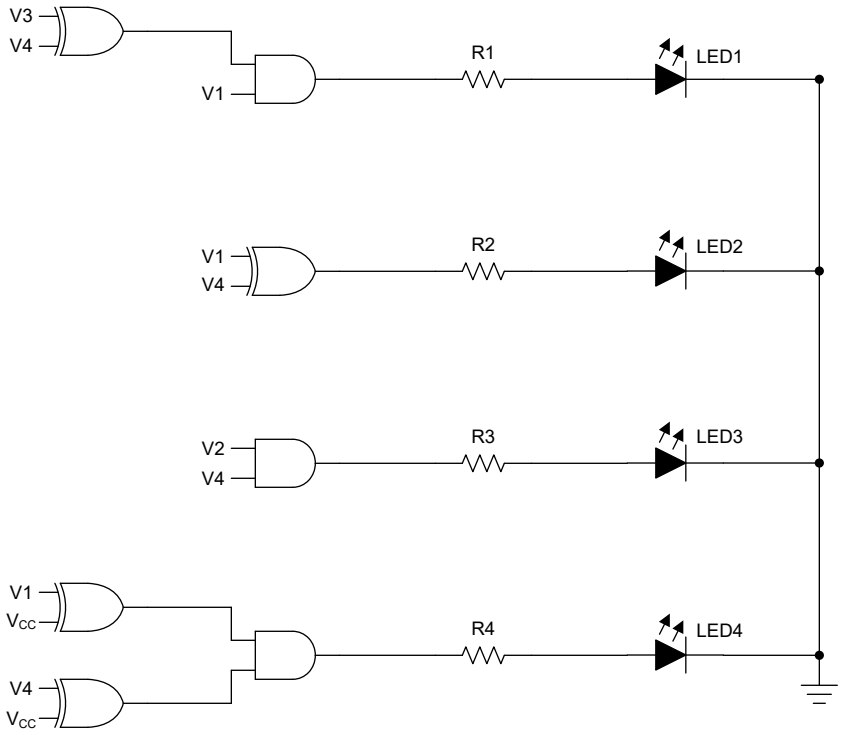


Figure 2-14. Digital Logic Gates

In this schematic, *V1* represents *HVIL-Send Logic-Higher*, *V2* represents *HVIL-Send Logic-Lower*, *V3* represents *HVIL-Return Logic-Higher*, and *V4* represents *HVIL-Return Logic-Lower*. *LED1* represents the *Normal Operation* LED, *LED2* represents the *Open Connection* LED, *LED3* represents the *Short to Battery* LED, and *LED4* represents the *Short to Ground* LED.

The logic of this circuit was tested and the results are found in Section 3.3. Table 2-5 shows the complete truth table of the design. It is important to note that this is a comprehensive truth table of all theoretical possibilities of this digital logic circuit, but not all input combinations are possible for the TIDA-020069. For example, it is not possible for *V1* to equal 0 while *V2* equals 1. This is because *HVIL-Send Logic-Lower* (*V2)* must be 1 when *HVIL-Send Logic-Higher* (*V1)* is 1. The same is true for *V3* and *V4*. Other possibilities are listed in the table that are not generated by the 4 different states, even when shifting where the short to battery or short to load occurs. There is only one status LED indicator on at any given point.

Table 2-5. Digital Logic Gates Truth Table

V1	V2	V3	V4	LED1	LED2	LED3	LED4
0	0	0	0	0	0	0	1
0	0	0	1	0	1	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	0	0	0
0	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	1	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	1	0	0
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	0
1	1	1	1	0	0	1	0

2.3.2 Status Indication

2.3.2.1 Normal Operation (Closed Connection) State

The TIDA-020069 is in normal operation (closed connection) state when all load resistors are connected in series. During this state, the onboard LED marked *Normal Operation* is turned on, as shown in Figure 3-7 test results image. This state represents a closed and secure connection of all high-voltage connectors in an HVIL system. In a HEV/EV, this is considered normal operation while the vehicle is powered on. In this state, the high-voltage battery is enabled, as the TIDA-020069 is indicating a secure connection of all high-voltage connectors.

Figure 2-15 illustrates the expected behavior of *HVIL-Send* and *HVIL-Return* during normal operation. The high-voltage connectors are modeled as resistors connected in series with the TIDA-020069. In this state, current flows though the interlock loop, though each high-voltage connector, and returns to the TIDA-020069.

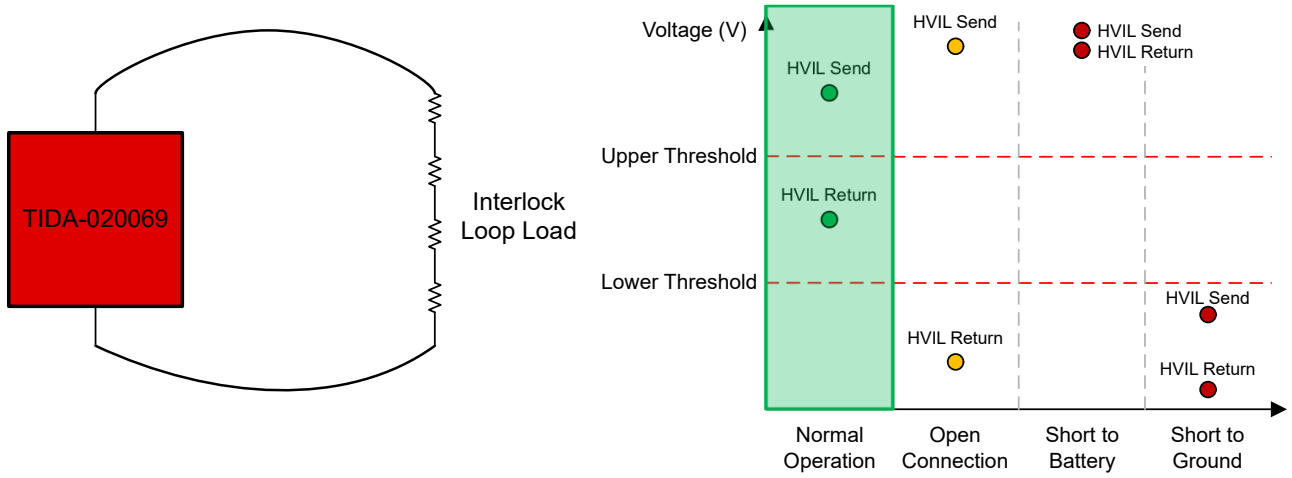


Figure 2-15. Normal Operation (Closed Connection) State

In normal operation, *HVIL-Send* is expected to be greater than the *Upper Threshold* voltage level and *HVIL-Return* is expected to be between the *Lower Threshold* and *Upper Threshold* voltage levels. The differential voltage between *HVIL-Send* and *HVIL-Return* is:

$$V_{DIF} = V_{HVIL-SEND} - V_{HVIL-RETURN} = I_{LOAD} \times R_{LOAD} \quad (9)$$

This differential voltage, V_{DIF}, along with an accurate measurement from the current-sense amplifier, $V_{CS\text{-}OUTPUT}$ are indicators that the TIDA-020069 is in normal operation.

The TIDA-020069 is designed to allow for flexibility to accommodate various OEM requirements for HVIL systems. Many variables can be adjusted to meet the requirements for each system, including: loop current (I_{LOAD}), loop resistance (R_{LOAD}), and supply voltage. Despite the changes in these variables, the *Lower Threshold* voltage level needs to be less than *HVIL-Return*, while the *Upper Threshold* voltage level needs to be less than *HVIL-Return* and greater than *Lower Threshold* during a closed connection for the TIDA-020069 to correctly interpret a normal operation state. The resistor divider ratios selected in Section 2.3.1.4 must be selected to meet these requirements.

2.3.2.2 Open Connection State

The TIDA-020069 is in an open connection state when one of the high-voltage connectors was disconnected or there is an open connection throughout the interlock loop. During this state, the onboard LED marked *Open Connection* is turned on, as shown in the test results image. An open load condition can happen due to a service disconnect switch, disconnecting the high-voltage connectors, or due to a loose connection in the wiring harness. An unintentional open load, which can result from collision or fault connectors, can be difficult to locate because the behavior is the same regardless of where in the loop the open occurs. During this state, the high-voltage battery of the HEV/EV is disabled, as the TIDA-020069 is indicating an improper connection of high-voltage connectors.

Figure 2-16 illustrates the expected behavior of *HVIL-Send* and *HVIL-Return* during an open load state. The high-voltage connectors are modeled as resistors that have an open between them. This open can occur at any point within the interlock loop: before the load, between load resistors, or after the load. In this state, no current flows through the interlock loop, as shown by a change in the *CS-Output* current sensing test point.

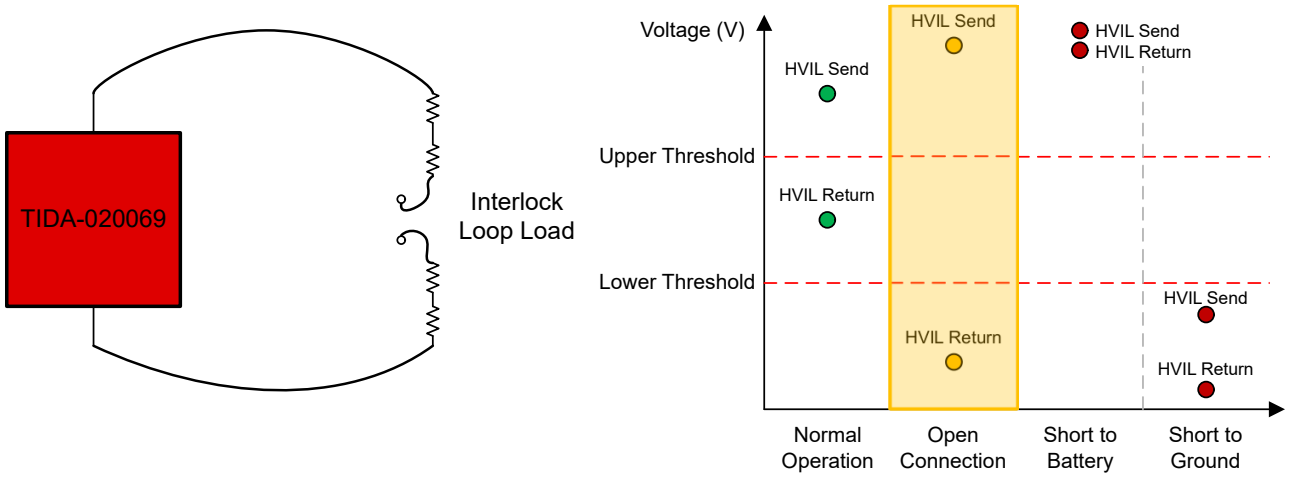


Figure 2-16. Interlock Line Open Load

In an open connection state, *HVIL-Send* is expected to be greater than the *Upper Threshold* voltage level set by the Section 2.3.1.4 circuit stage, while *HVIL-Return* is expected to be less than the *Lower Threshold* voltage level. The differential voltage between *HVIL-Send* and *HVIL-Return* increases during this state, as *HVIL-Send* is pulled closer to the 5V V_{CC} supply voltage coming from the TPS7B69-Q1 and *HVIL-Return* is pulled closer towards ground. *HVIL-Return* is not pulled entirely to ground in this case because *HVIL-Return* is connected to ground through the collector of the BJT transistor in the Section 2.3.1.1 circuit. The input voltage, V_{IN}, to the non-inverting input terminal of the TLV9002-Q1 used in the Section 2.3.1.1 circuit was set to 1V. This voltage is reflected onto the input of the inverting terminal, via the concept of *virtual short* in a closed feedback system, and is connected to the emitter of the BJT. Therefore, the value of *HVIL-Return*, which is connected to the collector of the BJT, is:

$$V_{HVIL-Return} = V_{IN-} + V_{CE-SAT} = V_{IN+} + V_{CE-SAT} = \left(V_i \times \left(\frac{R_2}{R_1 + R_2}\right)\right) + V_{CE-SAT} \quad (10)$$

The TIDA-020069 is designed to allow for flexibility to accommodate various OEM requirements for HVIL systems. Many variables can be adjusted to meet the requirements for each system, including: loop current (I_{LOAD}), loop resistance (R_{LOAD}), and supply voltage. However, the TIDA-020069 requires that the *Lower Threshold* voltage set in the *Modified Window Comparator* stage is greater than this *HVIL-Return* voltage calculated during the open condition. The resistor divider that sets *Lower Threshold* must yield a higher voltage than the resistor divider that sets V_{IN+} to the TLV9002-Q1.

2.3.2.3 Short-to-Battery State

The TIDA-020069 is in a short-to-battery state when a short to the 12V battery voltage is inserted at any point within the interlock loop. This short can be inserted between *HVIL-Send* and the load, between any load resistors (HV connectors), or between the load and *HVIL-Return*. During this state, the onboard LED marked *Short to Battery* is turned on, as shown in the test results image. This short-to-battery state can be the result of improper wiring connections, deteriorating connectors, or problems mishandling during servicing, where the 12V battery is shorted to the interlock pins. This state represents a failure mode and the TIDA-020069 is indicating that the high-voltage battery of the HEV/EV needs to be disabled immediately.

Figure 2-17 illustrates the expected behavior of *HVIL-Send* and *HVIL-Return* during the short-to-battery failure state. The high-voltage connectors are modeled as resistors connected in series with the TIDA-020069, but a short to the 12V battery was inserted into the interlock loop.

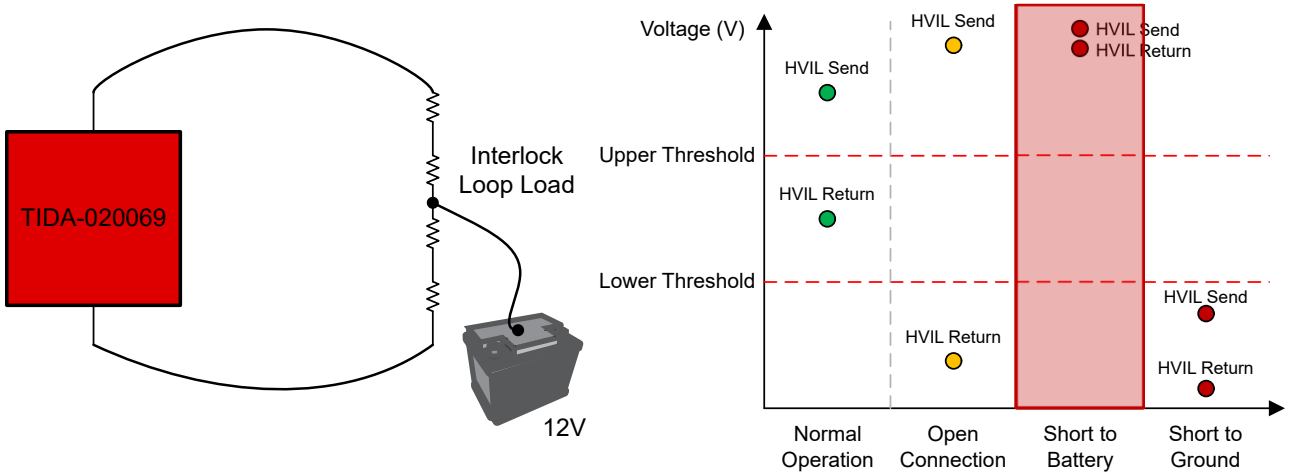


Figure 2-17. Interlock Line Short to 12V Battery

In this failure state, both the *HVIL-Send* and *HVIL-Return* voltages are pulled high. The clamping diodes of the Section 2.3.1.3 portion of the design clamp *HVIL-Send* and *HVIL-Return* to 5V (the supply voltage regulated by TPS7B69-Q1). This prevents an overvoltage effect and protects downstream devices that can be connected to *HVIL-Send* and *HVIL-Receive*, like an MCU.

The differential voltage, V_{DIF}, between *HVIL-Send* and *HVIL-Return* is very small in this failure mode, regardless of where the short is inserted within the interlock loop. *HVIL-Send* and *HVIL-Return* must both be greater in voltage than the *Upper Threshold* voltage for the TIDA-20069 state logic to work correctly. However, both *HVIL-Send* and *HVIL-Return* are higher in voltage in this state than $HVIL\text{-}Send_{Normal\ Operation}$ and $HVIL\text{-}Send_{Open\ Connection}$. Therefore, there are no additional design requirements for this state that are not already met by the design guidelines of Section 2.3.2.1 and Section 2.3.2.2.

The results of this state can be verified in the *Test Results* section.

2.3.2.4 Short-to-Ground State

The TIDA-020069 is in a short to ground state when a short to ground has been inserted at any point within the interlock loop. This short can be inserted between *HVIL-Send* and the load, between any load resistors (HV connectors), or between the load and *HVIL-Return*. During this state, the onboard LED marked *Short to Ground* is turned on, as shown in the test results image. This short-to-ground state can be the result of improper wiring connections, deteriorating connectors, or problems mishandling during servicing, where ground is shorted to the interlock pins. This state represents a failure mode and the TIDA-020069 is indicating that the high-voltage battery of the HEV/EV needs to be disabled immediately.

Figure 2-18 illustrates the expected behavior of *HVIL-Send* and *HVIL-Return* during the short-to-ground failure state. The high-voltage connectors are modeled as resistors connected in series with the TIDA-020069, but a short to ground was inserted into the interlock loop.

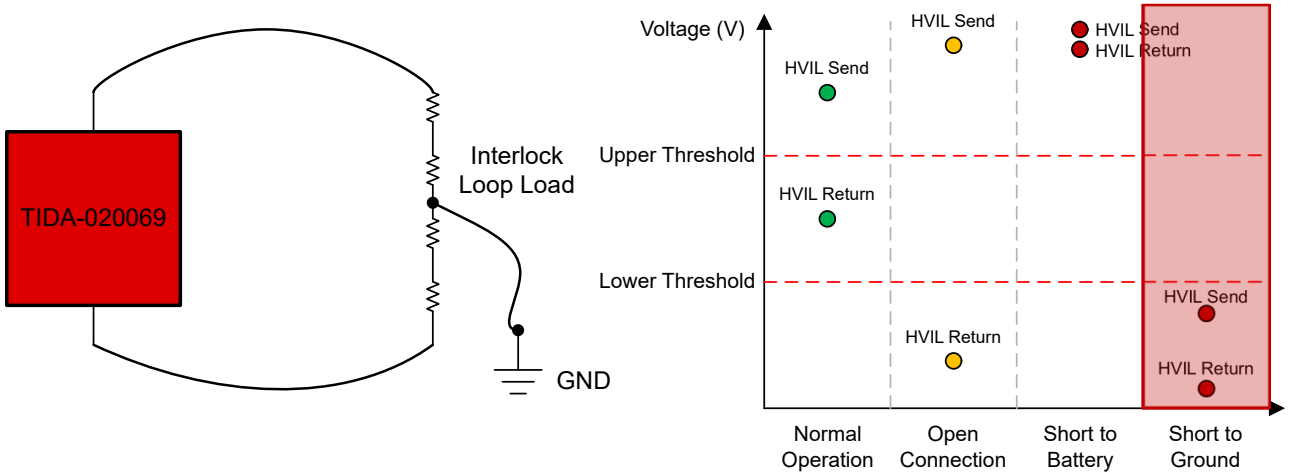


Figure 2-18. Interlock Line Short Circuit to Ground

In this failure state, both the *HVIL-Send* and *HVIL-Return* voltage are pulled low. The clamping diodes of the Section 2.3.1.3 portion of the design clamp *HVIL-Send* and *HVIL-Return* to ground and prevent these pins from getting pulled any lower than ground. This prevents an undervoltage effect and protects downstream devices that can be connected to *HVIL-Send* and *HVIL-Receive*, like an MCU.

Unlike the *Short-to-Battery* failure mode, the differential voltage, V_{DIF}, between *HVIL-Send* and *HVIL-Return* has a noticeable variation, depending on the location of where the short is inserted within the interlock loop. In Figure 2-18, both *HVIL-Send* and *HVIL-Return* are lower in voltage in this state than the *Lower Threshold* voltage. However, the voltage of *HVIL-Send* can vary in the failure state, depending on the location of the ground short. When the ground short occurs between the *HVIL-Send* node and the first load resistance, *HVIL-Send* is pulled to ground. When the ground short is inserted closer to the *HVIL-Return* node, the voltage at *HVIL-Send* increases. This HVIL-Send voltage can increase above the *Lower Threshold* voltage level. For proper operation of the TIDA-020069, *HVIL-Send* must be less than the *Upper Threshold* voltage level and *HVIL-Return* must be less than the *Lower Threshold* voltage level.

The results of this state can be verified in the *Test Results* section.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

The TIDA-020069 is categorized into four sections to explain the design in terms of the application:

- *Signal Chain*
- *Digital Logic*
- *Power Supply*
- *Header Connectors*

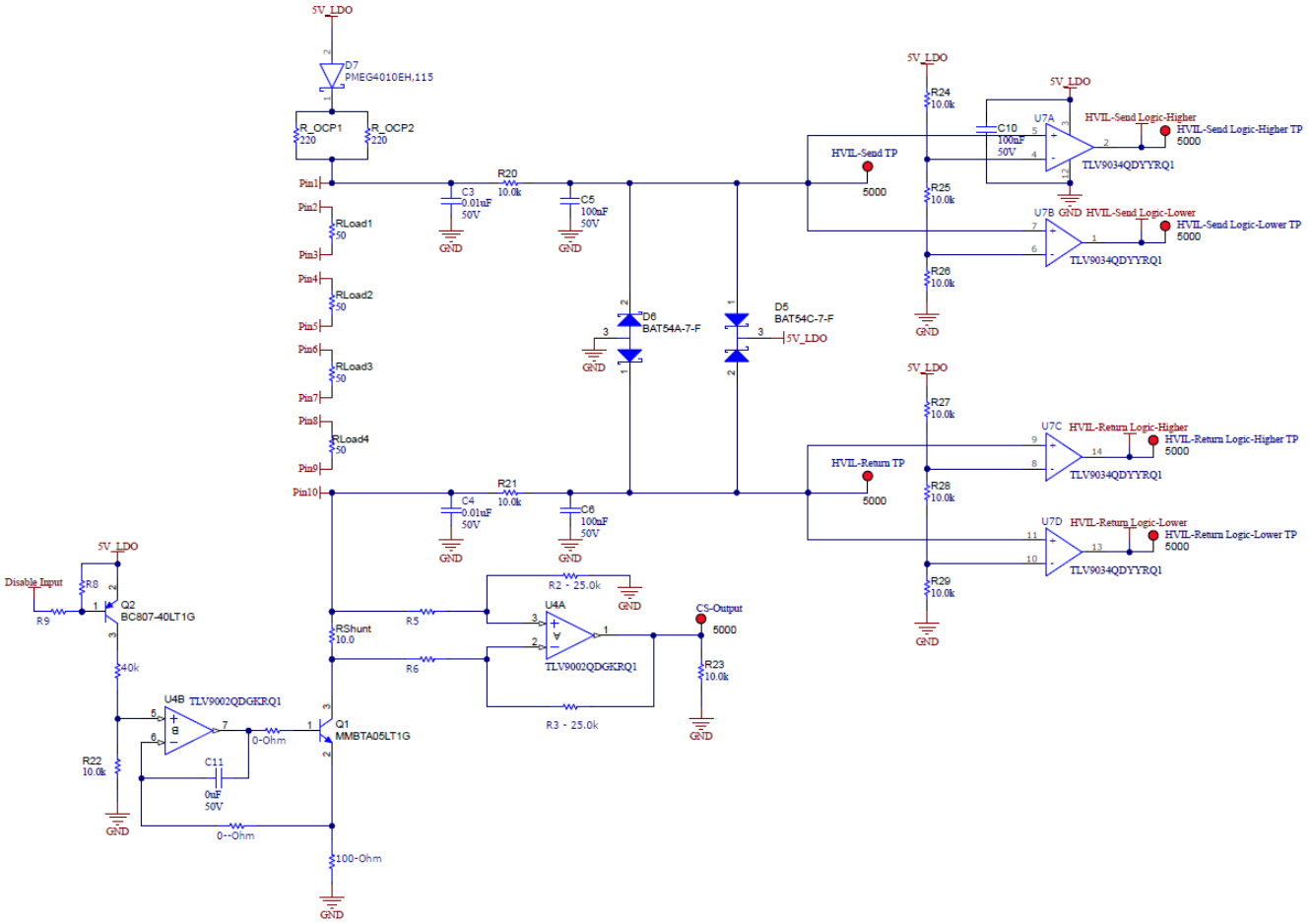


Figure 3-1. TIDA-020069 Schematic: Signal Chain

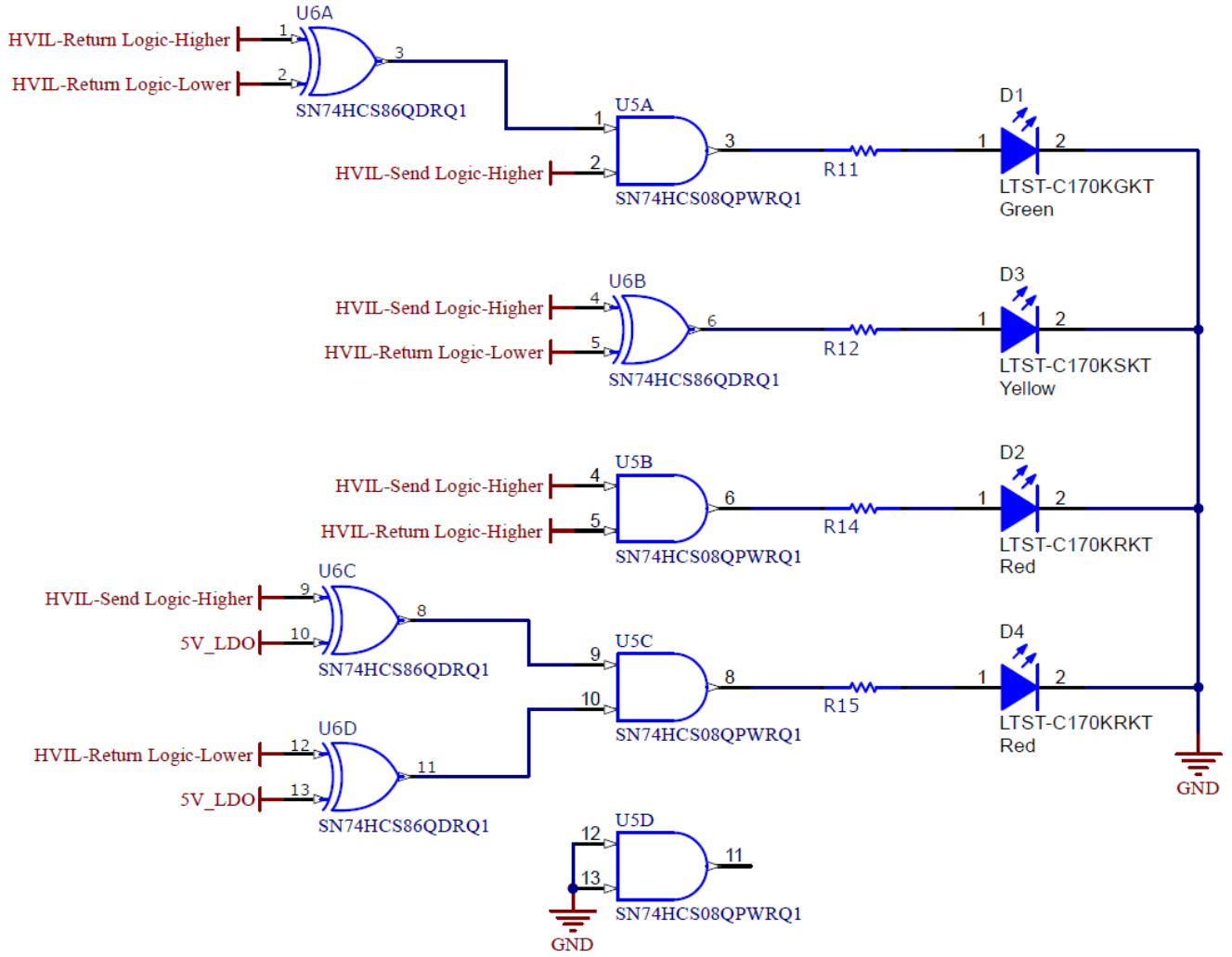


Figure 3-2. TIDA-020069 Schematic: Digital Logic

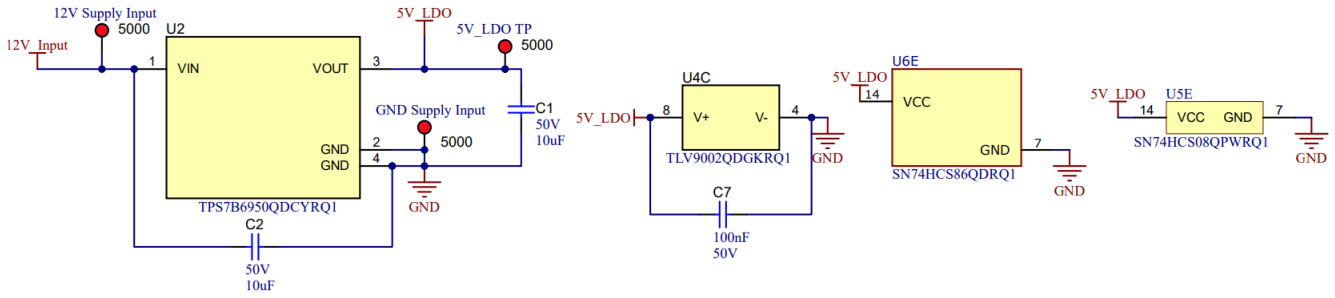


Figure 3-3. TIDA-020069 Schematic: Power Supply

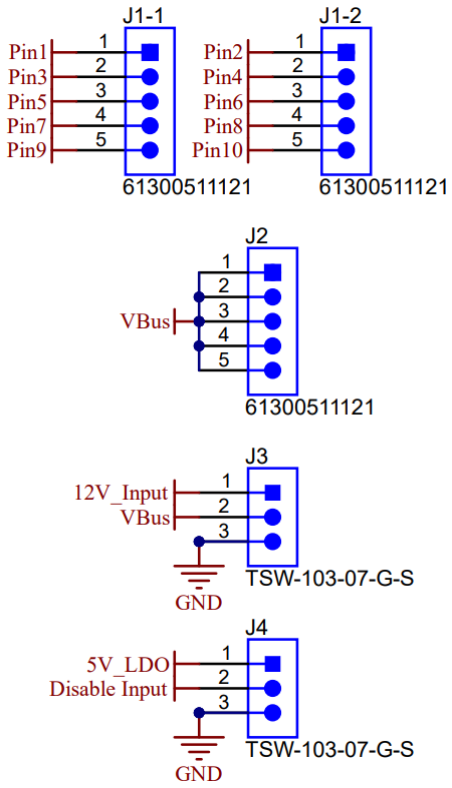


Figure 3-4. TIDA-020069 Schematic: Header Connectors

3.2 Test Setup

This reference design only requires a single 12V power supply for operation and testing. Onboard LED indicators are included in this design to visually display the state of the interlock. These LEDs are marked: *Normal Operation*, *Open Connection*, *Short to Battery*, and *Short to Ground* and turn on to indicate the corresponding state of the HVIL signal load.

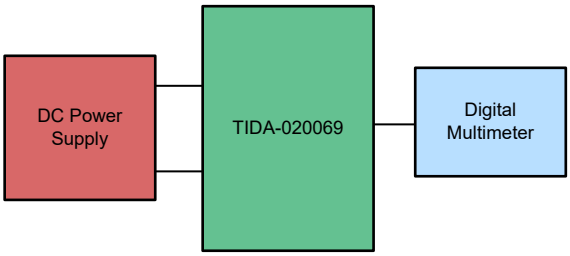


Figure 3-5. TIDA-020069 Test Setup

Multiple states are replicated and tested with this reference to verify both normal operation and the ability to diagnose different interlock states. The design features four 50Ω resistors that represent the impedance of HVIL connectors. These load resistors can be connected in series, left with an open connection, or have a short inserted between them. PCB jumper shorts are used with PCB header pins to configure the different modes of operation.

Figure 3-6 shows where different pin headers are located on the PCB. The 1 × 5 pin header columns labeled *J1-1* and *J1-2* are connected to each endpoint of load resistors: *RLoad1*, *RLoad2*, *RLoad3*, and *RLoad4*. Connecting all five rows of *J1-1* to *J1-2* together with 2-pin PCB shunt connectors creates a series connection between all four load resistors. This is the connection used for the *Normal Operation* condition. Disconnecting any 2-pin PCB shunt connectors between *J1-1* and *J1-2* creates an open connection (disconnect), which is used for the *Open Connection* condition.

The 1 × 5 pin header column labeled *J2* has a short between all pins, causing *J2* to behave like a supply voltage bus rail. The 1 × 3 pin header column labeled *J3* has row 1 connected to the 12V supply input, row 2 connected to *J2*, and row 3 connected to ground. When a single 2-pin PCB shunt connector is connected between row 1 and row 2 of *J3*, *J2* becomes a bus rail to the 12V supply voltage. When a single 2-pin PCB shunt connector is connected between row 2 and row 3 of *J3*, *J2* becomes a bus rail to the ground supply voltage. A 3-pin PCB shunt connectors between columns *J2*, *J1-1*, and *J1-2*, inserts a short to either the 12V supply voltage or ground supply to the corresponding row. This short can be inserted either before the four load resistors,in-between any of the resistors, or after the load.

The 3 × 1 pin header row labeled *J4* is used to control the shutdown functionality of the board. Column 1 is connected to the 5V voltage through the pullup resistor *R8*. Column 2 is connected to the base of transistor *Q2*, which is operating as a switch. Column 3 is connected to the ground supply voltage. When a 2-pin PCB shunt connector is inserted between column 1 and 2, the shutdown functionality is turned on (active high), and the current source enters shutdown mode. When a 2-pin PCB shunt connector is inserted between column 2 and 3, the shutdown functionality is inactive (active low), and the system operates as anticipated.

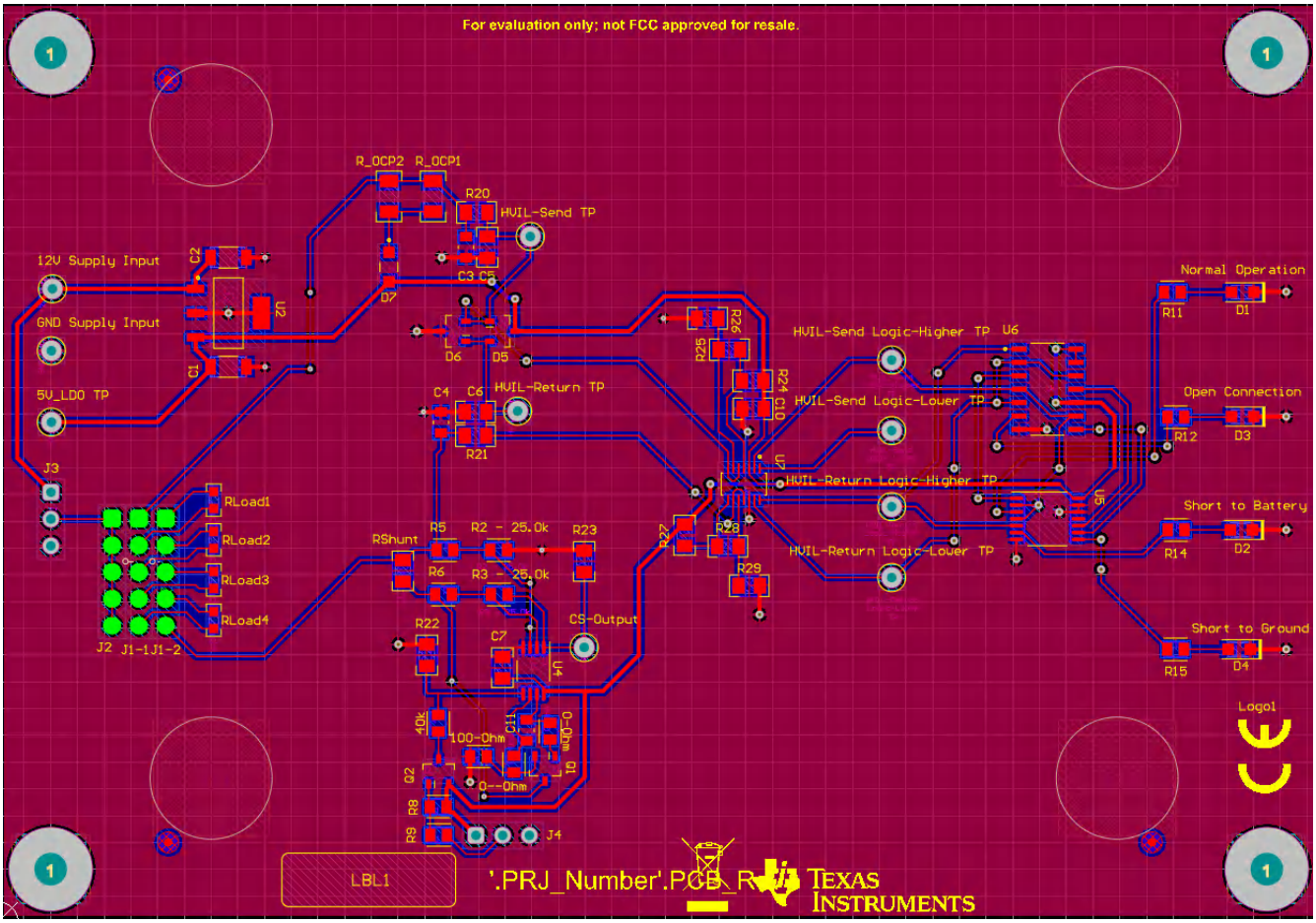


Figure 3-6. TIDA-020069 PCB Header Connections

DC voltage and current measurements were taken with a digital multimeter at numerous points on the board. The following test points were measured during multiple modes of operation: *5V_LDO TP*, *HVIL-Send TP*, *HVIL-Return TP*, *HVIL-Send Logic-Higher TP*, *HVIL-Send Logic-Lower TP*, *HVIL-Return Logic-Higher TP*, *HVIL-Higher Logic-Lower TP*, and *CS-Output*. The test results are located in the following section, *Test Results*.

3.3 Test Results

A digital multimeter is used to measure the voltages and currents at several test points of the TIDA-020069. The results are compared against the simulated values obtained via *TINA-TI* simulation of the circuit. The board was configured in 16 different states using PCB header shunt connectors.

Table 3-1. Measured Test Results

CONDITION	5V_LDO TP (V)	HVIL-SEND (V)	HVIL-RETURN (V)	HVIL-SEND LOGIC-HIGHER (V)	HVIL-SEND LOGIC-LOWER (V)	HVIL-RETURN LOGIC-HIGHER (V)	HVIL-RETURN LOGIC-LOWER (V)	CS-OUTPUT (V)	LOOP CURRENT (mA)	POWER SUPPLY CURRENT (mA)
Normal Operation	5.00	3.68	1.69	5.00	5.00	0.00	5.00	2.47	9.97	18
Open Loop	5.00	4.98	1.00	5.00	4.99	0.00	0.00	1.77	0.00	18
Short-to-Battery (Row #1)	5.00	5.26	5.24	5.00	5.00	5.00	5.00	0.33	15.98	20
Short-to-Battery (Row #2)	5.00	5.26	5.25	5.00	5.00	5.00	5.00	0.01	17.23	21
Short-to-Battery (Row #3)	5.00	5.26	5.25	5.00	5.00	5.00	5.00	0.01	18.70	21
Short-to-Battery (Row #4)	5.00	5.26	5.25	5.00	5.00	5.00	5.00	0.01	20.43	22
Short-to-Battery (Row #5)	5.17	5.44	5.44	5.18	5.18	5.18	5.18	0.01	22.53	23
Short-to-Ground (Row #1)	5.28	0.01	1.01	0.00	0.00	0.00	0.00	0.00	44.00	70
Short-to-Ground (Row #2)	5.19	1.55	0.98	0.00	0.00	0.00	0.00	0.00	29.81	56
Short-to-Ground (Row #3)	5.16	2.34	0.94	0.00	5.15	0.00	0.00	0.00	22.77	51
Short-to-Ground (Row #4)	5.18	2.84	0.86	0.00	5.16	0.00	0.00	0.00	18.57	54
Short-to-Ground (Row #5)	5.27	3.23	0.01	0.00	5.23	0.00	0.00	0.00	15.86	62
Shutdown (Normal Operation)	5.00	4.82	4.75	5.00	5.00	5.00	5.00	0.02	0.37	4
Shutdown (Open Loop)	5.00	4.99	0.01	5.00	5.00	0.00	0.00	0.00	0.00	3
Shutdown (Short-to-Battery)	6.49	6.75	6.74	6.49	6.49	6.49	6.49	0.01	-0.53	9
Shutdown (Short-to-Ground)	5.01	2.27	0.00	0.00	5.01	0.00	0.00	0.00	22.13	26

3.3.1 Normal Operation (Closed Connection) Test Results

Figure 3-7 shows the TIDA-020069 board configured in the normal operation (closed connection) state. In this state, all HVIL load resistors are connected in series and current is flowing through the load. This replicates the normal operation within an HEV/EV, where all high-voltage connectors are securely connected and the HVIL loop is closed.

The *Normal Operation* LED indicator is turned on in Figure 3-7, as expected for this state. This verifies the logical interpretation of the *HVIL-Send* and *HVIL-Return* voltages in this state.

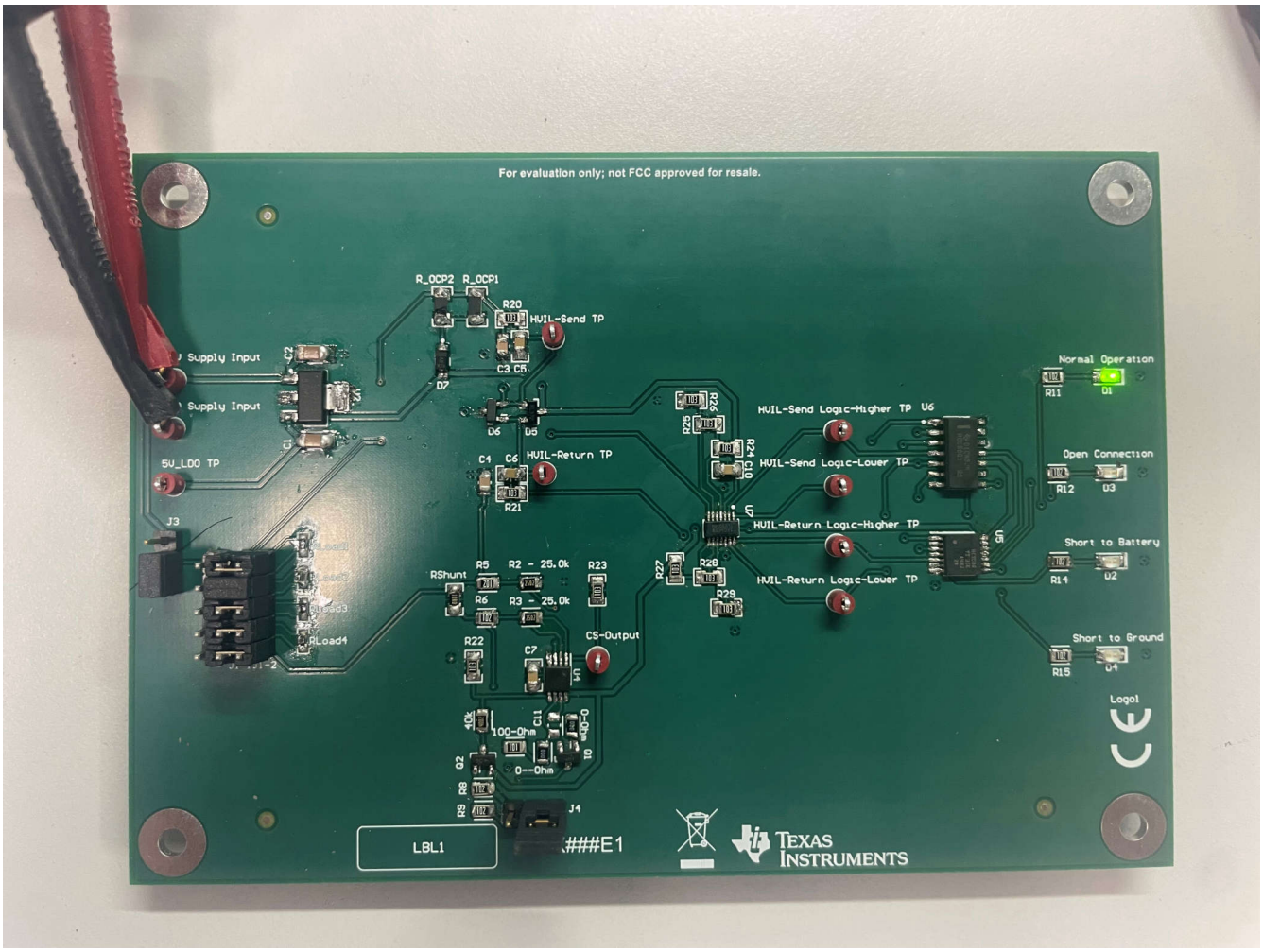


Figure 3-7. Normal Operation (Closed Connection) Test Results

3.3.2 Open Connection Test Results

Figure 3-8 shows the TIDA-020069 board configured in the open connection state. In this state, the HVIL load resistors are disconnected at some point within the HVIL loop and no current is flowing through the load. This replicates the a scenario within an HEV/EV where a high-voltage connector is disconnected. An open connection can be experienced during vehicle maintenance or as a result of collision. In this state, the high-voltage connectors are not connected and the HVIL loop is view as an open connection.

The *Open Connection* LED indicator is turned on in Figure 3-8, as expected for this state. This verifies the logical interpretation of the *HVIL-Send* and *HVIL-Return* voltages in this state.

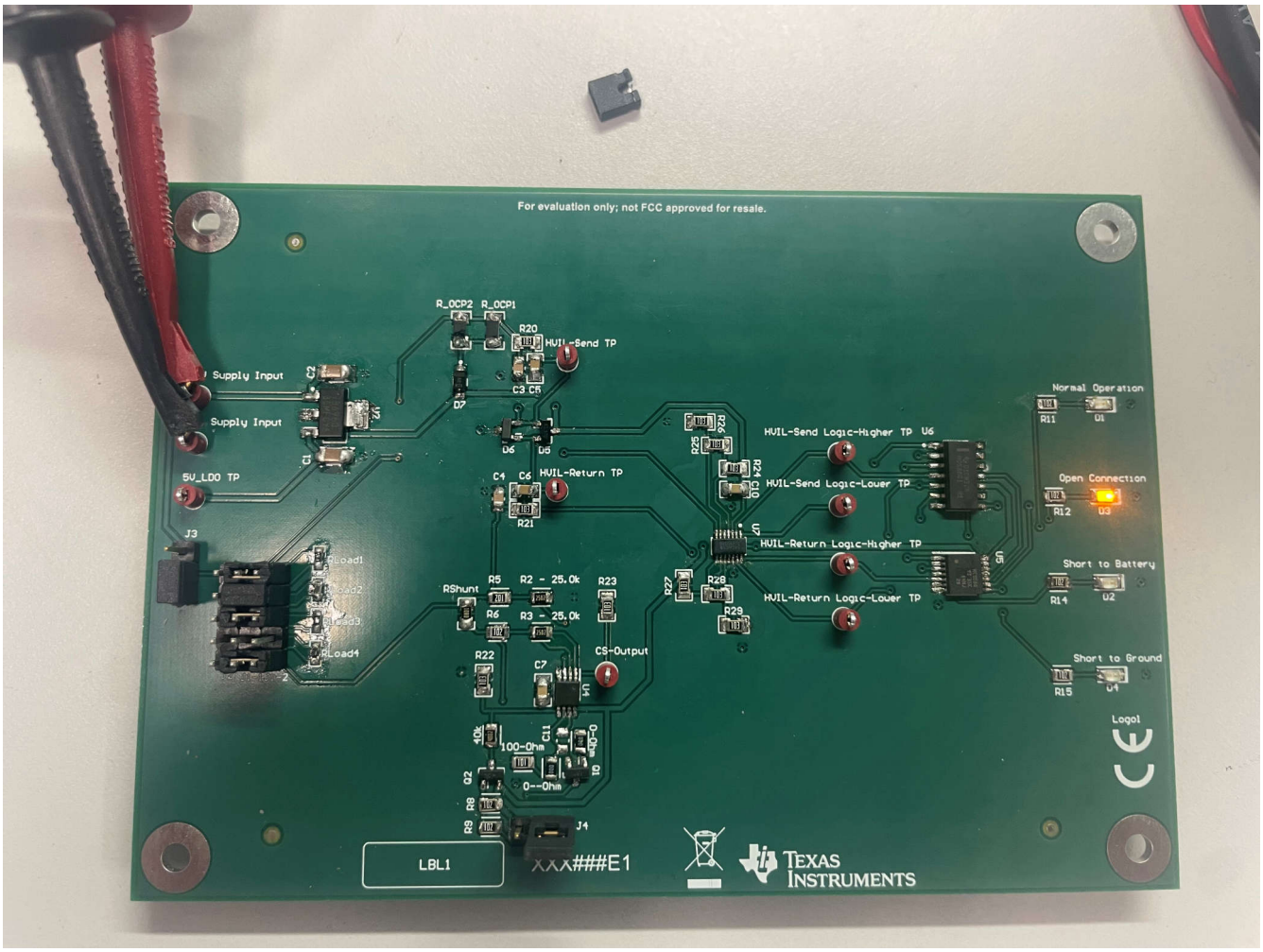


Figure 3-8. Open Connection Test Results

3.3.3 Short-to-Battery Test Results

Figure 3-9 shows the TIDA-020069 board configured in the short-to-battery failure state. In this state, the HVIL load has experienced a short to the 12V battery voltage at some point in the loop. This short can occur before, after, or between the load resistors. This replicates the failure mode within an HEV/EV, as the HVIL system cannot determine if the connectors are in a closed or open configuration during this short failure. This failure can also occur when the *HVIL-Send* and *HVIL-Return* pins are shorted together. In this scenario, current is still measured across the shunt resistor, but no current is flowing through the HVIL load resistors. This reference design accounts for this failure scenario.

The *Short to Battery* LED indicator is turned on in Figure 3-9, as expected for this state. This verifies the logical interpretation of the *HVIL-Send* and *HVIL-Return* voltages in this state.

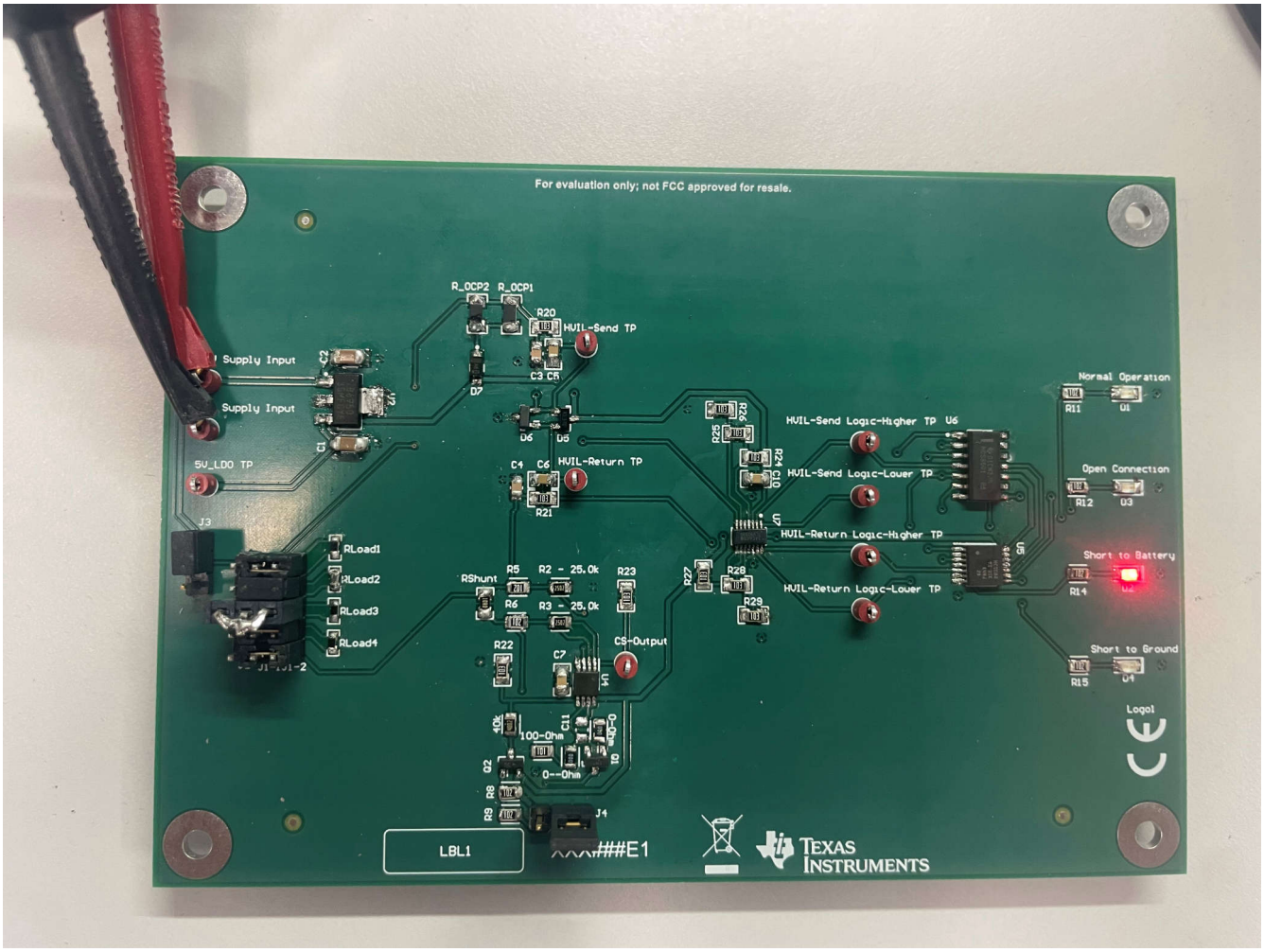


Figure 3-9. Short-to-Battery Test Results

3.3.4 Short-to-Ground Test Results

Figure 3-10 shows the TIDA-020069 board configured in the short-to-ground failure state. In this state, the HVIL load has experienced a short to ground at some point in the loop. This short can occur before, after, or between the load resistors. This replicates the failure mode within an HEV/EV, as the HVIL system cannot determine if the connectors are in a closed or open configuration during this short failure.

The *Short to Ground* LED indicator is turned on in Figure 3-10, as expected for this state. This verifies the logical interpretation of the *HVIL-Send* and *HVIL-Return* voltages in this state.

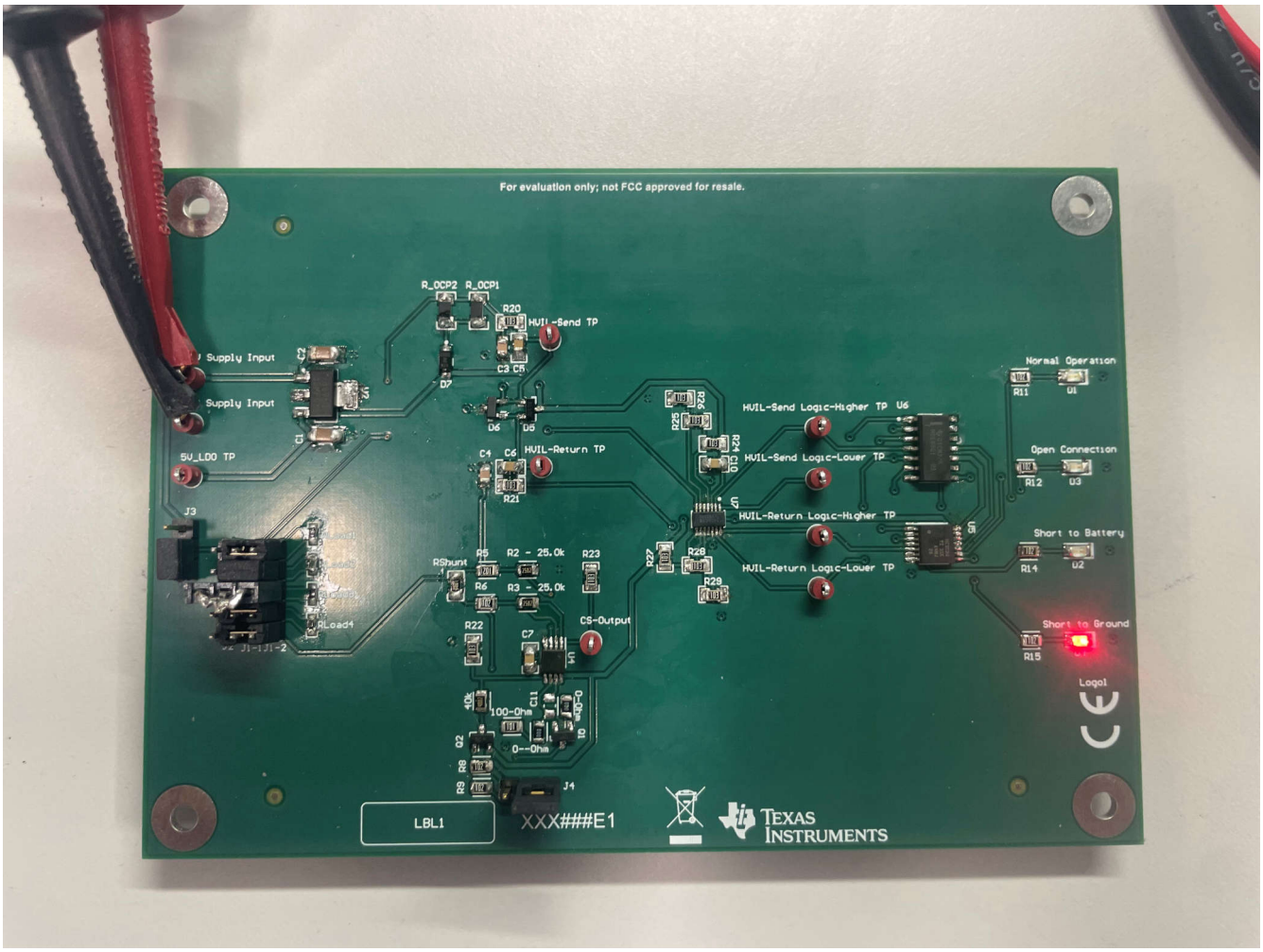


Figure 3-10. Short-to-Ground Test Results

3.3.5 Disable (Shutdown) Test Results

Figure 3-11 shows the TIDA-020069 board configured in the disable (shutdown) mode. In this state, the disable voltage at connector *J4* is pulled to a logic level high. The amplifier is disabled when this signal is active high. The output current of the constant current source is decreased by a factor of 100. The voltage drop across the HVIL load is also decreased by a factor of 100 in disable mode, and the voltage ranges of *HVIL-Send* and *HVIL-Return* appear similar to the short-to-battery failure mode. This optional input signal allows for a manual override that can force the HVIL design into a failure state until the overall system is ready to continue HVIL readings.

The *Short to Battery* LED indicator is turned on in Figure 3-11, as expected for this state. This verifies the logical interpretation of the *HVIL-Send* and *HVIL-Return* voltages in this state.

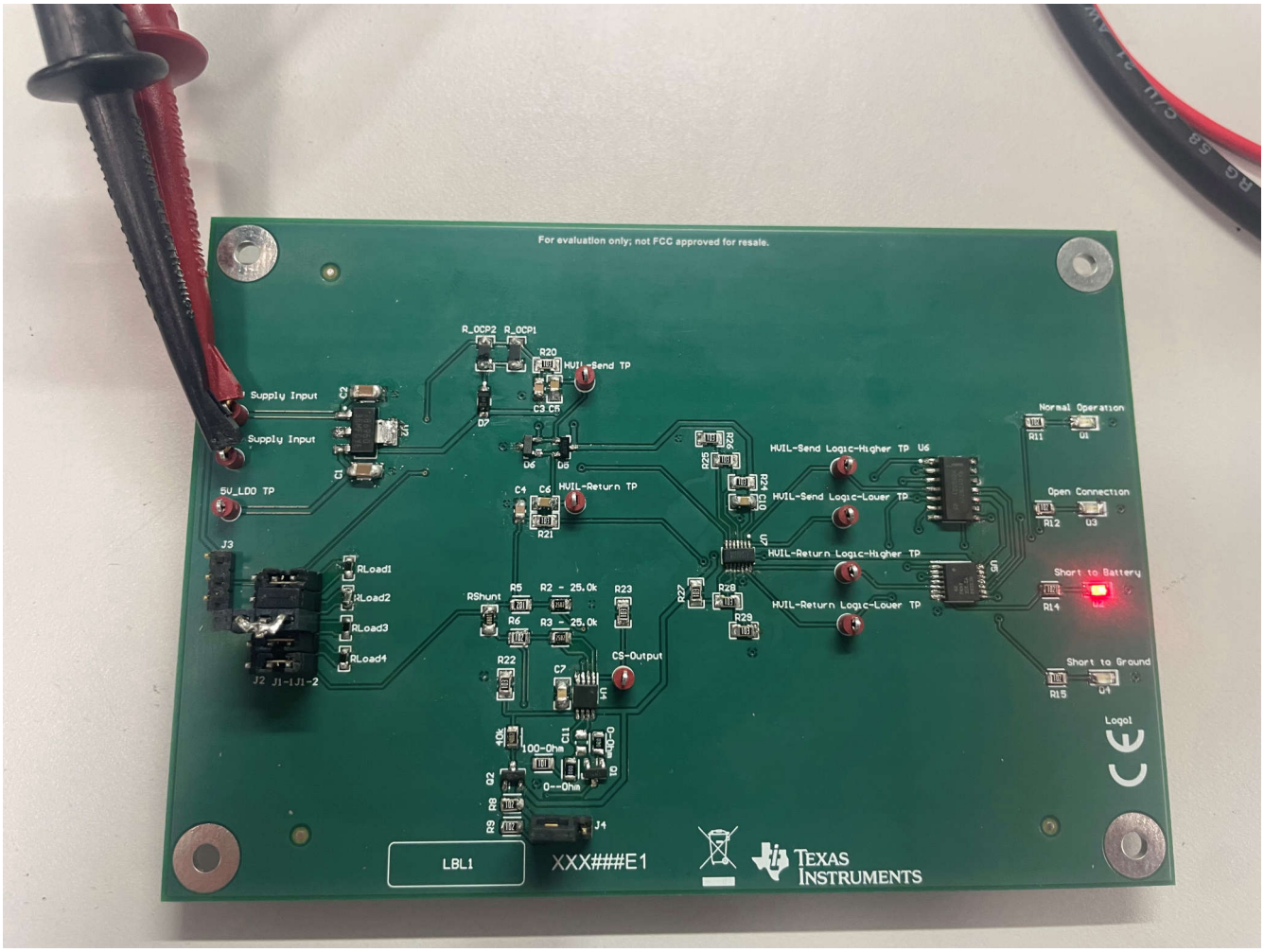


Figure 3-11. Disable (Shutdown) Test Results

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020069.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-020069.

4.3 PCB Layout Recommendations

The PCB layout of an interlock module must be done based on the arrangement and floor plan of a complete PCB.

- Place bypass capacitors C1, C2, C7, C8, C9, and C10 as close as possible to the corresponding component.
- Leave component C11 unpopulated.
  - A capacitor can be populated here for stability debugging purposes, if needed.
- Use 0Ω jumpers for the resistor components: 0-Ohm and 0--Ohm
  - Resistors can be populated here for stability debugging purposes, if needed.

Follow the layout guides in the data sheets listed for the following components:

- TLV9002-Q1
- TLV9034-Q1
- TPS7B69-Q1
- SN74HCS08-Q1
- SN74HCS86-Q1

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-020069.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-020069.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020069.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-020069.

5 Tools and Software

Tools

Analog Engineer's Circuit Cookbook: Amplifiers	Comprehensive collection of amplifier circuits with step-by-step instructions and formulas
TI Precision Labs (TIPL) training series	TI's comprehensive online classroom of on-demand courses and tutorials for analog signal chain designers

Software

TINA-TI	SPICE-based analog simulation program
PSPICE-FOR-TI	PSpice for TI™ design and simulation tool

6 Documentation Support

1. Texas Instruments, *TI Precision Labs - Op Amps* TI Training
2. Texas Instruments, Analog Engineer's Circuit Cookbook: Amplifiers
3. Texas Instruments, *High-side V-I with bipolar junction transistor (BJT) circuit* circuit design
4. Texas Instruments, *High-side current sensing with discrete difference amplifier circuit* circuit design

7 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9 About the Author

KIERNAN FARMER is systems engineer and product definer for Texas Instruments' amplifier business unit, working in Dallas, Texas. Kiernan brings experience in analog signal chain, specifically amplifier related circuits, to the automotive domain. Kiernan received his bachelor of electrical engineering degree from Florida State University.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265