Design Guide: TIDA-050074

140W, GaN-Based USB PD3.1 Adapter Reference Design

Description

This reference design is a gallium nitride (GaN) based, 140W AC-DC power with high efficiency and power density. The design supports wide input (90V–264V_{AC}) and output (5V–28V) voltage. The Power Factor Correction (PFC) is designed with UCC28056 which is a Transient Mode (TM) boost PFC controller plus LMG3622 device which is a 650V, 120mΩ GaN device with integrated driver. The DC-DC stage was designed by Asymmetric Half-Bridge Flyback (AHB) plus LMG2610 which is a 650V asymmetric half-bridge GaN (170mΩ–248mΩ) device with high- and low-side driver, level shift, and bootstrap diode integrated in 7mm × 9mm QFN package to minimize the PCB space. This reference design is customized for the application, such as the adapter design for USB power delivery (PD) 3.1 and the charger for power tools.

Resources

TIDA-050074	Design Folder
LMG3622	Product Folder
LMG2610	Product Folder
UCC28056	Product Folder

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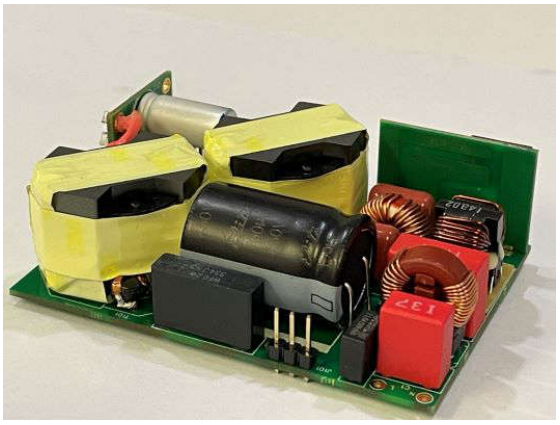
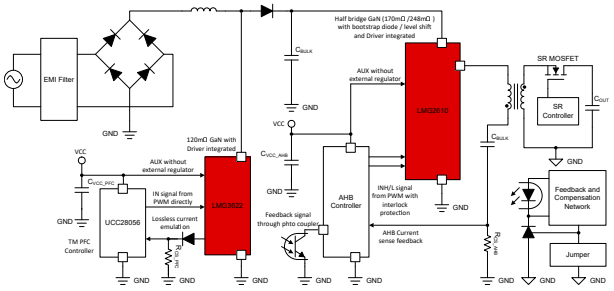
Features

- Wide output power range from 5V to 28V for USB PD3.1 application
- PFC is designed using a TI 120mΩ single GaN with driver integrated and UCC28056 TM PFC controller
- AHB is designed with the TI half-bridge GaN as a 170mΩ, 248mΩ GaN device with driver, level shift, and integrated bootstrap diode
- > 94% efficiency at 115V_{AC} input and > 95.5% efficiency at 230V_{AC} input
- High power density design: 27.33W/in^3 with PCB size: 50mm × 73mm × 23mm
- PFC is turned off at 5V and 9V output
- System feedback is designed using TL431. The output voltage (5V, 9V, 15V, 20V, and 28V) is set by the jumper

Applications

- Notebook PC power adapter design
- Other AC/DC adapters and PSU
- Mobile wall charger design
- Merchant battery charger





1 System Description

The TIDA-050074 reference design supports AC 100V–240V, 50Hz–60Hz input voltage, and provides DC 5V and 9V, 3A; 15V, 20V; and 28V, 5A output power. The design is based on low cost, high efficiency, and high power density with TM PFC + AHB topology. The ferrite core size was designed with RM10 for both PFC inductance and AHB transformer. The power supply dimensions are 50mm × 73mm × 23mm, and the power density is 27.33W/in^3.

The UCC28056 is utilized for TM boost PFC topology which supports TM and discontinuous conduction mode (DCM) operation for the PFC stage. To simplify the circuit, the system was designed without AUX winding. This design employs the LMG3622 (120mΩ GaN HEMT with driver integrated) for overall device reliability.

The system can run at a higher frequency because of the lower switching loss on GaN devices. This ability leads to a lower inductance value with less turns and thicker wires to increase overall efficiency. The PFC is turned off at 5V and 9V output condition to provide a more efficiency result.

The TI GaN driver is integrated with overcurrent protection (OCP), short-circuit protection (SCP), and overtemperature protection (OTP) functions. These features make the system design easy, reliable, and safe with less external components.

For the AHB stage, the design supports zero-voltage switching (ZVS) with a wider operation range. This design employs TI's LMG2610, a half-bridge GaN device with level shift, bootstrap diode, and integrated gate drivers. The 170mΩ, 248mΩ GaN device with a QFN 7mm × 9mm package size helps developers shrink the PCB size.

1.1 Key System Specifications

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	AC voltage	90		264	V
Output Current	5V	3			A
	9V	3			A
	15V	5			A
	20V	5			A
	28V	5			A

2 System Overview

2.1 Block Diagram

The system is combined of 2 parts, the PFC stage and DC-DC stage.

The PFC stage is designed with the UCC28056, eliminating the AUX winding on the L_{PFC} to simplify the design. The LMG3622 can drive the PFC at higher frequencies to reduce the size of the L_{PFC} with higher efficiency and density.

The DC-DC stage was designed with AHB topology providing the flexibility of the output voltage range and ZVS for high efficiency. The LMG2610 half-bridge GaN device with integrated low-side 170mΩ, high-side 248mΩ GaN-FET driver, level shift, and GaN-based bootstrap diode inside a 7mm × 9mm package size helps minimize the PCB size.

Instead of a USB PD controller, the feedback system is designed with the TL431 featuring a resistor divider array which sets the output voltage with a jumper.

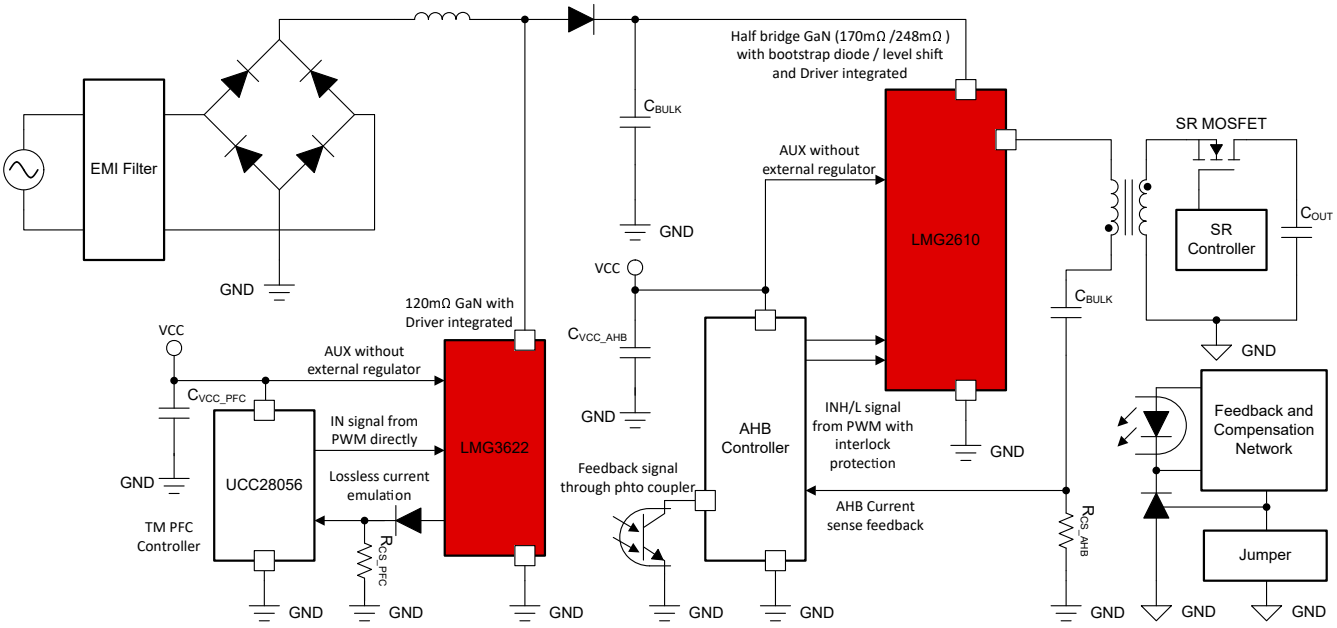


Figure 2-1. System Block Diagram of 140W Reference Design

2.2 Design Considerations

2.2.1 PFC Inductance Design

Based on the TM control method, the system works at ZVS when the input DC voltage is less than half of the output voltage. In PFC stage, the lowest efficiency was determined to occur at the lowest line voltage. The system does not have much switching loss, and the conduction loss dominates the system.

For TM PFC, the peak current was found at the phase angle equal to 90°, Equation 1 determines the value.

$$I_{PEAK} = 2 \times \sqrt{2} \times \frac{P_{IN}}{V_{AC}} \quad (1)$$

where

- P_{IN} is the input power which is the output power divides by the overall efficiency
- V_{AC} is the input RMS voltage

The output voltage was set as V_{OUT}, the duty cycle at this point is found with Equation 2.

$$\text{Duty} = \frac{V_{OUT} - \sqrt{2} \times V_{AC}}{V_{OUT}} \quad (2)$$

The target frequency is set at the lowest input AC voltage as F_{REQ_MIN}. Use Equation 3 to calculate the inductance value.

$$L_{PFC} = \frac{\sqrt{2} \times V_{AC}}{I_{PEAK}} \times \frac{\text{Duty}}{F_{REQ\_MIN}} \quad (3)$$

The flux density of the core material B_{MAX} is found using Equation 4.

$$B_{MAX} = \frac{L_{PFC} \times I_{PEAK}}{Ae \times N} \quad (4)$$

where

- A_e is the effective area of the core material
- N is the number of turns of the winding

Based on Equation 4, the peak current is fixed, and the A_e depends on the core shape. To keep the same flux density with the same core size, the turns *N* is proportional to the L_{PFC} value. From a system point of view, make the system run at higher frequency by implementing the GaN HEMT. Reducing the turns with thicker wire to minimize the copper loss minimizes the L_{PFC} value.

For this 140W design, the target efficiency is 93%, the input power is 150.54W. At 90V input voltage, assume the output voltage is 390V and the minimum frequency is 100kHz, I_{PEAK} is 4.731A. The duty cycle is 67.4%, and the inductance is 181µH.

In this design, the RM10 core size with 3C95 material from Ferroxcube is selected. Set the inductance value as 185µH with 30 turns by 0.1mm × 40P Litz wire to reduce the copper loss.

As the L_{PFC} value is fixed, the turn on time, T_{on}, can be calculated, at any angle θ as done in Equation 5.

$$\text{Ton}(\theta) = \frac{L_{PFC} \times I_{PEAK} \times \sin(\theta)}{\sqrt{2} \times V_{AC} \times \sin(\theta)} \quad (5)$$

Equation 5 shows the T_{on} time is constant at any phase angle.

The RMS current of the switching device I_{RMS} can be calculated as shown in Equation 6.

$$I_{RMS} = \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \times \frac{V_{AC}}{V_{OUT}}} \times I_{PEAK} \quad (6)$$

According to this formula, the RMS current is a constant which relates to the V_{AC}, V_{OUT}, and P_{IN} only. From the device point of view, the conduction loss can only be reduced by lowering the $R_{DS(on)}$.

2.2.2 Configuration of CS pin in LMG3622

For boost PFC design, a current shunt resistor is needed to detect the current for the system control and the over power protection.

LMG3622 integrates the current emulation function which supports a dependent current sourcing of I_{DS} through the internal current mirror. The gain of the current emulation is G_{CS}. With the very low value of C_{GS}, R_{CS} is designed with a high resistor value with a smaller package size which increases the efficiency and lowers the temperature stress on the PCB. The R_{CS} resistor was set with Equation 7.

$$R_{CS} = \frac{R_{Shunt}}{G_{CS}} \quad (7)$$

where

- R_{SHUNT} is the original current shunt resistor value.

The typical value of the G_{CS} of LMG3622 is 0.691mA/A. In this application, R_{CS} is designed as a 130Ω by 0603 package.

For most of the TM PFC, an AUX winding is needed to detect the ZVS condition and try to turn the device on at the valley for higher efficiency. To simplify the design, UCC28056 is designed by the resistors and capacitors divider to eliminate the AUX winding and combine the ZVS and CS in the same pin with SOT-23(6) package.

Instead of an AUX winding, the UCC28056 detects the ZVS with the capacitor and resistor divider. The sense capacitor induces high spike current during switching and converts the current to a high-voltage spike on the R_{CS} resistor which leads to over stress on the CS pin of TI-GaN. Figure 2-2 shows voltage spike on the R_{CS} resistor. The channel setting is:

- Ch1 is V_{DS} of LMG3622
- Ch2 is the R_{CS} voltage.

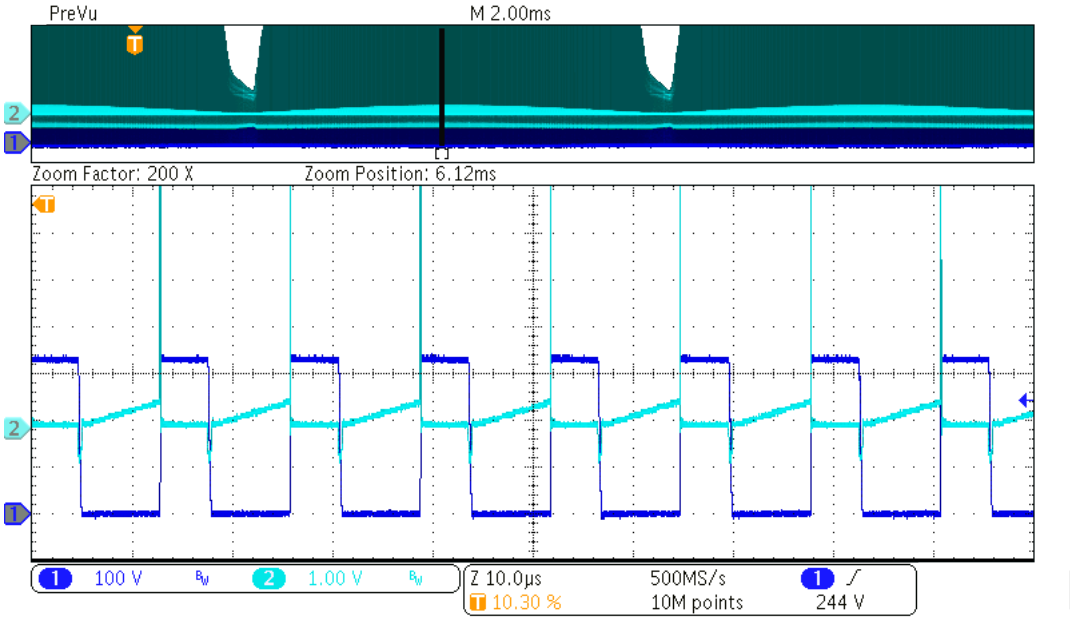


Figure 2-2. High Spike Voltage was Found on the R_{CS} When the Device Turns On and Off

One blocking diode (such as 1N4148) can be placed in series with the R_{CS} which is shown in Figure 2-3 to prevent a high-voltage spike on the CS pin to damage TI GaN from overvoltage stress.

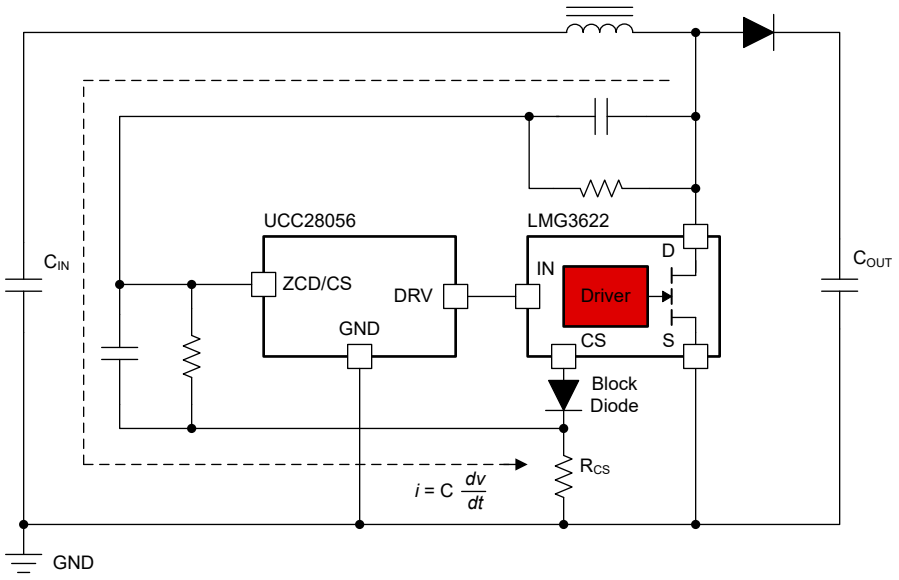


Figure 2-3. Blocking Diode in Series with R_{CS} to Prevent the Voltage Spike due to High Voltage Spike

Figure 2-4 shows the result on the CS pin with a blocking diode. The channel setting is:

- Ch1 is V_{DS} of LMG3622
- Ch2 is CS voltage of LMG3622.

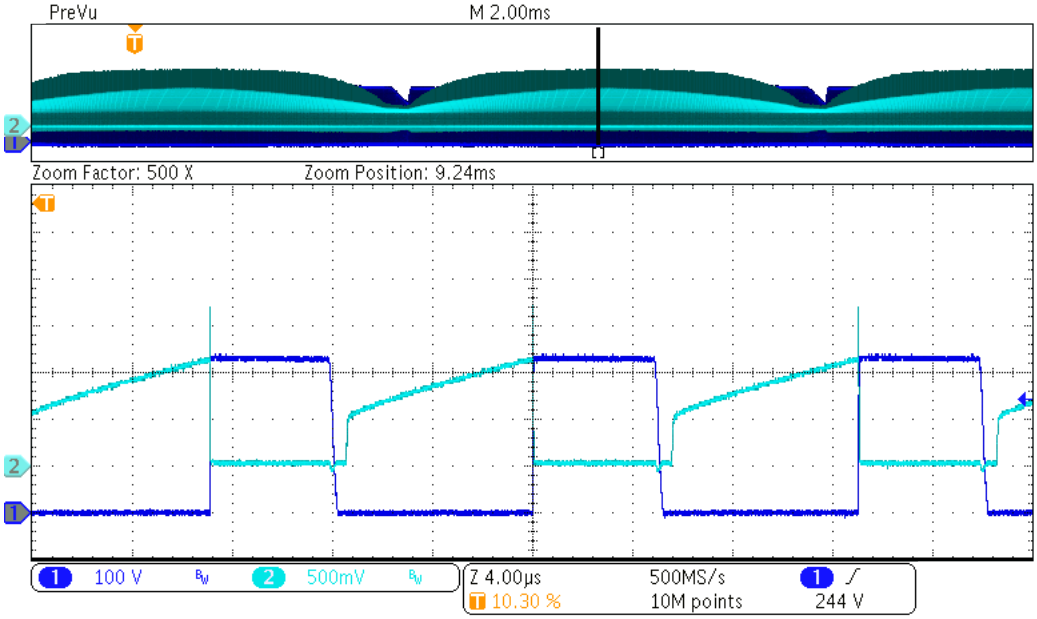


Figure 2-4. LMG3622 CS Pin Voltage With Block Diode

The circuit with high voltage on RCS has to implement the blocking diode by using the LMG362x device.

2.2.3 AHB Topology and the VCC Design

The DC-DC stage was designed with AHB topology. The DC transfer function of AHB is similar to buck topology and Equation 8 shows the transfer function.

$$\frac{V_{OUT}}{V_{IN}} = \frac{Duty}{N_{PS}} \quad (8)$$

where

- N_{PS} is the turn ratio between primary and secondary side

According to the transfer function, the system can only run when

$$V_{IN} > N_{PS} \times V_{OUT} \quad (9)$$

For better standby power and efficiency, turn off the PFC stage at low voltage and low power condition. Based on this application design, the turns ratio is 5.5, and $V_{OUT} \times N_{PS}$ is 154V which can be higher than the V_{IN} voltage (the maximum voltage at 90Vac is 127V) and the system does not operate correctly.

For normal operation the system is designed to power on the PFC stage during the start-up condition for period of time, and then turn off the PFC stage when the V_{OUT} is set as 5V or 9V.

Figure 2-5 shows the design concept by using 2pcs N-channel signal MOSFET as a load switch for the V_{CC} of the PFC stage. Through the 4s RC delay plus the start-up time of the AUX voltage, the PFC is powered on to make the AHB operate normally. The PFC remains turned on when the V_{OUT} > 12V when the output voltage is stable to pull the optotransistor low, but power off the PFC stage when the V_{OUT} < 12V.

In Figure 2-5 the V_{CC} load switch is designed to turn on the PFC stage for a period of time to make sure the whole system powers on successfully.

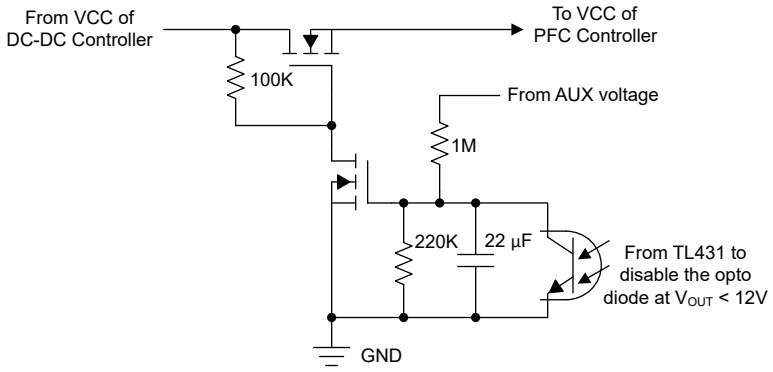


Figure 2-5. V_{CC} Load Switch Design for the PFC Stage

2.2.4 LMG2610 for AHB Topology

AHB is a half-bridge topology which provides the ZVS for the system. With proper design, the system can operate at around 50% duty cycle with lower the RMS current which means lower conduction loss. The best practice is to choose a higher $R_{DS(on)}$ device with lower $C_{O(TR)}$ to optimize the design.

Before the system starts-up, the system must turn on the low-side device to charge the high-side bootstrap capacitor and reset C_{RES}. When the system starts-up, the output voltage is 0V which means the magnetic inductance can be simulated as a shorted circuit and the system total inductance is L_{RES} only. The system suffers high reset current if the C_{RES} is not discharged properly. The system must put the main switching device at the high side.

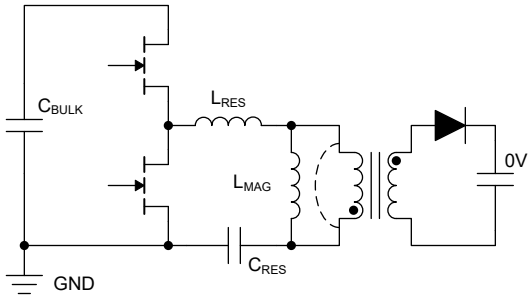


Figure 2-6. AHB Equivalent Circuit During Start-Up

The higher $R_{DS(on)}$ device with lower current limit inside the device helps to limit the charge voltage of C_{RES}, which reduces the reset current at the low side. Figure 2-7 shows the waveform of the start-up current. The channel setting is:

- Ch1: SW voltage of U102 (LMG2610)
- CH4: The transformer current

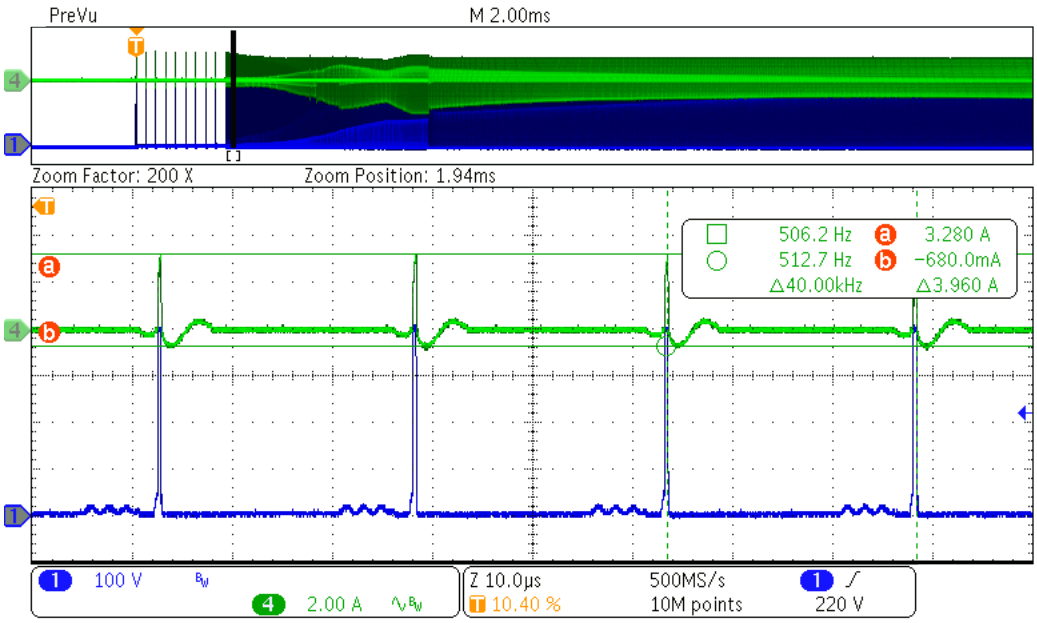


Figure 2-7. Start-Up Waveform With V_{OUT} is set as 28V and 5A Load Current

In Figure 2-7, the lower current limit of the high-side device prevents charging the C_{RES} too fast during the system start-up.

Before the system is stable, the low-side reset current is higher than the static state. Chooses lower $R_{DS(on)}$ to prevent the OCP was triggered and C_{RES} reset properly.

Figure 2-8 illustrates a lower $R_{DS(on)}$ is chosen to prevent the OCP from triggering and C_{RES} is reset properly.

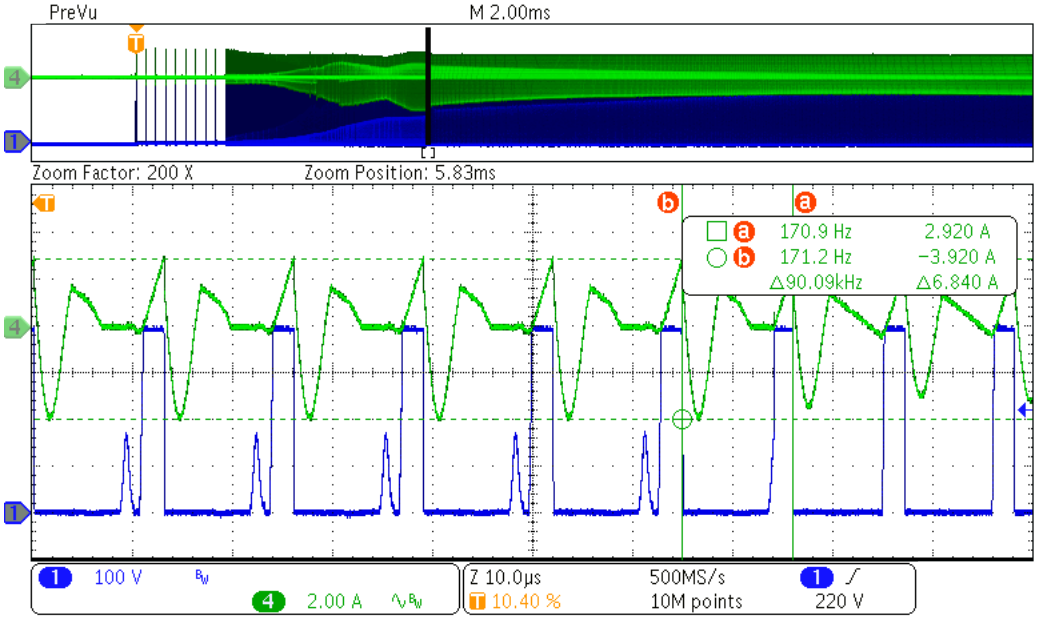


Figure 2-8. Start-Up Waveform With V_{OUT} is set as 28V and 5A Load Current

In this case, LMG2610 is an excellent match with the AHB topology with higher $R_{DS(on)}$ at the high side (248mΩ) and lower resistance at the low side (170mΩ) to balance the performance, and the cost.

2.3 Highlighted Products

2.3.1 UCC28056

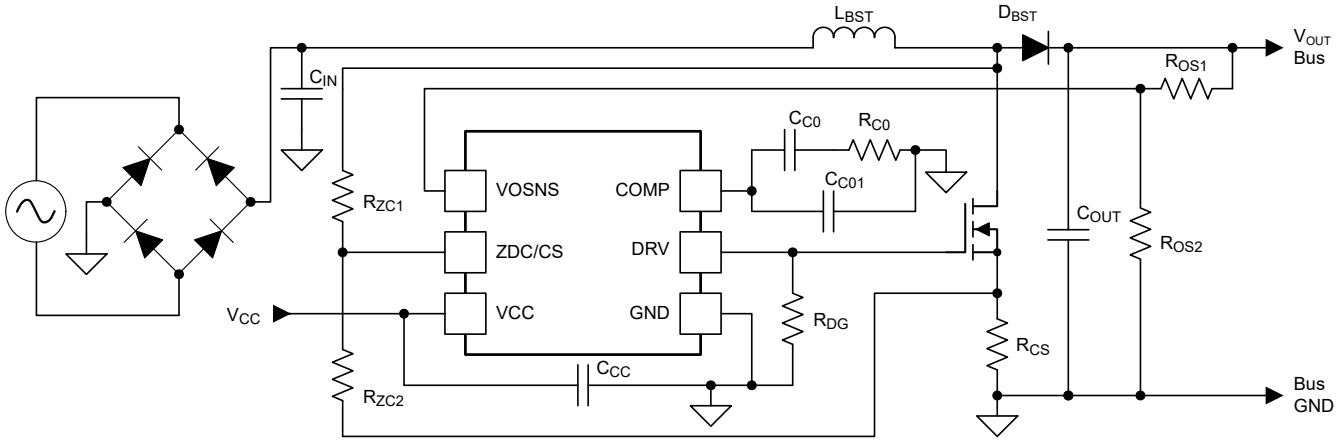


Figure 2-9. Simplified Application Circuit Diagram

The UCC28056 device drives PFC boost stages based on a mixed mode method that operates in TM and discontinuous conduction mode (DCM) at reduced load, automatically reducing switching frequency. This device incorporates burst mode operation to further improve light load performance, enabling systems to meet challenging energy standards while eliminating the need to switch off the PFC. UCC28056 can drive a PFC power stage up to 300W, providing a sinusoidal line input current with low distortion, close to unity power factor. These features along with FET drain valley turn-on with a simple boost inductor allows the lowest component count and reduced system cost.

- Excellent light load efficiency and high efficiency over a wide range of load due to multi-mode TM and DCM control
- Enables low system cost through FET drain valley synchronized turn-on which eliminates the need for a second winding on the boost inductor
- Burst mode with soft-entry and soft-exit periods enables ultra-low audible noise output
- Low start-up current consumption (< 46µA)
- Wide V_{CC} range 8.5V to 34V
- Cycle-by-cycle current limit
- Second independent OVP
- Integrated OTP

2.3.2 LMG3622

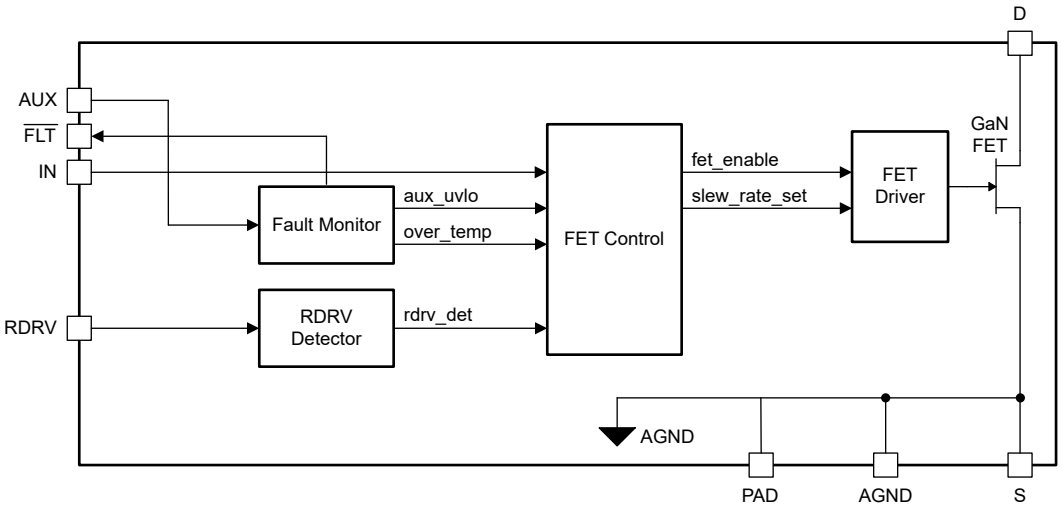


Figure 2-10. LMG3622 Functional Block Diagram

The LMG3622 is a 650V 120mΩ GaN power FET intended for switch-mode power-supply applications. The LMG3622 simplifies design and reduces component count by integrating the GaN FET and gate driver in a 8mm by 5.3mm QFN package.

Programmable turn-on slew rates provide EMI and ringing control. The current-sense emulation feature reduces power dissipation compared to the traditional current-sense resistor and allows the low-side thermal pad to be connected to the cooling PCB power ground.

Low quiescent currents and fast start-up times support converter light-load efficiency requirements and burst-mode operation.

Extended feature descriptions are provided in the following list:

- 650V, 120mΩ GaN power FET
- Integrated gate driver with low propagation delays and adjustable turn-on slew-rate control
- Current-sense emulation with high bandwidth and high accuracy
- Cycle-by-cycle overcurrent protection
- Overtemperature protection with FLT pin reporting
- AUX quiescent current: 240µA
- AUX standby quiescent current: 50µA
- Maximum supply and input logic pin voltage: 26V
- 8mm × 5.3mm QFN package with thermal pad

2.3.3 LMG2610

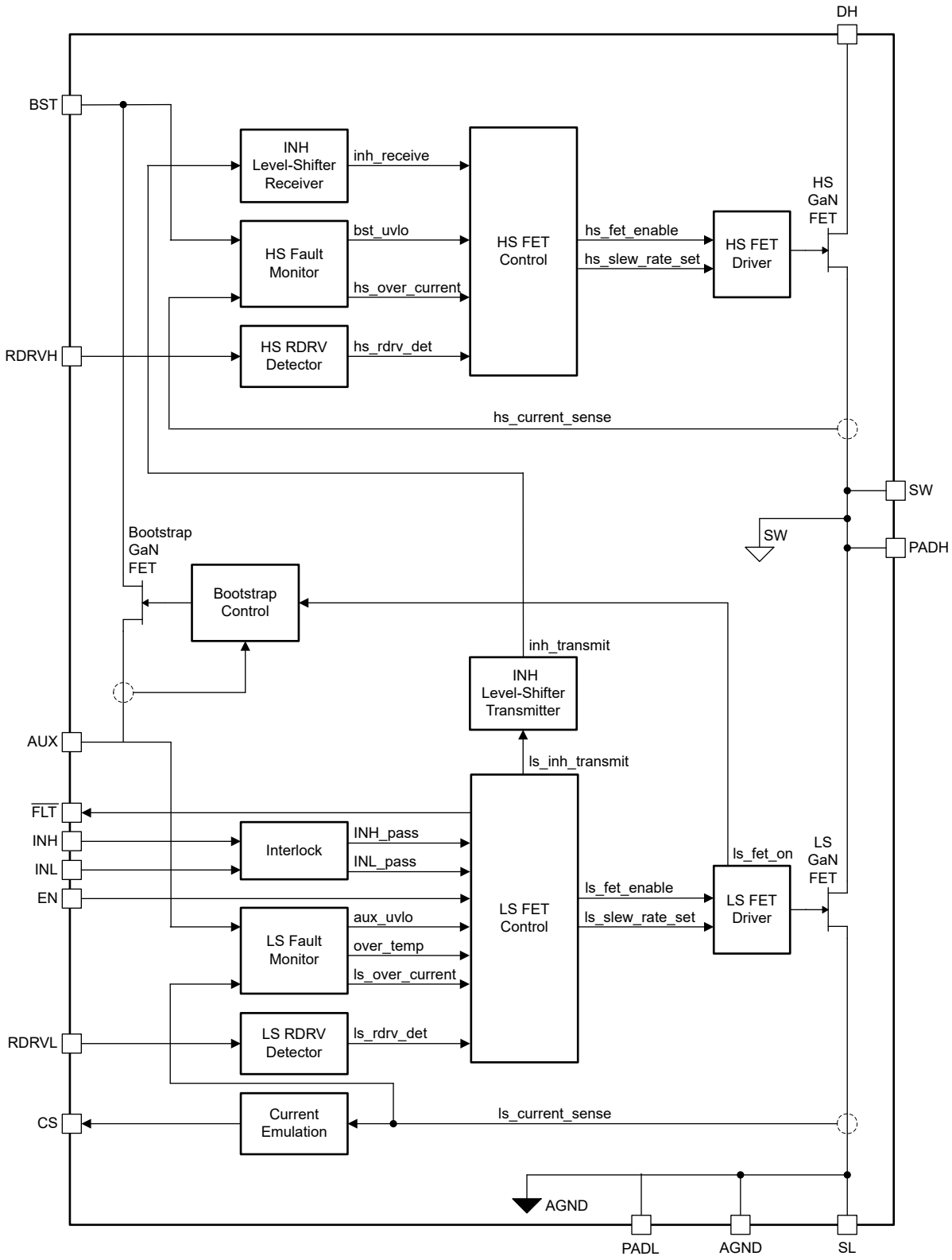


Figure 2-11. LMG2610 Function Block Diagram

The LMG2610 simplifies design, reduces component count, and reduces board space by integrating half-bridge GaN HEMT, gate drivers, bootstrap diode, and high-side gate-drive level shifter in a 9mm × 7mm QFN package.

The asymmetric GaN HEMT resistances are optimized for AHB operating conditions. Programmable turn-on slew rates provide EMI and ringing control.

The high-side gate-drive signal level shifter eliminates noise and burst-mode power dissipation problems found with external designs. The smart-switched GaN bootstrap FET has no diode forward-voltage drop, avoids overcharging the high-side supply, and has zero reverse-recovery charge.

The LMG2610 supports converter light-load efficiency requirements and burst-mode operation with low quiescent currents and fast start-up times. Protection features include FET turn-on interlock, undervoltage lockout (UVLO), cycle-by-cycle current limit, and overtemperature shut down.

- 650V GaN HEMT half bridge
- 170mΩ low-side and 248mΩ high-side GaN HEMT
- Integrated gate drivers with low propagation delays and adjustable turn-on slew-rate control
- Current-sense emulation with high-bandwidth and high accuracy
- Low-side, high-side gate-drive interlock
- High-side gate-drive signal level shifter
- Smart-switched bootstrap diode function
- Low-side, high-side cycle-by-cycle overcurrent protection
- AUX idle quiescent current: 240µA
- AUX standby quiescent current: 50µA
- BST idle quiescent current: 60µA
- Maximum supply and input logic pin voltage: 26V
- 9mm × 7mm QFN package with dual thermal pads

3 Hardware, Test Requirements, and Test Results

3.1 Hardware

Figure 3-1 and Figure 3-2 show the TIDA-050074 boards with overall dimensions of about 50mm × 73mm × 23mm.

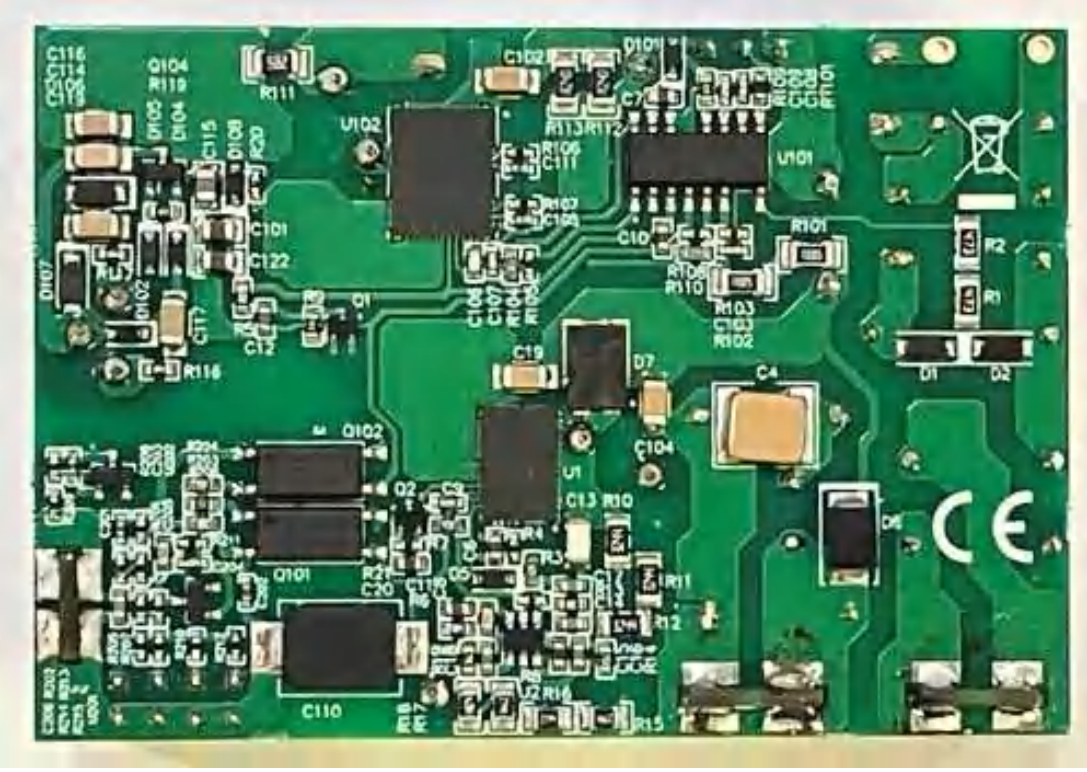


Figure 3-1. TIDA-050074 Bottom View

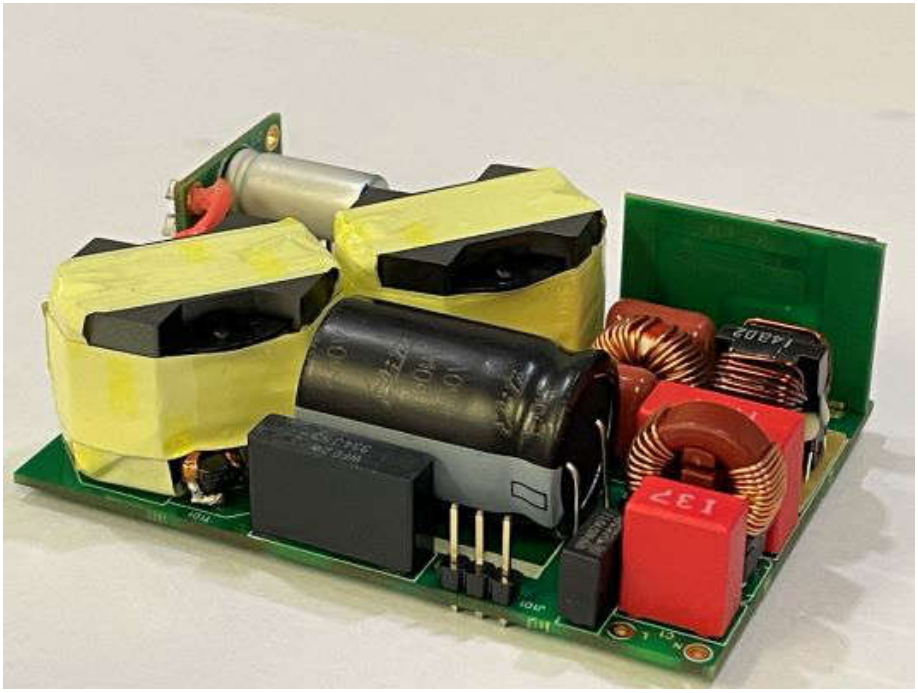


Figure 3-2. TIDA-050074 Angle View

3.2 Test Setup

The following test equipment is required when working with this reference design:

Voltage Source Isolated AC source or variable AC transformer capable of 264V_{RMS} and capable of handling 200W power level.

> **CAUTION**
> Do not apply DC voltage to this board when testing. Damage to equipment and components is possible.

Power Analyzer Capable of measuring 1mW to 200W of input power and capable of handling 264V_{RMS} input voltage. Some power analyzers can require a precision shunt resistor for measuring input current to measure input power of 5W or less. Read the user manual for the power analyzer for proper measurement setups for full power and for stand-by power.

Oscilloscope > 4-channel, 500MHz bandwidth. Probes capable of handling 600V.

Current probe > 15A DC or AC current probe for oscilloscope.

Load To obtain the full load current 3.00A from 5V, 9V, and 5A from 15V, 20V and 28V. The output voltage can be obtained from C121 to eliminate the cable drop.

This remainder of this section describes the test setup of the reference design board.

> **WARNING**
> This reference design is not encapsulated and there are accessible voltages that are greater than 50V_{DC}. Use appropriate handling precautions to avoid injury.

The AC input power goes through the power analyzer to support the reference design board. Connect the output ports to the electric load to monitor the output condition. TIDA-050074 was design for 5V–28V which is set with the jumper from J201 to J204.

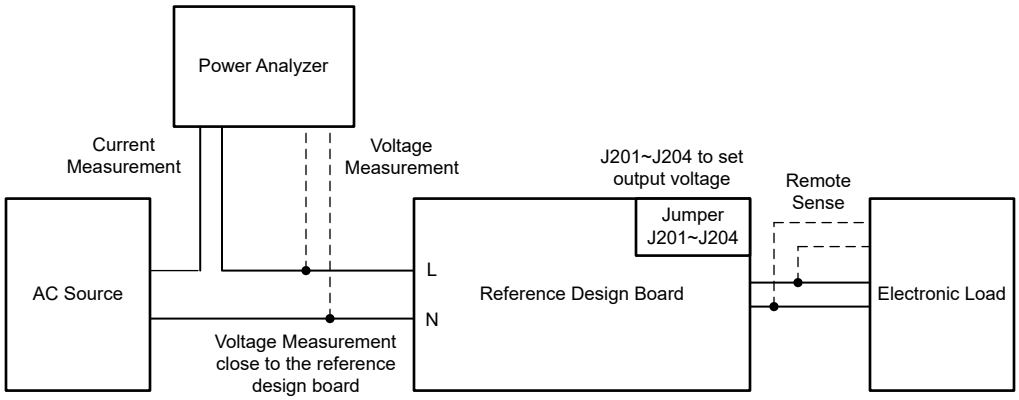


Figure 3-3. Test Setup Diagram

This reference design is a compact design without test points. Connect the AC inlet on the L and N of the board close to F1 and C1. Place the voltage sense of the power analyzer close to L and N which is shown in Figure 3-3. Adjust the input voltage and read the power analyzer for the right input voltage to eliminate the effect of the AC cable drop. Read the input power with the average or integration function from the power analyzer.

Figure 3-4 illustrates the AC input and voltage sense from the power meter connected close to the reference design board.

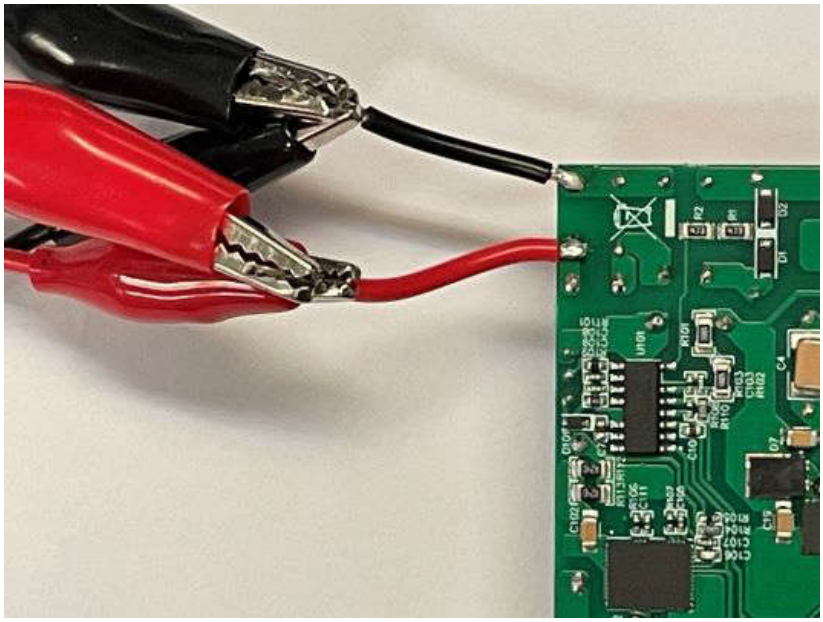


Figure 3-4. AC Input Connection Setting

Connect the output wires on the output (VOUT and RTN). Solder 2 wires on the output (VOUT and RTN) which is connected to the electronic load. Solder another 2 wires on the lead of C121 which is connected to the remote sense of the electronic load to eliminate the loss of the cable drop.

Figure 3-5 shows V_{OUT} and RTN connected to E-load and remote sense connects from the lead of C121.

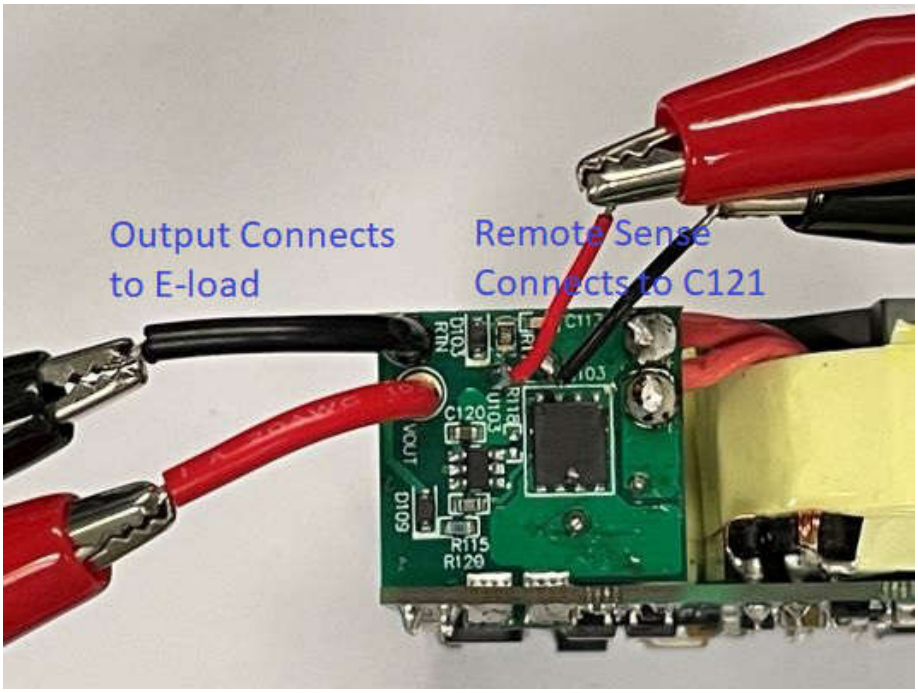


Figure 3-5. Output Connection

Table 3-1 details the output jumper settings for the output voltage through the jumper. Turn off the AC power source and make sure the voltage on the board is fully discharged before changing the output voltage setting.

Table 3-1. Output Jumper Settings

V_{OUT}	J201	J202	J203	J204
5V	NC	NC	NC	NC
9V	Jumper	NC	NC	NC
15V	Jumper	Jumper	NC	NC
20V	Jumper	Jumper	Jumper	NC
28V	Jumper	Jumper	Jumper	Jumper

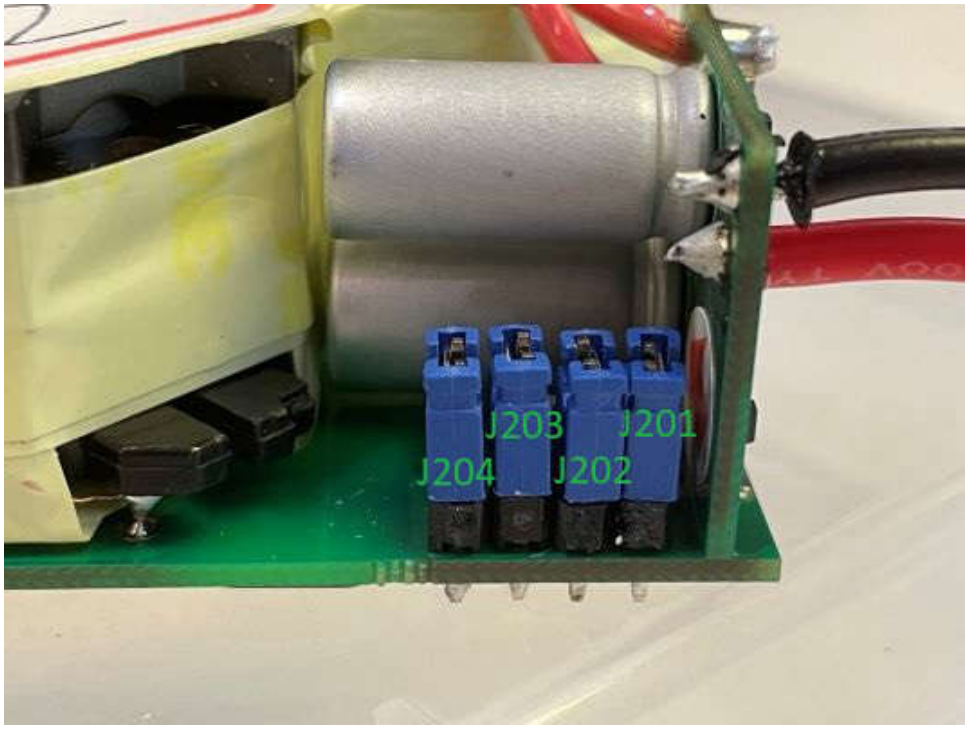


Figure 3-6. Jumper for the V_{OUT} Setting

3.3 Test Results

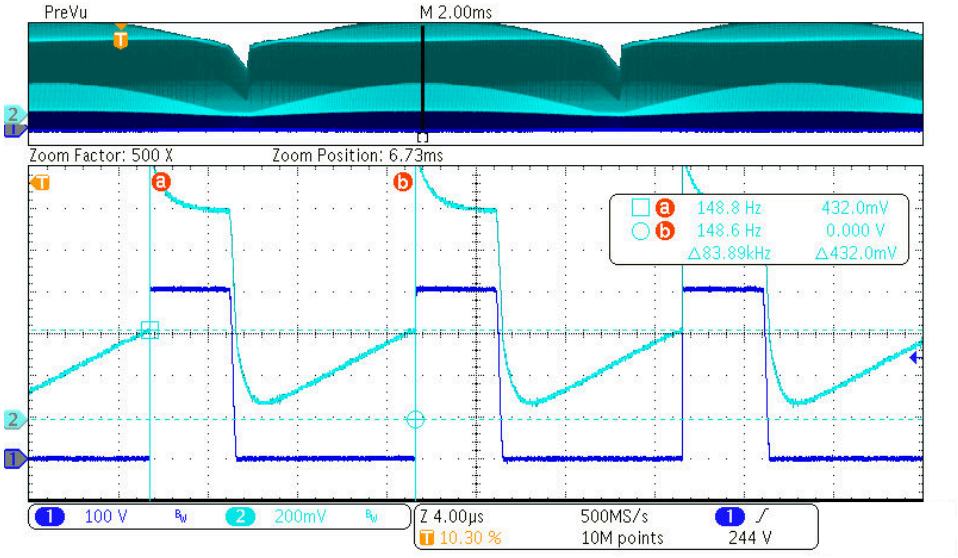
3.3.1 Switching Waveform

3.3.1.1 Switching Waveform on the PFC Stage

The PFC stage was measured at 140W full load condition. The waveform of V_{DS} and ZCD/CS pin was captured close to UCC28056 to confirm the operation of the PFC controller and TI-GaN.

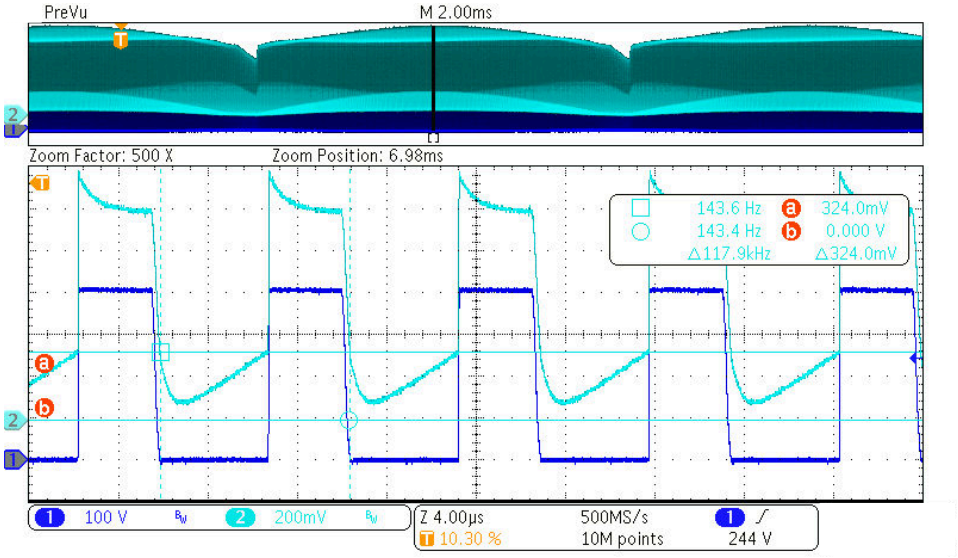
The channel setting of Figure 3-7 to Figure 3-12 is:

- Ch1: VDS voltage of the U1 (LMG3622)
- CH2 is the ZCD/CS voltage of U2 (UCC28056)



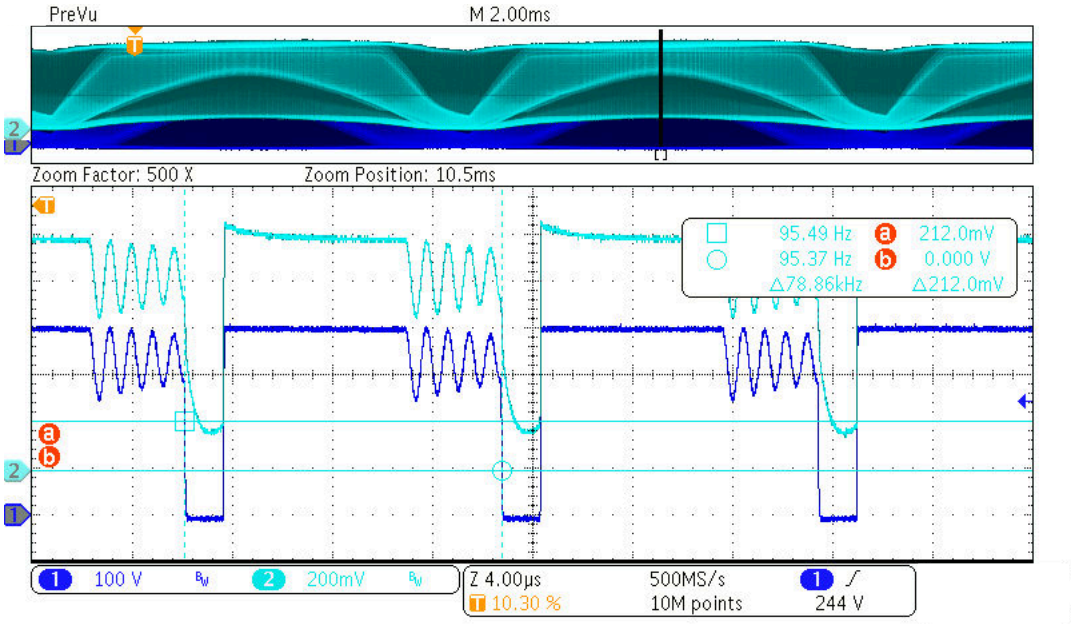
The operation frequency is 83.8kHz. The system works in CrM.

Figure 3-7. Switching Waveform of PFC Stage at 90Vac Input and 140W Load



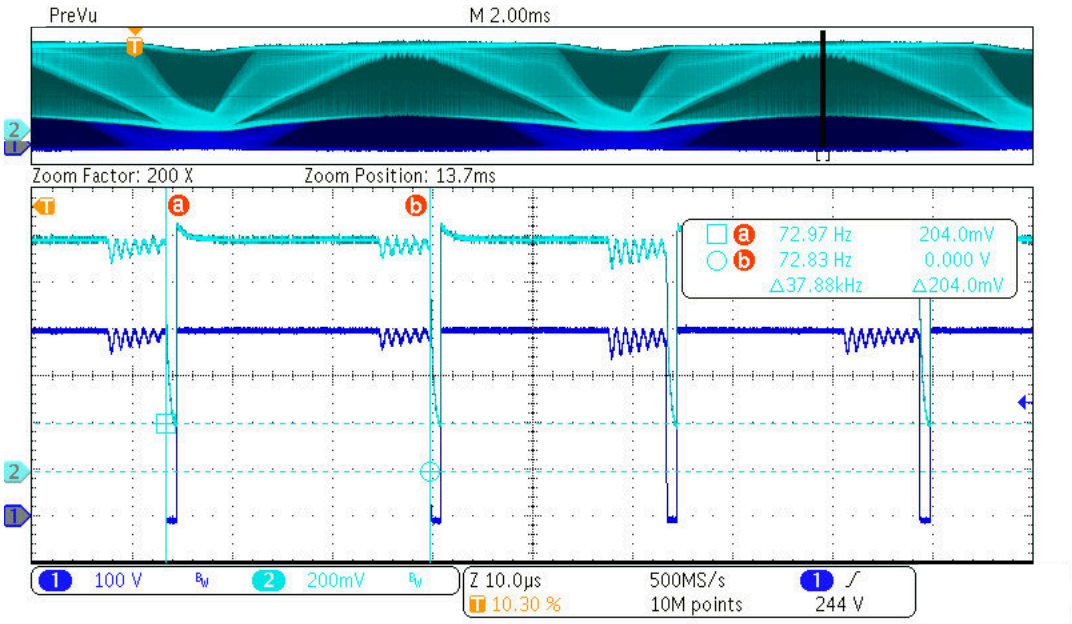
The operation frequency is 117.9kHz. The system works in CrM.

Figure 3-8. Switching Waveform of PFC Stage at 115Vac Input and 140W Load



The operation frequency is 78.86kHz. The system works in DCM.

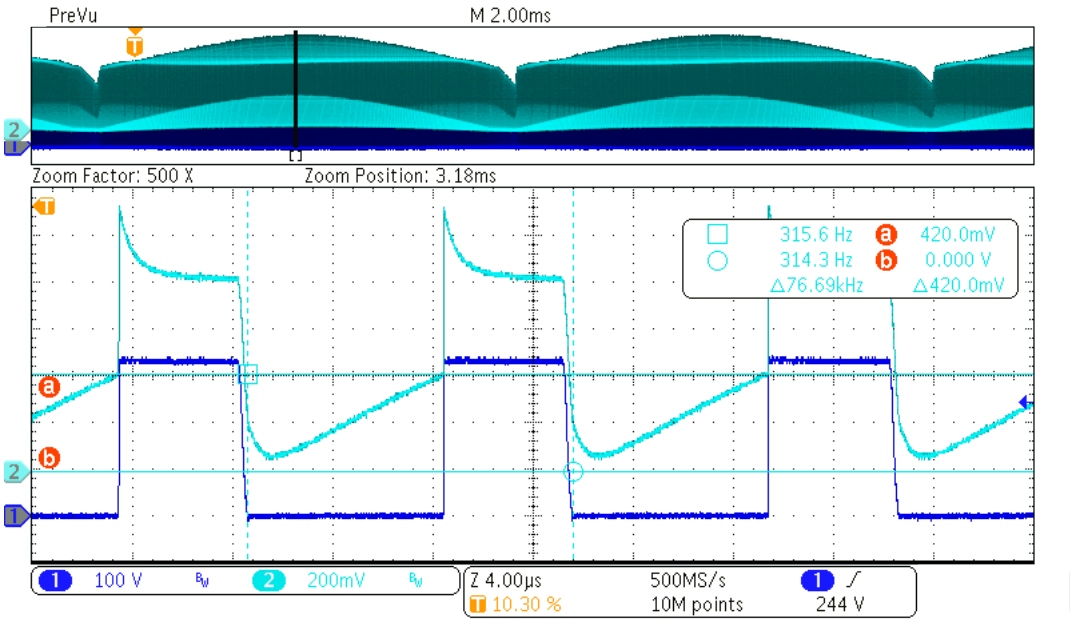
Figure 3-9. Switching Waveform of PFC Stage at 230Vac Input and 140W Load



The operation frequency is 37.88kHz. The system works in DCM.

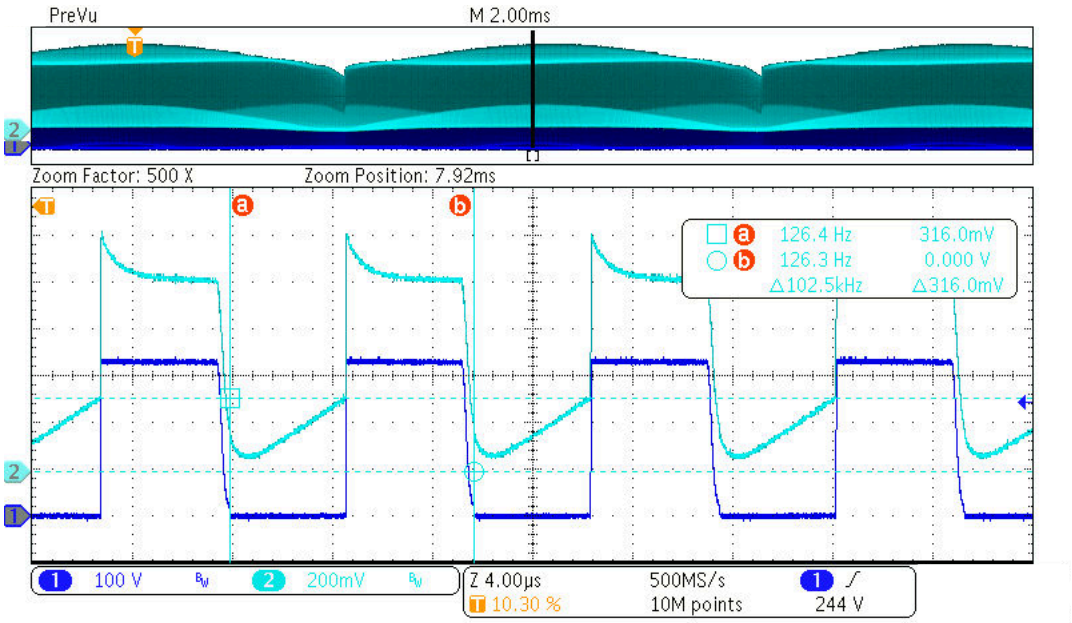
Figure 3-10. Switching Waveform of PFC Stage at 264Vac Input and 140W Load

When the output voltage of the PFC is lower, the duty cycle and the operation frequency are lower.



The PFC output voltage is set as 320V. The operation frequency is 76.69kHz. The system works in CrM.

Figure 3-11. Switching Waveform of PFC Stage at 90Vac Input and 140W Load



The PFC output voltage is set as 320V. The operation frequency is 102.5kHz. The system works in CrM.

Figure 3-12. Switching Waveform of PFC Stage at 115Vac Input and 140W Load

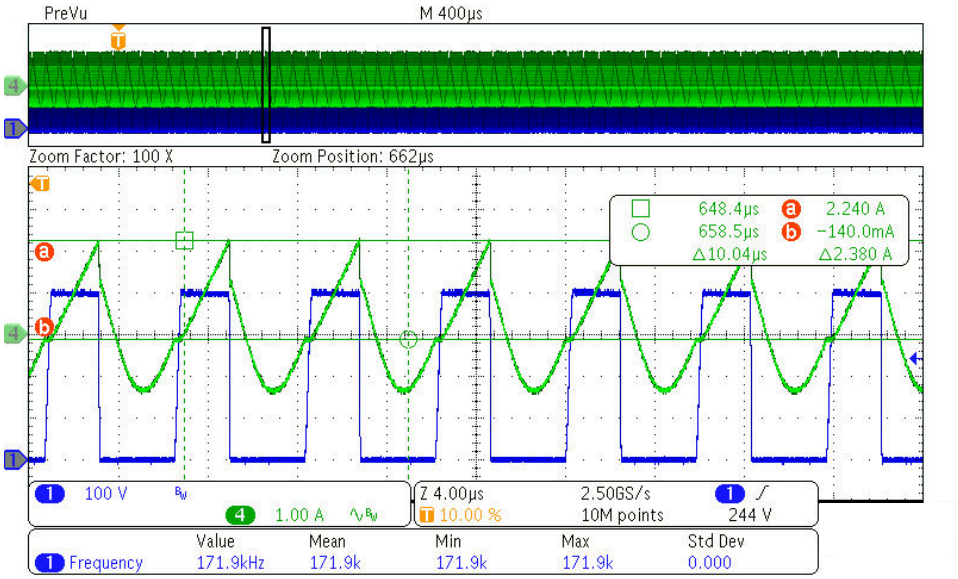
3.3.1.2 Switching Waveform on the AHB Stage

For output voltage is 15V, 20V, and 28V, the PFC is always on and the bulk cap voltage is not related to the input voltage. The waveform of V_{DS} and the transformer current was captured at full load based on different output voltage.

The channel setting for Figure 3-13 to Figure 3-22 is:

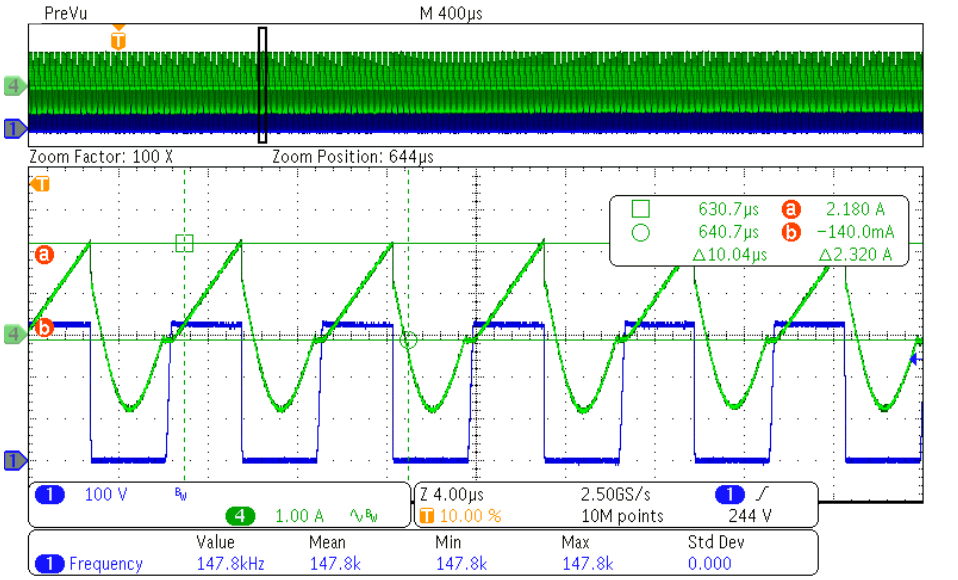
- Ch1: SW (V_{DS} of low side device) voltage
- Ch4: The transformer current

The conditions for Figure 3-13 and Figure 3-14 are 28V–5A, 140W.



The operation frequency is about 171.9kHz.

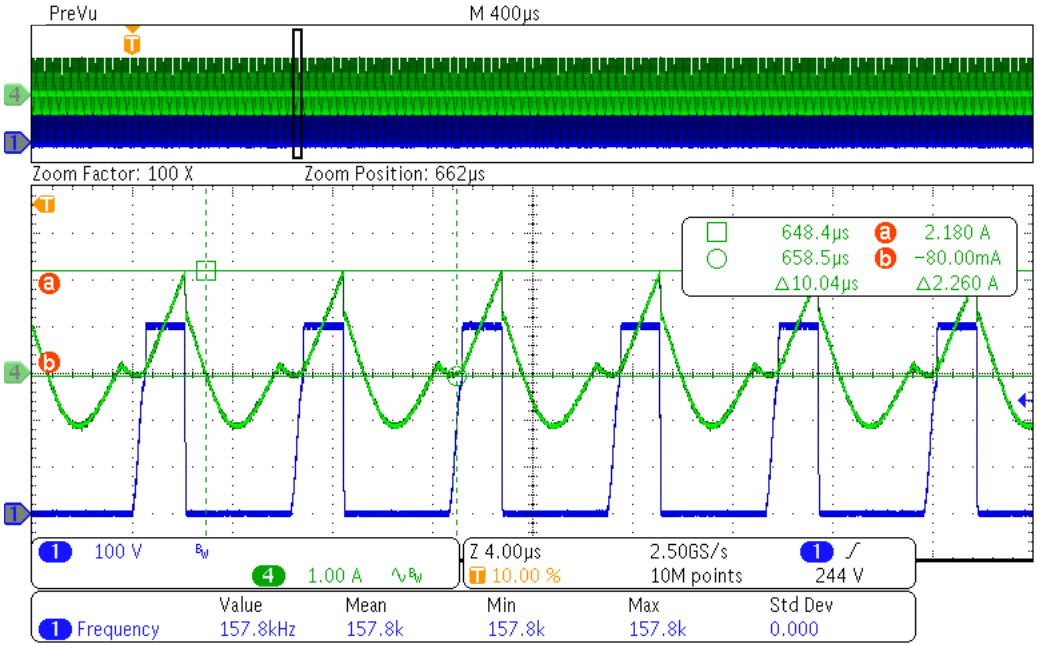
Figure 3-13. 28V–5A AHB Switching Waveform (V_{PFC} = 390V)



The operation frequency is about 147.8kHz.

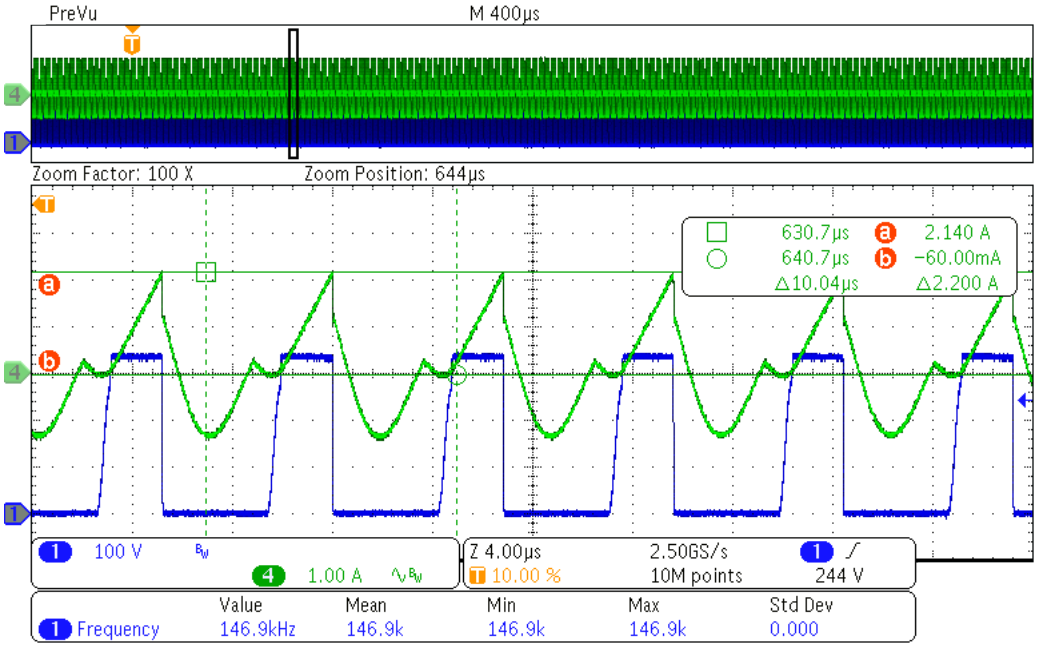
Figure 3-14. 28V–5A AHB Switching Waveform (V_{PFC} = 320V)

The conditions for Figure 3-15 and Figure 3-16 are 20V–5A (100W).



The operation frequency is about 157.8kHz.

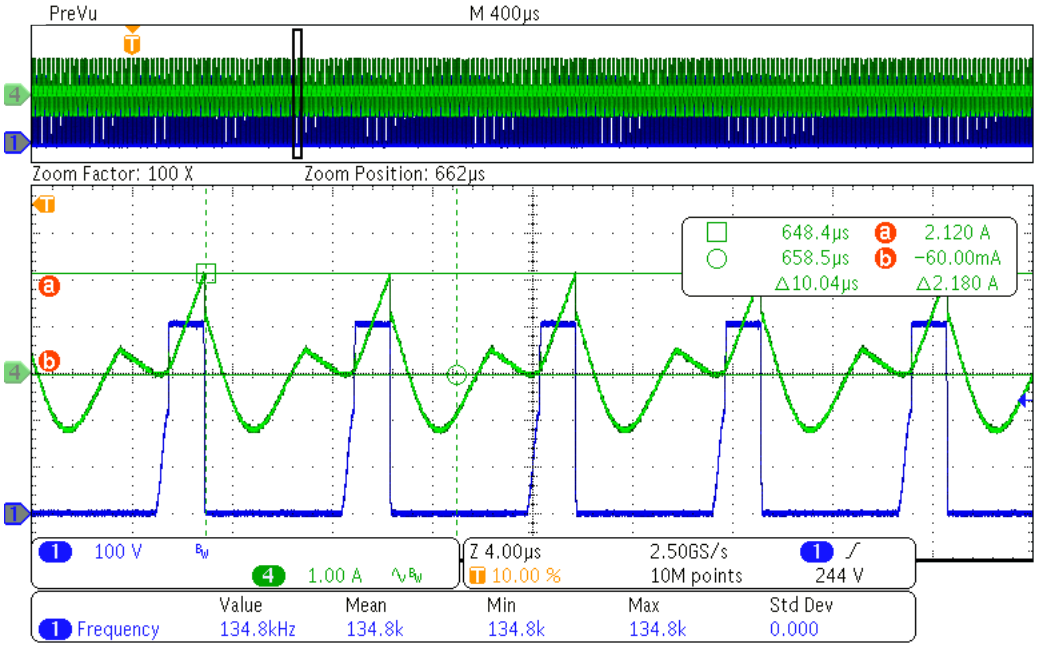
Figure 3-15. 20V–5A AHB Switching Waveform (V_{PFC} = 390V)



The operation frequency is about 146.9kHz.

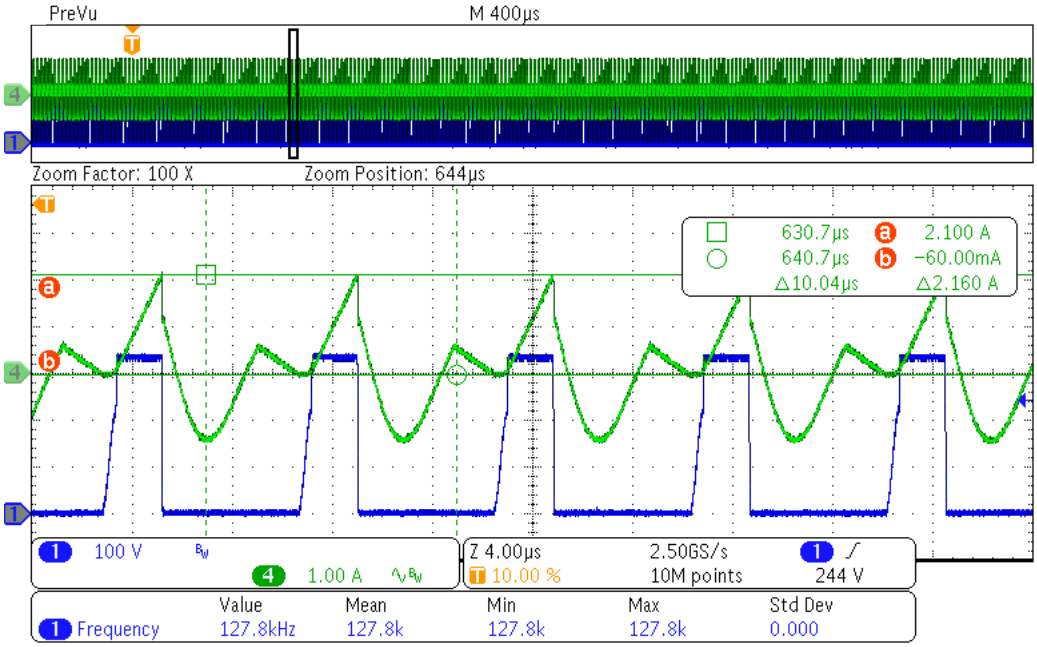
Figure 3-16. 20V–5A AHB Switching Waveform (V_{PFC} = 320V)

The conditions for Figure 3-17 and Figure 3-18 are 15V–5A (75W).



The operation frequency is about 134.8kHz.

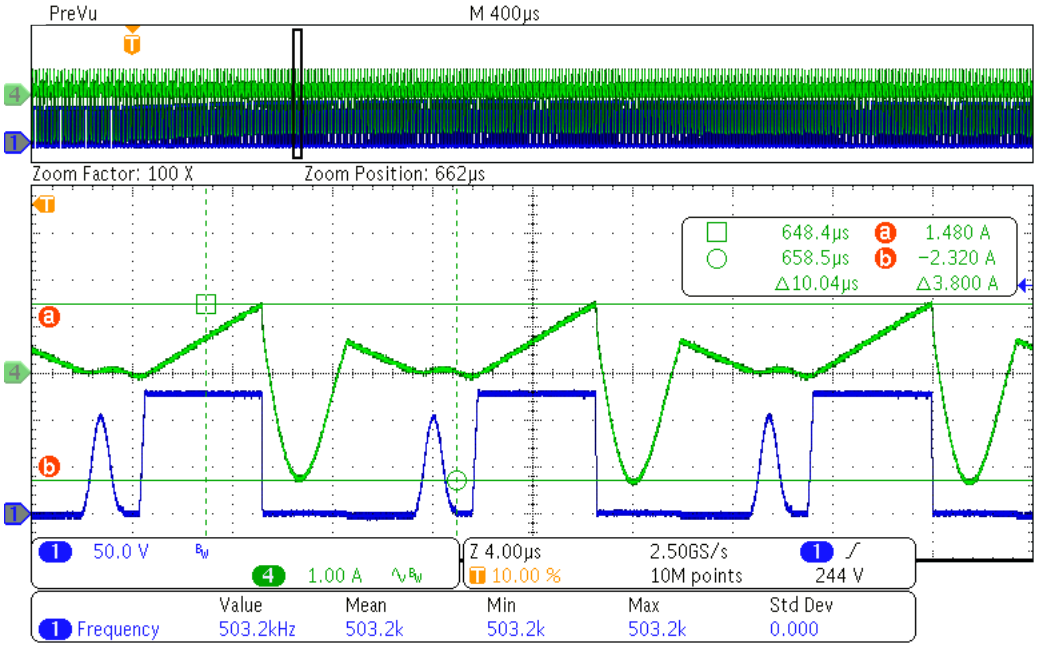
Figure 3-17. 15V–5A AHB Switching Waveform (V_{PFC} = 390V)



The operation frequency is about 134.8kHz.

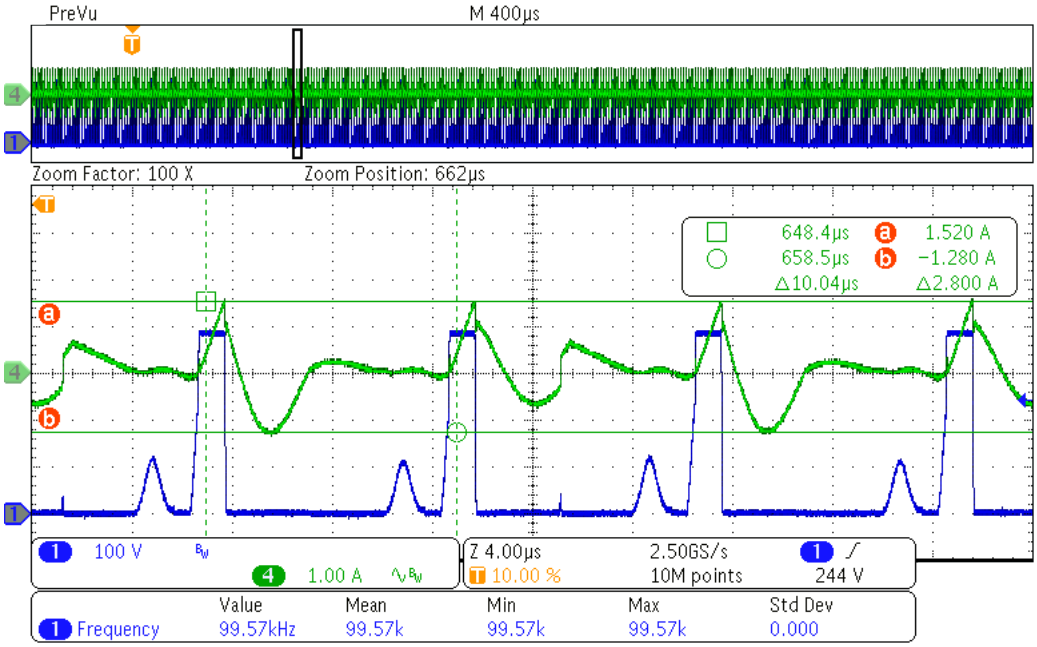
Figure 3-18. 15V–5A AHB Switching Waveform (V_{PFC} = 320V)

The conditions for Figure 3-19 and Figure 3-20 are 9V–3A (27W).



The operation frequency is about 74.1kHz.

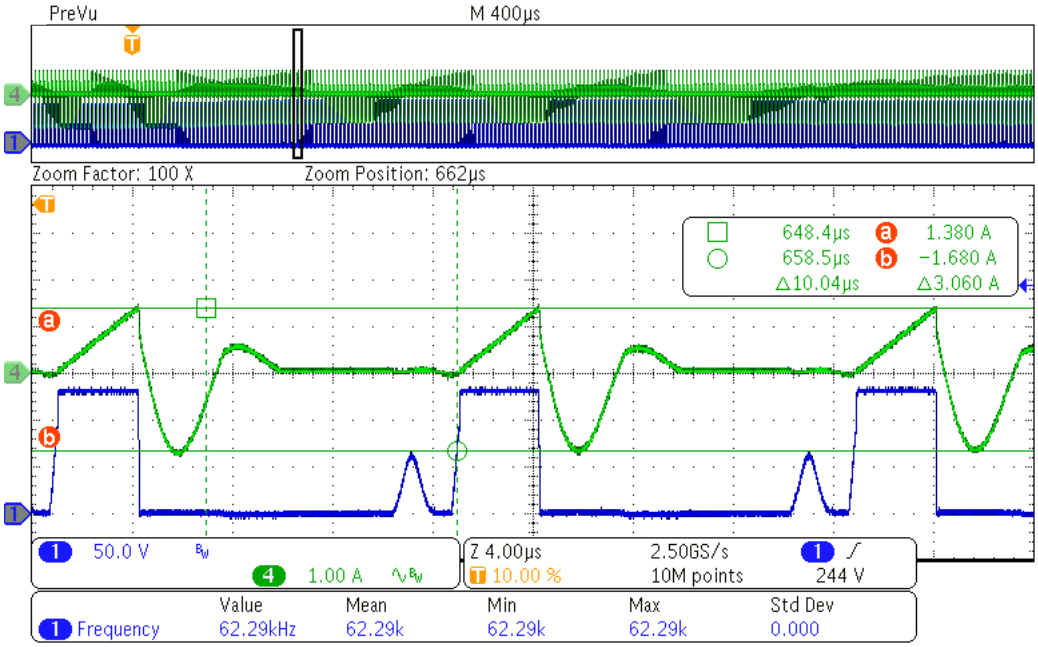
Figure 3-19. 9V–3A AHB Switching Waveform at 90Vac Input



The operation frequency is about 99.57kHz.

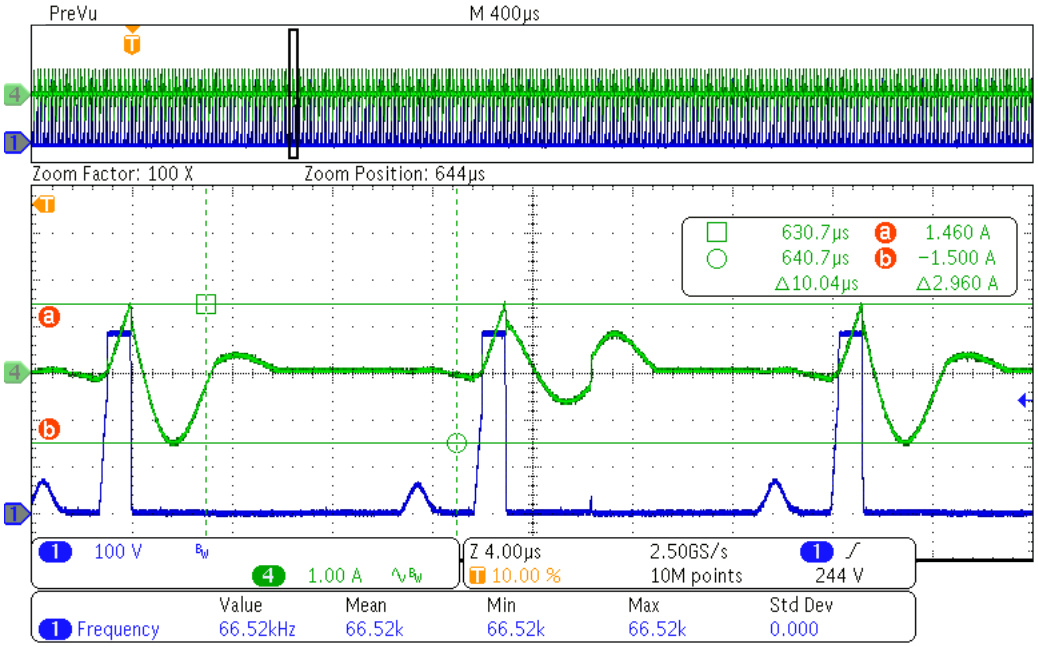
Figure 3-20. 9V–3A AHB Switching Waveform at 264Vac Input

The conditions for Figure 3-21 to Figure 3-22 are 5V–3A (15W).



The operation frequency is about 62.3kHz.

Figure 3-21. 5V–3A AHB Switching Waveform at 90Vac Input



The operation frequency is about 66.52kHz.

Figure 3-22. 5V–3A AHB Switching Waveform at 264Vac Input

3.3.2 Efficiency Test Result

The efficiency result tested burn-in at 100% load conditions at room temperature for 30 minutes, then the load was decreased to 75%, 50%, 25% and 10% load in 5-minute increments to make the system stable. Read the input power by integrated the energy for 1 minute.

The test results at 28V are shown in Table 3-2 to Table 3-5.

Table 3-2. 28V Efficiency Result at 115Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN}(W)	EFFICIENCY
100%	27.934	5.0093	139.93	148.18	94.43%
75%	27.935	3.7501	104.76	111.31	94.12%
50%	27.938	2.4889	69.535	74.517	93.31%
25%	27.939	1.2459	34.810	37.558	92.68%
10%	27.939	0.4959	13.856	15.306	90.53%
				Average Efficiency	93.64%

Table 3-3. 28V Efficiency Result at 230Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{OUT} (W)	EFFICIENCY
100%	27.934	5.0093	139.93	146.31	95.64%
75%	27.935	3.7501	104.76	110.03	95.21%
50%	27.936	2.4891	69.535	73.715	94.33%
25%	27.938	1.2460	34.810	37.144	93.72%
10%	27.939	0.4959	13.856	15.135	91.55%
				Average Efficiency	94.72%

Table 3-4. 28V Efficiency Result at 115Vac Input (VPFC is set as 320V)

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	27.934	5.0093	139.93	147.83	94.66%
75%	27.935	3.7501	104.76	110.70	94.63%
50%	27.938	2.4890	69.538	74.253	93.65%
25%	27.938	1.2459	34.808	37.825	92.02%
10%	27.939	0.4968	13.881	15.604	88.96%
				Average Efficiency	93.74%

Table 3-5 shows the efficiency test results at 28V and 90Vac input and full load.

Table 3-5. 28V Efficiency Result at 90Vac Input

V_{PFC} (V)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
390V	27.934	5.0089	139.92	149.77	93.42%
320V	27.933	5.0095	139.93	149.47	93.62%

Figure 3-23 shows the 28V efficiency comparison curve.

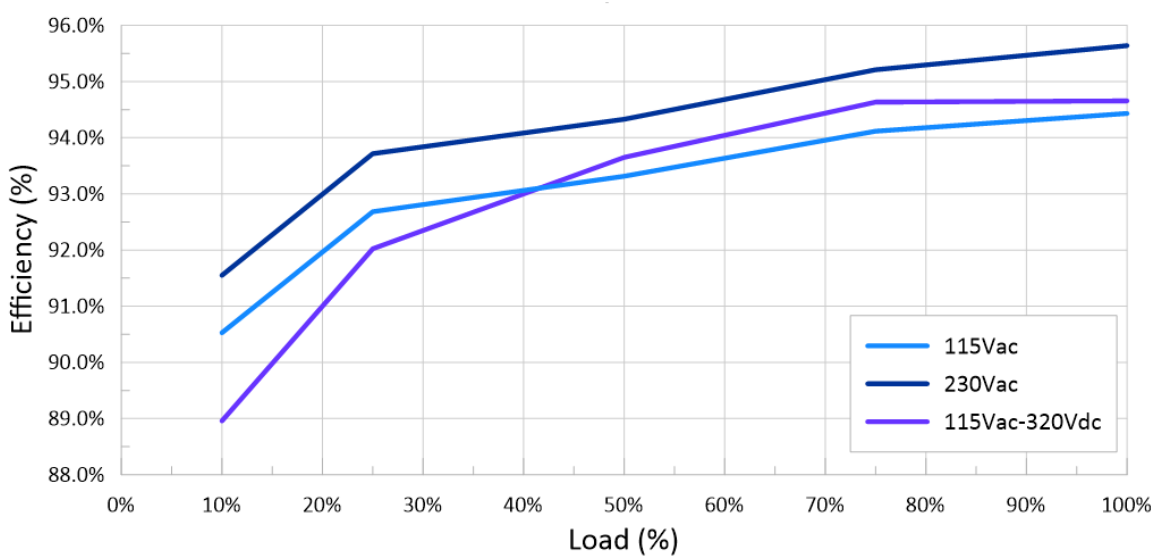


Figure 3-23. Efficiency Result at V_{OUT} = 28V

Table 3-6 and Table 3-7 shows the test results at 20V.

Table 3-6. 20V Efficiency Result at 115Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	20.060	4.9960	100.22	106.730	93.90%
75%	20.060	3.7509	75.244	80.339	93.66%
50%	20.063	2.4898	49.953	53.836	92.79%
25%	20.063	1.2468	25.015	27.187	92.01%
10%	20.064	0.4968	9.969	11.068	90.07%
				Average Efficiency	93.09%

Table 3-7. 20V Efficiency Result at 230Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	EFFICIENCY
100%	20.060	4.9950	100.200	105.500	94.98%
75%	20.060	3.7512	75.249	79.464	94.70%
50%	20.061	2.4910	49.971	53.278	93.79%
25%	20.061	1.2469	25.014	26.894	93.01%
10%	20.061	0.4969	9.968	10.783	92.44%
				Average Efficiency	94.12%

Figure 3-24 shows the 20V efficiency comparison curve.

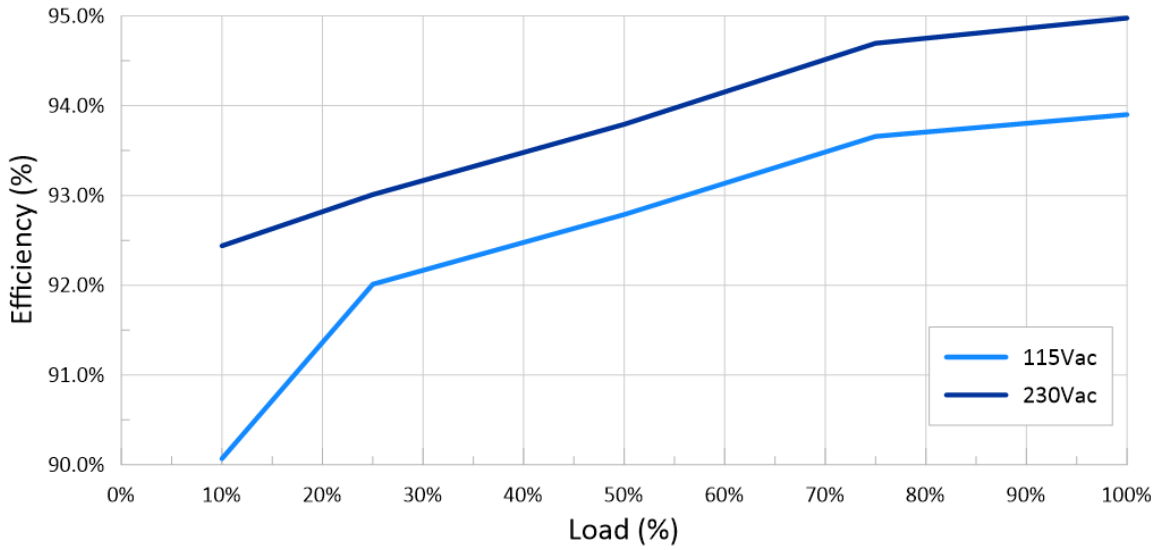


Figure 3-24. Efficiency Result at V_{OUT} = 20V

Table 3-8 and Table 3-9 show the test results at 15V.

Table 3-8. 15V Efficiency Result at 115Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	15.121	5.0114	75.778	81.572	92.90%
75%	15.124	3.7509	56.728	61.308	92.53%
50%	15.125	2.4909	37.675	40.949	92.00%
25%	15.125	1.2469	18.859	20.692	91.14%
10%	15.125	0.4969	7.515	8.527	88.13%
				Average Efficiency	92.14%

Table 3-9. 15V Efficiency Result at 230Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	15.123	5.0117	75.792	80.679	93.94%
75%	15.123	3.7518	56.738	60.662	93.53%
50%	15.125	2.4907	37.672	40.469	93.09%
25%	15.125	1.2477	18.872	20.467	92.21%
10%	15.121	0.4969	7.513	8.226	91.34%
				Average Efficiency	93.19%

Figure 3-25 shows the 15V efficiency comparison curve.

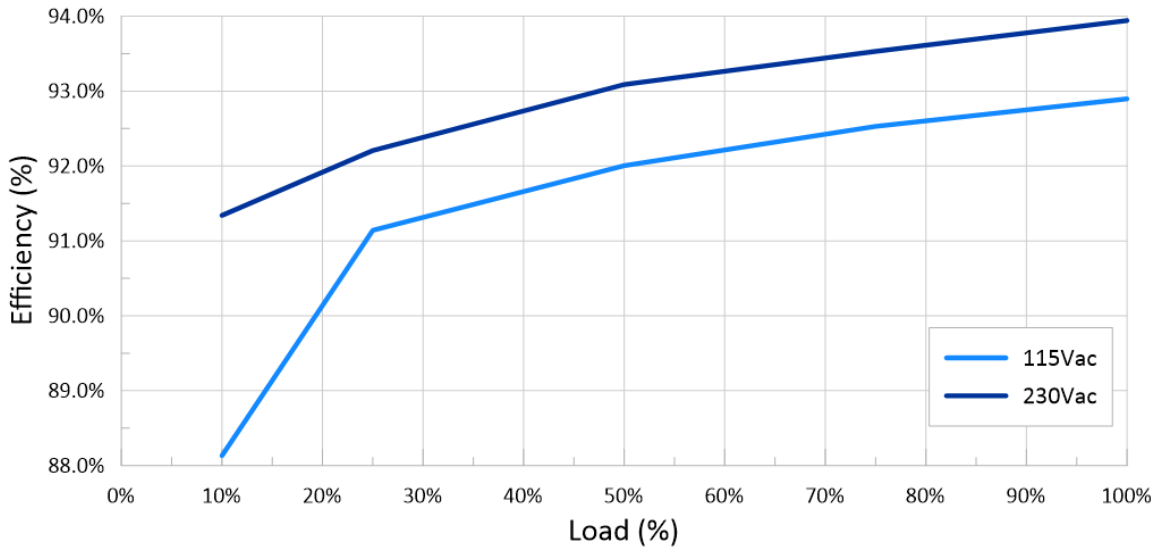


Figure 3-25. Efficiency Result at V_{OUT} = 15V

Table 3-10 and Table 3-11 show the test results at 9V.

Table 3-10. 9V Efficiency Result at 115Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	9.0925	2.9991	27.269	29.639	92.00%
75%	9.0925	2.2490	20.449	22.422	91.20%
50%	9.0938	1.4986	13.628	14.953	91.14%
25%	9.0938	0.7488	6.809	7.689	88.56%
10%	9.0925	0.2987	2.716	3.037	89.73%
				Average Efficiency	90.73%

Table 3-11. 9V Efficiency Result at 230Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	9.0925	2.9992	27.270	29.398	92.76%
75%	9.0925	2.2491	20.450	22.078	92.63%
50%	9.0925	1.4988	13.628	14.972	91.02%
25%	9.0938	0.7490	6.811	7.826	87.03%
10%	9.0913	0.2989	2.718	3.152	86.20%
				Average Efficiency	90.86%

Figure 3-26 shows the 9V efficiency comparison curve.

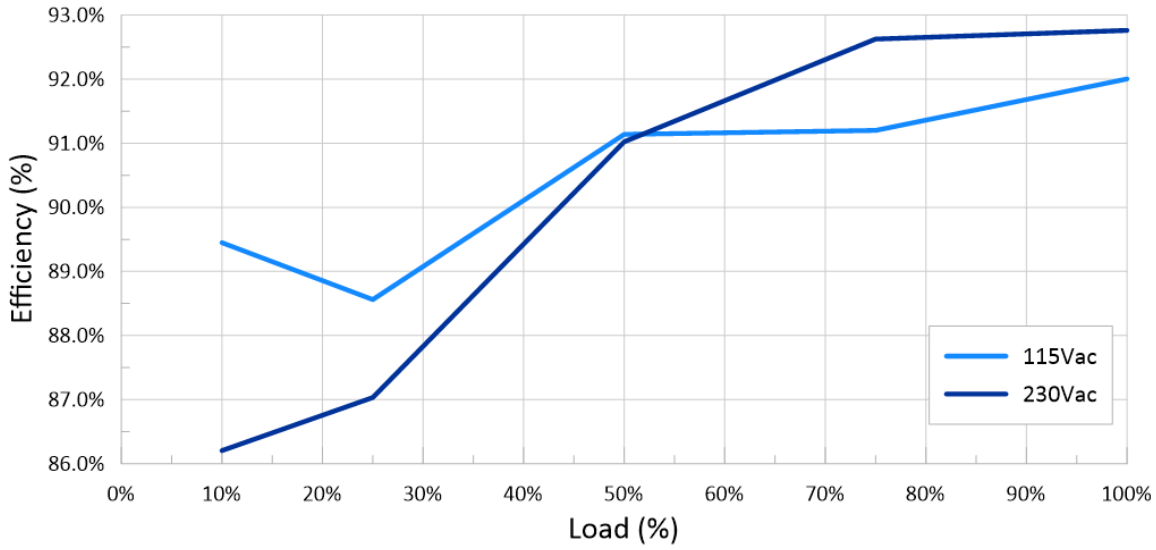


Figure 3-26. Efficiency Result at V_{OUT} = 9V

Table 3-12 and Table 3-13 show the test results at 5V.

Table 3-12. 5V Efficiency Result at 115Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	5.1688	2.9997	15.505	16.999	91.21%
75%	5.1700	2.2495	11.630	12.816	90.75%
50%	5.1700	1.4992	7.751	8.698	89.12%
25%	5.1663	0.7474	3.862	4.540	85.06%
10%	5.1688	0.2993	1.547	1.867	82.89%
				Average Efficiency	89.03%

Table 3-13. 5V Efficiency Result at 230Vac Input

LOAD	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{IN} (W)	EFFICIENCY
100%	5.1700	2.9988	15.504	17.021	91.09%
75%	5.1700	2.2493	11.629	13.304	87.41%
50%	5.1700	1.4989	7.7492	8.9764	86.33%
25%	5.1700	0.7490	3.8722	4.8724	79.47%
10%	5.1688	0.2989	1.5448	1.9854	77.81%
				Average Efficiency	86.07%

Figure 3-27 shows the 5V efficiency comparison curve.

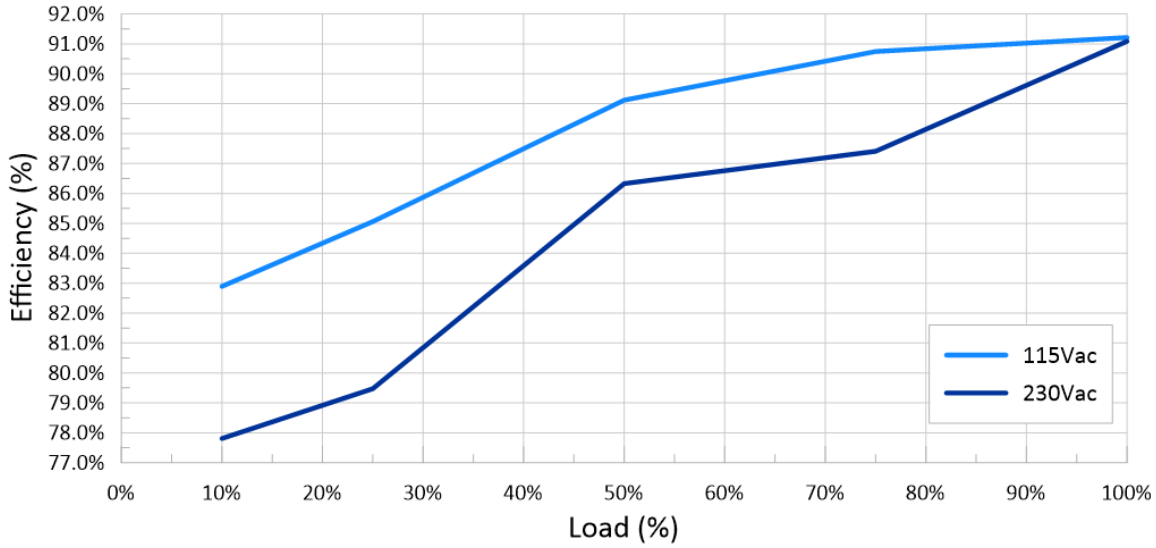


Figure 3-27. Efficiency Result at V_{OUT} = 5V

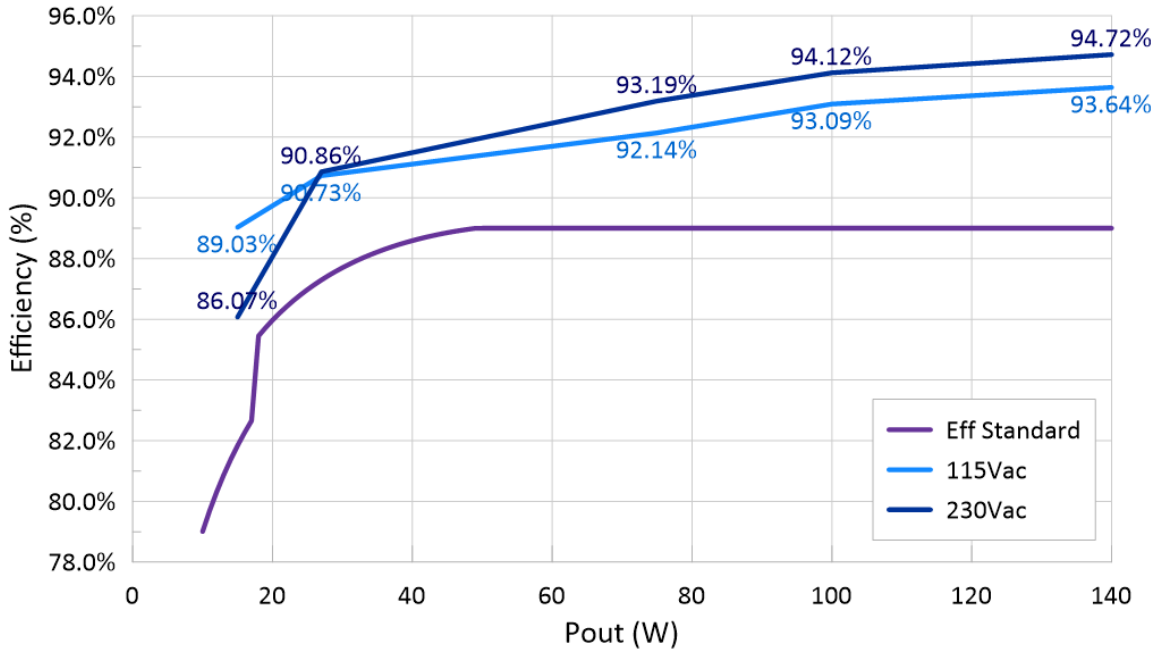


Figure 3-28. Average Efficiency Result of 4 points

3.3.3 Thermal Test Result

The worst case of the thermal result was at full load (28V, 5A) condition. The system burn in was for > 50 minutes at room temperature with the thermal camera.

Table 3-14 shows the thermal test results.

Table 3-14. Thermal Result at 28V-5A Load Condition

V_{IN}	V_{PFC}	LMG2610	AHB CONTROLLER	LMG3622	PFC DIODE
90V, 50Hz	390V	92.9°C	95.2°C	100.9°C	99.5°C
90V, 50Hz	320V	96.1°C	87.9°C	98.2°C	98.9°C
115Vac, 60Hz	390V	88.1°C	90.0°C	85.8°C	90.2°C
115Vac, 60Hz	320V	92.1°C	82.9°C	84.8°C	90.2°C
230Vac, 50Hz	390V	80.7°C	80.7°C	70.8°C	74.8°C
264Vac, 63Hz	390V	79.5°C	97.7°C	68.8°C	72.3°C

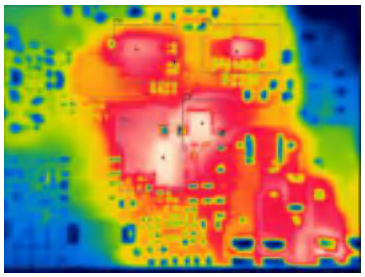


Figure 3-29. Thermal Result at V_{IN} = 90Vac, 50Hz (V_{PFC} = 390V)

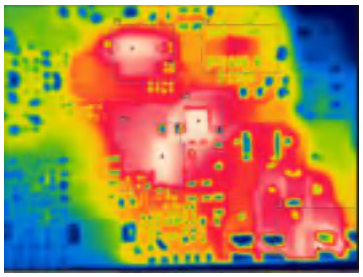


Figure 3-30. Thermal Result at V_{IN} = 90Vac, 50Hz (V_{PFC} = 320V)

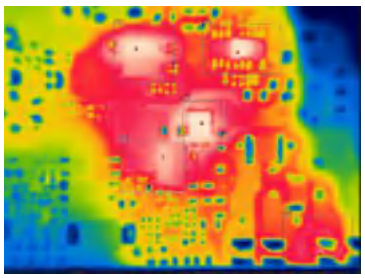


Figure 3-31. Thermal Result at V_{IN} = 115Vac, 60Hz (V_{PFC} = 390V)

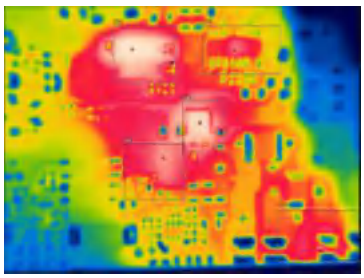


Figure 3-32. Thermal Result at V_{IN} = 115Vac, 60Hz (V_{PFC} = 320V)

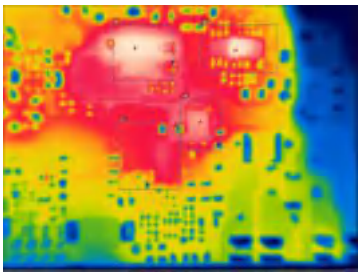


Figure 3-33. Thermal Result at V_{IN} = 230Vac, 50Hz (V_{PFC} = 390V)

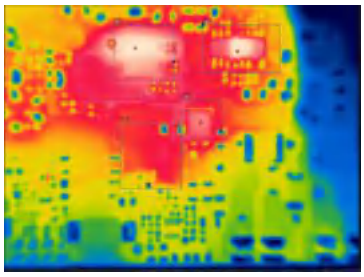


Figure 3-34. Thermal Result at V_{IN} = 264Vac, 63Hz (V_{PFC} = 390V)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050074.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050074.

4.1.3 Layout Prints {Optional Section}

4.2 Tools

SLUC641	UCC28056x Design Calculator

4.3 Documentation Support

1. Texas Instruments, *LMG3622 650V 120mΩ GaN FET With Integrated Driver, Protection and Current Sensing Data Sheet*
2. Texas Instruments, *LMG2610 Integrated 650V GaN Half Bridge for Active-Clamp Flyback Converters Data Sheet*
3. Texas Instruments, *UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

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