Design Guide: TIDA-050073

3.8V to 30V input, 3A, 1.2V low-output-ripple power supply with second stage filter reference design

Description

This low ripple power supply reference design supports a 1.2V output voltage at up to 3A of current from a 3.8V to 30V input. Such a low ripple voltage is required for many applications such as ADC, RF transceiver, and analog front end (AFE). Using the TPS62933F power converter combined with a second stage LC filter enables a very simple low ripple power design to create a 1.2V output voltage at 3A currents.

Resources

TIDA-050073	Design Folder
TPS62933F	Product Folder

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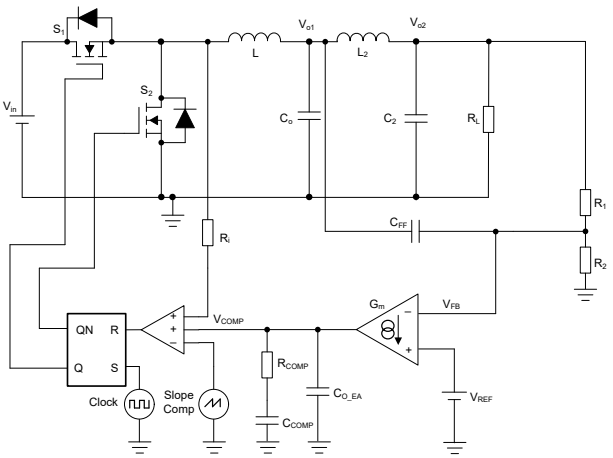
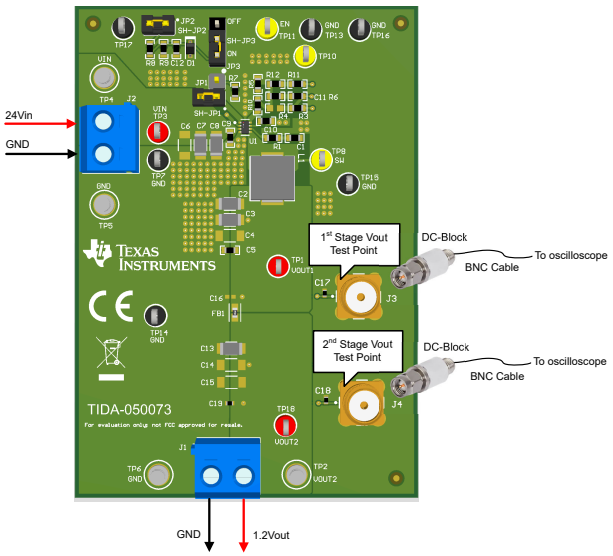
Features

- <1mV low output ripple peak to peak amplitude
- Wide input voltage range of 3.8V to 30V
- Up to 3A continuous output current
- Peak current control mode with internal compensation
- Operating junction temperature: –40°C to 150°C

Applications

- Test and Measurement
- Medical
- Wireless Infrastructure





1 System Description

The TIDA-050073 enables a very simple low output ripple step-down regulator design where the second stage filter is used with TPS62933F synchronous buck converter. This design demonstrates a low output ripple power supply to generate a 1.2V rail at up to 3A of current from 3.8V to 30V input voltage. The optimized internal loop compensation eliminates external compensation components. Low ripple voltage is required for many applications such as ADC, RF transceiver and analog front end (AFE).

Table 1-1. Key System Specifications

Design Parameter	Example Value
Input voltage range	24V nominal, 3.8V to 30V
Output voltage range	1.2V
Switching frequency	500kHz
Transient response, 50% load step	ΔV_O = ±5%
Output ripple voltage	<1mV
Output current rating	3A

2 System Overview

2.1 Block Diagram

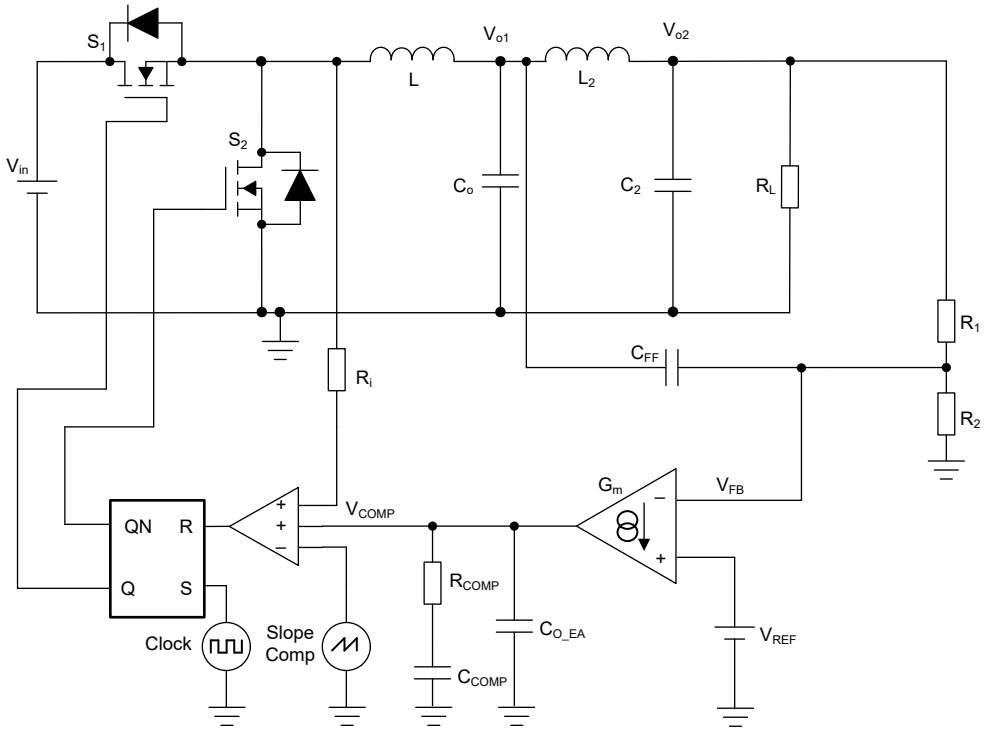


Figure 2-1. TIDA-050073 Block Diagram

2.2 Design Considerations

Low ripple and low noise normally indicate two different features of power supply. Ripple refers to the output voltage variation with switching frequency, which is measured by scope and reduced by using second stage LC filter. Noise normally refers to the voltage variation in frequency range of 100Hz-100kHz, which is usually measured with noise spectrum and limited by unique IC design. For some application which only requires low ripple but not low noise, a second stage LC filter design method is proposed for general purpose peak current mode buck regulators.

Figure 2-2 shows the scheme of buck converter with second stage filter. A second-order low pass filter is formed by inductor L2 and capacitor C2. A new pair of conjugate poles is introduced with the filter, which can reduce the output voltage ripple and noise at switching frequency through the high frequency gain attenuation. The selection method of inductor L2 and capacitor C2 are analyzed in the application note.

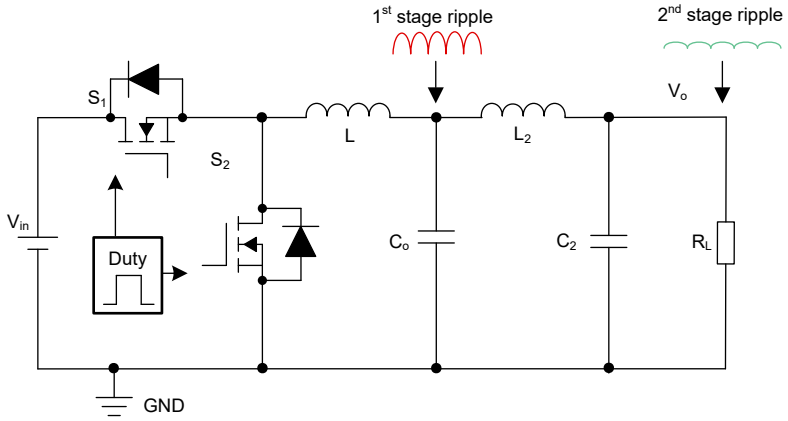


Figure 2-2. Buck Converter with Second Stage Filter

Figure 2-3 to Figure 2-5 show the schemes of power designs with second stage filter, correspond to the power designs with first stage sense, second stage sense and hybrid sense. The following summarizes advantages and disadvantages of each design.

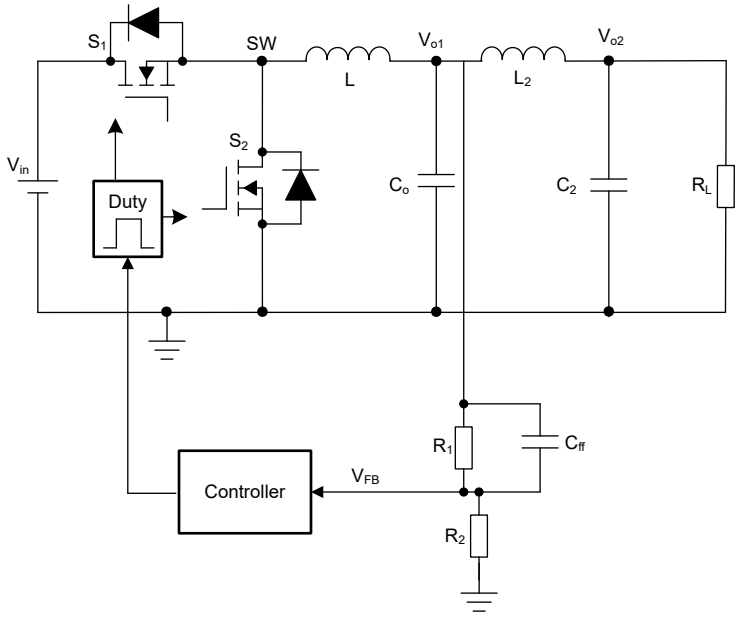


Figure 2-3. Scheme of Converter Second Stage Filter Design with First Stage Sense

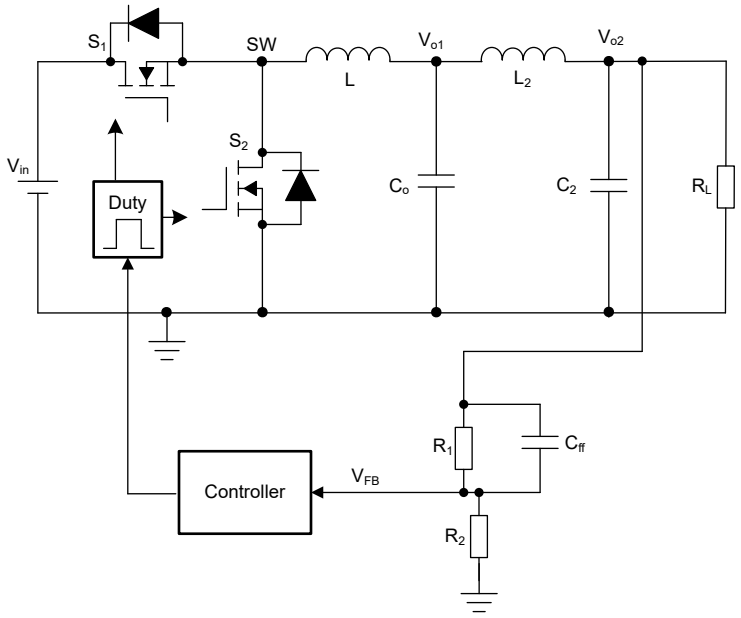


Figure 2-4. Scheme of Converter Second Stage Filter Design with Second Stage Sense

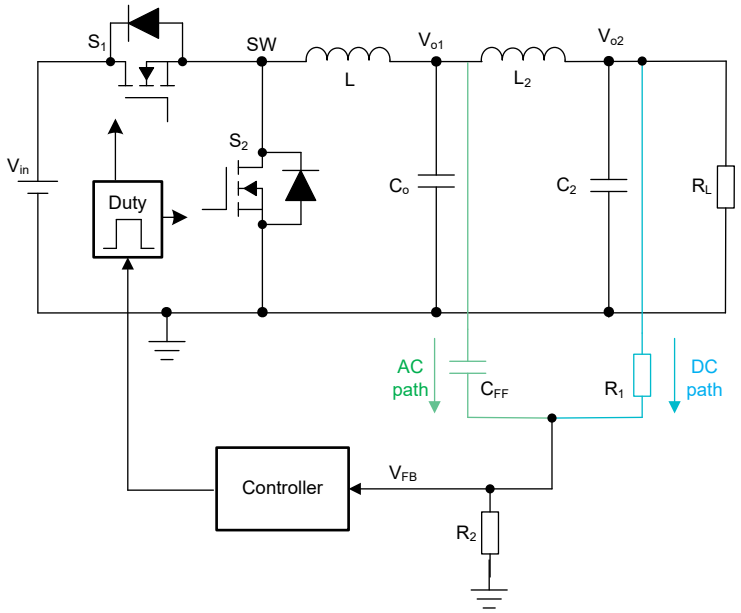


Figure 2-5. Scheme of Converter Second Stage Filter Design with Hybrid Sense

- With first stage sense, the feedback sense point is Vo1 and the voltage drop on DCR of L2 can't be compensated, so load regulation performance is worse. But the stability is good as the double poles of second stage filter are not included in the control loop.
- With second stage sense, the voltage drop on DCR of L2 can be compensated. But the double poles of second stage filter can have obvious impacts on the loop response. When the values of L2 and C2 become larger, the double poles frequency of second stage filter reduces and can be closer to bandwidth, which can cause less phase margin and possible instability. That limits the maximum value of second stage filter components selection and the ability to reduce output ripple.
- With hybrid sense, the feed forward capacitor Cff is connected with Vo1 and upper feedback resistor R1 is connected with Vo2. The AC disturbance of Vo1 can be coupled to VFB and reduce the portion of Vo2 AC disturbance in total feedback. That can help to reduce the effects of second stage filter on loop stability. And the load regulation performance is also good since the DC regulation is based on feedback from Vo2. So the loop stability and output accuracy can be made sure of at the same time with the hybrid feedback sense.

Due to the obvious advantages of hybrid sense, the reference design is based on this sense approach.

Figure 2-6 shows the TIDA-050073 Block Diagram, using a PCM buck converter TPS62933F with second stage filter and hybrid sense. The application note discusses how to analyze hybrid sense loop stability.

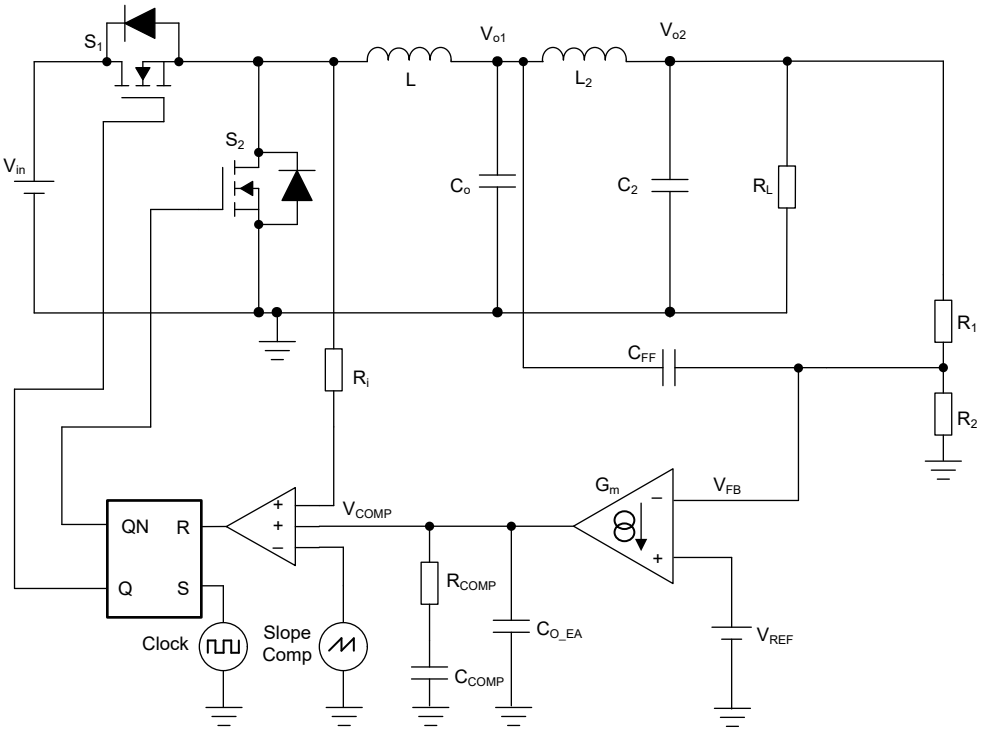


Figure 2-6. TIDA-050073 Block Diagram

2.3 Highlighted Products

The TPS62933F is a high-efficiency, easy-to-use synchronous buck converter with a wide input voltage range of 3.8V to 30V, and supports up to 3A continuous output current and 0.8V to 22V output voltage.

The device employs fixed-frequency *Peak Current Control* mode for fast transient response and good line and load regulation. The optimized internal loop compensation eliminates external compensation components over a wide range of output voltage and operation frequency. *Forced Continuous Conduction Mode* (FCCM) keeps switching frequency at a constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output voltage ripple under light load. The switching frequency can be set by the configuration of the RT pin in the range of 200kHz to 2.2MHz, which allows the user to optimize system efficiency, filtering size, and bandwidth. The soft-start time can be adjusted by the external capacitor at the SS pin, which can minimize the inrush current when driving large capacitive load.

The device provides complete protections including OTP, OVP, UVLO, cycle-by-cycle OC limit, and UVP with Hiccup mode. This device is in a small SOT583 (1.6mm × 2.1mm) package with 0.5mm pin pitch, and has an optimized pin-out for easy PCB layout and promotes good EMI performance.

2.4 System Design Theory

Figure 2-7 shows the reference design schematic. The components values are derived from this application note.

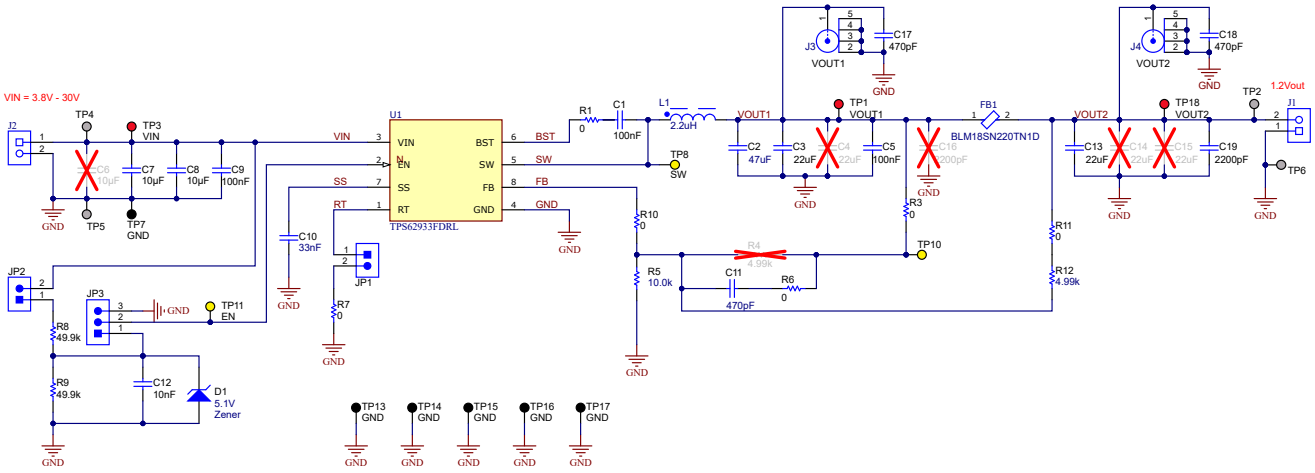


Figure 2-7. Reference Design Schematic

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

For testing purposes, this reference design requires the following equipment:

- A power supply that is capable of supplying at least 3A of load and up to 30V.
- Current and Voltage Multimeters to measure the currents and voltages during the related tests.
- Coaxial (coax) cable with DC blocker to measure output voltage ripple.
- Oscilloscope to capture voltages and a current.
- The TIDA-050073 board is a printed circuit board (PCB) with all the devices in this design.
- Resistive load or electronic load that is capable at least 3A.

3.2 Test Setup

Figure 3-1 shows the set up used to test the TIDA-050053.

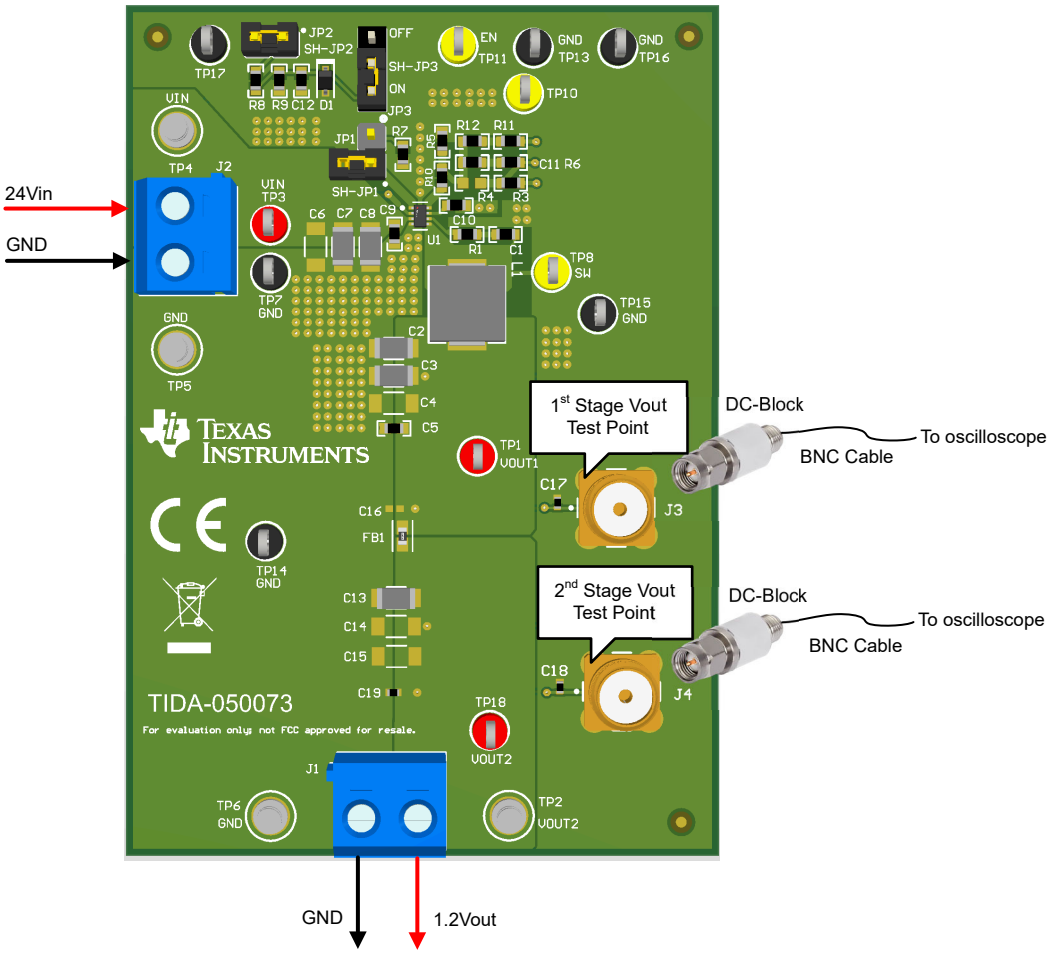


Figure 3-1. Test Setup

3.3 Test Results

3.3.1 Output Ripple

Figure 3-2 to Figure 3-5 show the output voltage ripple at 24Vin-1.2Vout-500kHz-0A / 0.5A / 1A / 3A, where Channel2 (Vo_1) is first stage Vout ripple and Channel1 (Vo_2) is second stage Vout ripple. Vout ripple is controlled to within 1mV after LC filter with hybrid sense.

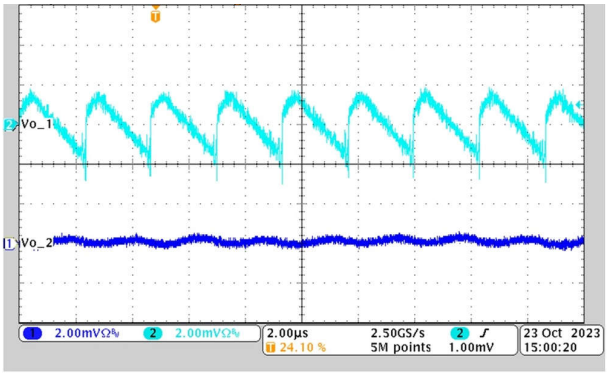


Figure 3-2. Output Voltage Ripple (0A)

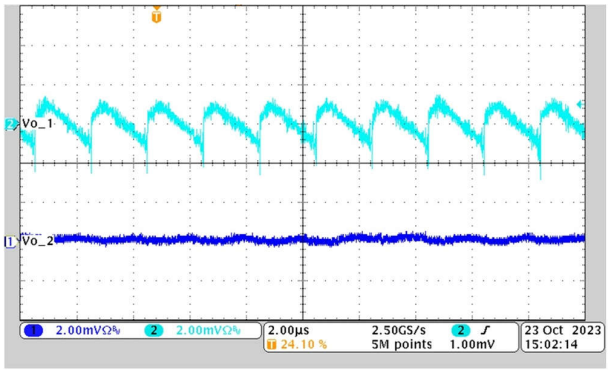


Figure 3-3. Output Voltage Ripple (0.5A)

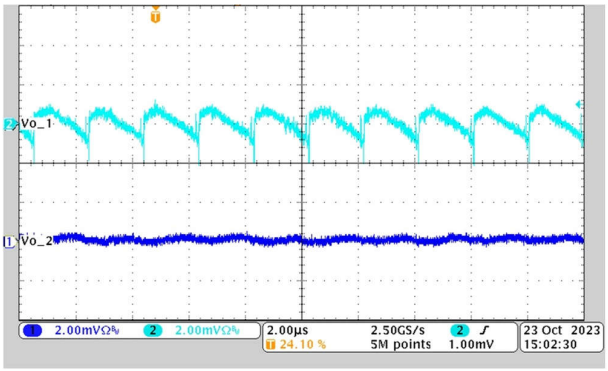


Figure 3-4. Output Voltage Ripple (1A)

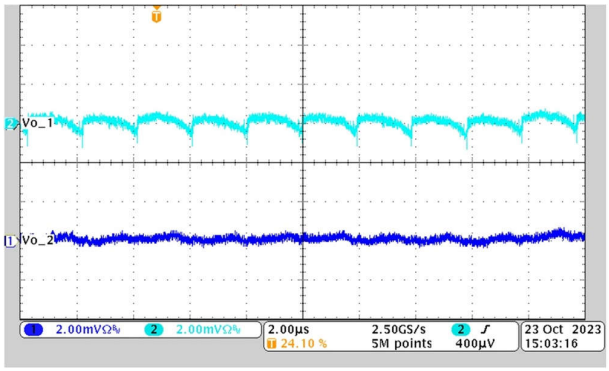


Figure 3-5. Output Voltage Ripple (3A)

3.3.2 Load Transient

Figure 3-6 and Figure 3-7 show the transient response from 0A to 1.5A and from 0.75A to 2.25A with 24V input. Vout peak-to-peak is within ±5% target range.

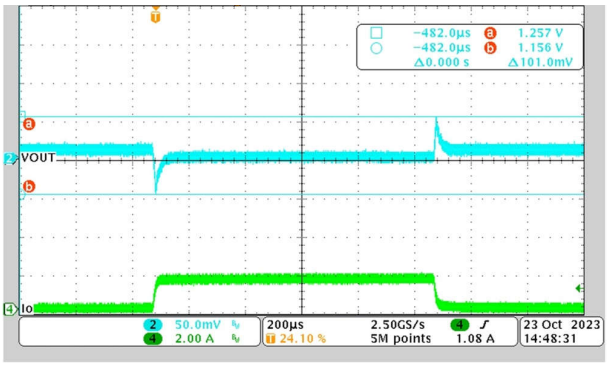


Figure 3-6. Load Transient Performance (0A to 1.5A)

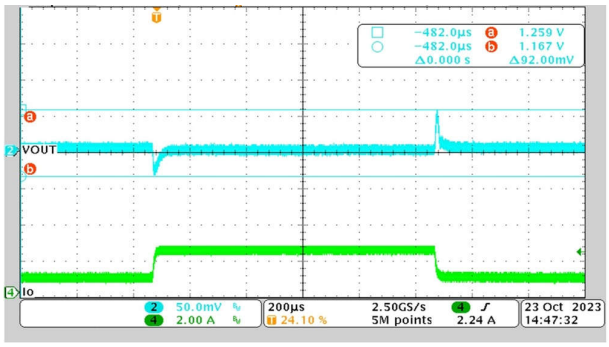


Figure 3-7. Load Transient Performance (0.75A to 2.25A)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050073.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050073.

4.1.3 PCB Layout Recommendations

To download the layer plots, see the design files at TIDA-050073.

4.1.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050073.

4.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050073.

4.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050073.

4.2 Documentation Support

1. Texas Instruments, *TPS62933F 3.8-V to 30-V, 3-A Synchronous Buck Converter in SOT583 Package*, data sheet.
2. Texas Instruments, *TPS6291xEVM-077 Evaluation Module*, user's guide.
3. Texas Instruments, *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part I: Filter Design for Output Ripple Reduction*, application note.
4. Texas Instruments, *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part II: Hybrid Sense Network Design for Stability*, application note.

4.3 Support Resources

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5 About the Authors

Miranda Gu is an applications engineer at Texas Instruments responsible for providing application support and technical design challenges of customers. Miranda also helps to understand customers needs and create new designs.

Andrew Xiong is a systems engineer at Texas Instruments responsible for defining new products and technology platforms based on our marketing strategy and business opportunities.

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