Design Guide: TIDA-010945

Precision signal chain for digital multimeters reference design

Description

This reference design explains the theory, design, and testing of a high-performance signal chain for DC measurements. The main target application is digital multimeters (DMMs), however the design can also be applicable to other applications, such as data acquisition (DAQ) and condition monitoring. This design achieves high DC accuracy using a high performance 24-bit analog-to-digital converter, ADS127L21, and a low-noise programmable gain amplifier, PGA855, with a typical nonlinearity of ± 2.4ppm and low drift over temperature. These devices are highly integrated, simplifying the overall signal chain design.

Resources

TIDA-010945	Design Folder
ADS127L11	Product Folder
ADS127L21	Product Folder
PGA855	Product Folder
REF7040	Product Folder

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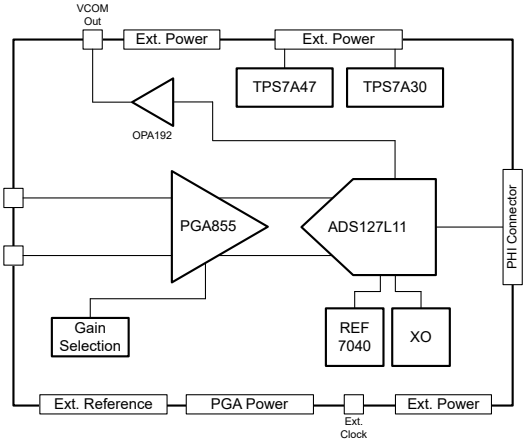
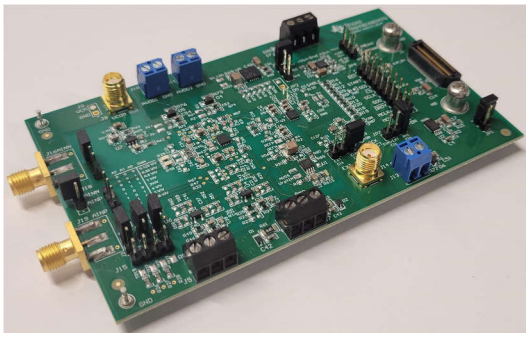
Features

- Programmable gain from 0.125V/V to 16V/V
- Wide bandwidth: 357kHz (Sinc3 filter, max-speed)
- Configurable digital filter settings for the ADC
- SNR of 110dB (Sinc4 filter) without the need for high speed ADC input drivers and reference buffers
- Low gain drift and non-linearity enables high DC accuracy post-calibration
- At full-scale input: 25°C ± 5°C (post-calibration)
  - Estimated typical: TUE = ± 6ppm, INL ± 2.4ppm
  - Estimated maximum: TUE = ± 32ppm, INL ± 12.2ppm
  - Estimated temperature drift (typical)
    - Offset drift: 350nV/°C
    - Gain drift: 1.5ppm/°C
  - Measured from 1unit (post-calibration)
    - TUE: ± 9ppm

Applications

- Digital multimeter (DMM)
- Data Acquisition (DAQ)
- Condition Monitoring





1 System Description

This design features an easily selectable input gain stage, allowing for a wide range of input signals. This is beneficial for applications, such as DMMs, which have multiple input ranges, as switching between gains is relatively simple.

PGA855 can drive the input of ADS127L21 without an additional ADC driver, and ADS127L21 has integrated input and reference buffers, eliminating the need for external amplifiers. The high integration greatly simplifies the design and saves space. The system has a wide bandwidth, high dynamic range, as well as low non-linearity, allowing for excellent AC accuracy and DC precision.

1.1 Key System Specifications

Key System Specifications

Table 1-1 lists the key system specifications realized by this reference design.

Table 1-1. Specifications

PARAMETER	SPECIFICATIONS
Input signal range	0V to 32.768V (with 0.125V/V gain)
Gain Options	0.125, 0.25, 0.5, 1, 2, 4, 8, 16V/V
Digital Filter Options	Wideband, low-latency, programmable IIR and FIR
Resolution	24 bits
Data Rate	Up to 512kSPS (wideband filter) Up to 1.365MSPS (low-latency filter)
SNR (1kHz, Gain = 1V/V)	108dB (wideband filter) 110dB (low-latency filter)
THD (1kHz, Gain = 1V/V)	–121.4dB (wideband filter) –121.4 dB (low-latency filter)
Bandwidth	224kHz (wideband filter) 357kHz (low-latency filter)
Calculated Typical DC Accuracy	Offset error: ± 76µV Gain error: ± 360ppm
Calculated Typical Temperature Drift Accuracy	Offset drift: 350n V/°C Gain drift: 1.1ppm/°C

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the system block diagram.

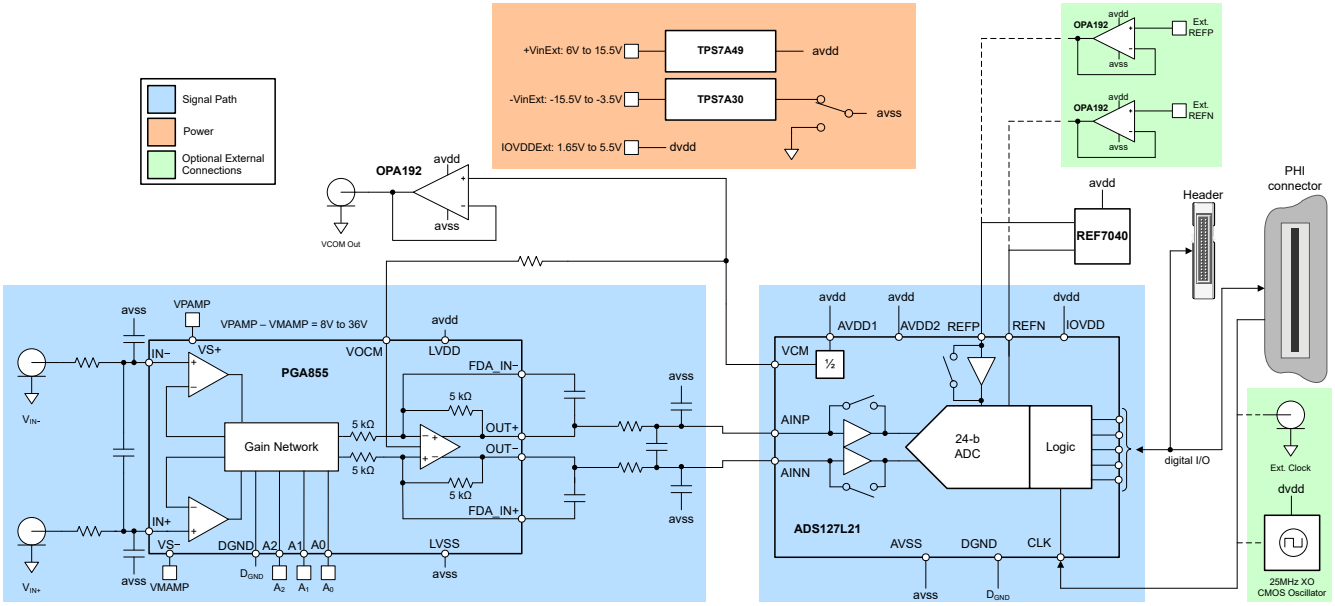


Figure 2-1. System Block Diagram

2.2 Design Considerations

The design is intended to be used with a Precision Host Interface (PHI) board, allowing for easy connection with the ADS127L21 GUI. The PHI board is a peripheral used to interface with GUIs for several of Texas Instrument's delta-sigma ADCs. This board cannot be ordered individually, however, the board is provided with the purchase of ADS127L11EVM-PDK or ADS127L21EVM-PDK. The ADC power and clocking are sourced from the PHI controller by default. The reference design additionally contains an on-board, high precision 4.096V series reference to maximize the ADC's dynamic range. However, the user can choose to use an external reference, clock, and power supply, depending on the system specifications. Regardless of how the ADC is powered, the PGA855 must be powered externally. Additionally, there is a header on the board which allows access to the digital lines from the ADC if the PHI controller board is not used.

The ADC has two input ranges: 1x and 2x, where the 1x range is defined by VIN = ± VREF and the 2x range is defined by VIN = ± 2 × VREF. The 2x input range doubles the available range when using a reference voltage of 2.5V or less. The 2x input range typically improves SNR by 1dB when using a 2.5V reference, but also requires driving the inputs to the 5V supply rails to achieve full dynamic range. The best available dynamic range (4dB improvement, typical) is through the use a 4.096V or 5V reference voltage (program the ADC to the high-reference range mode).

This design has a wide input range, due to the PGA855 gain settings. The maximum input signal to the board depends on the PGA855 power supplies, the PGA gain setting, and the input range selection on the ADC. The maximum recommended power supply for the PGA855 is 36V unipolar or ± 18V bipolar. For example, with a 4.096V reference, the system full-scale range varies from ± 0.256V (16V/V gain) to ± 32.768V (1/8V/V gain), when the PGA855 is powered from ± 18V supplies.

2.3 Highlighted Products

2.3.1 ADS127L21

The ADS127L21 is a 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) featuring a programmable digital filter with data rates up to 512kSPS using the wideband filter and up to 1365kSPS using the low-latency filter. The device offers an excellent combination of ac performance and dc precision with low power consumption.

Programmable infinite and finite impulse response (IIR and FIR) digital filters allow custom filter profiles, such as A-weighting compensation and frequency notch filters. The wideband or low-latency filter option optimize ac-signal performance or data throughput of dc signals, all in one device.

The low-drift modulator achieves excellent dc precision with low wideband noise for outstanding ac performance. The power-scalable architecture features four speed modes to optimize data rate, resolution, and power consumption. Signal and reference input buffers reduce driver loading for increased accuracy.

2.3.2 PGA855

The PGA855 is a high-bandwidth programmable gain instrumentation amplifier with fully differential outputs. The PGA855 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain selection pins. The output common-mode voltage can be independently set using the VOCM pin.

The PGA855 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs). The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream device against overdrive damage.

The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of 0.3pA/$\sqrt{\text{Hz}}$, making the PGA855 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers excellent gain flatness even at high frequencies, making the PGA855 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages up to ± 40V beyond the power-supply voltages.

2.3.3 REF70

The REF70 is a family of high precision series voltage references that offers the industry's lowest noise (0.23ppm$_{p-p}$), very low temperature drift coefficient (2ppm/°C), and high accuracy (± 0.025%). The REF70 offers a high PSRR, low drop-out voltage and excellent load and line regulation to help meet strict transient requirements. This combination of precision and features is designed for applications such as test and measurement that demand a precise reference to be paired with precision, high-resolution data converters such as ADS8900B, ADS127Lx1 and DAC11001A, to achieve excellent signal chain performance.

3 System Design Theory

The front-end is a key building block to a digital multimeter, and many data acquisition systems as well. Digital multimeters measure across a wide selection of ranges. A switching matrix with individual gain resistors for every range can take up a lot of space, especially in a multichannel data acquisition system.

The PGA855 gain settings allow for a wide input range and are controlled with three digital signals, allowing for easier switching between gains. DMMs have several different input ranges, for example 100mV, 1V, 10V, and 100V, so the design is simplified when multiple input ranges can be handled with one input stage. The PGA855 gain is controlled with 3 digital lines, making switching between gain stages relatively easy when using a microcontroller or a processor.

The amplifier must be able to accurately scale signals to the full-scale range of the data converter, without sacrificing resolution on the data converter. Accuracy and precision are key to any DMM design. A meter's reading needs to be close to the true value and repeatable. Most initial DC errors can be calibrated relatively easily, however nonlinearities, drift, and noise must be low to enable accuracy and precision.

Additional input scaling for a high-voltage input, and input protection can be added onto this design to fully complete the analog front-end signal chain.

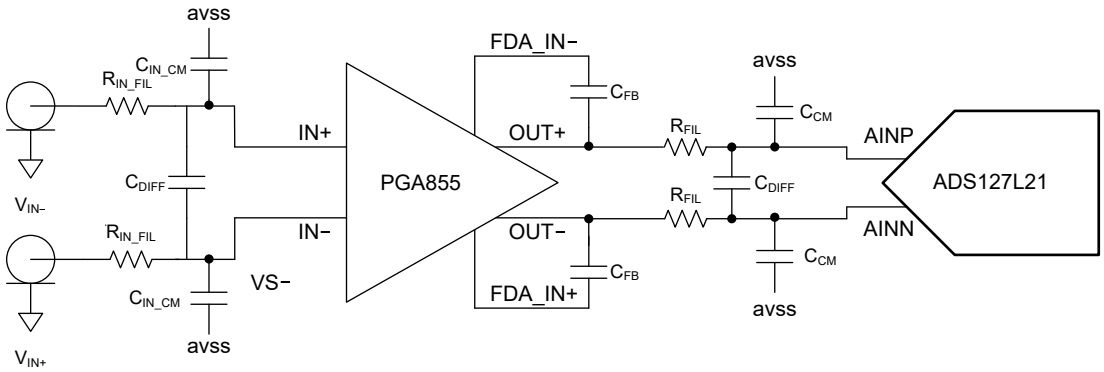


Figure 3-1. PGA and ADC Input Filters

The R-C-R differential low-pass filter at the input of the PGA, as shown in Figure 3-1 helps reduce EMI/RFI high frequency extrinsic noise. This filter can be customized per the bandwidth and application requirements. Using the 10-to-1 ratio for differential capacitor C_{IN_DIFF} versus common-mode capacitors C_{IN_CM} offers good differential and common-mode noise rejection. This ratio also tends to be less sensitive to the tolerance variation and mismatch of the filter capacitors.

The feedback capacitor, C_{FB}, is in parallel with the PGA855 output-stage internal 5kΩ feedback resistors (see Figure 2-1) to implement additional noise filtering. The internal resistors have ± 15% absolute resistance variation, and this variation must be taken in to account when implementing noise filtering. On this board, C_{FB} is set to 25pF, providing a typical f–3dB corner frequency of 1MHz. The estimated minimum f–3dB corner frequency for this circuit ranges from approximately 904kHz to 1.119MHz when accounting for the feedback-resistor variation. The filter at the ADS127Lx1 inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that can otherwise degrade because of incomplete amplifier settling. The ADC input precharge buffers significantly reduce the input charge that raises the ADC input impedance to decrease gain error.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Description

Figure 4-1 shows the TIDA-010945 hardware, indicating different circuit blocks, connectors, and interfaces from the System Block Diagram.

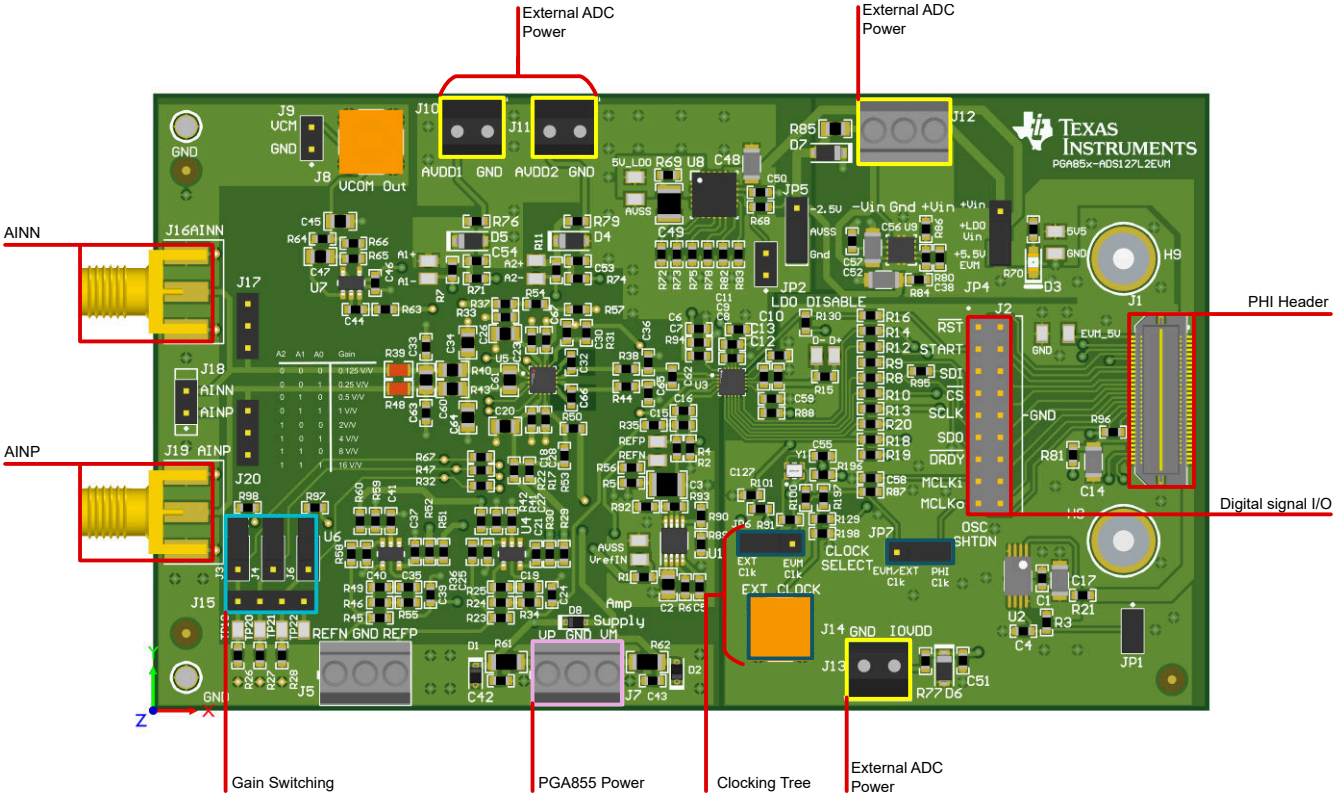


Figure 4-1. Board Layout and Interfaces

4.1.1 Board Interface

Table 4-1. Board Connectors and Headers

CONNECTOR	DESCRIPTION
J1	QSH connector to connect to PHI, best practice is to power the board before connection
J2	SPI signals header, use for debugging and probing, or to connect to another board (if no QSH)
J3, J4, J6	Used for PGA gain control. See Table 4-2
J15	Used to probe the gain control pins
J16	Negative input
J19	Positive input
J18	Used to short the inputs together
J17, J20	Used to short the inputs to ground
J7	Positive and negative power rail inputs for the PGA855
J10, J11, J12, J13	Used to power the board externally. See Section 4.1.2 for more details
JP4, JP5	Used to select on-board LDOs or external supplies
J5	Used to connect an external reference
J9	Test points for the Vcm signal
J8	Used to connect the Vcm signal from the ADC to external equipment

Table 4-1. Board Connectors and Headers (continued)

CONNECTOR	DESCRIPTION
J14	External clock input
JP6, JP7	Used to select the board clock or an external clock
JP1	EEPROM enable
JP2	LDO enable

The PGA gains can be adjusted by adding and removing jumpers on the gain control pins.

Table 4-2. Gain Settings

GAIN (V/v)	A0 (J3)	A1 (J4)	A2 (J9)
0.125	0	0	0
0.25	1	0	0
0.5	0	1	0
1	1	1	0
2	0	0	1
4	1	0	1
8	0	1	1
16	1	1	1

4.1.2 Power Supplies

The default state of the TIDA-010945 hardware is that all ADC power supplied are generated using the USB power from the PHI controller. The PGA must be powered with external supplies to connector J7. The PGA855 can be powered with a single supply (8V to 36V) or a dual supply (± 4V to ± 18V). See PGA855 Low-Noise, Wide-Bandwidth, Fully Differential Output Programmable-Gain Instrumentation Amplifier data sheet for detailed power supply recommendations and specifications. The design board is fitted with 36V diodes D1, D2, and D3. This allows for ± 18V bipolar supplies, as well as asymmetrical bipolar power supplies, so long as the supplies are within the recommended operating conditions.

The external power connections can be used in cases where the PHI does not provide the needed voltage. For example, the PHI does not provide bipolar voltages, so if a bipolar supply is needed, an external power supply is required. Change the 0Ω resistor connections (R71, R74, and R81) to use the external power connections for AVDD and IOVDD. J10 is used to power AVDD1, J11 is used to power AVDD2, and J13 is used to power IOVDD. Refer to the recommended operating conditions in the ADS127L21 data sheet for detailed specifications. Connector J12 can optionally be used to supply power to the onboard 5V and –2.5V regulators. In this case, the allowable voltage range for –VinExt is –15.5V < –VinExt < –3.5V and +VinExt is 6V< +VinExt < 15.5V.

The 5.5V voltage from the PHI is regulated to 5V using a low-noise TPS7A4700 LDO. By default, placing the shunt in position 1–2 on jumper JP4 routes 5.5V from the PHI to the LDO. The 5V LDO can also be supplied by external power on J12 by moving the shunt on (JP4) to position 2-3. The 5V LDO output is used for the AVDD connections and can be reprogrammed to different output voltages using R72, R73, R75, R78, R82, and R83. There is an additional LDO that generates –2.5V for AVSS, using the low-noise TPS7A3001 LDO. This LDO is only supplied by external power on J12. By default, AVSS is connected to GND with a shunt on (JP5) 1–2. If AVSS must be set to –2.5V, then connect an external negative supply to J12 and move the shunt on (JP5) to position 2-3.

An external reference can be connected to the board through connector J5. There are appropriate buffers and connections on the board for an external reference. This is not necessary if the on-board voltage reference (REF7040) is used. REF7040 is sufficient to meet the specifications in the ADS127L21 512-kSPS, Programmable Filter, 24-Bit, Wideband Delta-Sigma ADC data sheet

This board is configured with the REF7040, however, the board can easily be replaced with other precision references from TI's catalog of precision series voltage references, such as REF6241. Swapping the reference

can require populating R90 and R92 instead of R89 and R93 as some references are not completely pin-to-pin compatible.

4.1.3 Clocking Tree

The board supports three different clock options:

- PHI clock (no external connections)
- Local clock (no external connections)
- External, user-supplied clock

The default position for jumper (JP7) is 2-3, which routes the PHI digital controller board clock to the CLK pin on the ADS127L21 (U3). If the board is used without the PHI controller, then the jumper can be moved to 1-2 to directly route the local clock to ADS127L21.

Jumper (JP6) 2-3 enables the local 32.768MHz oscillator (Y1) on the board, which is the default position required to work with the ADS127L21EVM-PDK-GUI software. If inactive (JP6) 1-2, allows an external clock supplied on the SMA connector (J14).

The ADS127L21EVMPDK-GUI software by default uses the 32.768MHz (Y1) oscillator, but can also select the 24MHz PHI clock source. An external clock source can be used by placing jumper JP6 in the 1-2 position. A CMOS square-wave signal with an amplitude equal to IOVDD (2.5V when using the PHI board) must be used with a frequency within the specified range of the ADS127L21.

4.2 Software Requirements

This reference design is intended to be used with a dedicated software: ADS127L21 EVM-PDK-GUI, shown in Figure 4-2. Refer to the ADS127L21EVM-PDK user's guide for information on how to use the software.

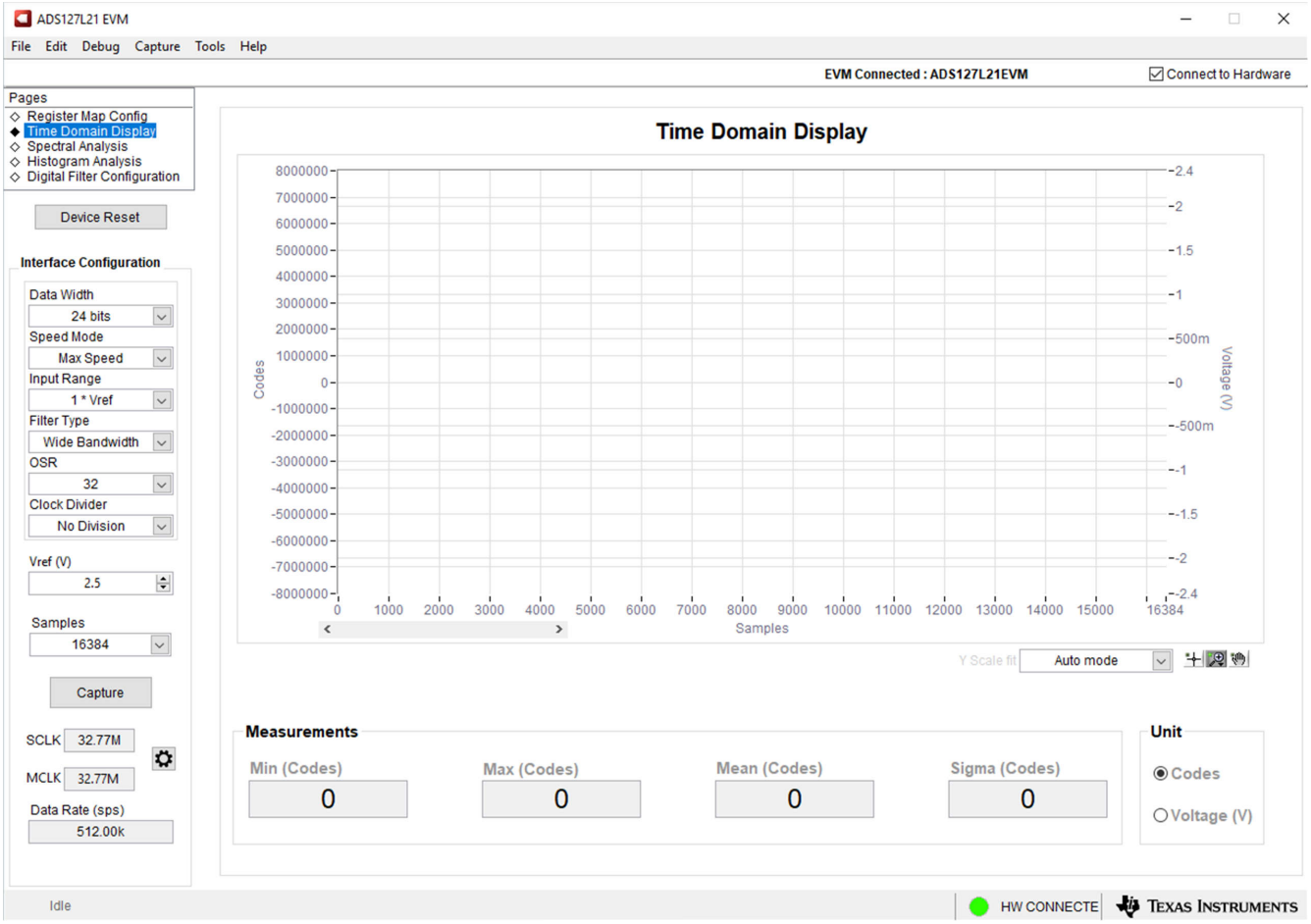


Figure 4-2. ADS127L21 GUI

4.3 Test Setup

Use the basic setup in Figure 4-3 to evaluate the PCB. The board is evaluated through the PHI board to a PCB running the ADS127L21EVM-PDK-GUI software. The default reference value in the GUI is 2.5V, which must be updated to 4.096V.

The following components are required to run all tests:

- Reference Design PCB
- PHI board
- PC running the ADS127L21 software
- ± 15V power supplies
- Low noise DC source
- 6.5 digit digital multimeter
- For temperature drift measurements: temperature chamber

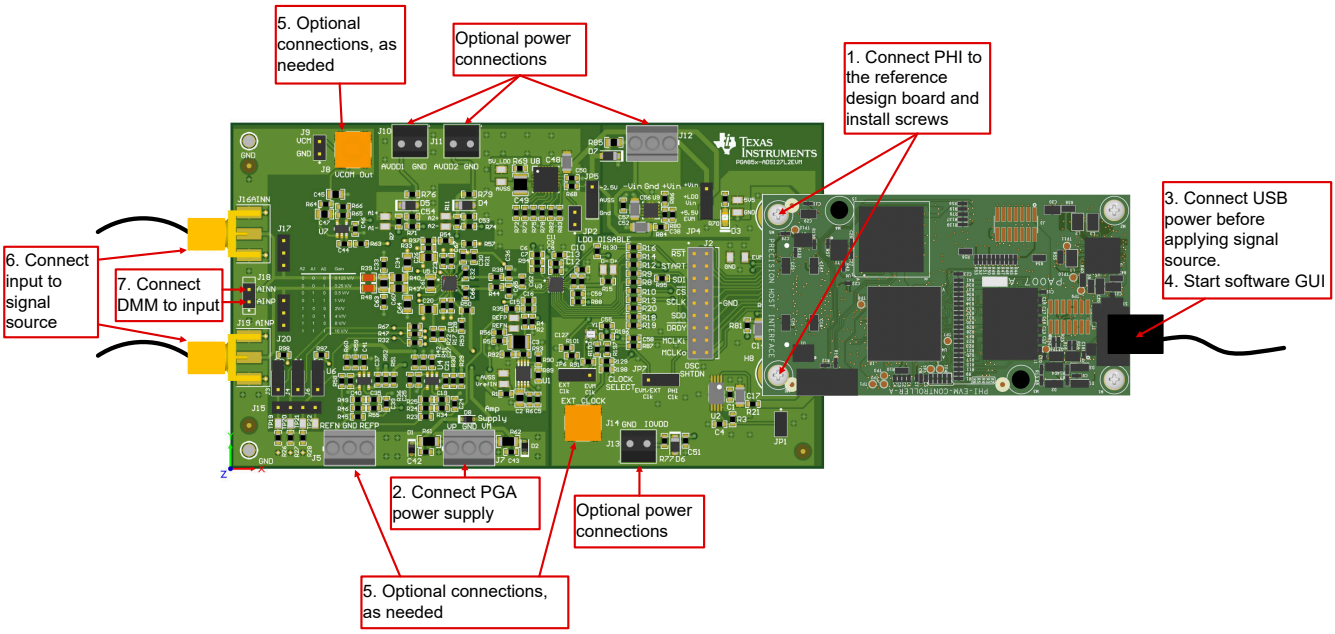


Figure 4-3. Test Setup for DC Accuracy

Connect the hardware and power on as shown in Figure 4-3.

Use twisted pairs or SMA connectors to connect the precision DC source to the input of the signal chain, using the shortest connections possible. This reduces the amount of noise coupled into the signal chain, allowing for high-accuracy measurements.

To test a single-ended signal, connect the negative input (AINN) directly to ground using jumper J17 and connect the desired signal to the positive input (AINP) using the SMA connector (J19) or one of the pin connectors (J18 pin 2, or J20 pin 1).

4.4 Test Results

This section presents sample test results. All the test results are done under the following ADC conditions:

SETTING	CONFIGURATION
Speed Mode	High Speed
Data Rate	11.72kSPS
Filter	Sinc4
OSR	1024
Clock Configuration	PHI Clock (24MHz)
Voltage Reference Range	High-Reference Range

SETTING	CONFIGURATION
VCM Output	Enabled
Reference Buffer	Enabled
Analog Positive Input Buffer	Enabled
Analog Negative Input Buffer	Enabled
PGA Power	± 15V

The tests were performed with the ADS127L11, using the associated GUI; however, the performance of the performance is very similar to the performance of the ADS127L21. All tests use a single-ended input signal.

4.4.1 DC Accuracy Tests

Drift and non-linearity are key specifications for DC accuracy, as unlike initial errors like gain and offset errors, these cannot be easily calibrated by using two-point or three-point calibration. In this section, gain and offset drifts and non linearity of the signal chain are measured to calculate the DC accuracy achieved by the signal chain post-calibration.

Use jumper J18 to short the inputs together to measure the offset error. Use the GUI to capture data to produce a graph similar to Figure 4-4. Since the output is zero when the inputs are shorted together, any non-zero output is the offset error. Reading the histogram in Figure 4-4, the offset error is 27.7µV.

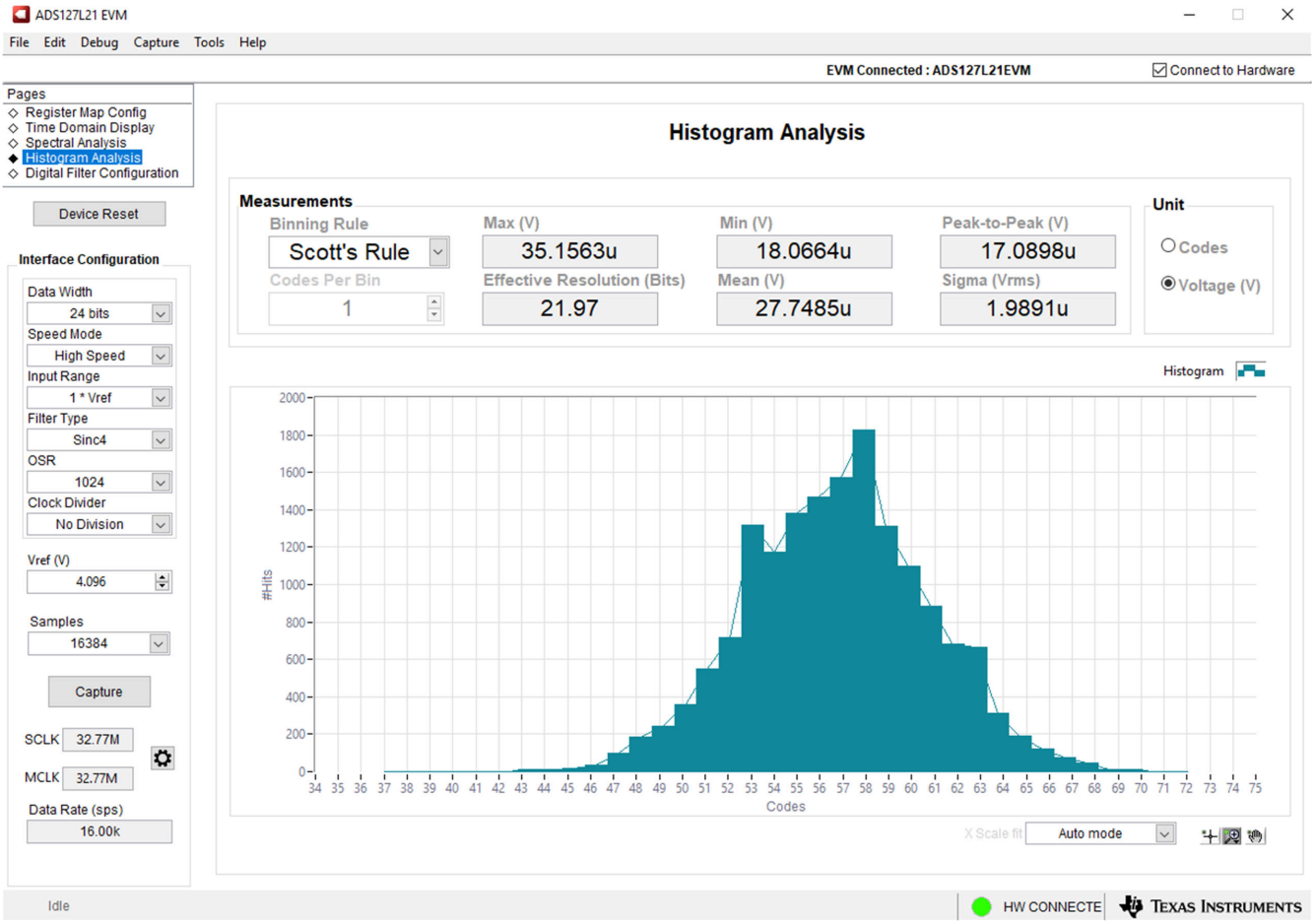


Figure 4-4. Offset Measurement (G = 1, T_A = 25°C)

Remove the short from J18 and collect data from 0V to ± full-scale. The full-scale range (FSR) depends on the reference and the gain settings and can be calculated with the following equation:

$$\text{FSR} = \frac{2V_{\text{ref}}}{\text{Gain}} \quad (1)$$

Be sure not to violate the input range of the PGA. Repeat the data collection for different gain settings, making sure the temperature chamber settles to the correct temperature before collecting data. Collect data at ± 95% of the full-scale range to perform gain error calculations.

To collect temperature drift data, repeat the same trials over multiple temperatures. To account for reference accuracy error, measure the reference value and input the result into the GUI on the left-hand side, under "Interface Configuration".

4.4.2 Gain and Offset Temperature Drift

Offset drift is the change in the offset voltage across a temperature range. The signal chain offset drift can be calculated from the offset data collected using the box method. The box method takes the maximum and minimum offset over the range and divides the offset by the temperature range as shown in Equation 2:

$$\text{Offset Drift}\left(\frac{\mu V}{°C}\right) = 10^6 \times \frac{V_{OFSMAX} - V_{OFSMIN}}{T_{MAX} - T_{MIN}} \quad (2)$$

Gain error is the difference between the actual and the ideal slopes of the signal chain. Gain error is measured by applying dc test voltages at –95% and 95% of the full-scale range. The error is calculated by subtracting the difference of the dc test voltages (ideal slope), scaled by the gain (G), from the difference in the output voltages (actual slope), as shown in Equation 3:

$$\text{Gain Error}\left(\text{ppm of FSR}\right) = 10^6 \times \frac{\Delta V_{\text{OUT}} - G\ \Delta V_{\text{IN}}}{G\ \Delta V_{\text{IN}}} \quad (3)$$

The gain drift can be found by using the box method again, using the minimum and maximum gain error across gain stages:

$$\text{Gain Drift}\left(\frac{\text{ppm}}{°C}\right) = 10^6 \times \frac{GE_{MAX} - GE_{MIN}}{T_{MAX} - T_{MIN}} \quad (4)$$

The typical gain and offset drift errors an be estimated by using adding the typical values listed in the PGA855 and ADS127L21 data sheets. The same can be done for the maximum errors:

Table 4-3. Estimated Offset and Gain Drift

	PGA855 (TYP)	ADS127L21 (TYP)	ESTIMATED VALUE (TYP) FOR PGA855 + ADS127L21	PGA855 (MAX)	ADS127L21 (MAX)	ESTIMATED VALUE (MAX) FOR PGA855 + ADS127L21
Offset Drift (µV/°C)	0.3	0.05	0.35	1	0.2	1.2
Gain Drift (ppm/°C)	1	0.5	1.5	2	1	3

For the range 20°C–30°C, the expected error from drift is around ± 3.5µV of offset and ± 15ppm of gain error. Below, the offset and gain error across temperature measured from one unit is displayed:

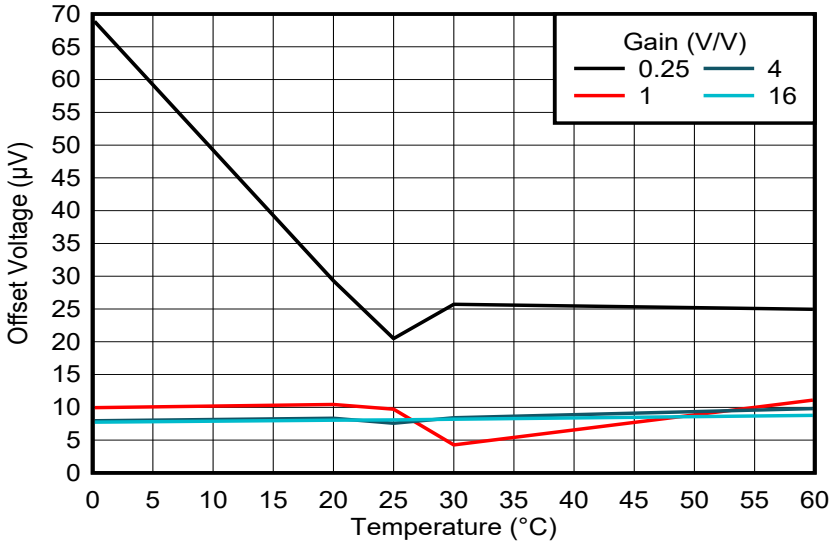


Figure 4-5. Offset Voltage (RTI) Versus Temperature

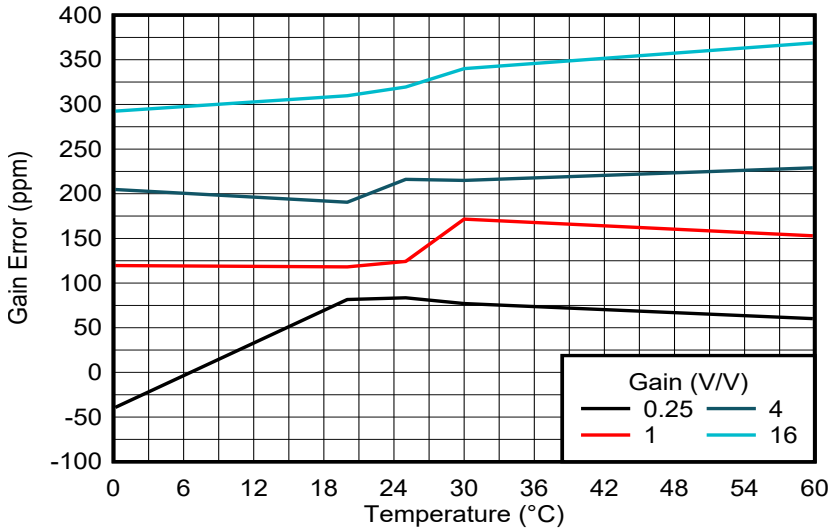


Figure 4-6. Gain Error Versus Temperature

From Figure 4-5 and Figure 4-6, we can calculate the temperature drift for the unit, using Equation 2 and Equation 4:

GAIN (V/V)	0.25	1	4	16
Offset Drift (µV/°C)	0.81	0.11	0.04	0.02
Gain Drift (ppm/°C)	2.06	0.89	0.64	1.28

4.4.3 Nonlinearity

Initial errors like offset and gain errors can be significantly reduced or fully eliminated with a two point or a three point calibration. However, nonlinearity cannot be easily calibrated. Integral nonlinearity (INL) is a measure of the deviation of the system's actual output from the best output, given a certain input. INL is measured by applying a series of dc test voltages along a straight line computed from the slope and offset transfer function of the system. INL is the maximum of the difference in the actual output from the best output for the full scale input range. The INL calculation uses the least-sqaured error best fit method to determine the new straight line to minimize the root-sum-square of the INL errors above and below the original end-point line.

Figure 4-7 shows the measured INL for one unit across temperature (with a fixed gain of 1V/V) and across gains (at 25°C).

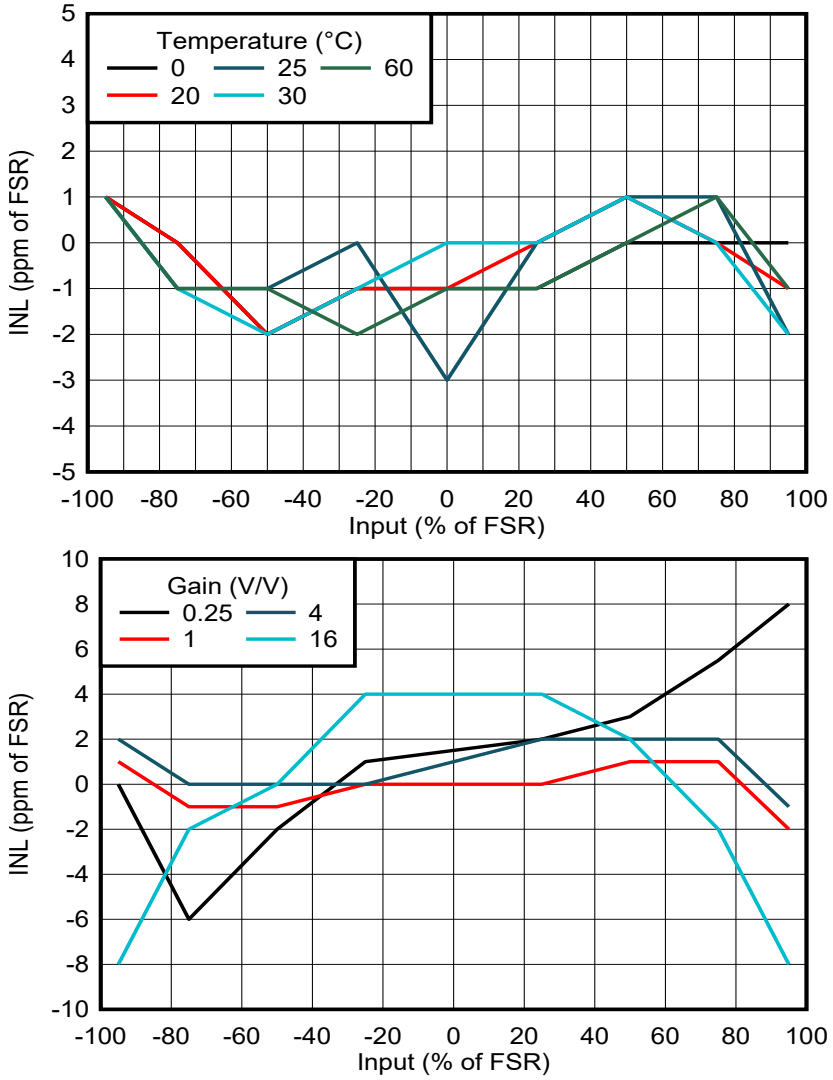


Figure 4-7. INL Error Versus Input Voltage

The typical INL listed in the ADS127L21 data sheet is 0.4ppm, with a maximum of 1.8ppm across the range 0°C to 70°C. For the PGA855, the typical INL listed is 2ppm, with a maximum of 10ppm, which is consistent with the data collected for one unit, as shown in Figure 4-7.

4.4.4 SNR and Noise Performance

For more information about the noise performance and SNR of the design, please refer to the following application note: *Achieve High SNR with the PGA855, Fully Differential Programmable-Gain Amplifier*

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010945.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010945.

5.2 Software

ADS127L21 EVM Software User Interface	This reference design is intended to be used with the dedicated GUI for the ADS127L21 EVM

5.3 Documentation Support

1. Texas Instruments, *ADS127L21 512-kSPS, Programmable Filter, 24-Bit, Wideband Delta-Sigma ADC* data sheet
2. Texas Instruments, *PGA855 Low-Noise, Wide-Bandwidth, Fully Differential Output Programmable-Gain Instrumentation Amplifier* data sheet
3. Texas Instruments, *ADS127L21EVM-PDK Evaluation Module* user's guide

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

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