Design Guide: TIDA-010262

Four-Port 10BASE-T1L Single-Pair Ethernet With Power Over Data Line Reference Design

Description

This reference design showcases an Ethernet gateway that functions as a bridge between four 10BASE-T1L single-pair Ethernet (SPE) ports with power over data lines (PoDL) and a 1000BASE-T Ethernet port. The four SPE ports function as power source equipment (PSE), providing 24V to field devices. The gateway is controlled by the AM6442 microprocessor and utilizes the Linux® operating system, allowing for flexible and scalable open-source software.

As an example, the reference design interfaces with edge processing board (TIDA-010261) over SPE with PoDL.

Resources

TIDA-010262	Design Folder
TIDA-010261	Design Folder
AM6442, DP83TD510E, DP83867IR	Product Folder
TQ-3P-SOM-TQMA64XXL	Product Folder

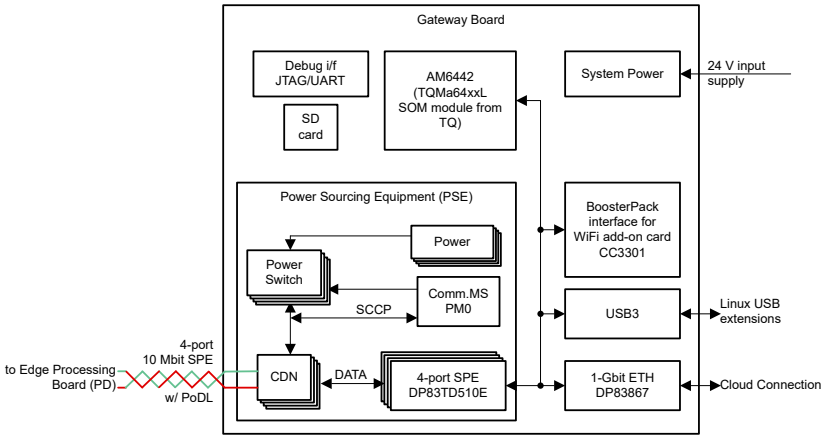
Ask our TI E2E™ support experts

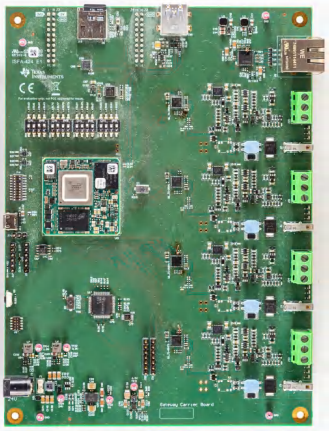
Features

- 24V power supply input
- AM6442 microprocessor with dual-core 64-bit Arm® Cortex®-A53 and quad-core Cortex-R5F
- Four 10 BASE-T1L single-pair Ethernet (SPE) ports
- Each SPE is enabled with power over data line (PoDL) IEEE802.3cg
- One MSPM0 to drive four port serial communication classification (SCCP)
- Gigabit 1000BASE-T Ethernet port for cloud connection
- USB 3.1 support and µSD card interface
- Linux® operating system
- Optional LaunchPad™ interface to connect to CC3301 Wi-Fi® 6 and Bluetooth® low-energy BoosterPack™

Applications

- Factory automation and control
- Communication module
- Communication switch





1 System Description

This design features four-port 10BASE-T1L single-pair Ethernet (SPE) with power over data line (PoDL), a 1000BASE-T Ethernet port, a USB 3.1 port and a BoosterPack plug-in module connector to interface to CC3301 Wi-Fi 6 and Bluetooth® low energy BoosterPack plug-in module. The design is controlled by the AM6442 microprocessor, which is on a system-on-module.

The design uses the Linux operating system to enable users to customize and extend the design with open source software.

1.1 Terminology

- Single pair Ethernet (SPE)
- Power over Data Line (PoDL)
- Power sourcing equipment (PSE)
- Powered device (PD)
- microprocessor (MPU)
- System-on-module (SOM)
- Industrial communication subsystem (ICSS)
- Programmable real-time unit (PRU)
- Error correction code (ECC)
- Physical layer transceiver (PHY)
- Physical medium dependent (PMD)
- Media access controller (MAC)

2 System Overview

2.1 Block Diagram

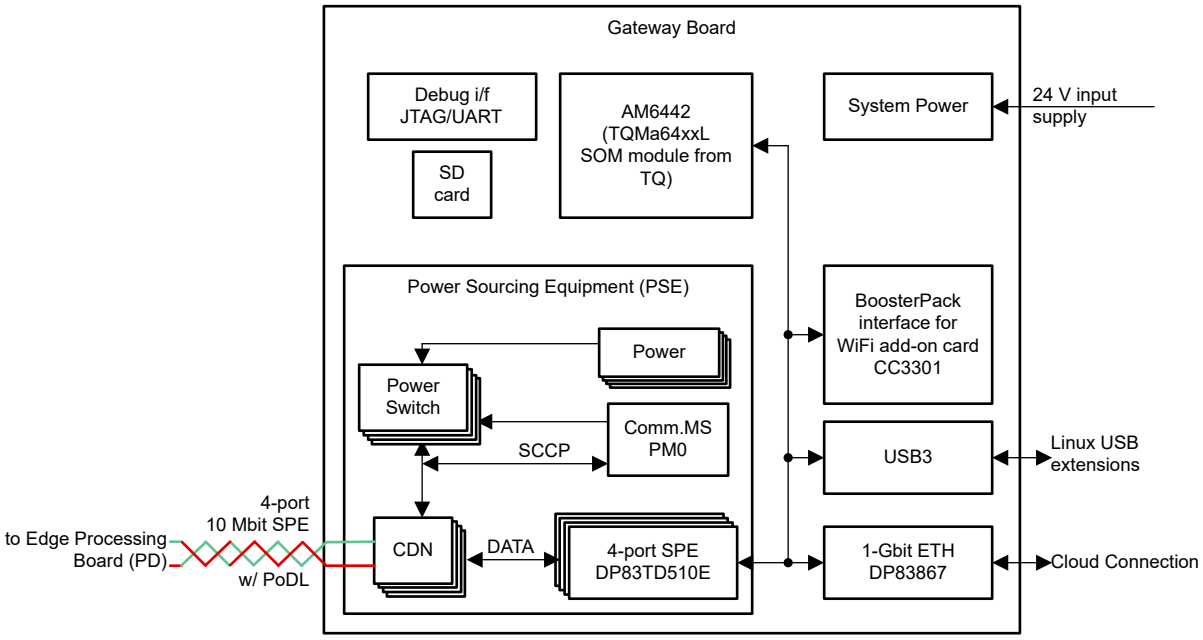


Figure 2-1. Gateway Board

2.2 Design Considerations

This reference design shows the implementation of the digital back of four single-pair Ethernet (SPE) 10BASE-T1L ports with the option for powering the remote sensors or actuators through Power over Data Line (PoDL). PoDL is standardized by IEEE802.3cg. The PoDL is implemented including serial communication classification protocol (SCCP) to negotiate the desired power class between the power sourcing equipment (PSE) and a powered device (PD).

To implement SPE together with PoDL, on the data side the design needs an Ethernet PHY such as the DP83TD510E, for translating the interface from the media access controller (MAC) to the medium-dependent interface (MDI) on the single pair Ethernet cable. One the MAC side, a media-independent interface (MII) such as the reduced gigabit MII (RGMII) is used.

To add power and SCCP communication to the single pair Ethernet cable, two things are needed: a coupling network to separate power and data on the line, and a device for adding the required communication protocol. The coupling network can be seen as a frequency filter, where the low-frequency component (especially the DC) is going to the power part and the high-frequency components are treated as data going to the PHY. The communication protocol plays an important role, similar to Power over Ethernet (PoE), the PSE needs to make sure to properly power only the PD requesting power. Otherwise the equipment that is connected to SPE can get damaged. The reference design supports four ports of SPE with PoDL, but required only a single microcontroller (MCU) for the SCCP communication.

The reference design uses an AM6442-based system-on-module (SOM) and also supports a gigabit Ethernet port for cloud connection. The Arm Cortex-A53 cores operate the Linux® operating system (OS).

The reference design offers Joint Test Action Group (JTAG) access and an isolated Universal Serial Bus (USB) Universal Asynchronous Receiver or Transmitter (UART) interface to simplify bring up and debug. For storing an application, use either an onboard micro Secure Digital (SD) card connector, a NOR flash, or an eMMC on the module. The boot mode switches allow selection of which peripheral to start from.

2.3 Highlighted Products

2.3.1 AM6442 Microprocessor

The AM6442 microprocessor is equipped with a dual 64-bit Arm Cortex-A53 microprocessor subsystem that operates at up to 1.0GHz. Additionally, the AM6442 features 2 × dual-core Arm Cortex-R5F MCUs that can operate at up to 800MHz for real-time processing tasks, such as industrial Ethernet software stacks, Ethernet packet switching, or motor control. The AM6442 also supports 2 × gigabit Industrial Communication Subsystems (PRU-ICSSG), which can support up to 4 physical gigabit Ethernet ports. The integrated Ethernet switch (CPSW3G) supports two additional gigabit Ethernet ports.

The AM6442 supports high-speed interfaces such as USB 3.1 Dual-Role Device (DRD), LPDDR4 and DDR4 memory with ECC, security features, media and data storage, and general connectivity.

In this reference design, a system-on-module (SOM) TQMa64xxL from the manufacturer TQ is used, which includes all necessary components such as the AM6442 MPU, power management, LPDDR4 memory, eMMC NAND flash, clock generation, and EEPROM. For more technical information, please refer to the SOM data sheet.

2.3.2 DP83867 gigabit Ethernet Physical Transceiver

The DP83867 device is a robust, low power, fully-featured physical layer transceiver (PHY) with integrated physical medium dependent (PMD) sublayers to support 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. The device is designed for easy implementation of 10-, 100-, 1000Mbps Ethernet LANs. The device interfaces directly to twisted pair media via an external transformer. This device interfaces directly to the media access controller (MAC) layer through the IEEE 802.3 Standard Media Independent Interface (MII), the IEEE 802.3 Gigabit Media Independent Interface (GMII) or Reduced GMII (RGMII). This reference design used the RGMII interface for the connection between MAC and PHY.

2.3.3 DP83TD510E Single-Pair Ethernet Physical Transceiver

The DP83TD510E is an ultra-low power Ethernet physical layer transceiver compliant with the IEEE 802.3cg 10BASE-T1L specification. The PHY has very-low-noise coupled receiver architecture enabling long cable reach and very-low power dissipation. The PHY supports a long cable reach of more than 2000 meters. The DP83TD510E has external MDI termination to support intrinsic safety requirements. The device interfaces with the MAC layer through MII, Reduced MII (RMII) , RGMII, and RMII low-power 5MHz master mode. This reference design used the RGMII interface for the connection between MAC and PHY.

2.3.4 MSPM0G1107 Microcontroller

The MSPM0G1107 microcontroller (MCU) is part of the highly-integrated, ultra-low-power 32-bit MSP MCU family based on the enhanced Arm Cortex-M0+ 32-bit core platform operating at up to 80MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from –40°C to 105°C, and operate with supply voltages ranging from 1.62V to 3.6V. The MSPM0G110x devices provide up to 128KB embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM with ECC and hardware parity option.

In this reference design the MSPM0G1107 is used to handle the Serial Communication Classification Protocol (SCCP), which is part of the Power over Data Line (PoDL) communication for the power-sourcing equipment (PSE) role.

2.3.5 LMK1C1106 6-Channel Output LVCMOS 1.8V Buffer

The LMK1C110x is a modular, high-performance, low-skew, general-purpose clock buffer family. All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range. The LMK1C110x supports a synchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

In this reference design this clock buffer provides five times 25MHz frequency to the five Ethernet PHYs.

2.3.6 LMK6C Low-Jitter, High-Performance, Bulk-Acoustic-Wave (BAW) Fixed-Frequency LVCMOS Oscillator

The LMK6C is a low-jitter, high-performance, bulk-acoustic-wave (BAW) fixed-frequency LVCMOS oscillator. The high-performance clocking, mechanical stability, flexibility, and small package options for this device are designed for reference and core clocks in industrial applications.

In this reference design the 25MHz BAW oscillator is used to source the clock buffer, which clocks the five Ethernet PHYs.

2.3.7 TLVM13630 High-Density, 3V to 36V Input, 1V to 6V Output, 3A Step-Down Power Module

The TLVM13630 synchronous buck power module is a highly-integrated, 36V, 3A DC/DC design that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for V_{IN} and V_{OUT} located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

In this reference design, the LLVM13630 power module generates a 5V system supply.

2.3.8 LM74700-Q1 Reverse-Polarity Protection Ideal Diode

The LM74700-Q1 is an ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low-loss reverse-polarity protection with a 20mV forward voltage drop. The wide supply input range of 3.2V to 65V allows control of many popular DC bus voltages such as 24V industrial systems.

In this reference design, the LM74700-Q1 acts as reverse polarity protection for the 24V system input voltage.

2.3.9 TPS62825A Synchronous Step-Down DC-DC Converter

The TPS6282x is an easy-to-use synchronous step-down DC/DC converter family with a very-low-quiescent current of only 4µA. Based on the DCSControl topology, the device provides a fast transient response. The internal reference allows regulation of the output voltage down to 0.6V with a high feedback voltage accuracy of 1% over the junction temperature range of –40°C to 125°C. The family devices are pin-to-pin and BOM-to-BOM compatible. The entire design requires a small 470nH inductor, a single 4.7µF input capacitor, and two 10µF output capacitors or a single 22µF output capacitor.

In this reference design, two TPS62825A are used to generate 3.3V and 1.8V system power.

2.3.10 LMR36006 Ultra-Small Synchronous Step-Down Converter

The LMR36006 regulator is an easy-to-use, synchronous, step-down DC/DC converter. With integrated high-side and low-side power MOSFETs, up to 0.6A of output current is delivered over a wide input voltage range of 4.2V to 60V.

In this reference design, the LMR36006 device is used to generate 6.5V for the PoDL subsystem.

2.3.11 TLV62568A High-Efficiency Step-Down Buck Converter With Forced PWM

The TLV62568A device is a synchronous step-down buck DC/DC converter optimized for high efficiency and compact design size. The device integrates switches capable of delivering an output current up to 2A. At the whole load range, the device operates in pulse width modulation (PWM) mode with 1.5MHz switching frequency. In shutdown, the current consumption is reduced to less than 2µA.

In this reference design two TLV62568A devices generate 2.5V and 1.0V for the DP83867 Ethernet PHY power supply.

3 System Design Theory

This section provides more details about the different functional sections on the reference design. Figure 3-1 shows the blocks that are discussed in the subsections.

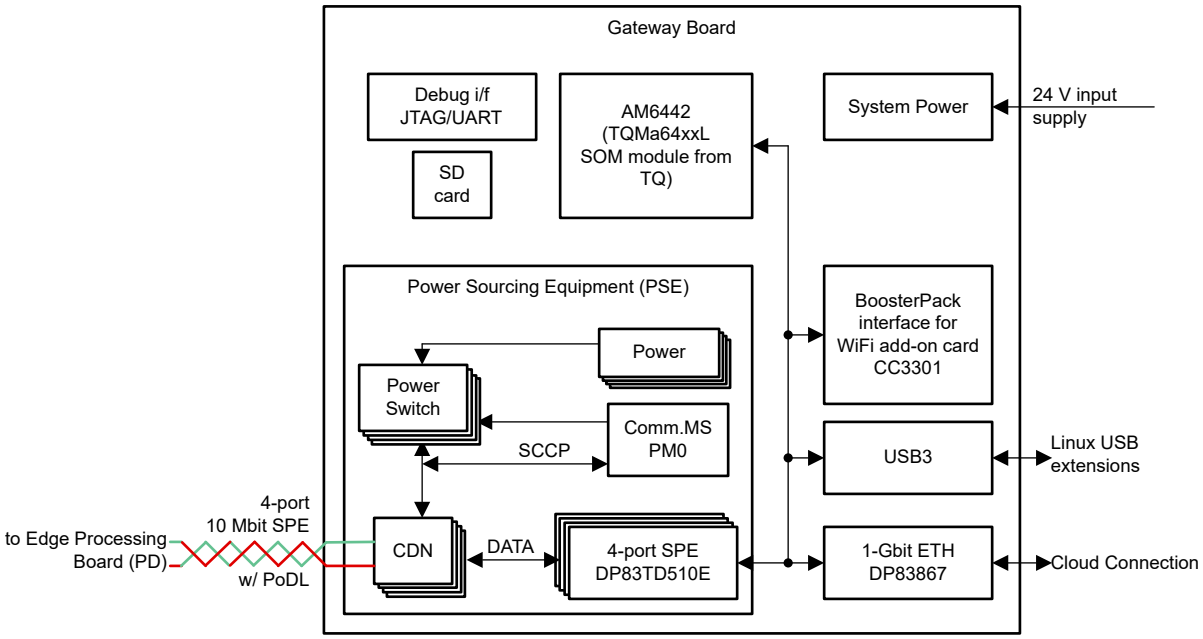


Figure 3-1. System Block Diagram

3.1 Power Subsystem

This section gives details about the power subsystem on the reference design. Figure 3-2 shows the power tree.

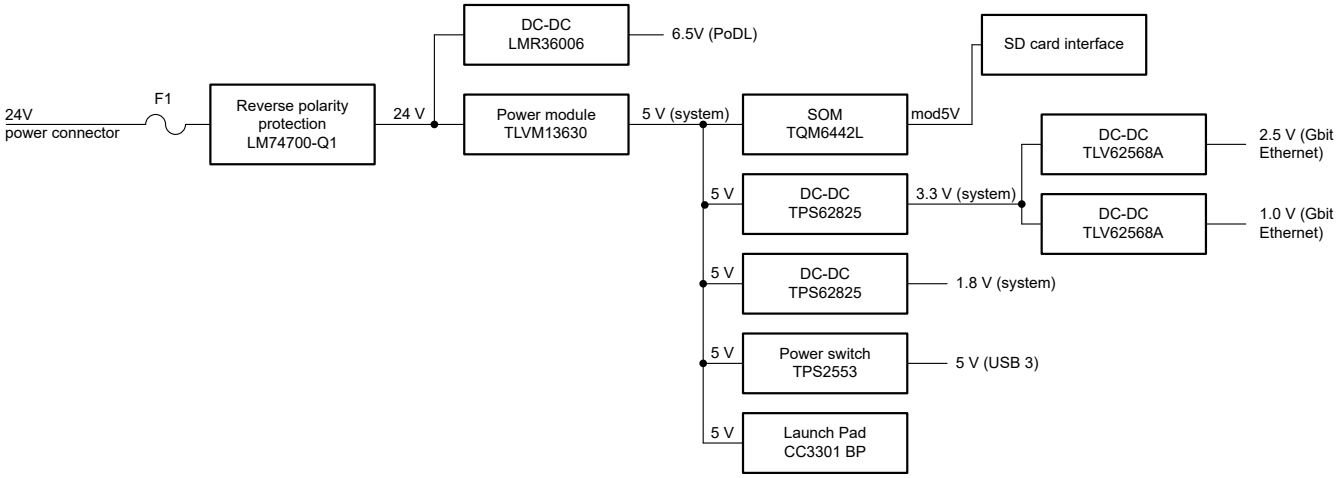


Figure 3-2. Gateway Board Power Tree

The nominal input voltage of this reference design is 24V, provided through the board main power connector. The fuse F1 protects the design from overcurrent higher than 2A. After that, the LM74700-Q1 provides the correct applied voltage polarity, and secures reverse polarity protection. Next 24V is provided to the DC-DC controllers to generate the required power-supply voltages.

The 6.5V voltage supply rail is generated by the ultra-small synchronous DC-DC controller LMR36006 from the 24V supply. The 6.5V rail is used by the power-over data line (PoDL) subsystem.

The 5V voltage supply rail is generated by the high-density TLVM13630 integrated power module of 24V supply. The 5V is used to supply the TQMa6442L system-on-module (SOM) that includes the AM6442 processor, PMIC, and DDRLP memory. In addition, the 5V supplies additional DC-DC converters on this reference design. The rail also provides the 5V power supply to the LaunchPad connector for the CC3301 Wi-Fi booster pack and to the TPS2553 power switch which supplies 5V at the USB 3 connector interface.

The 3.3V voltage supply rail is generated by the highly-accurate TPS62825 DC-DC step-down converter of the 5V supply. The 3.3V is used to supply various subsystems in this reference design like the DP83TD510E SPE PHYs, PoDL subsystem, and UART communication interface. Furthermore, the 3.3V is used as input for DC-DC to generate additional voltages at the Gbit Ethernet subsystem.

The 1.8V voltage supply rail is also generated by a second highly-accurate TPS62825 DC-DC step-down converter of the 5V supply. The 1.8V is used to supply various subsystems in this reference design.

The Gbit Ethernet subsystem with DP83867 Ethernet PHY requires additional accurate voltages of 2.5V and 1.0V. Those two voltages are generated by the highly-efficient TLV62568A step-down converter of the 3.3V supply rail.

3.2 AM6442 System on Module Subsystem

This section gives details about the AM6442 system on module on the reference design. Figure 3-3 shows the system-on-module (SOM) block diagram.

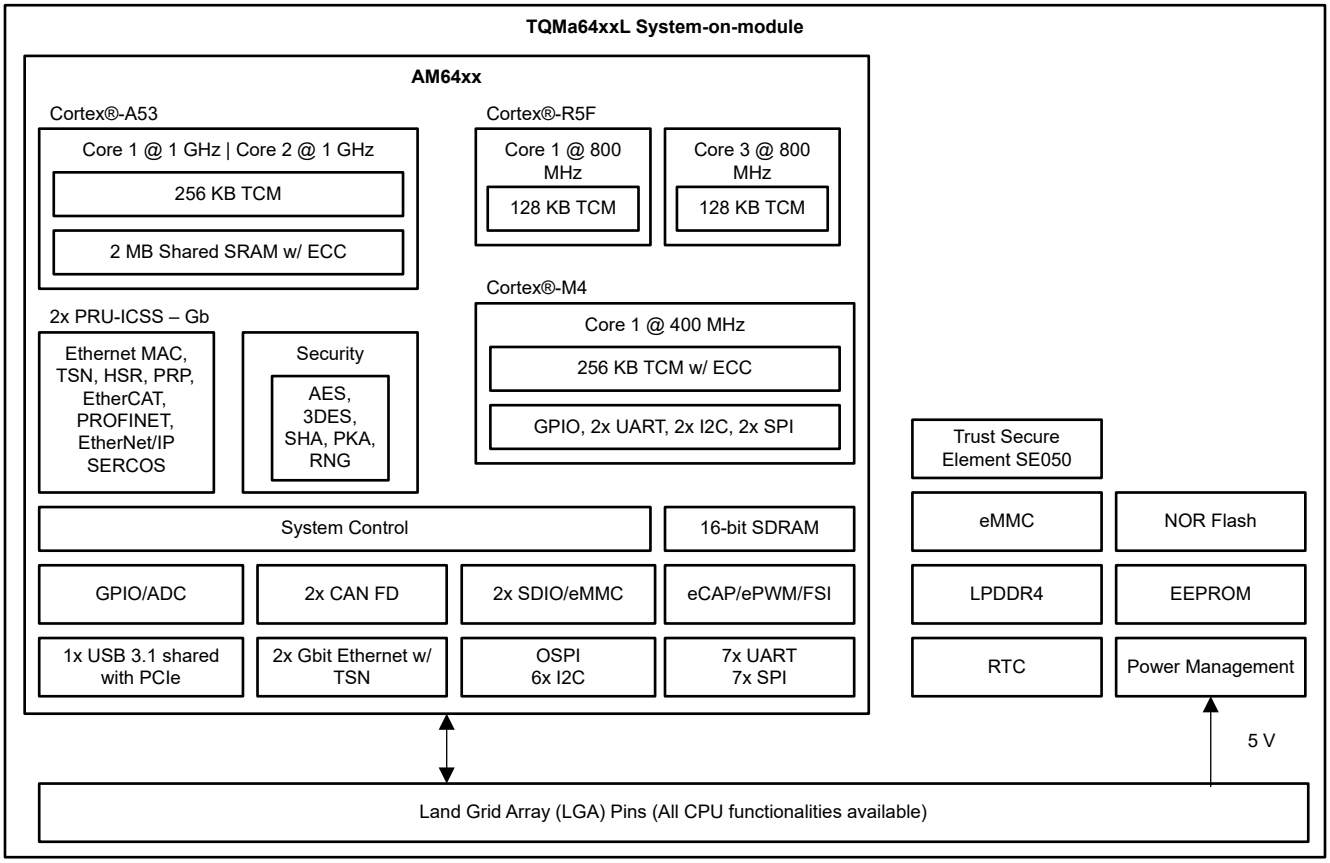


Figure 3-3. TQMa64xxL System-on-Module Block Diagram

The TQMa64xxL embedded module is based on the AM64x processor family. This land grid array (LGA) module is designed to use the pin-compatible processors on one module design. This module is design for headless applications with extended real-time requirements. The CPU offers integrated programmable real time unit (PRU) up to four times gigabit Ethernet interfaces with TSN support for the realization of real-time applications. In addition, the processor has various interfaces such as USB 2.0, CAN-FD, UART, SerDes, and so forth.

The SOM simplifies the PCB development because all of the sensitive signals, like the DDR memory interface and the power management are encapsulated within the SOM. The SOM supports a land grid array (LGA), which is directly soldered onto the carrier board. Most of the AM6442 signals are exposed on the balls of the SOM, and are accessible by this reference design, like five RGMII interfaces, USB 3 interface, SPI, UART, and GPIOs.

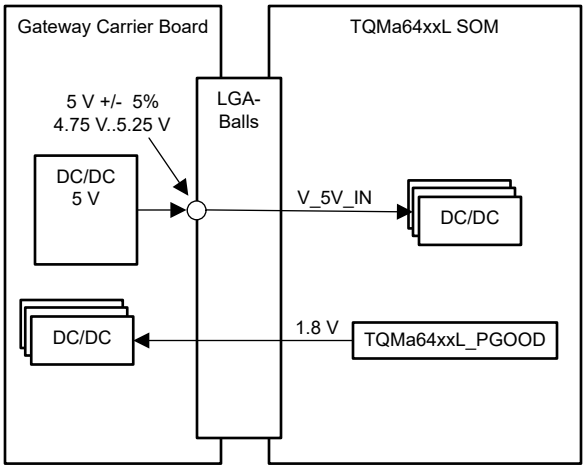


Figure 3-4. TQMa64xxL Power Block Diagram

The power supply of the SOM requires 5V via the LGA-balls. The 5V power supply is generated by the power supply subsystem in this reference design. Refer to the design checklist from TQ for additional details about how to integrate the SOM onto a carrier board.

3.3 Ethernet Subsystem

There are two Ethernet subsystems in this reference design. One subsystem consisting of four DP83TD510E Ethernet PHYs, supporting single-pair Ethernet. The second subsystem with one DP83867 device supports gigabit Ethernet for cloud connection, see Figure 3-5.

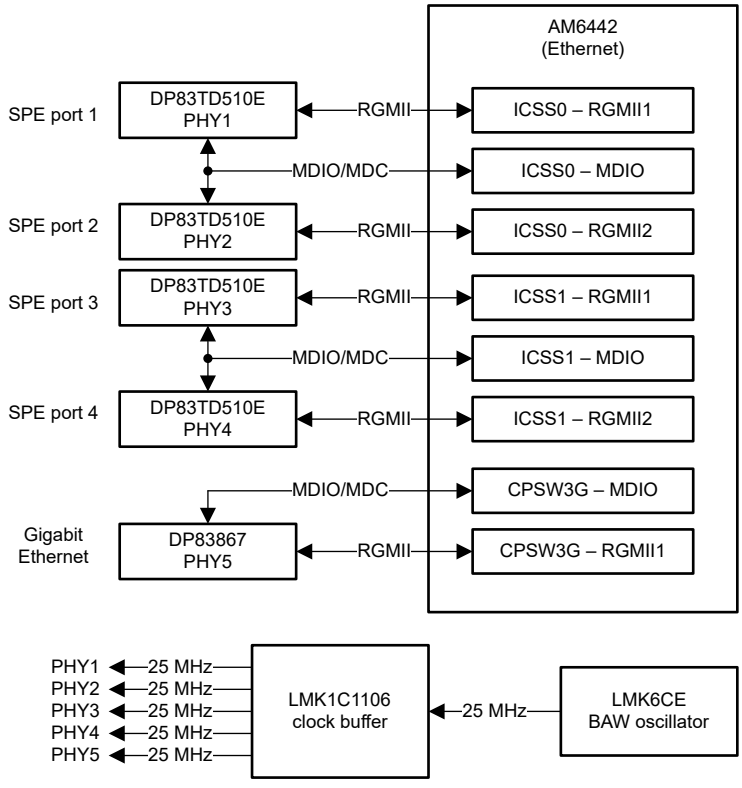


Figure 3-5. Ethernet Subsystem and Clocking on Gateway Board

The MAC-to-Ethernet PHY connection for all five PHYs is RGMII. RGMII can be used for 1000Mbps speed as well as for 10Mbps speed. The MAC enables the appropriate speed on the RGMII clock line towards the Ethernet PHY.

The five MACs are integrated into the AM6442 microprocessor. Four of the five MACs are within the industrial communication subsystem (ICSS) peripheral. The fifth MAC port is within the CPSW peripheral. All MACs are accessible as network interfaces in the Linux operating system.

The DP83867 Gbit Ethernet PHY is configured for the MDIO address 1. The RGMII interface is connected to the CPSW peripheral of the AM6442 processor. The DP83867 is also connected to the MDIO, MDC interface of the CPSW. The Gbit Ethernet port uses a standard RJ45 Ethernet connector. The two LEDs inside the RJ45 connector show the link-up and receive or transmission activity state of the PHY.

The DP83TD510E PHYs are configured to use MDIO address 0 and 1. Two of the four Ethernet PHYs are connected to ICSS0 and the second two devices are connected to ICSS1. The MDIO, MDC lines of each of the two PHYs are connected to the appropriate ICSS0 or ICSS1 peripheral. For the SPE ports there are two connector options available in parallel: Phoenix Contact SPE-T1 connector or standard screw terminal from Wurth Electronics. Each SPE port has three LEDs to indicate PHY states link (short reach and long reach) and receive or transmit activity.

Within the MDI path of the PHYs, PoDL is coupled onto the MDI path.

The 25MHz clock source is generated by the 25MHZ BAW oscillator LMK6CE. This 25MHz clock is fed into the LMK1C1106 LMCMOS clock buffer with up to 6 outputs. The 25MHz outputs are connected to the five Ethernet PHYs.

3.4 Power Over Data Line (PoDL) Subsystem

This reference design follows the approaches documented in the *How to Implement an IEEE 802.3cg or 802.3bu-Compliant PoDL PSE* application note.

3.5 Additional Subsystems

This section details additional subsystems supported in the reference design.

3.5.1 USB 3.1 Interface

This reference design supports a USB 3.1 Gen1 compliant interface. As a USB host, this interface supports SuperSpeed (5Gbps), high speed (480Mbps), full speed (12Mbps), and low speed (1.5Mbps). As a device the interface supports high speed (480Mbps), and full speed (12Mbps). The reference design is limited to USB 2.0 on-the-go support. For controlling VBUS power supply, this reference design uses the TPS2553 device, a precision adjustable current-limited power-distribution switch. The enable pin is controlled by the AM64xx USB driver via an GPIO.

For ESD and surge protection of the USB port, this reference design uses TPD4EUSB30, a 4-Channel ESD protection for SuperSpeed USB 3.0 interface.

3.5.2 Micro SD Card Interface

The processor board provides an micro Secure Digital (µSD) card interface connected to MMC1 port of the AM6442 processor. The µSD card interface supports UHS1 operation including operations at the 3.3V IO level.

For ESD and surge protection of the µSD card, the TPD4S009 device is used. This is a 4-channel ESD design for high-speed interfaces.

The µSD card enables this reference design to boot a Linux OS from an external attached memory.

3.5.3 SimpleLink™ CC3301 Wi-Fi® 6 and Bluetooth® Low-Energy BoosterPack™ Interface

This reference design supports a booster pack interface to attach an external CC3301 Booster Pack (BP-CC3301).

3.5.4 AM6442 UART Interface

The AM6442 SoC UART0 interface is used to interface the PC with the Linux serial terminal console. The AM6442 UART0 port is interfaced with FT232RQ for UART-to-USB functionality and terminated on a micro B connector (J12). When the EVM is connected to a PC host using the provided USB cable, the PC host can establish a Virtual Com Port which can be used with any terminal emulation application. The FT332RQ is bus powered. Virtual Com Port drivers for the FT232RQ can be obtained from manufacturers website: ftdichip.com/products/ft232rq/.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

4.1.1 Board Interface

Figure 4-1 shows various connectors, switches, and jumpers used to interface with the reference design.

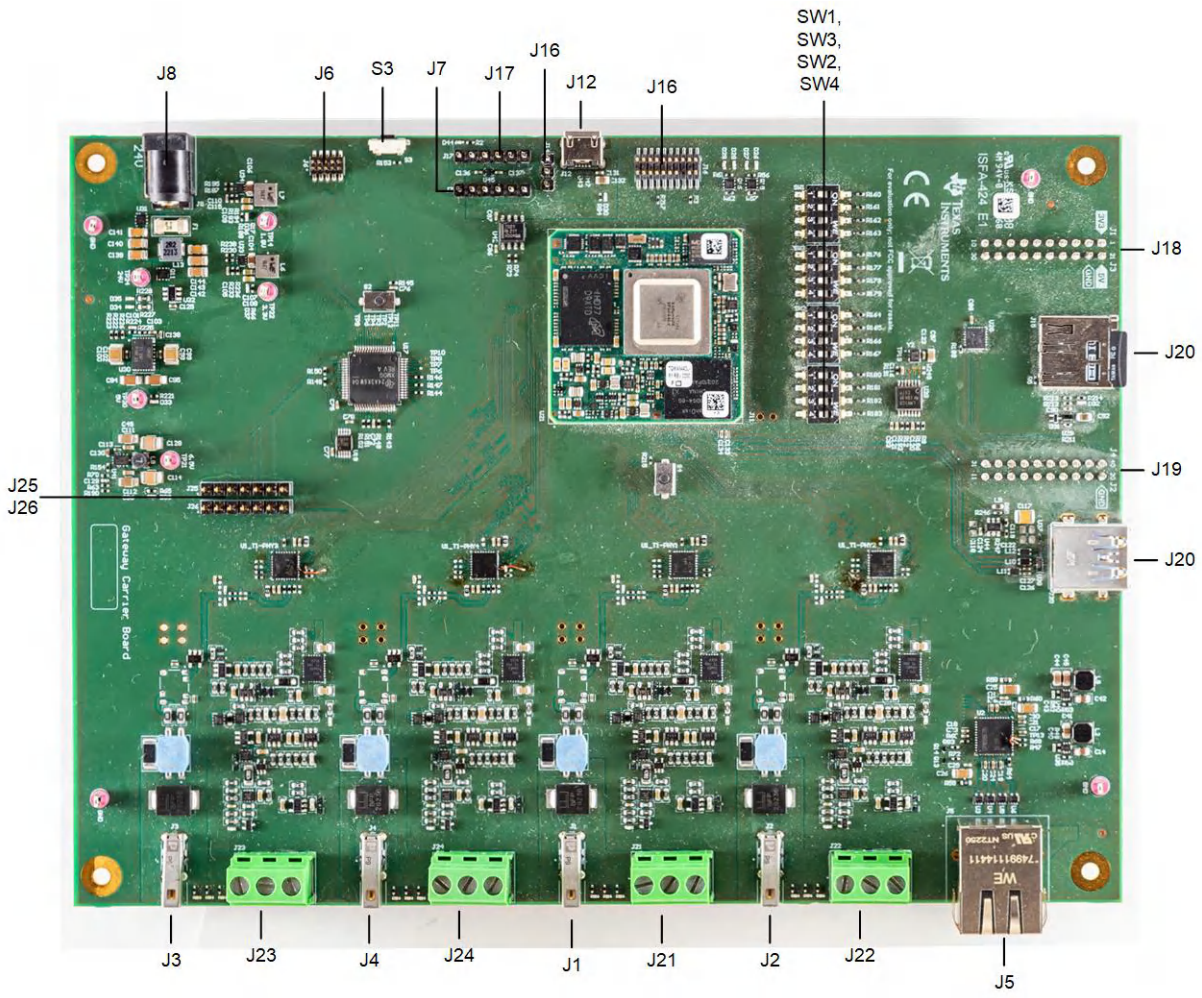


Figure 4-1. Interfaces on Gateway Board

Table 4-1. Board Connectors, Switches, and Headers

CONNECTOR	DESCRIPTION
J8	External 24V supply
J6	JTAG interface MSPM0
S3	RESET button MSPM0
J17	UART0 TXD, RXD interface of AM6442
J7	UART TXD, RXD interface of MSPM0
J14	Power supply selector for ISO7021 - set jumper to 1-2 for selecting power from FTDI device. Refer to schematic.
J12	Micro USB interface to UART0 serial console terminal of AM6442
SW1, SW2, SW3, SW4	AM6442 boot mode switches
J18, J19	Interface to CC3301 Wi-Fi and Bluetooth® BoosterPack Plug-in Module (BP-CC3301)
J20	USB 3 Type A connector

Table 4-1. Board Connectors, Switches, and Headers (continued)

CONNECTOR	DESCRIPTION
J15	µSD card slot
J5	Gigabit RJ45 connector
J16	JTAG interface AM6442
S4	RESET button AM6442
J1, J21	Single pair Ethernet connector port 1
J2, J22	Single pair Ethernet connector port 2
J3, J23	Single pair Ethernet connector port 3
J4, J24	Single pair Ethernet connector port 4
J25, J26	PoDL debug interface for single pair Ethernet port 3

4.1.1.1 Boot Switch Configuration

Place the boot switch selectors (SW1, SW2, SW3, and SW4) into the selected boot mode. See Figure 4-2 for booting from the SD card. Refer to the AM6442 technical reference manual for boot mode description and boot mode configuration.

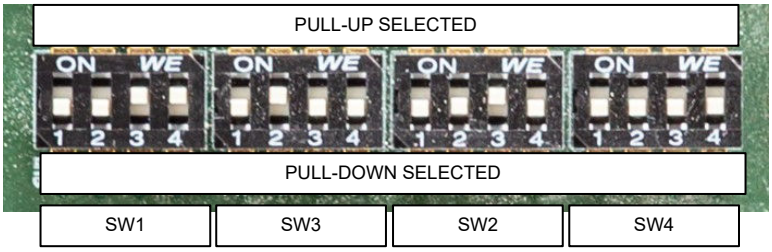


Figure 4-2. AM6442 Boot Switch Configuration for Booting From SD Card

4.1.1.2 Starting up the Reference Design

Perform the following steps to start-up the reference design:

- Connect a USB cable between a PC and the micro USB connector (J12)
- Open a serial terminal (for example, TeraTerm) and connect to the USB serial port of the reference design. Configure the serial port to 11500 baud, 8N1.
- Add µSD card with Linux image to µSD card slot (J15)
- Use bench supply to provide 24V to power connector (J8)
- Once power is applied, the reference board boots from external µSD card

Once 24V power is applied, the reference board boots from external µSD card. Use the serial terminal console to interface and control the reference design.

4.2 Software Requirements

4.2.1 PoDL PSE Protocol Programming

The MSPM0 (U17) must be programmed with PoDL power sourcing equipment (PSE) software to enable power over data line communication with the powered device (PD) like the edge processing board. Use MSPM0 programming tools to flash the PoDL-PDE application binary to the MSPM0. Programming needs to be applied one time to enable PoDL communication.

4.2.2 Create an SD Card Image With U-Boot and Linux

U-Boot is the bootloader that loads the Linus image. An Linux SD card image typically holds both images on a single card.

Get the gateway Linux image for the µSD card. Follow the SDK user guide on how to create a SD card image.

4.3 Test Setup and Procedure

Perform the following steps to start-up the reference design:

- Connect a USB cable between a PC and the micro USB connector (J12)
- Open a serial terminal (for example, TeraTerm) and connect to the USB serial port of the reference design. Configure the serial port to 11500 baud, 8N1.
- Add a µSD card with Linux image to µSD card slot (J15)
- Connect an Ethernet cable between RJ45 connector (J5) and a network Ethernet switch (optional step)
- Use a bench supply to provide 24V to power connector (J8)
- Once power is applied, the reference board boots from external µSD card.

When 24V power is applied to J8, the reference board boots from external µSD card. Use the serial terminal console to interface and control the reference design.

Figure 4-3 shows the Linux console boot prompt.

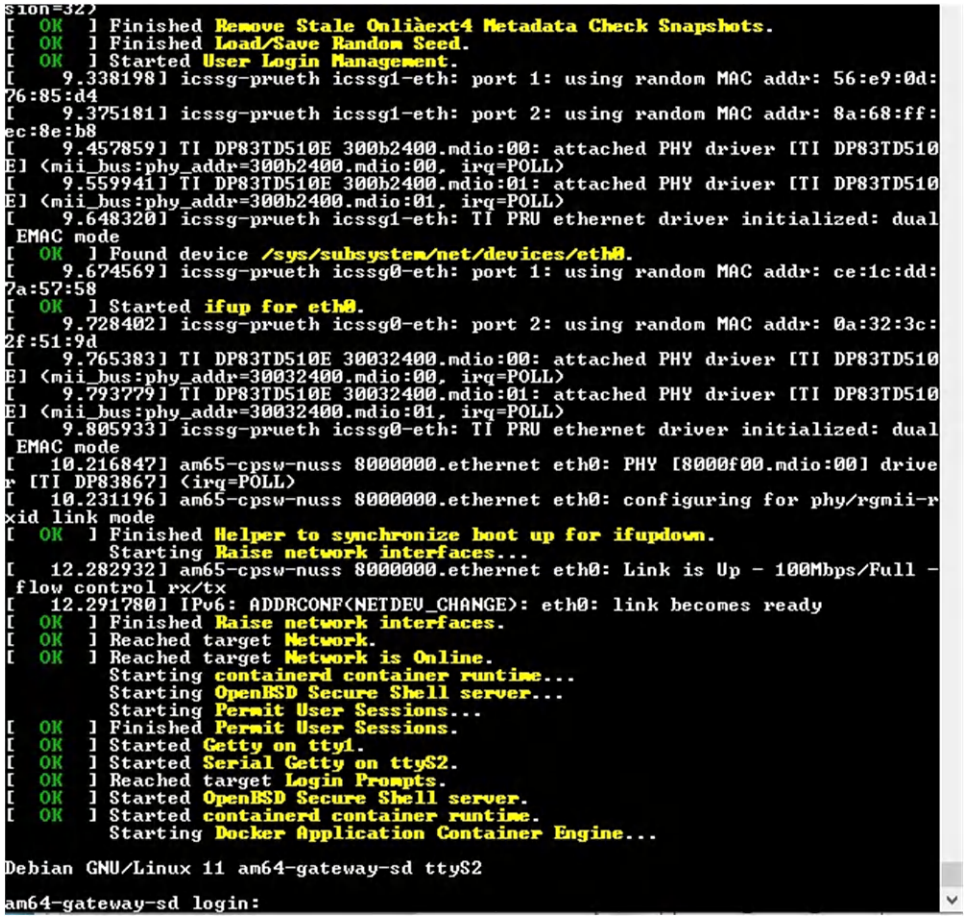


Figure 4-3. Linux Console After Booting

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010262.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010262.

5.2 Documentation Support

1. Texas Instruments, *AM64x Sitara™ Processors Data Sheet*
2. Texas Instruments, *DP83TD510E Ultra-Low Power 802.3cg 10Base-T1L 10M Single Pair Ethernet PHY* data sheet
3. Texas Instruments, *DP83867E/IS/CS Robust, High Immunity, Small Form Factor 10/100/1000 Ethernet Physical Layer Transceiver* data sheet
4. Texas Instruments, *MSPM0G110x Mixed-Signal Microcontrollers* data sheet

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

6 About the Author

THOMAS MAUER: Thomas Mauer is a System Engineer in the Factory Automation and Control Team at Texas Instruments Freising. He is responsible for developing reference design products for the industrial segment. Thomas brings his extensive experience in industrial communications like Industrial Ethernet and fieldbuses and industrial applications to this role. Thomas earned his degree in Electrical Engineering (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2023) to Revision A (October 2024)	Page
• Changed document title	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265