Design Guide: TIDA-010261

10BASE-T1L SPE Sensor With Power Over Data Lines (PoDL) Reference Design

Description

This reference design shows an implementation of a singe-pair Ethernet (SPE) communication back end including power over data lines (PoDL). The design uses a Sitara AM2434 MCU interfacing an analog front end on one side and a Ethernet physical (PHY) layer on the other. The powerful MCU allows not only forwarding sensor data to Ethernet, but also for performing data processing on the edge.

Resources

TIDA-010261, TIDA-010262	Design Folder
DP3TD510E, AM2434	Product Folder
MSP430FR2476, TPS2660	Product Folder
TPS798-Q1, TLVM13630	Product Folder
TPS62825A, TPS61023	Product Folder
LM74700-Q1, TVS3300	Product Folder
CSD19538Q2	Product Folder

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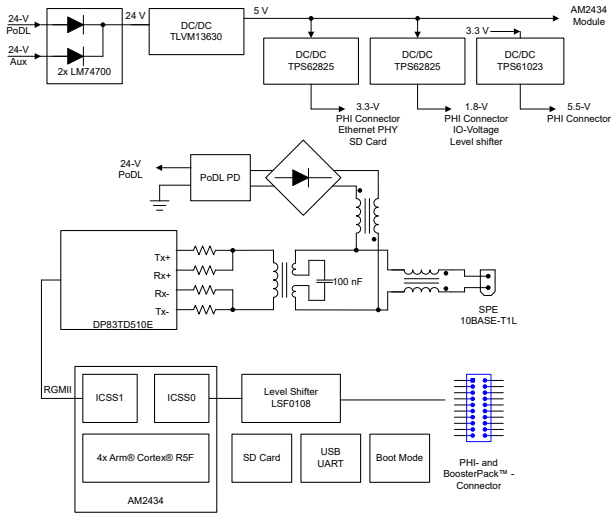
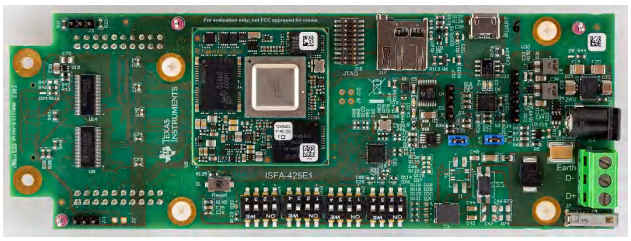
Features

- 10BASE-T1L single-pair Ethernet
- Implements PoDL power delivery (PD), Type E, Class 12, compliant to 802.3cg including serial communication classification protocol (SCCP)
- Auxiliary 24-V supply
- AM2434 MCU with quad-core Arm® Cortex®-R5F and programmable real-time unit
- PHI and BoosterPack™ Plug-in Module to connect to existing modules
- Optimized for evaluation and debugging

Applications

- Factory automation and control
- Communication module





1 System Description

This design implements a digital back end for sensors and actuators. For communication to upper layers, the design makes use of 10BASE-T1L SPE allowing up to 1 km of cable length with 10Mbps data throughput.

Two options are available to power the design, either (1) acting as a PoDL PD being powered from the Ethernet lines, (2) or operating in stand-alone mode by attaching a 24-V power supply.

The Sitara AM2434 processor on the board allows implementation of powerful sensors or actuators with the possibility to perform processing of data, like fast Fourier transform (FFT) calculations directly on the edge.

The interface option of having a PHI and BoosterPack connector, allows the design to connect to the TIDA-010249 reference design which implements a four-channel integrated electronics piezoelectric (IEPE) vibration sensor front end. In the example shown in this design guide, the vibration sensor can be used for not only capturing vibration data of four analog channels, but also processing the data, like calculating an FFT and make decisions based on the results.

1.1 Key System Specifications

PARAMETER	SPECIFICATION
Ethernet Standard	10BASE-T1L, IEEE 802.3cg
Power over Data Lines (PoDL)	Class 12, Type E
Data Coupling	Inductive
External Power Supply	24-V nominal, 200 mA
External Interfaces	BoosterPack and PHI headers
Supported OS	FreeRTOS
Communication Protocols	DHCP, TCP/IP, MQTT

2 System Overview

2.1 Block Diagram

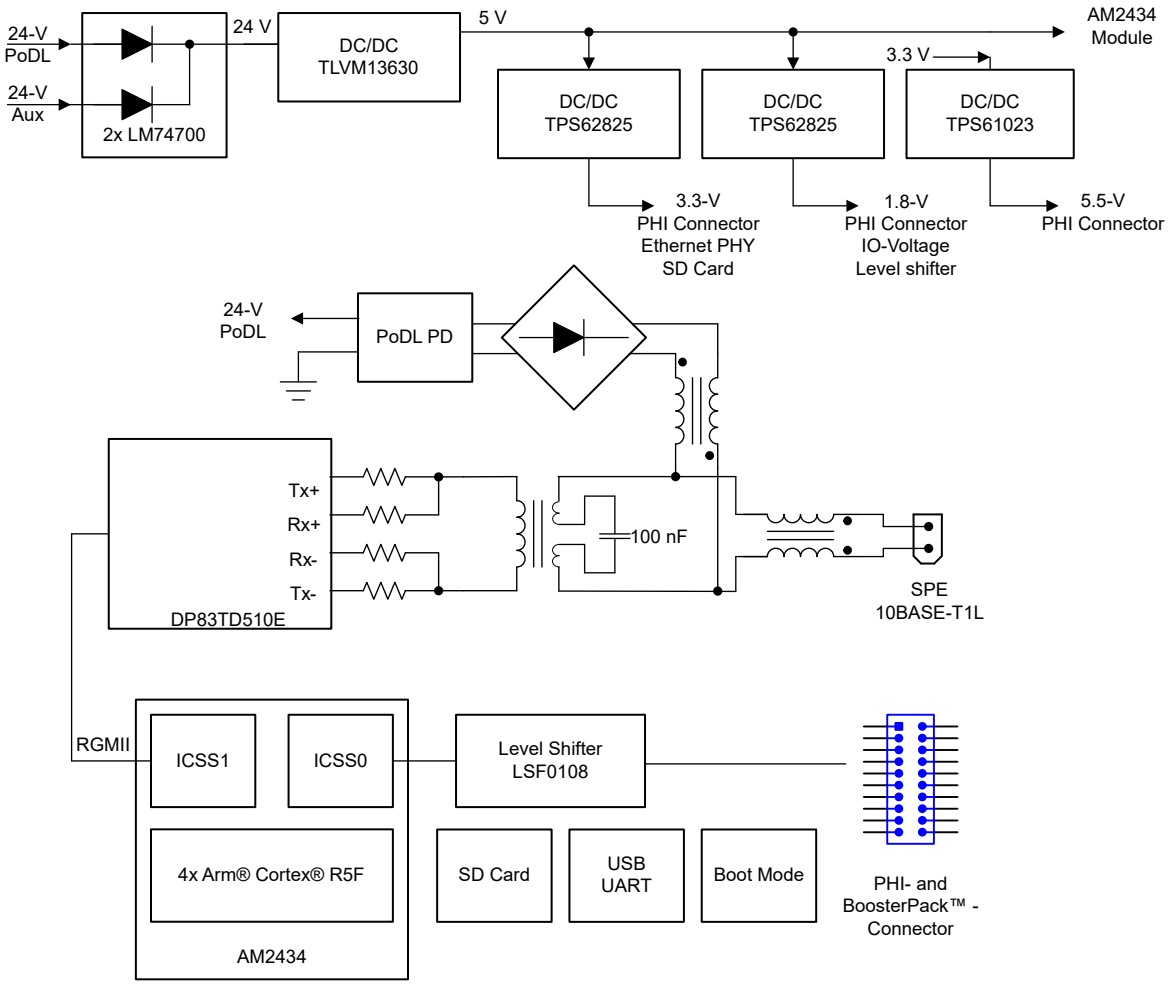


Figure 2-1. TIDA-010261 Block Diagram

2.2 Design Considerations

This reference design shows the implementation of the digital back end of a single-pair Ethernet (SPE) 10BASE-T1L sensor or actuator with the option for powering the design through Power over Data Lines (PoDL). PoDL is standardized by IEEE802.3cg. PoDL is implemented including serial communication classification protocol (SCCP) to signal the desired power class from the powered device (PD) to a power sourcing equipment (PSE).

To implement SPE together with PoDL, on the data side the design needs an Ethernet PHY such as the DP83TD510E, for translating the interface from the (media access controller) MAC to the medium-dependent interface (MDI) on the cable. On the MAC side, a media-independent interface (MII) such as a reduced gigabit MII (RGMII) is used.

To add power to this communication line, two things are needed: a coupling network to separate power and data on the line, and a device for doing the required handshaking. The coupling network can be seen as a frequency filter, where the low-frequency component (especially the DC) is going to the power part and the high-frequency components are treated as data going to the PHY. More details on this are explained in the PoDL PD and Coupling Network section. The handshaking plays an important role, similar to standard Ethernet PoE, a power sourcing equipment (PSE) needs to make sure, to provide power only to devices supporting power. Otherwise the equipment gets damaged. This handshaking is described in detail in Section 3.2.

Besides the SPE interface, this design offers a flexible interface using a PHI connector and BoosterPack connector to interface a wide range of extension boards connecting to analog-to-digital converters (ADCs), for example. This interface is equipped with a couple of level shifters to support different voltage levels as needed by what the interface gets connected to. This interface is connected to one of the Integrated Control and Safety System (ICSS) of the Sitara processor, so a wide set of interfaces can be implemented. The MCU Plus SDK offers an example implementation for ADS127, showing a Serial Peripheral Interface (SPI) implemented on ICSS and inter-processor communication.

The reference design offers Joint Test Action Group (JTAG) access and an isolated Universal Serial Bus (USB) Universal Asynchronous Receiver or Transmitter (UART) interface to simplify bringup and debug. For storing an application, use either an onboard micro Secure Digital (SD) card connector, a NOR flash, or an eMMC on the module. The boot mode switches allow selection of which peripheral to start from.

If instead of the AM2434-based module, a pin-compatible AM6442 module is used, the processor also offers Arm Cortex-A53 cores making it possible to run FreeRTOS™, but also Linux®. This allows for the ability to build a Linux® based SPE sensor with even more processing power.

2.3 Highlighted Products

This section presents the most important devices of this reference design. For detailed information check the product page and data sheet of the devices.

2.3.1 DP83TD510E

The DP83TD510E is an ultra-low power Ethernet physical layer transceiver compliant with the IEEE 802.3cg 10Base-T1L specification. The PHY has very low noise coupled receiver architecture enabling long cable reach and very low power dissipation. The DP83TD510E has external MDI termination to support intrinsic safety requirements. The device interfaces with MAC layer through MII, Reduced MII (RMII) , RGMII, and RMII low power 5-MHz master mode. The transceiver also supports RMII back-to-back mode for applications that require cable reach extension beyond 2000 meters. The DP83TD510E supports a 25-MHz reference clock output to clock other modules on the system and offers integrated cable diagnostic tools; built-in self-test, and loopback capabilities for ease of design or debug.

2.3.2 AM2434

The AM2434 is an extension of Sitara's industrial-grade portfolio into high-performance microcontrollers. The AM2434 device is built for industrial applications, such as motor drives and remote I/O modules, which require a combination of real-time communications and processing. The AM2434 provides scalable performance with up to four Cortex-R5F MCUs, one Cortex-M4F, and two instances of Sitara's gigabit TSN-enabled PRU_ICSSG.

The AM2434 SoC architecture was designed to provide best-in-class real-time performance through the high-performance Cortex-R5F cores, tightly-coupled memory banks, configurable SRAM partitioning, and dedicated low-latency paths to and from peripherals for rapid data movement in and out of the SoC. This deterministic architecture allows for AM2434 to handle the tight control loops found in servo drives while the peripherals like FSI, GPMC, ECAPs, PWMs, and encoder interfaces help enable a number of different architectures found in these systems.

The SoC provides flexible industrial communications capability including full protocol stacks for EtherCAT target, PROFINET device, Ethernet-IP adapter, and IO-Link Controller. The PRU_ICSSG further provides capability for gigabit and TSN based protocols. In addition, the PRU_ICSSG enables additional interfaces including a UART interface, sigma-delta decimation filters, and absolute encoder interfaces.

Functional safety features can be enabled through the integrated Cortex-M4F along with dedicated peripherals which can all be isolated from the rest of the SoC. The AM2434 also supports secure boot.

2.3.3 TPS2660

The TPS2660 is part of the TPS2660x family of devices. These devices are compact, feature-rich, high-voltage eFuses with a full set of protection features. The wide supply input range of 4.2 V to 60 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±60 V. Integrated back-to-back FETs provide a reverse current blocking feature making the device an excellent choice for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source, and device protection are provided with many adjustable features including

overcurrent, output slew rate, and overvoltage, undervoltage thresholds. The internal robust protection control blocks along with the high-voltage rating of the TPS2660x helps to simplify the system design for surge protection.

A shutdown pin provides external control for enabling and disabling the internal FETs as well as placing the device in a low-current shutdown mode. For system status monitoring and downstream load control, the device provides fault and precise current monitor output. The MODE pin allows flexibility to configure the device between the three current-limiting fault responses (circuit breaker, latch off, and Auto-retry modes).

The devices are available in a 5-mm × 4.4-mm, 16-pin HTSSOP as well as 5-mm x 4-mm, 24-pin VQFN package and are specified over a –40°C to +125°C temperature range.

2.3.4 TPS79801-Q1

The TPS79801-Q1 is the first device in a line of 50-V high-voltage micropower low-dropout (LDO) linear regulators. This device is capable of supplying 50-mA output current with a dropout voltage of only 300 mV. Designed for low quiescent current high-voltage (50 V) applications, 40 µA operating and 1 µA in shutdown makes the TPS79801-Q1 a desirable choice for battery-powered or high-voltage systems. Quiescent current is also well-controlled in dropout.

Other features of the TPS79801-Q1 include the ability to operate with low equivalent series resistance (ESR) ceramic output capacitors. This device is stable with only 1 µF on the output; most older devices require from 10-µF to 100-µF tantalum capacitors for stability. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse input-battery protection, reverse output current protection, current limiting, and thermal limiting to protect the device in various fault conditions.

This device is available in a fixed output voltage of 5 V (TPS79850) and with an adjustable output voltage with a 1.275-V reference voltage (TPS79801). The TPS798xx-Q1 regulator is available in a 8-pin MSOP-PowerPAD(DGN) package with an exposed pad for enhanced thermal management capability.

2.3.5 MSP430FR2476

The MSP430FR2476 (MSP430FR247x) microcontroller (MCU) is part of the MSP430™ MCU value line portfolio of ultra-low-power low-cost devices for sensing and measurement applications. MSP430FR247x MCUs integrate a 12-bit SAR ADC and one comparator. The MSP430FR247x MCUs support an extended temperature range from –40°C up to 105°C, so higher temperature industrial applications can benefit from the Ferroelectric Random Access Memory (FRAM) data-logging capabilities of the devices.

MSP430FR247x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits include the MSP-TS430PT48 48-pin target development board. TI also provides free MSP430Ware™ software, which is available as a component of the Code Composer Studio™ IDE desktop and cloud versions within TI Resource Explorer. MSP430 MCUs are also supported by extensive online collateral, such as TI's housekeeping example series, MSP Academy training, and online support through the TI E2E™ support forums.

The MSP430 ultra-low-power (ULP) FRAM microcontroller platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the nonvolatile behavior of flash.

The TI MSP430 family of low-power microcontrollers consists of devices with different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The MCU features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally-controlled oscillator (DCO) allows the MCU to wake up from low-power modes to active mode in less than 10 µs (typical).

2.3.6 TLV7031

The TLV7031 single-channel device is a low-voltage, nanoPower comparator. This device is available in an ultra-small, leadless packages as well as standard 5-pin SC70, SOT-23, VSSOP, and TSSOP packages, making

the device applicable for space-critical designs like smartphones, smart meters, and other portable or battery-powered applications.

The TLV7031 offers an excellent combination of speed and power, with a propagation delay of 3 µs and a quiescent supply current of 315 nA. The benefit of fast response time at nanoPower enables power-conscious systems to monitor and respond quickly to fault conditions. With an operating voltage range of 1.6 V to 6.5 V, these comparators are compatible with 3-V and 5-V systems.

The TLV7031 device also makes sure no output phase inversion with overdriven inputs and internal hysteresis, so engineers can use this comparator for precision voltage monitoring in harsh, noisy environments where slow-moving input signals must be converted into clean digital outputs.

The TLV7031 has a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load. The TLV704x has an open-drain output stage that can be pulled beyond V_{CC}, making this device appropriate for level translators and bipolar to single-ended converters.

2.3.7 ATL431

The ATL431 device is a three-terminal adjustable shunt regulator, with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between V_{ref} (approximately 2.5 V) and 36 V, with two external resistors. This device has a typical output impedance of 0.05 Ω. Active output circuitry provides a very sharp turn-on characteristic, making this device an excellent replacement for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

The ATL431 has > 20 × improvement cathode current range over the TL43x predecessor and is also stable with a wider range of load capacitance types and values.

The ATL431 device is characterized for operation from –40°C to +85°C.

2.3.8 LM74700-Q1

The LM74700-Q1 is an automotive AEC Q100-qualified ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low loss, reverse polarity protection with a 20-mV forward voltage drop. The wide supply input range of 3.2 V to 65 V allows control of many popular DC bus voltages such as 12-V, 24-V, and 48-V automotive battery systems. The 3.2-V input voltage support is an excellent choice for severe cold crank requirements in automotive systems. The device can withstand and protect the loads from negative supply voltages down to –65 V.

The device controls the GATE of the MOSFET to regulate the forward voltage drop at 20 mV. The regulation scheme enables graceful turn off of the MOSFET during a reverse current event and provides zero DC reverse current flow. Fast response (< 0.75 µs) to reverse current blocking makes the device desirable for systems with output voltage holdup requirements during ISO7637 pulse testing as well as power fail and input micro-short conditions.

The LM74700-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. The high-voltage rating of the LM74700-Q1 helps to simplify the system designs for automotive ISO7637 protection. With the enable pin low, the controller is off and draws approximately 1 µA of current.

2.3.9 TPS62825A

The TPS6282A is an easy-to-use synchronous step-down DC-DC converter with a very low quiescent current of only 4 µA. Based on the DCS-Control topology, the device provides a fast transient response. The internal reference allows the designer to regulate the output voltage down to 0.6 V with a high feedback voltage accuracy of 1% over the junction temperature range of –40°C to 125°C. The device is pin-to-pin and BOM-to-BOM compatible. The entire design requires a small 470-nH inductor, a single 4.7-µF input capacitor, and two 10-µF or a single 22-µF output capacitor.

The TPS6282A is available in two varieties. The first includes an automatically entered power-save mode to maintain high efficiency down to very light loads for extending the system battery run-time. The second runs in forced-PWM maintaining a continuous conduction mode to provide the least ripple in the output voltage and a quasi-fixed switching frequency. The TPS6282A device features a Power Good signal and an internal soft start circuit. The device is able to operate in 100% mode. For fault protection, the device incorporates a HICCUP

short-circuit protection as well as a thermal shutdown. The device is available in a 6-pin 1.5 × 1.5-mm QFN package, offering the highest power density.

2.3.10 TPS61023

The TPS61023 device is a synchronous boost converter with 0.5-V ultra-low input voltage. The device provides a power supply design for portable equipment and smart devices powered by various batteries and super capacitors. The TPS61023 has typical 3.7-A valley switch current limit over full temperature range. With a wide input voltage range of 0.5 V to 5.5 V, the TPS61023 supports super capacitor backup power applications, which can deeply discharge the super capacitor.

The TPS61023 operates at 1-MHz switching frequency when the input voltage is above 1.5 V. The switching frequency decreases gradually to 0.5 MHz when the input voltage is below 1.5 V down to 1 V. The TPS61023 enters power-save mode at light load condition to maintain high efficiency over the entire load current range. The TPS61023 consumes a 20-µA quiescent current from V_{OUT} in light load condition. During shutdown, the TPS61023 is completely disconnected from the input power and only consumes a 0.1-µA current to achieve long battery life. The TPS61023 has 5.7-V output overvoltage protection, output short circuit protection, and thermal shutdown protection.

The TPS61023 offers a very small design size with 1.2-mm × 1.6-mm SOT563 (DRL) package and minimum amount of external components.

2.3.11 TLVM13630

The TLVM13630 synchronous buck power module is a highly-integrated 36-V, 3-A DC/DC design that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for V_{IN} and V_{OUT} located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

With an output voltage range from 1 V to 6 V, the TLVM13630 is designed to quickly and easily implement a low-EMI design in a small PCB footprint. The total design requires as few as four external components and eliminates the magnetics and compensation part selection from the design process.

Although designed for small size and simplicity in space-constrained applications, the TLVM13630 module offers many features for robust performance: precision enable with hysteresis for adjustable input voltage UVLO, integrated VCC, bootstrap and input capacitors for increased reliability and higher density, constant switching frequency over the full load current range for enhanced load transient performance, negative output voltage capability for inverting applications, and a PGOOD indicator for sequencing, fault protection, and output voltage monitoring.

2.3.12 LSF0108

The LSF0108 device supports bidirectional voltage translation without the need for a DIR pin which minimizes system effort (for PMBus, I^2C, SMBus, and so forth). The device supports up to 100-MHz up translation and greater than 100-MHz down translation at ≤ 30-pF capacitance load and up to 40-MHz up or down translation at 50-pF capacitance load which allows the LSF0108 to support more consumer or telecom interfaces (MDIO or SDIO).

The LSF0108 supports 5-V tolerance on the I/O port which makes the device compatible with TTL levels in industrial and telecom applications. The LSF0108 is able to set up different voltage translation levels on each channel which makes the device very flexible.

3 System Design Theory

This section provides details about the different functional sections on the reference design. Figure 3-1 shows the location and size of these functional blocks.

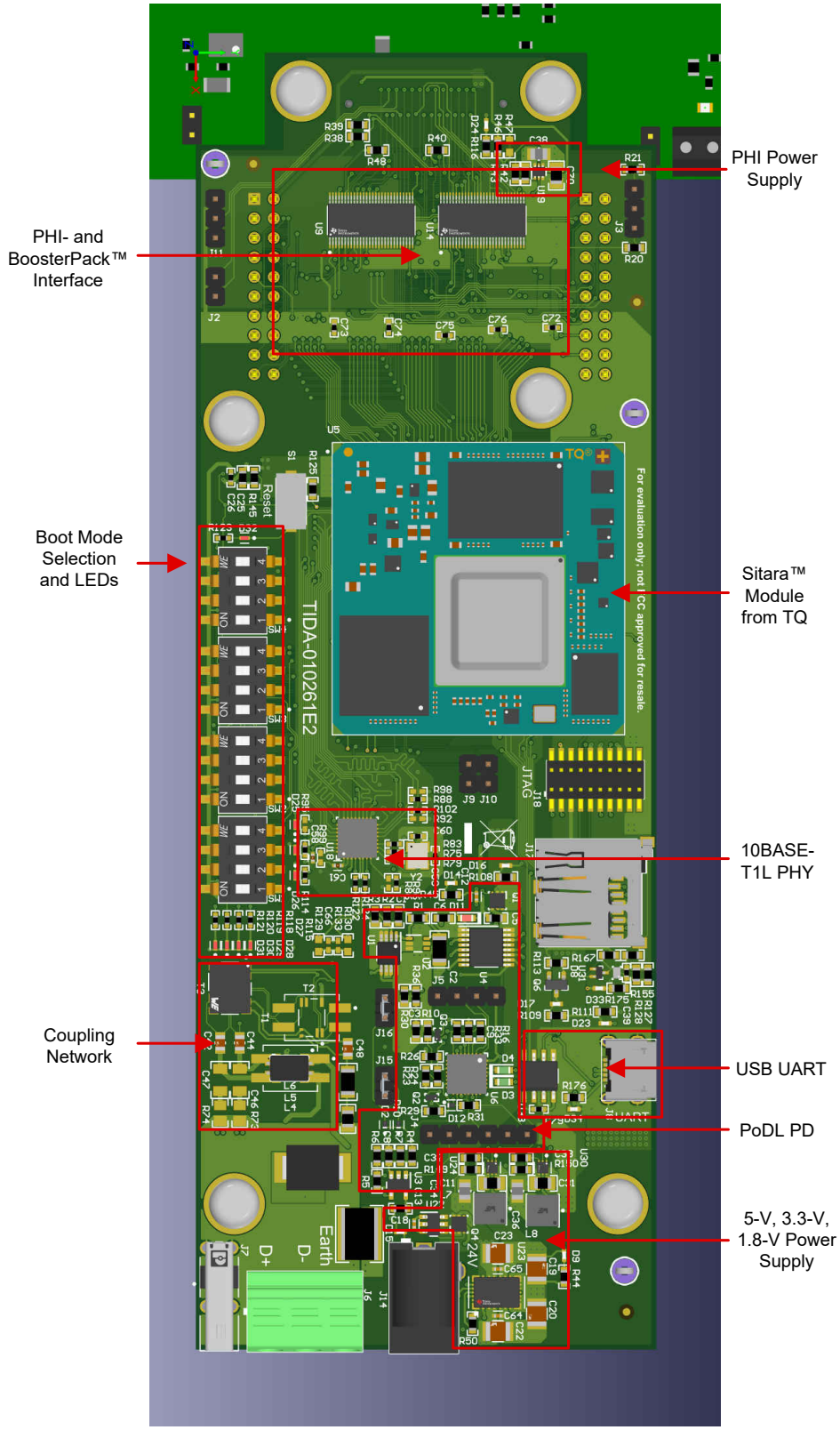


Figure 3-1. TIDA-010261 Functional Blocks

3.1 Power Supply

The PoDL voltage, as well as the auxiliary input voltage are specified to be 24 V. Because we want to be able to use both supply inputs and do not want to feed back power but have no requirements on priority, the two rails are connected together with a diode OR. To reduce power consumption and voltage drop, this is done using two ideal diodes with the LM74700 device.

By using the Sitara processor on a module, the power tree for this part is simplified, because the module contains its own power tree and just needs a regulated 5-V input. Besides that, 1.8 V and 3.3 V need to be generated for the peripherals on board. The PHI interface is specified to have an additional 5.5-V rail so one more regulator is needed.

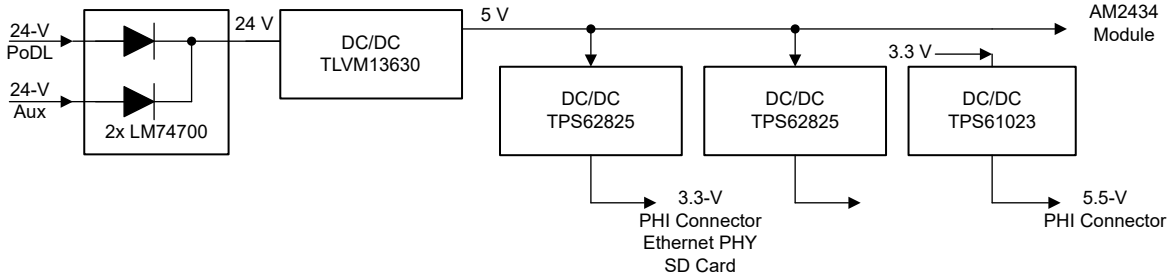


Figure 3-2. Power Supply Power Tree

Because the system operates in power class 12, about 12 W is available. Only a few Watts are needed by the onboard electronics, but to have enough headroom for further extensions connected to either BoosterPack or PHI connector, the 5-V rail is designed to provide up to 3 A. For space reasons, a power module TLVM13630 is chosen.

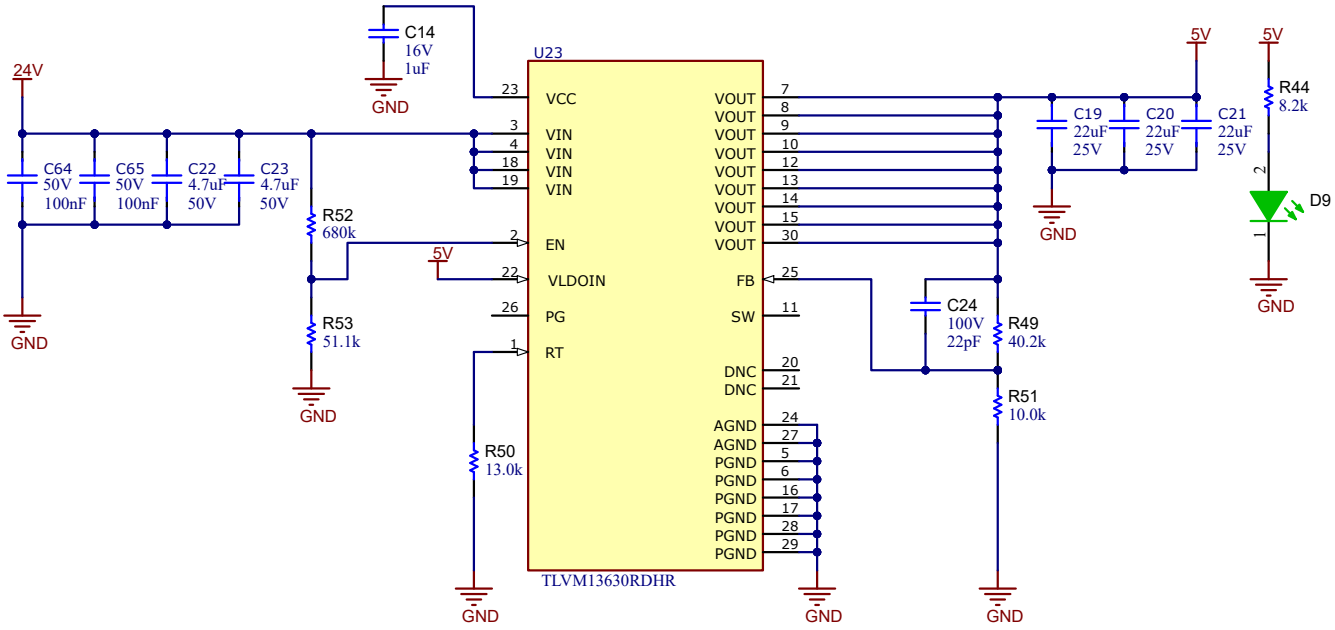


Figure 3-3. 5-V Regulator Schematic

The schematic shows the implementation, the undervoltage lockout can be programmed with R52 and R53. The output voltage is set with R49 and R51 to 5 V. A low current LED (D9) indicates the presence of output voltage.

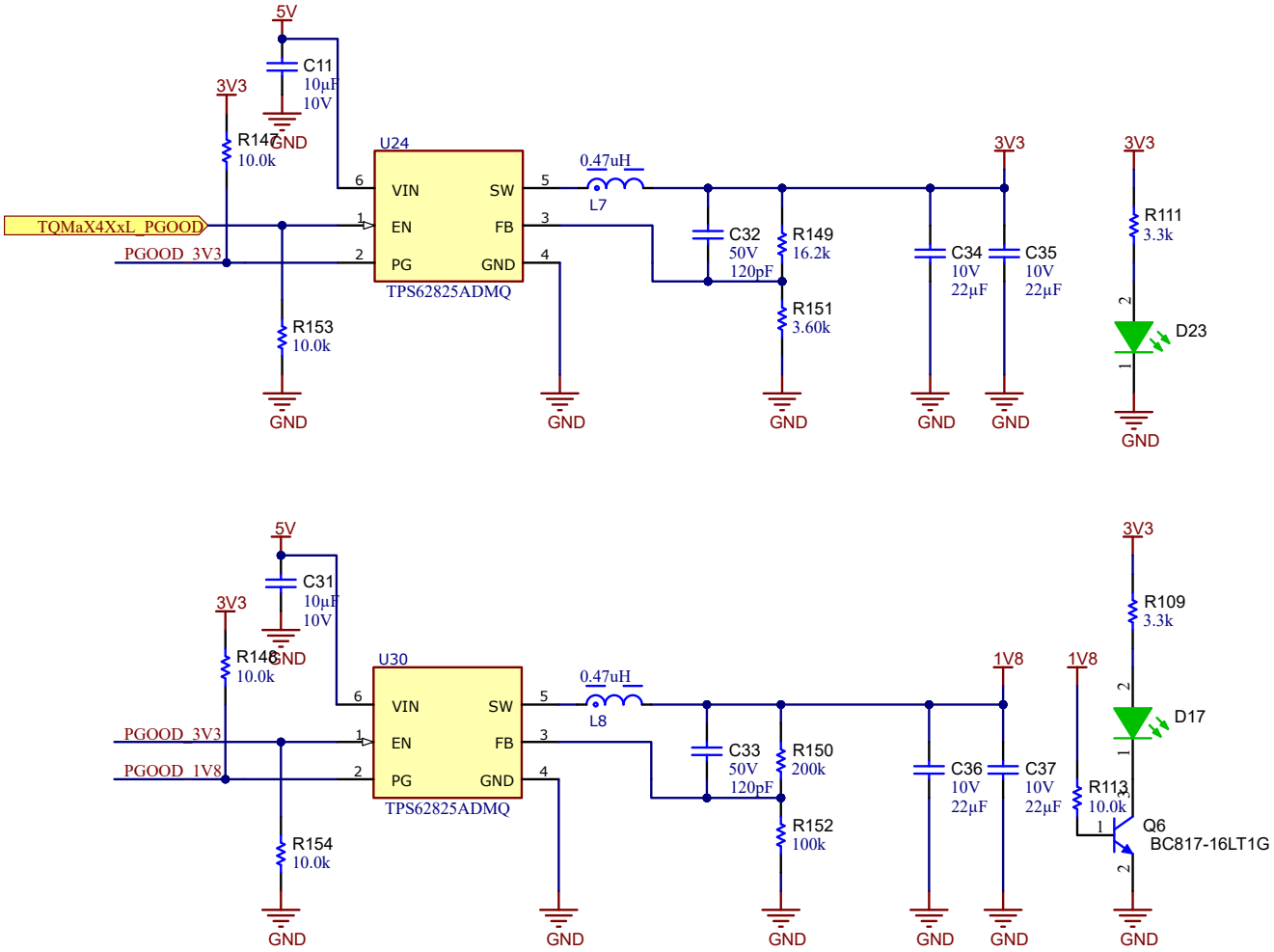


Figure 3-4. 3.3-V and 1.8-V Regulator Schematic

For the 3.3 V and 1.8 V, the same regulator with different voltage divider is used as shown in Figure 3-4 The TPS62825A device gives a small solution with up to 2 A of output current. The presence of output voltage is signaled with an LED. The 1.8-V rail needs an additional transistor, because the forward voltage of the LED is more than 1.8 V. To keep the power-up sequence, the 3.3-V regulator gets the enable signal from the Sitara module, and signals the power good to the enable signal of the 1.8-V regulator, so they start up one after another. The 1.8-V power good signal can be used for further sequencing.

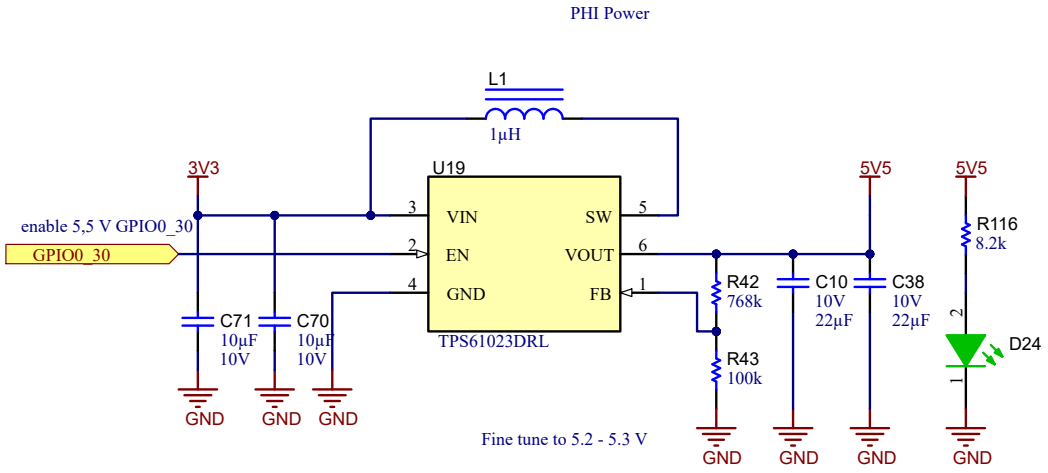


Figure 3-5. 5.5-V Boost Regulator Schematic

Figure 3-5 shows how the boost regulator is used to provide the 5.5 V to the PHI connector. Because the regulator is not always needed, the regulator can be enabled by GPIO0.30 from the Sitara processor. The TPS61023 is a synchronous boost regulator, so this device is able to turn the output off completely.

This boost regulator needs to be operated from the 3.3-V rail, because operating the regulator from 5 V violates the minimum on-time of the regulator. By using the 3.3 V as input voltage, the minimum on-time of the regulator is not violated.

3.2 PoDL PD and Coupling Network

For implementation of PoDL, the data and power path must get separated. The power path is handled by the powered device (PD), the data path can be fed directly to the Ethernet PHY.

Figure 3-6 shows a simplified image of the implementation of this coupling network. PoDL is accomplished with a small transformer instead of capacitive coupling, not because of the higher isolation voltage, but specifically because the small transformer is more robust to common-mode noise. To use a transformer with power, a split winding on the cable side is beneficial, so a capacitor for DC blocking can be inserted. Also, an AC common-mode termination can be inserted at this point on the cable side.

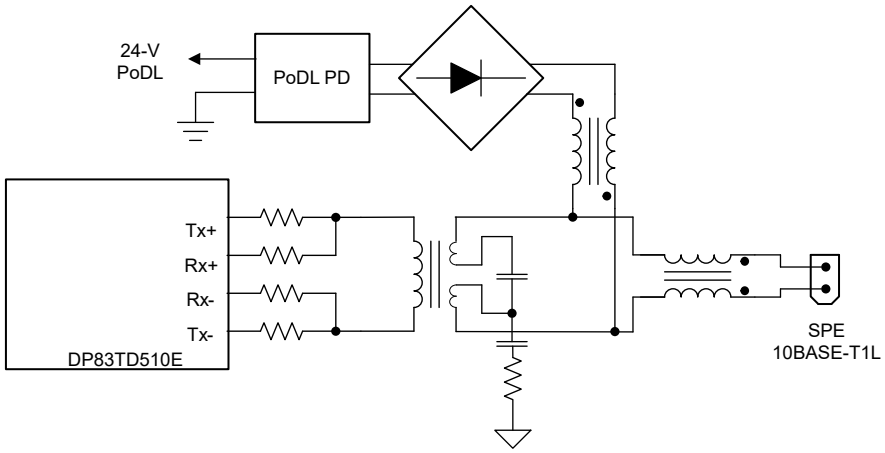


Figure 3-6. PoDL Implementation

The common-mode choke is on the cable side of this circuit, so the choke also blocks noise coming from the power supply; therefore, the common-mode choke must be rated for this current.

For the low-frequency path going to the PD, a differential-mode choke is used, the inductance has a direct influence on the droop of the signal coming from the Ethernet PHY. The higher the inductance, the lower the droop. However, a large inductance is bigger and more expensive. So the selection is always a trade-off between these parameters. Using two separate inductors here is possible, but this also increases the space requirements. To provide the possibility to evaluate different implementations, the PCB features multiple footprints for all magnetic parts.

The PD is programmed to make use of the serial communication classification protocol (SCCP) to communicate to a power sourcing equipment (PSE) being a type E and power class 12 device. More details about the implementation of a powered device (PD) are found in the *IEEE 802.3cg 10BASE-T1L Power over Data Lines Powered Device Design* application note.

3.3 Sitara™ Technology Module

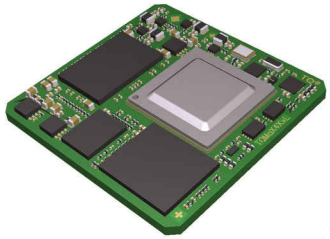


Figure 3-7. Sitara™ TQMAX4XXL Board

A system on module (SOM) from TQ is used to simplify the design. The module includes almost everything needed to start the processor. The module is powered by 5 V and generates all necessary voltages internally, so the designer does not need to take care of all the low voltage levels, especially sequencing.

The JTAG interface is used for easy development so software can be loaded to all the cores and the state can be observed. When software development is finished, this header is not used anymore and the software can be stored on an SD card for changing the software easily on the internal eMMC or NOR flash of the modules. Typically, a production device uses these internal memories. For prototyping, an SD card is more practical.

A UART interface is important for debugging and bringup which is implemented with a USB UART interface with an additional isolation in this circuit. It is useful to have the circuit isolated, especially when using the circuit powered over PoDL, to avoid ground loops or to short parts of the rectifier that is part of the PoDL PD circuit.

3.4 Boot Mode

After releasing out of reset, the processor has an internal ROM code that starts executing. This code reads in a couple of pin states to know about some initial configuration and where to boot from further. There are four small switches on the board to select where to boot from. Table 3-1 shows the two relevant configurations.

Table 3-1. Relevant Boot Mode Configurations

Boot Device	SW1	SW2	SW3	SW4
SD	1100	0000	0010	0000
eMMC	1100	0100	0010	0000

3.5 PHI and BoosterPack™ Headers

Two options are implemented to add extensions to this board. The PHI interface allows direct interface to many ADC EVMs. The BoosterPack header allows extensions to a lot of other parts, such as interfaces, motor drivers, ADCs and much more. Also, both interfaces can be used to create custom boards and connect them to SPE.

Both interfaces connect to the programmable real time unit (PRU) through level shifters. The level shifters allow use of either 1.8 Vio or 3.3 Vio, for flexibility. All the IOs can either be used from the PRU or as a system GPIO that can be accessed by and through the processor cores. To change the IO-Voltage, either R46 or R47 needs to be assembled. By default, the IO-Voltage is set to 1.8 V. For further details on changes refer to the schematic.

Figure 3-8 shows the pinout of the BoosterPack headers and Figure 3-9 shows the pinout of the PHI connector.

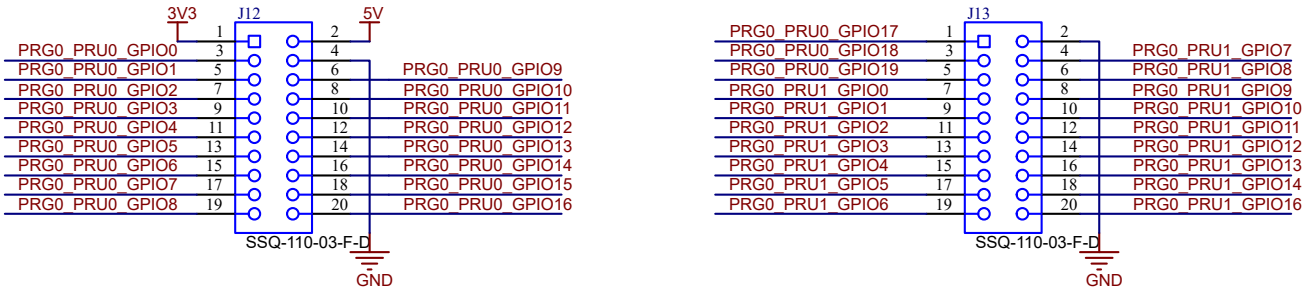


Figure 3-8. BoosterPack™ Header Pinout

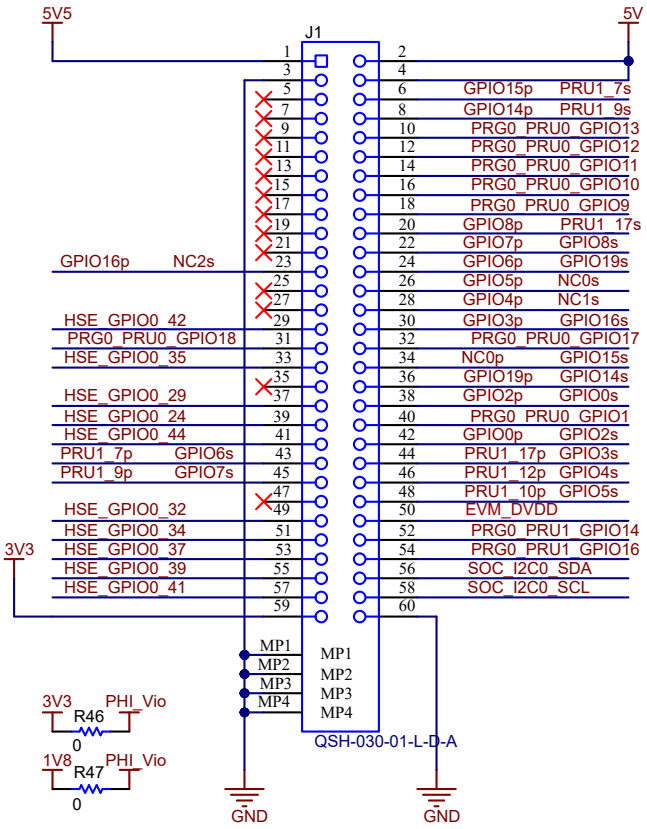


Figure 3-9. PHI Header Pinout

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

Figure 4-1 shows the important interfaces of the reference design.

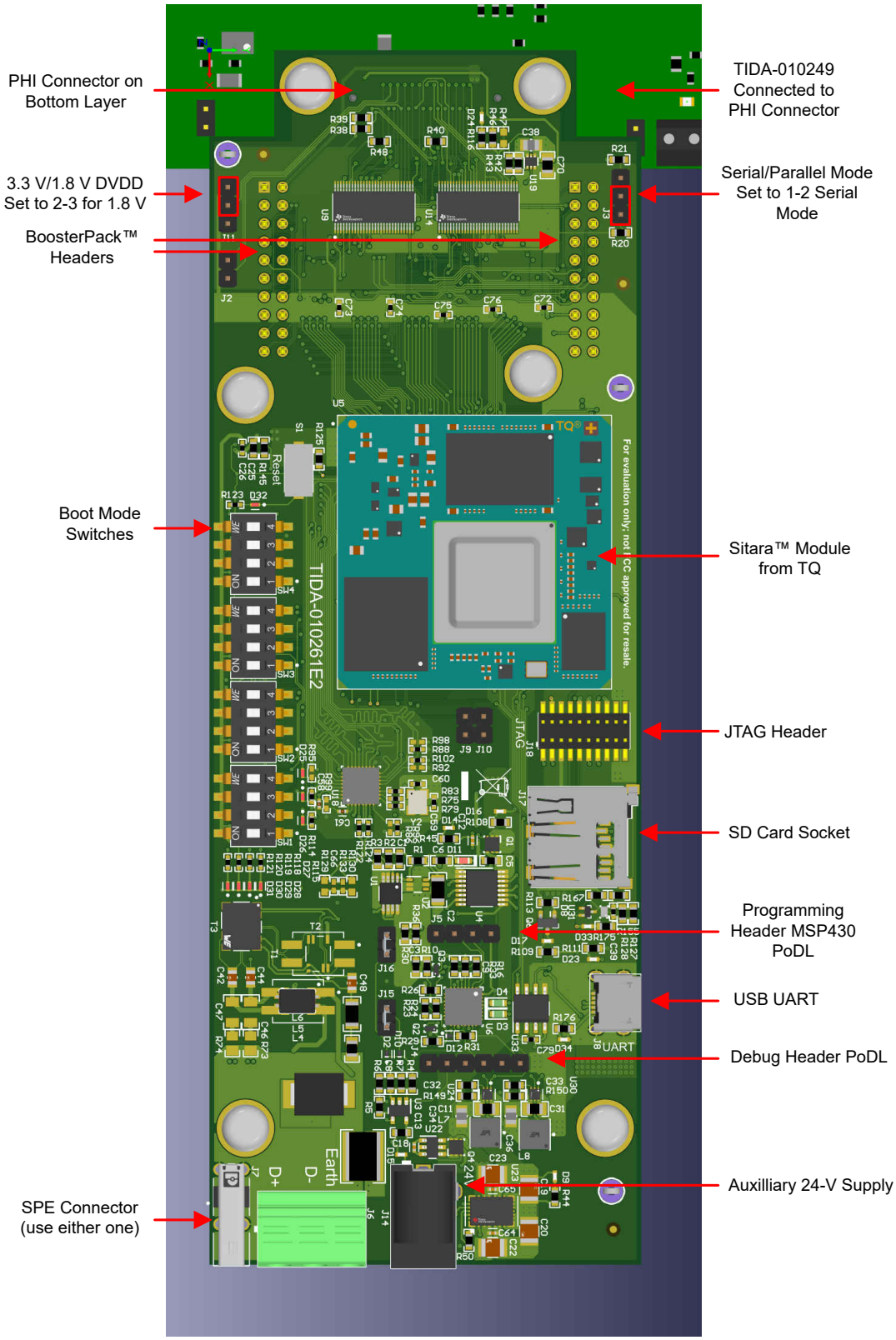


Figure 4-1. Overview of Important Connectors

To power the board, either a 10 BASE-T1L SPE switch or gateway with enabled PoDL (according to 802.3cg) with SCCP can be used. If such a device is not available, a media converter without power can be used and power can be supplied externally through a 24-V, 0.5-A power supply through the barrel jack. The board can also be operated without an SPE connection.

If the PHI connector is used, make sure to set the serial mode or parallel mode according to the connected ADC board. Also the voltage selection has to be correct to not damage the connected ADC. The settings shown above are for a connection to TIDA-010249.

For software development, the USB connector provides access to UART, so debug output can be seen. To avoid ground loops, especially when powered through PoDL, this interface is isolated.

Software can be loaded through a JTAG header or from an SD card.

The MSP430, responsible for PoDL can be programmed and debugged through the corresponding pin headers. The additional PoDL debug header allows easy access to SCCP-related data in and outputs, so a logic analyzer can be connected for debugging.

4.1.1 Boot Switch Configuration

Set the boot switches as explained in Section 3.4 to SD boot. For other configurations as explained in Table 3-1, refer to the TRM of the selected Sitara processor.

4.1.2 Reference Design Start-Up

Use the following steps to start the reference design:

1. Connect a personal computer (PC) to micro USB connector J8 for terminal output, the D34 LED lights up
2. Start terminal software with 115200 8N1 configuration
3. Connect either a 24-V minimum, 500-mA power supply to J14, or connect a PoDL PSE to J7 or J6
4. When powered from aux connector J4, the following LEDs light up: D15, D16, D9, D23, D17, D34, and D23
5. When powered from PoDL the following LEDs light up: D14, D16, D9, D23, D17, D34, and D23
6. More LEDs can light up, depending on the software that is running and on the Ethernet link state. For further details and the software-controllable LEDs, refer to the schematic.

4.2 Software Requirements

4.2.1 PD Firmware

To get the PoDL circuit working, program U6 with a firmware implementing the PD functionality. This can be with or without support for SCCP. The hardware supports both options, also firmware for both is available and tested. Connect J5 to an MSP430 debugger and load the firmware. This step only needs to be done once.

4.2.2 MCU Firmware

The easiest way to boot the Sitara MCU is to prepare an SD card containing the bootloader (tiboot3.bin) and an application (app). Use the bootloader, which is part of the Sitara SDK. For the application, the SDK provides examples used in this reference design. The interface through the PHI connector can be tested by using the PRU_IO example, interfacing an ADS127L11 through this interface and showing the samples. For more information and how to get started, refer to the SDK. documentation.

To test the Ethernet circuit of the design, use this example from the SDK with only slight modification to support the DP83TD510E Ethernet PHY.

4.3 Test Setup

The overall setup for testing is shown in Figure 4-2. The reference design is combined with the TIDA-010249 to provide an analog front end and ADCs. This is connected through the PHI header. The software is loaded onto an SD card and started in TIDA-010261.

The setup is powered through a media converter, not only providing power, but also converting single-pair Ethernet to standard Ethernet. This is connected to a standard PC, providing a Dynamic Host Configuration Protocol (DHCP) server as well as an Message Queuing Telemetry Transport (MQTT) broker.

A function generator is used to have a signal on the ADC. This setup captures the signal from the generator, stores the raw samples, calculates an FFT and transfers all the data formatted as JavaScript Object Notation

(JSON) strings to an MQTT broker. Here, other devices in the network can subscribe and do further processing or visualization.

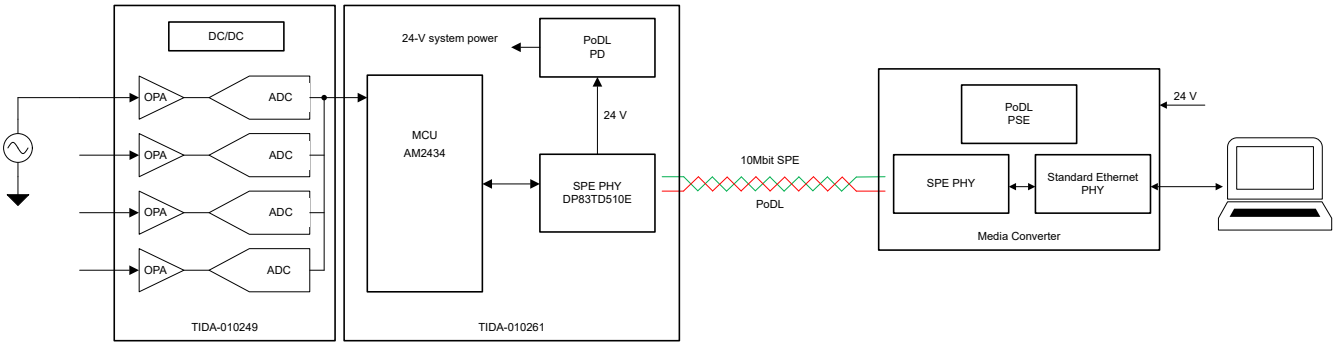


Figure 4-2. Test Setup

4.4 Test Results

The messages sent to the MQTT broker can be received by any machine allowed to connect to the broker and subscribe to the message. Using Linux on the machine running the broker is done with mosquitto_sub -h 127.0.0.1 -v -t 'adc1raw' . This command shows all raw samples of the first ADC channel, as this is transmitted as topic adc1raw. The output on command line is shown in Figure 4-3.

```
adc1raw { "ADC 1 Raw Data: ": [ 138656, 152891, 165682, 176798, 186080, 193470, 198931, 202392, 203830, 203191, 200434, 195719
, 189070, 180434, 170011, 157848, 144021, 128848, 112369, 94677, 76051, 56679, 36794, 16518, -3952, -24299, -44380, -64108, -8
3267, -101530, -118694, -134665, -149267, -162328, -173809, -183550, -191374, -197271, -201152, -203006, -202875, -200660, -19
6377, -190168, -182027, -171974, -160251, -146938, -132104, -115968, -98644, -80311, -61164, -41374, -21190, -823, 19562, 3982
3, 59691, 78883, 97280, 114701, 130952, 145935, 159400, 171273, 181491, 189858, 196303, 200678, 203108, 203474, 201768, 198114
, 192355, 184682, 175166, 163860, 150887, 136403, 120550, 103509, 85396, 66386, 46820, 26726, 6384, -14012, -34305, -54213, -7
3651, -92295, -109958, -126529, -141836, -155682, -167951, -178537, -187299, -194277, -199196, -202077, -203015, -201858, -198
649, -193370, -186242, -177246, -166368, -153829, -139741, -124263, -107457, -89627, -70912, -51420, -31458, -11126, 9326, 297
13, 49790, 69319, 88145, 106088, 122998, 138644, 152944, 165632, 176618, 185863, 193264, 198764, 202099, 203518, 202916, 20011
1, 195395, 188638, 180031, 169645, 157478, 143828, 128686, 112196, 94633, 76148, 56857, 36947, 16707, -3670, -23994, -44090, -
63860, -82953, -101131, -118293, -134214, -148826, -161978, -173432, -183160, -191031, -196904, -200872, -202827, -202678, -20
0479, -196279, -190166, -182073, -172128, -160495, -147138, -132289, -116117, -98779, -80495, -61326, -41582, -21458, -1067, 1
9364, 39636, 59487, 78713, 97158, 114620, 130840, 145781, 159249, 171117, 181364, 189681, 196076, 200537, 202974, 203355, 2016
56, 197947, 192210, 184577, 175093, 163810, 150866, 136437, 120721, 103705, 85632, 66702, 47062, 27036, 6775, -13611, -33918,
-53896, -73350, -92010, -109700, -126305, -141651, -155595, -167932, -178574, -187416, -194309, -199252, -202215, -203152, -20
1979, -198744, -193560, -186375, -177344, -166500, -153924, -139862, -124384, -107629, -89808, -71066, -51617, -31676, -11347,
 9115, 29447, 49464, 69065, 87929, 105827, 122744, 138401, 152679, 165433, 176484, 185771, 193217 ] }
```

Figure 4-3. MQTT Message on Command Line

A improved view can be achieved by using Node-RED as shown in Figure 4-4 by creating a flow to display the samples. Also this can be used to visualize the results of the FFT, transmitted in the adc1fft topic.

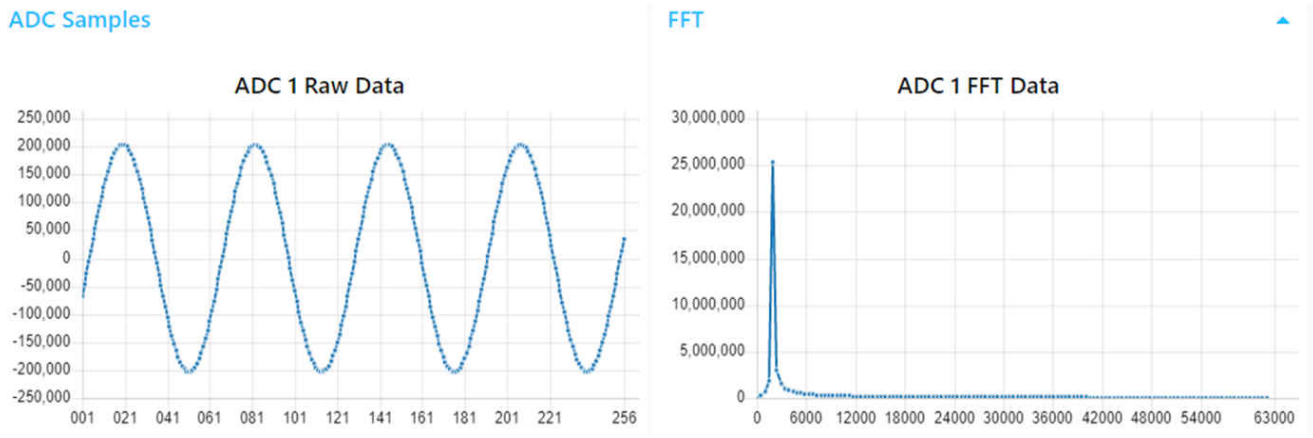


Figure 4-4. MQTT Messages in Node-RED

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010261.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010261.

5.2 Tools and Software

Tools

TIDA-010249	Four-channel synchronous vibration sensor interface reference design

Software

MCU-PLUS-SDK-AM243X	AM243x software development kit (SDK) for Sitara™ microcontrollers

5.3 Documentation Support

1. Texas Instruments, *DP83TD510E Ultra-Low-Power 802.3cg 10BASE-T1L 10M Single Pair Ethernet PHY Data Sheet*
2. Texas Instruments, *AM243x Sitara™ Microcontrollers Data Sheet*
3. Texas Instruments, *TPS2660x 60-V, 2-A Industrial eFuse With Integrated Reverse Input Polarity Protection Data Sheet*
4. Texas Instruments, *TPS798xx-Q1 50 mA, 3 V to 50 V, Micropower, Low-Dropout Linear Regulator Data Sheet*
5. Texas Instruments, *MSP430FR247x Mixed-Signal Microcontrollers Data Sheet*
6. Texas Instruments, *TLV703x and TLV704x Small-Size, Nanopower, Low-Voltage Comparators Data Sheet*
7. Texas Instruments, *ATL431, ATL432 2.5-V Low I_Q Adjustable Precision Shunt Regulator Data Sheet*
8. Texas Instruments, *LM74700-Q1 Low I_Q Reverse Battery Protection Ideal Diode Controller Data Sheet*
9. Texas Instruments, *TPS6282x 2.4-V to 5.5-V Input, 1-, 2-, 3-, 4-A Step-down Converter with 1% Output Accuracy Data Sheet*
10. Texas Instruments, *TPS61023 3.7-A Boost Converter with 0.5-V Ultra-low Input Voltage Data Sheet*
11. Texas Instruments, *TLVM13630 High-Density, 3-V to 36-V Input, 1-V to 6-V Output, 3-A Power Module With Enhanced HotRod™ QFN Package Data Sheet*
12. Texas Instruments, *LSF0108 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Applications Data Sheet*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

STEFFEN GRAF is a systems engineer at Texas Instruments, where he is responsible for developing reference designs in the industrial segment. Steffen has an extensive experience in single-pair Ethernet, Power over Data Lines, as well as IO-Link. He earned his master of science degree in electrical engineering at the University of applied science in Darmstadt, Germany.

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