*Design Guide: TIDA-010255*

# *High-Efficiency, 230-$V_{AC}$, 2-kW, 3-phase GaN Inverter Reference Design for Servo Drives and Robotics*

## Description

This reference design demonstrates a high-efficiency, 320-$V_{DC}$ input 3-phase power stage using six fast switching GaN-FETs with integrated driver, protection and temperature reporting with hot-side MCU control especially for motor-integrated servo drives and robotics applications. Accurate phase-current sensing is achieved with isolated delta-sigma modulators, the DC-link voltage is measured with a non-isolated small form-factor delta-sigma modulator and an analog phase voltage feedback option allows validation of advanced sensorless designs like InstaSPIN-FOC™. For easy evaluation, the design offers a 3.3-V I/O interface signal with a 180-pin connector for C2000™ MCU controlCARDs, as well as a standard header to connect to other MCUs like the Sitara™ AM2631.

## Resources

| | |
|---|---|
| TIDA-010255 | Design Folder |
| LMG3422R030, AMC1306M05, AMC1035 | Product Folder |
| ISO7741, ISO7730 | Product Folder |
| TPSM560R6H, TPSM82903 | Product Folder |
| F28379D C2000™ MCU controlCARD™ | Tools Folder |

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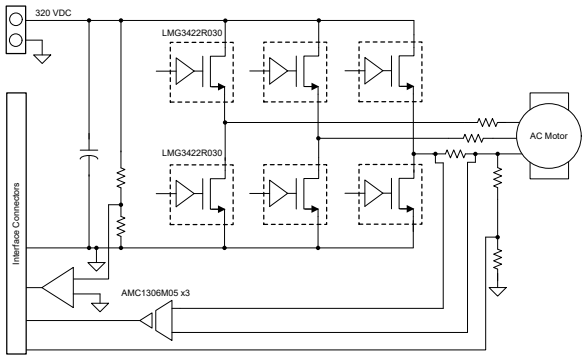
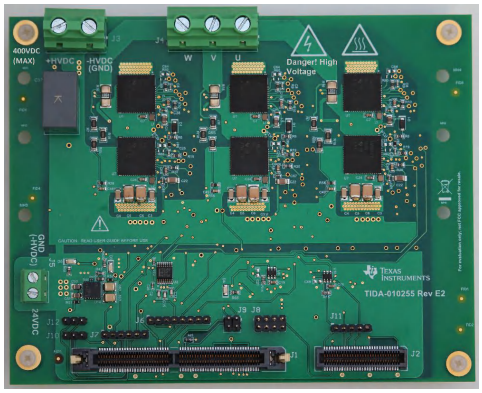
## Features

- High-efficiency, 3-phase GaN-FET power stage with 99.4% peak efficiency at 16-kHz PWM at 320-V DC-link voltage helps reduce the heat sink size
- LMG3422R030 600-V, 30-mΩ GaN FETs with integrated driver, overcurrent and overtemperature protection, and temperature reporting
- LMG3422R030 integrated protection increases reliability and reduces system cost, on-chip temperature sensor enables precise monitoring of the die temperature to maximize safe operation area (SOA)
- Zero reverse recovery losses reduce switch node oscillations, and fast switching capability dV/dt (30 V/ns, configurable from 20 V/ns to 100 V/ns) with low dead time of 120-ns minimize phase voltage distortions
- Precision phase current sensing with ±50-A linear range using 1-mΩ shunt and isolated delta-sigma modulator AMC1306M05
- Interface with 3.3 V I/O enables easy evaluation of TI GaN technology for motor drives with C2000, Sitara, or other MCUs

## Applications

- Single and multiaxis servo drives
- Industrial and collaborative robot



# 1 System Description

AC input 3-phase inverters with high energy efficiency up to IEC 61800-9 energy class IES2 not only help reduce the global energy footprint, but also enable smaller form factor and higher power density designs with reduced heat sink size. Form factor and weight play an important role, especially with motor-integrated servo drives used in industrial robot and factory automation applications where the motors are part of a mechanical moving system, such as a 6-axis robot.

Motor integrated 3-phase inverters are often supplied from single-phase 200- to 230-$V_{AC}$ input, equivalent to a rectified 320 $V_{DC}$. Input power levels are typically less than 3 kW. Today the vast majority of 230-$V_{AC}$-input servo drives leverage IGBT-based power switches with PWM switching frequencies from 8 kHz to 16 kHz. Due to the power losses of the insulated-gate bipolar transistors (IGBTs), the size of the heat sink can be more than 30% of the overall 3-phase inverter size.

Gallium nitride (GaN) power transistors help reduce power losses versus IGBTs significantly, even at low pulse-width modulation (PWM) switching frequencies of 8 kHz to 16 kHz. GaN-FETs with integrated drivers, such as the LMG3422R030, reduce both switching and conduction losses and can achieve 99.4% peak efficiency at 16-kHz PWM. This reduces the overall power losses by more than a factor of 4 compared to traditional IGBT-based 3-phase inverters, as shown in this reference design at 7-$A_{RMS}$ output phase current.

The TIDA-010255 reference design realizes a high-efficiency, hot-side MCU controlled 320 $V_{DC}$, 2-kW, 3-phase, power stage, using six fast switching LMG3422R030 600-V, 30-mΩ GaN-FETs. The LMG3422R030 includes an integrated driver, protection, and temperature reporting and helps increase reliability while reduce the system cost for external protection and temperature monitoring circuits. Buck modules with integrated inductors and bootstrap supplies reduce the footprint for power management and gate drive bias supply. Accurate and high linearity phase current sensing is achieved using 1-mΩ in-phase current shunts with a ±50-mV input, reinforced isolated modulator AMC1306M05. Due to the hot-side control, where the MCU ground (GND) is equal to power GND (DC–), isolation is not required to sense the DC-link voltage and the three phase voltages. A non-isolated AMC1035 delta-sigma modulator measures the DC-link voltage. A non-isolated analog phase voltage feedback option enables advanced sensorless designs like InstaSPIN-FOC using a C2000 MCU with 12-bit integrated ADCs.

For evaluation of TI's GaN technology with industrial drives, the design offers 3.3-V I/O interface signals with either a 180-pin HSEC connector for use with C2000 MCU controlCARDs, such as the F28379D controlCARD, or standard headers to connect to other MCUs like the Sitara AM2631 or AM2431.

The design was tested without a heat sink at room temperature with a DC-link voltage of 320 $V_{DC}$ and 16-kHz PWM up to 7.7-$A_{RMS}$ continuous 3-phase output current. For testing at higher currents or testing at higher ambient temperature a heat sink can be mounted at the bottom side of the PCB. Mounting holes are provided on the PCB.

## 1.1 Key System Specifications

| SUBSECTION | PARAMETER | SPECIFICATION |
|---|---|---|
| Input supply | DC-bus voltage | 320 V (TYP), 400 V (MAX) |
| | Control supply voltage | 24 V ±20% (TYP), 60 V (MAX) |
| Power switch | GaN-FET | LMG3422R030, bottom-side cooling |
| | Slew rate | 30 V/ns (TYP), configurable, 100 V/ns (MAX) with this design. |
| | Overcurrent and overtemperature protection | LMG3422R030 integrated |
| | Fault reporting | Overcurrent, overtemperature, and UVLO fault feedback |
| | Temperature sensing (phase V) | Encoded: 9-kHz PWM at 3.3 V |
| | 3-phase complementary PWM | 8 kHz – 16 kHz (TYP), and higher, see section 3. |
| | PWM dead time | 150 ns (MCU), results effective 120 ns (TYP), can be lower, see Section 3. |
| | 3-phase output current (no heat sink) | 7.7 $A_{RMS}$ (TYP) at 27°C ambient, no heat sink |
| | Heat sink | None, but provision to add |
| Phase current sense | Shunt | 1-mΩ shunt, 3 W |
| | Isolated modulator | ±50 mV (linear input voltage range) |
| | Measurement range | ±50 A (linear range) |
| DC bus voltage sense | Measurement range | 0 V to 480 V (linear range), configurable |
| Phase voltage sense | Measurement range | 0 V to 480 V, configurable |
| Isolation | None | MCU connected to DC–, hot side control |
| MCU interface | C2000 controlCARD | 180-pin HECC (5V supply and 3.3 V I/O) |
| | MCU | 100-mil standard headers (3.3 V I/O) |
| PCB | Layer stack | 6 layers, 70-µm copper |
| | Clearance distances | 1. 6 mm (top and bottom layer), 0.6 mm (inner layers) |
| | PCB size | 148 mm × 116 mm (5826 mil × 4566 mil ) |

# 2 System Overview

## 2.1 Block Diagram

Figure 2-1 shows the system block diagram of the TIDA-010255 320-$V_{DC}$ input, high-efficiency, hot-side MCU controlled 3-phase power stage using six fast switching GaN FETs with integrated driver, protection and temperature reporting. Buck converter modules with integrated inductors and bootstrap supplies reduce the PCB size for power management and gate-drive bias supply. Accurate, shunt-based phase current sensing is achieved with the isolated delta-sigma modulator AMC1306M05. The DC-link voltage is sensed with a non-isolated AMC1035 delta-sigma modulator and an analog feedback option is provided for the three phase voltages. A dual-connector option with 3.3-V I/O allows connection to a C2000™ MCU controlCARD or to other MCUs, such as the Sitara™ AM2631.

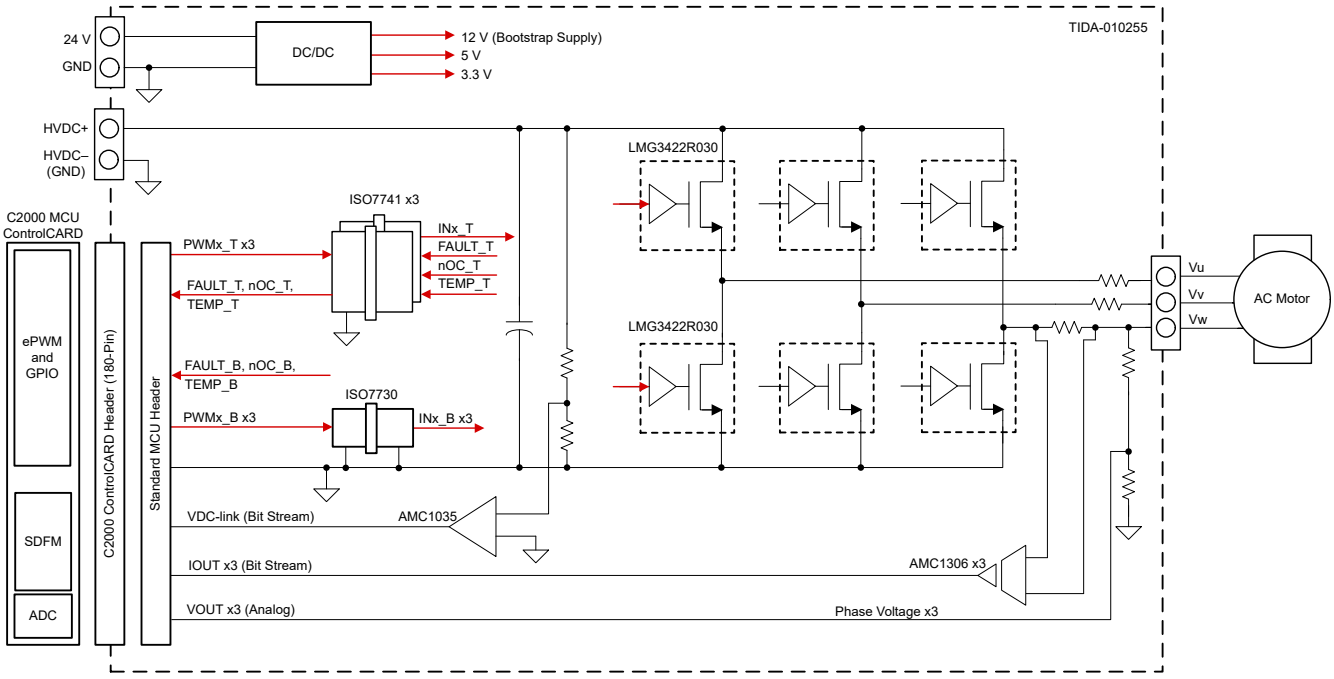



**Figure 2-1. TIDA-010255 Block Diagram**

## 2.2 Highlighted Products

The TIDA-010255 reference design features the following key devices from Texas Instruments.

### 2.2.1 LMG3422R030

The LMG342xR030 GaN FET with integrated driver and protection enables designers to achieve new levels of power density and efficiency in power electronics systems. The following key features help significantly increase power efficiency and improve system robustness for motor-integrated drive applications:

- 600-V 30-mΩ GaN FET with integrated gate driver, fast switching and zero reverse recovery charge significantly reduce power losses versus IGBTs
- Configurable 20-V/ns to 150-V/ns slew rate for optimization of switching performance and EMI mitigation
- Advanced power management features and robust protection, such as cycle-by-cycle overcurrent and latched short circuit protection with less than 100-ns response, self-protection from internal overtemperature and UVLO monitoring and reporting
- Real-time and accurate digital temperature PWM output helps managing the LMG3422R030 junction temperature to optimize the safe operating area (SOA)
- Integrated 5-V low dropout (LDO) to supply digital isolators or current sensors helps reduce BOM and footprint
- Qualified for JEDEC JEP180 for hard-switching topologies
- Operating junction temperature absolute maximum ratings: –40°C to 150°C

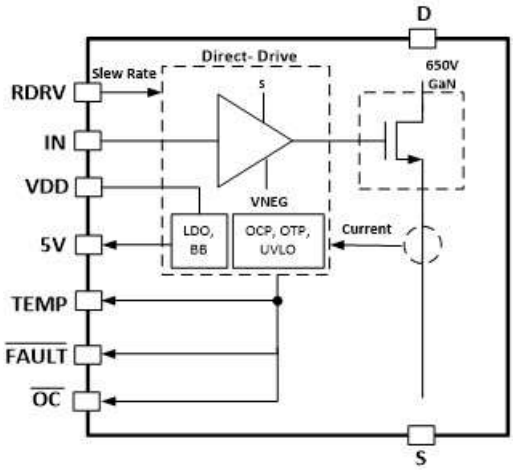



**Figure 2-2. LMG3422R030 Block Diagram**

### 2.2.2 ISO7741

The ISO7741 is a high-performance, quad-channel digital isolator with 3000 $V_{RMS}$ (DBQ package) isolation ratings per UL 1577.

Three ISO7741 devices implement the level shifting of the signal between the MCU and the top-side LMG3422R030 GaN-FETs. The ISO7730, from the same family of digital isolators, provide a tight propagation match between bottom-side and top-side signal chain and also translate the 3V3 CMOS signals from the MCU to 5-V CMOS signals with the LMG4322R030 GaN-FETs. The key features of the ISO7741 are:

- Default output low (F-version) helps drive PWM low, if the input power or signal is lost
- Low propagation delay: 10.7 ns typical (5-V supplies) provide tight propagation matching between the top and bottom PWM signals
- Maximum-rated isolation working voltage 566 VDC and high common mode transient immunity (CMTI) of 100 kV/µs (TYP) to operate with 230 $V_{AC}$ hot-side controlled power systems, where the logic GND is referred to the negative DC-bus voltage
- Quad (ISO7741F) or triple channel (ISO7730F) digital isolation reduce footprint
- Wide ambient temperature range: –55°C to 125°C

### 2.2.3 AMC1306M05

The AMC1306M05 is a small, high-precision, reinforced isolated delta-sigma modulator for shunt-based precision phase current sensing. The key features for this design are:

- ±50-mV differential input voltage range allows use of a smaller shunt and reduce power losses by 80% versus modulators with ±250-mV input voltage range
- Very low offset ±50 µV and offset drift 1 µV/°C (max) and high SNR 82.5 dB (TYP) eliminates the need for offset calibration and enable excellent DC and AC performance
- High common mode transient immunity (CMTI), 100 kV/µs (TYP), to operate at the higher slew rate of GaN-FETs. The AMC1306M05-Q1 version supports a CMTI of 100 kV/µs (MIN).
- Maximum-rated isolation working voltage 2121 $V_{DC}$ to operate in hot-side controlled power systems, where the logic GND is referred to the negative supply rail
- Extended industrial temperature range: –40°C to +125°C

### 2.2.4 AMC1035

The AMC1035 is a non-isolated delta-sigma modulator optimized for accurate voltage and temperature sensing with hot side MCU controlled 3-phase power stages. The key features of the AMC1035 are:

- ±1-V input voltage range with high differential input resistance: 1.6 GΩ (TYP) to directly interface to high-impedance resistor dividers for voltage sensing
- Very low offset ±0.5 mV and offset drift 6 µV/°C (MAX) and high SNR 87 dB (TYP) enable excellent DC and AC performance
- Small form factor 8-pin SOIC (4.9 mm × 3.9 mm)
- Fully specified over the extended industrial temperature range: –40°C to +125°C to work at the high ambient temperatures with motor integrated inverters

### 2.2.5 TPSM560R6H

The TPSM560R6H power module is a highly integrated 600-mA power design that combines a 60-V input, step-down DC/DC converter with power MOSFETs, a shielded inductor, and passives in a thermally-enhanced QFN package:

- Wide input voltage range up to 60 V, transient protection up to 66 V
- Small footprint QFN package (5.0 mm × 5.5 mm × 4.0 mm) with integrated shielded inductor
- Excellent thermal performance up to 9.6-W output power at 85°C, no airflow
- Operating junction temperature range: –40°C to +125°C

### 2.2.6 TPSM82903

The TPSM82903 is a 3-A, 3-V to 17-V, highly efficient, small, and flexible synchronous step-down DC/DC converter MicroSiP™ package module that is easy to use:

- Small package 3 mm × 2.8 mm with integrated inductor
- Configurable output voltage options: 0.6 V to 5.5 V
- ±0.9% feedback voltage accuracy across temperature (–40°C to 125°C)

For more information on each of the devices, see their respective product folders at www.ti.com or click on the links for the product folders in the *Resources* section of this reference design.

# 3 System Design Theory

## 3.1 Power Switches

The hot-side controlled 3-phase power stage utilizes six LMG3422R030 600-V 30-mΩ GaN FETs with integrated gate driver, fast switching and zero reverse recovery charge, which significantly reduces power losses versus IGBTs for use in 320-$V_{DC}$ input motor integrated drives.

### 3.1.1 GaN-FET Selection Criterion

The LMG3422R030 was selected due to bottom-side cooling and a very low $R_{DS(on)}$ of 30-mΩ to minimize power losses at already low PWM switching frequencies between 8 kHz to 16 kHz. The device also achieves a maximum continuous output current of at least 7.7 $A_{RMS}$ without heat sink at ambient room temperatures as typically present in test labs.

A comparison of the estimated 3-phase inverter power switch losses (LMG3422R030 at 25°C $T_j$) with 320-V DC-link voltage and 16-kHz PWM versus the output phase current is shown in Figure 3-1. For applications which require less than around 6.5 $A_{RMS}$ continuous output current, the LMG3422R050 offers lower power losses despite a higher $R_{DS(on)}$, since the device offers a lower output charge $Q_{OSS(tr)}$.

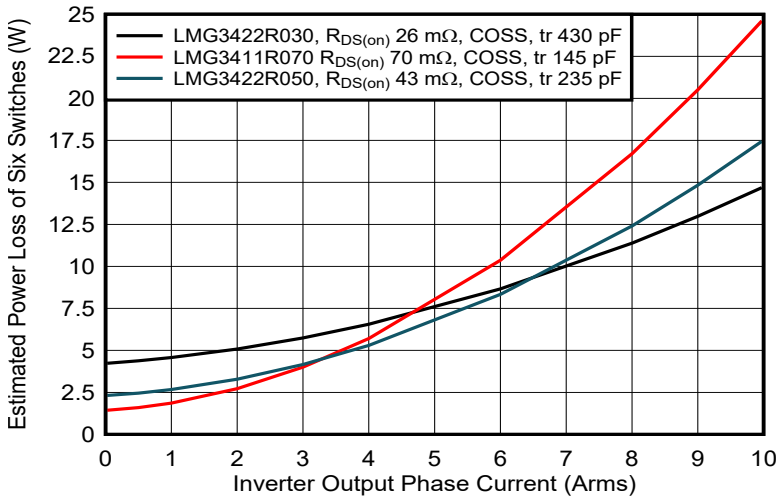



**Figure 3-1. Estimated Power Switch Losses of a 320 $V_{DC}$-fed 3-Phase Inverter at 16-kHz PWM**

### 3.1.2 HVBUS Decoupling and 12-V Bootstrap Supply

Although the LMG3422R030 GaN-FETs are rated for 600-V, this design is rated for 400 $V_{DC}$ (MAX). The PCB clearance between traces or polygons on each copper layer with voltages higher than 60 $V_{DC}$ or 25 $V_{AC}$ between each other is minimum 0.8 mm for inner layers and 1.6 mm for the top and bottom layers.

The design uses a multichannel schematic with the same components for each of the three half-bridges. To distinguish between the phase _U, _V, or _W are appended to the component designators. In the following description the phase designator is not shown, for example instead of R20_U, R20_V, and R20_W, just R20 is used.

Figure 3-2 shows the schematic of a half-bridge phase V with two 600-V rated LMG3422R030 devices. Each half-bridge has four parallel decoupling capacitors across HVBUS and GND, 2-times 10 nF and 2-times 100 nF, rated 1 kV.

A 12-$V_{DC}$ non-isolated rail supplies the three bottom-side LMG3422R030 devices. A bootstrap configuration using a high-voltage diode D1, a 3.3-Ω current limit resistor R6, and a 10-uF bulk capacitor C1 provide a floating 12-V supply for the each of the three top-side LMG34022R030 devices. A 16-V Zener diode in parallel to the C1 bulk capacitor makes sure the supply voltage of the LMG3422R030 remains below the VDD maximum recommended voltage of 18 V. This is required since during third quadrant operation the switch node voltage is lower than GND and the bootstrap capacitor can be charged up to sum of the 12-V supply rail and the third quadrant source-to-drain voltage $V_{SD}$, which is typically 5 V at 20-A source current. Due to the large C1 bulk capacitor of 10-uF and the 3.3-Ω current limit resistor R6, the bottom-side GaN-FETs need to be turned on

long enough after power up to make sure the C1 bulk capacitor is charged close to 12 V, before the top-side GaN-FETs are turned on.

For the LMG3422R030 integrated buck-boost converter, a 4.7-µH inductor is placed from the LMG3422R030 BBSW pin to the switch node floating ground (top-side GaN-FET) and GND (bottom side GaN-FET), respectively. A 2.2-µF capacitor bypasses the internal buck-boost converter negative output (VNEG), which is used to turn off the depletion mode GaN-FET.

### 3.1.3 GaN_FET Turn-on Slew Rate Configuration

The LMG3422R030 allows adjustment of the drive strength of the device to obtain a desired slew rate, which provides flexibility when optimizing switching losses and noise coupling. Generally, high slew rates provide lower switching losses, but high slew rates can also create higher voltage overshoot, noise coupling, and EMI emissions. In this design the turn-on slew rate is configured to 30 V/ns through a 200-kΩ resistor (R9 for top-side and R19 for the bottom side GaN-FETs). A 100-pF capacitor (C8 for top-side and C25 for bottom side GaN-FETs) is placed in parallel for transient noise rejection. The turn-on slew rate can be adjusted by changing R9 for the top-side and R19 for the bottom side LMG3422R030 respectively, as described in the LMG3422R030 (*LMG342xR030 600-V 30-mΩ GaN FET With Integrated Driver, Protection, and Temperature Reporting*) data sheet. The maximum configured slew rate in this design is not to exceed 100 V/ns, so as to not exceed the typical specified common mode transient immunity (CMTI) of the isolated modulator AMC1306M05 and digital isolator ISO7741.

### 3.1.4 PWM Input Filter and Dead-Time Calculation

An input low-pass filter at the LMG3422R030 IN pin is recommend to help improve immunity against transient switching noise. This design uses a 3-MHz input low-pass filter with R10 (100 Ω) and C10 (560 pF) for the top side and R20 and C48 for the bottom side. To achieve good propagation delay match, capacitors with 5% tolerance or better are recommended. The time constant and especially the capacitance is higher than the LMG3422R030 data sheet recommended 100 Ω and 22 pF to further increase the transient noise immunity of the system at very high switching currents. Make adjustments during testing according to the needs of the system.

The effective propagation delay in this design for turn-on and turn-off is a function of the 1.9 V (TYP) positive-going input threshold voltage of the LMG3422R030 and the negative-going input threshold voltage of 1 V (TYP). Equation 1 and Equation 2 show the effective signal delay assuming a 5-V CMOS logic PWM signal.

$$t_{D\_IN(ON)} = -\ln\left(1 - \frac{V_{IN,IT+}}{5\ V}\right) \times C10 \times R10 = 27\ ns \quad (1)$$

$$t_{D\_IN(OFF)} = -\ln\left(\frac{V_{IN,IT-}}{5V}\right) \times C10 \times R10 = 90\ ns \quad (2)$$

In addition to the PWM signal delay through the input filter per Equation 1 and Equation 2, the LMG3422R030 has a turn-on and turn-off delay, which depends on the configured slew rate. With a 30 V/ns slew rate configuration the LMG3422R030 typical turn-on delay is around 75 ns, while the turn-off delay is around 44 ns. Hence, the effective PWM signal to switch node voltage delay is around 102 ns for turn-on and around 134 ns for turn off. Since the effective turn-on delay is 32 ns shorter than the turn-off delay, this has to be considered when configuring complementary PWM dead-time generated by the PWM module of the MCU.

In this design the TMS320F28379D MCU was configured to generate a 150 ns PWM dead-time, which yields an effective typical dead-time of around 120 ns (118 ns). This provides enough margin to handle variations in the overall effective turn-on and turn-off delay.

A smaller PWM filter time-constant of 10 ns with C10 (100 pF) and C48 (100 pF) is possible, but was not tested with this design. The smaller PWM filter with 10-ns time constant reduces the propagation delay $t_{D\_IN(ON)}$ to around 4.7 ns and $t_{D\_IN(OFF)}$ to around 16 ns and allows further reduction of the effective dead time.

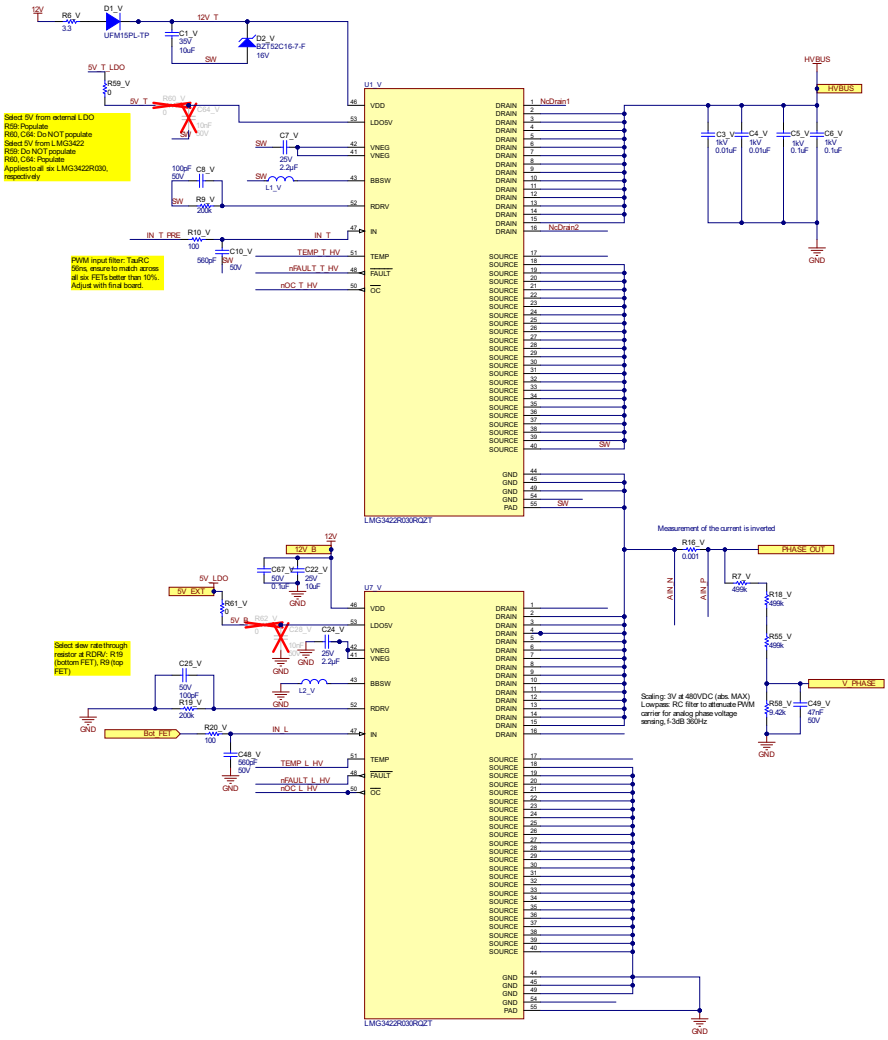



**Figure 3-2. Schematic of Half-Bridge Phase V With LMG3422R030 on Top and Bottom**

### 3.1.5 Signal Level Shifting

GaN-FETs switch faster than IGBTs and the dV/dt slew rate can be 30 V/ns or even higher, as configured in this design. Therefore digital isolators with high common-mode transient immunity (CMTI) of 100 V/ns (TYP) like the ISO7741F quad-channel digital isolator. The suffix F with the ISO7741F help drive the outputs of the device low, if the input power or signal are lost. The ISO7741F has one forward channel for the PWM signal and three channels in the opposite direction for the three fault and temperature reporting signals of the corresponding top-side GaN-FET. The device level shifts the 3.3-V I/O signals to 5-V I/O signals to the corresponding top-side GaN-FETs which refer to the floating switch node GND (SW), as shown in Figure 3-3.

The design has two options to provide the 5-V supply for the top-side digital isolator U4 (ISO7741F) at VCC1, as shown in Figure 3-3. When the external 5-V LDO (U13) is used (default configuration with this design), the resistor R60 and capacitor C64 need to be unpopulated, and R59 needs to be populated. If the 5 V is supplied through the internal 5-V LDO of the LMG3422R030 at pin LDO5V, R59 needs to be unpopulated and R60 and C64 need to be populated.

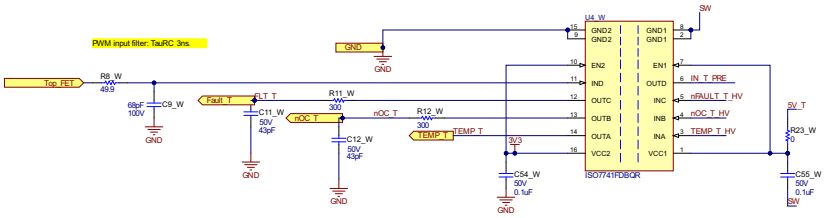



**Figure 3-3. Schematic of Digital Isolator-Based Level Shifter for Top-Side GaN-FETs**

The ISO7730F triple-channel digital isolator is from the same family that the ISO7741F is and provides a tight propagation match between bottom-side and top-side PWM signals, while translating the 3.3-V CMOS signals from the MCU to 5-V CMOS signals with the LMG4322R030 bottom side GaN-FETs, as shown in Figure 3-4.

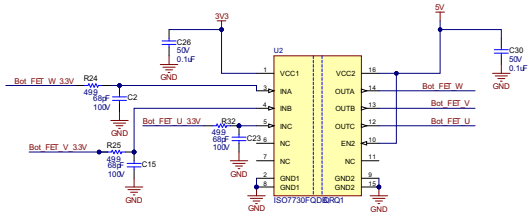



**Figure 3-4. Schematic of Digital Isolator-Based Level Shifter for Bottom-Side GaN-FETs**

### 3.1.6 LMG3422R030 Fault Reporting

The LMG3422R030 GaN-FETs integrate overcurrent protection (OCP), short-circuit protection (SCP), overtemperature protection (OTP), and undervoltage lockout (UVLO). For details see the *LMG3422R030* data sheet. The individual $\overline{\text{FAULT}}$ and the $\overline{\text{OC}}$ feedback signals of each of the three top-side GaN FETs are level shifted to 3.3 V through the ISO7741 quad-channel digital isolator. Each fault signal is low-pass filtered to attenuate high-frequency transient noise with a 300 Ω and 47-pF RC low-pass filter and logically combined using triple input AND gates for the three bottom-side and three top-side Gan-FETs, as shown in Figure 3-5. Hence the MCU can monitor fault and overcurrent events with the top-side or bottom-side GaN-FETs, respectively. The signals nOC_T, nOC_L, GaN_FAULT_L, and GaN_FAULT_T are routed to the C2000 controlCARD connector J2 and the MCU header J11.

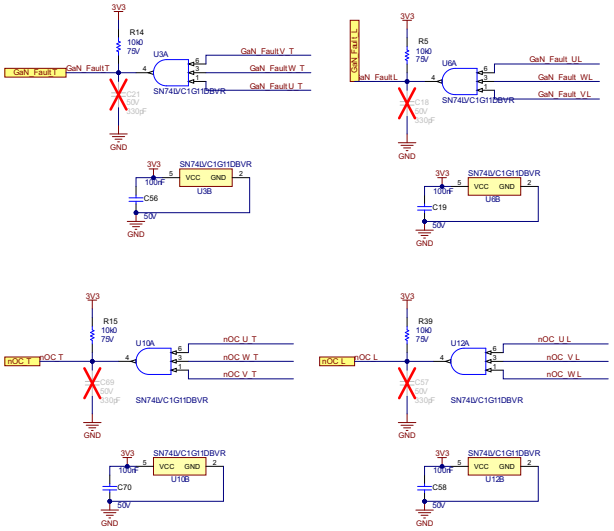



**Figure 3-5. GaN-FET Fault and Overcurrent Reporting Schematic**

### 3.1.7 LMG3422R030 Temperature Monitoring

The TEMP pin of each LMG3422R030 is a push-pull digital output that gives information about the GaN FET junction temperature. The LMG342R030 TEMP pin outputs a fixed 9-kHz pulsed waveform. The device junction

temperature is encoded as the duty cycle of the PWM waveform. The PWM duty cycle is around 3% at a temperature of 25°C and 82% at a temperature of 150°C. For temperatures above 150°C, the duty cycle continues to increase linearly until overtemperature fault occurs. When an overtemperature fault occurs, the TEMP pin is pulled high to indicate this fault. There is a hysteresis to clear overtemperature fault.

The TEMP signals are level shifted from 5 V to 3.3 V for each of the six LMG3422R030 devices, as shown in Section 3.1.4. In this design, only the PWM temperature signals of the phase V half-bridge TOP_TEMP_V and BOT_TEMP_V are available to the MCU. A 1.5-kHz low-pass filter with R13 (R33) and C20 (C47) attenuates the 9-kHz PWM carrier before the two signals are routed to the C2000 controlCARD connector J1 and the MCU header J7. For more precise *temperature sensing*, offset and gain calibration as well as over-sampling through an ADC integrated on the MCU are recommended. Equation 3 shows a simplified transfer function to calculate the LMG3422R030 junction temperature form the low-pass filtered TEMP PWM signal, assuming a 3.3-V supply voltage.

$$\mathrm{Tj}_{\mathrm{LMG3422}}[^{\circ}\mathrm{C}] = \frac{(\mathrm{TOP\_TEMP\_V}[\mathrm{V}] - 0.099[\mathrm{V}])}{2.607[\mathrm{V}]} \times 125[^{\circ}\mathrm{C}] + 25[^{\circ}\mathrm{C}] \quad (3)$$

## 3.2 Phase Current Sensing

The 3-phase inverter output phase current is measured using a 1-mΩ shunt and an AMC1306M05 high-precision, reinforced isolated delta-sigma modulator with a ±50-mV linear input voltage range. This allows use of a smaller shunt and reduces the shunt losses by 80% compared to a 5-mΩ shunt as required for modulators with ±250-mV input voltage range. In this design, the AMC1306M05 provides a maximum input range of ±64 A and a linear input voltage range of ±50 A. Figure 3-6 shows the AMC1306M05 schematic.

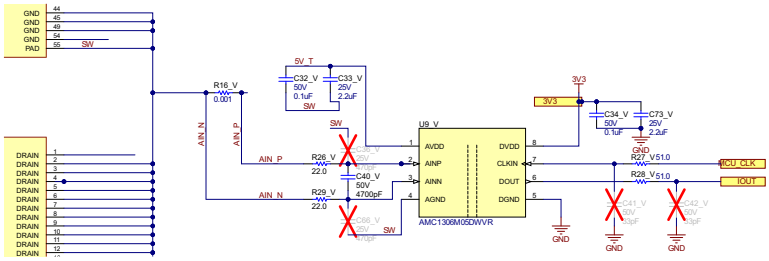



**Figure 3-6. Schematic of Phase V Current Sensing With Shunt and AMC1306M05 Isolated Modulator**

### 3.2.1 Shunt

The power losses of the 1-mΩ shunt at nominal maximum output current of 7.7 $A_{RMS}$ without heat sink are 60 mW with a capability to handle 40 $A_{RMS}$ (transient) at 1.6-W losses in the case where a heat sink is mounted with that design. The package and power rating of the shunt R16 were chosen for 3 W to also have an option to be replaced with higher resistance shunts, such as 5 mΩ to evaluate the AMC1306M25 with ±250-mV linear input voltage range and test the system at higher load current with a heat sink for the bottom-side cooled GaN-FETs.

In the layout, use a Kelvin connection from the shunt to the differential input filter R26, R29, C40 and route the signal AIN_N and AIN_P differentially. Connect the AMC1306 AGND to the shunt terminal which is connected to the top-side source (SW) of the GaN-FET. For easier routing in this design, AIN_N has the same potential as switch node (SW) and the phase current measures the inverted motor phase current.

### 3.2.2 AMC1306M05 Analog Input-Filter

To avoid aliasing, attenuate noise above half of the sampling frequency of the isolated modulator, depending on the oversampling ratio of the sinc$^3$ decimation filter. Although the AMC1306M05 integrated amplifier has a bandwidth of 800 kHz and a high common-mode rejection ratio, an external anti-aliasing low-pass filter and optional common mode input filter capacitors are added for systems with either lower than 20-MHz modulator clock frequency or systems with higher frequency system noise. The cutoff frequency of the differential input filter R26, R29, and C40 is set for 770 kHz, and can be adjusted to the transient noise spectrum of the 3-phase inverter PCB. This input filter provides additional input signal attenuation of around 22 dB at 10 MHz, when a modulator clock of 20 MHz is used.

As a general guideline, the common mode capacitor C36 and C66 are chosen to be 10- to 20-times smaller than the differential filter capacitor. In this design 470 pF was chosen, which gives a cut-off frequency of 15-MHz. A mismatch of the two common mode capacitors 336 and C66 changes the corresponding low-pass filter cut-off frequency and hence can convert common mode noise around and above the cut-off frequency into residual differential noise. Capacitors with tolerance of 5% or better are chosen to make sure any residual differential noise is attenuated respectively by the lower cutoff frequency of the 770-kHz differential low-pass filter.

### 3.2.3 AMC1306M05 Digital Interface

The digital interface is simple with just a modulator clock input and a bit-stream data output. R28 is a 51-Ω serial termination resistor. The capacitor C42 is optional for slew rate reduction with lower radiated emissions (EMI), if required. The radio frequency (RF) filter R27 and C41 with a cutoff frequency of 95-MHz is optional to attenuate high-frequency RF noise on the clock signal, if present in the system.

A single modulator clock signal MCU_CLK_I needs to be provided by the MCU for the three current sensing modulators. Figure 3-7 shows that the corresponding clock buffer outputs have 51-Ω series termination and are routed in star topology with similar length to each of the three AMC1306M05 modulators. The AMC1306M05 supports modulator clocks from 5 MHz to 21 MHz.

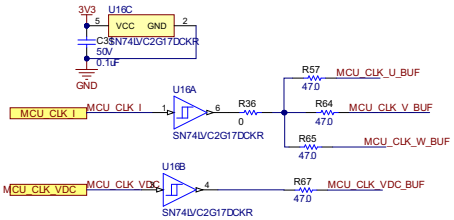



**Figure 3-7. Clock Buffer Circuit Schematic**

### 3.2.4 AMC1306M05 Supply

The AVDD analog supply is powered from the +5V_T bootstrap supply referenced to the switch node SW and decoupled with two parallel capacitors C32 (100 nF) and C33 (2.2 µF). The DVDD digital supply is powered by 3.3 V and decoupled with 100 nF and 2.2 µF too.

## 3.3 DC-Link (HV_BUS) Voltage Sensing

The TIDA-010255 is designed to operate at a nominal DC-link voltage of 320 $V_{DC}$ and a maximum DC-link voltage up to 400 $V_{DC}$, corresponding to a single-phase 200-$V_{AC}$ to 250-$V_{AC}$ input. Accurate sensing of the DC-link voltage is important to calculate the corresponding duty cycle of the three-phase PWM, monitor for overvoltage and undervoltage, and estimate the amplitude of phase voltages.

Due to the hot-side control architecture, the DC-link voltage can be sensed through a non-isolated delta-sigma modulator AMC1035 with a corresponding high-voltage resistor divider. The AMC1035 has a maximum bipolar input voltage range of ±1.25 V and a linear input voltage range of ±1 V. The high-impedance resistor dividers R1, R2, R3, and R4 are scaled to provide a 1-V signal at the AMC1035 input at 480-$V_{DC}$ bus voltage. R1, R2, and R3 are high-voltage resistors.

The AMC1035 analog input filter is designed similar to the AMC1306M05 in Section 3.2.2. However, the cutoff frequency is initially set to around 23-kHz. The analog input filter is determined by R4, R42, R44, and C65, and can be changed to any desired lower or higher cutoff frequency, for example in systems which monitor the AC voltage ripple on the DC-bus.

The MCE pin is set to low to configure for a bitstream data output at DOUT. Data at DOUT changes with the rising edge of the clock signal present on CLKIN. The line termination and filtering are similar as described in Section 3.2.3. A separate clock signal MCU_CLK_VDC_BUF is provided to allow the same of a different clock rate for DC-link voltage sensing, and is then configured for the three current-sensing modulators AMC1306M05. The AMC1035 supports clock input signals from 9 MHz to 21 MHz. The REFOUT is not used in this design and is terminated with C27 (3.3 nF) and a series resistor R17 (56 Ω).

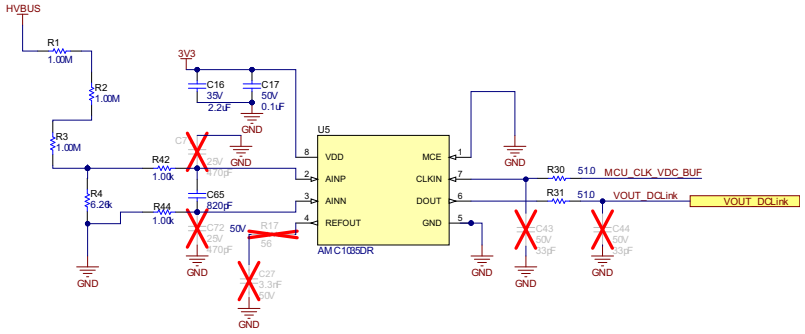



**Figure 3-8. DC-link Voltage Sensing With Non-isolated Modulator Schematic**

## 3.4 Phase Voltage Sensing

The TIDA-010255 provides an option to sense the three phase voltages with an analog-to-digital converter, typically integrated in the hot-side control MCU. Due to the very low dead-time of the LMG3422R030 GaN-FETs of 100 ns, the phase voltage can accurately be estimated using the PWM duty cycle and the DC-link voltage.

The phase voltage to GND is sensed using a high-voltage resistor divider and a low-pass filter to attenuate the PWM switching frequency. The high-impedance resistor divider R7, R18, R55, and R4 is scaled to provide a 3-V signal at a 480-$V_{DC}$ phase to GND voltage. The low-pass filter R58 and C49 has a cutoff frequency of 360 Hz to attenuate the PWM carrier frequency. Schottky diodes to clamp the maximum voltage at V_PHASE to around 3.6 V are not added intentionally, since the voltage is not supposed to exceed 3 V even during operating conditions with 480-$V_{DC}$ transient DC-link voltage, while the 360-Hz low-pass filter needs to suppress high-frequency transients.

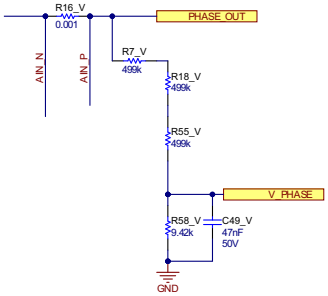



**Figure 3-9. Phase V to GND Analog Phase Voltage Sensing Schematic**

## 3.5 Control Supply

The TIDA-010255 requires an external 24-V DC supply with a tolerance of ±20% at connector J5 to generate the 12-V, 5-V, and 3.3-V non-isolated power rails to supply the signal chain and the C2000 MCU controlCARD through the 180-pin connector J1 and J2.

**WARNING**

The TIDA-010255 is a hot-side MCU controlled power stage with functional isolation only for the high-side power switches and related sensing components like the isolated delta-sigma modulators. The GND reference of the 24-V control supply is connected to the high-voltage GND HV_GND.

The point-of-load supplies for 12 V, 5 V, and 3.3 V are shown in Figure 3-10. A diode D6 protects for reverse polarity connection of the 24-V supply.

The first stage of the power tree converts the 24-V input to 12-V output. The TPSM560R6H power module with integrated shielded inductor is used for this DC/DC buck conversion. The output voltage is configured through the feedback resistors R41 (10 kΩ) and R43 (90 kΩ) following the *standard $R_{FBB}$ values* table in the *TPSM560R6H, 60-V Input, 1-V to 16-V Output, 600-mA Power Module in an Enhanced HotRod™ QFN Package*

data sheet for VOUT equals 12 V. The input and output capacitances follow the *minimum input capacitance* and *minimum output capacitance* requirements from the TPSM560R6H data sheet.

The second stage of the power tree converts 12 V to 5 V. The TPSM82903, 3-A, 3-V to 17-V, DC-DC converter with integrated inductor in a very small MicroSiP package module is used for this conversion. The output voltage is configured through the feedback resistors R34 (732 kΩ) and R45 (100 kΩ) for VOUT equal to 5 V. Reduce the resistance of R43 to 182 kΩ and R45 to 24.9 kΩ according to the *setting the output voltage* table in the *TPSM82903, 3-A, 3-V to 17-V, High Efficiency and Low $I_Q$ Buck Converter Module in a MicroSiP Package with an Integrated Inductor* data sheet.

The third stage of the power tree converts 5 V to 3.3 V with the TPSM82903 too. The output voltage is configured through the feedback resistors R46 (113 kΩ) and R47 (24.9 kΩ) following the *setting the output voltage* table in the *TPSM82903* data sheet for VOUT equal to 3.3 V. The 3.3-V output can be disabled by pulling down the 3V3_EN signal through the MCU, if desired.

Indicator LEDs D3, D4, and D5 turn on, when the corresponding 12-V, 3.3-V, and 5-V rails are available.

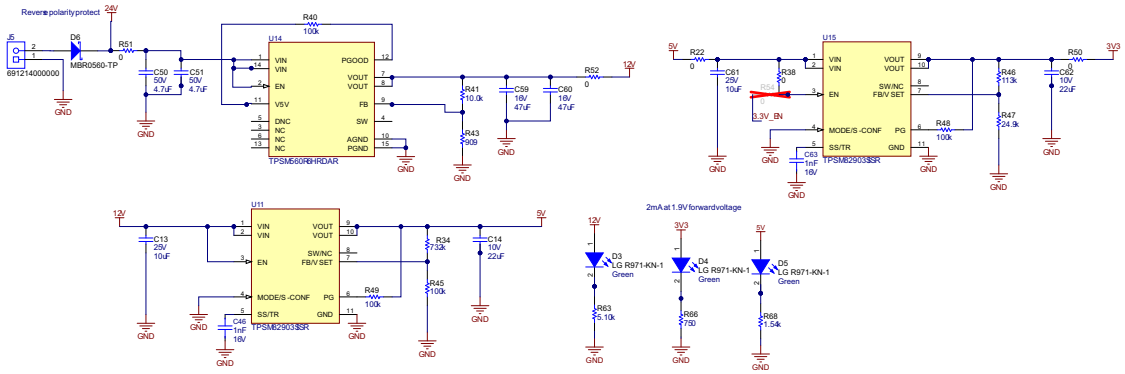



**Figure 3-10. Schematic of 24-V Control Supply With 12-V, 5-V, and 3.3-V Rails**

## 3.6 MCU Interface

Two connectors to interface to MCUs with 3.3-V I/O are provided for easy evaluation on the 3-phase GaN-FET power stage. A 180-pin connector J1 and J2 fits the pin assignment of the C2000 controlCARDs, such as the F28379D controlCARD. The 5-V rail generated in the TIDA-010255 also provides power to the C2000 controlCARD.

The design supports clock edge delay compensation for the digital interface to delta-sigma modulators AMC1035 and AMC1306. The C2000 MCU, for example, generates a 20-MHz clock with ePWM6B (AMC1035) and ePWM7B (AMC1306) and a phase-shifted 20-MHz clock with the ePWM6A and ePWM7A. The ePWM6B or ePWM7B clock signal connects to the clock buffer and drives the AMC1306M05 or AMC1035 clock input. The ePWM6B, ePWM7B clock signal connects to the SDFM clock input, for example, SD1_C1 and SD1_C2. The phase shift between ePWM6A and ePWM6B or ePWM7A and ePWM7B can now be adjusted in software until an optimum setup and hold time of the bitstream data signal at the SDFM data input, for example, SD1_D1 versus the rising clock edge at SD1_C1 is measured.

The headers J6, J7, J8, J9, and J11 are generic to interface to other MCUs like a Sitara AM2631. For the pin assignment of the MCU connectors, see Section 4.1.2.

# 4 Hardware, Software, Testing Requirements, and Test Results

## 4.1 Hardware Requirements

### 4.1.1 PCB

The six GaN-FETs LMG3422R030 devices are mounted on top of the PCB, as well as the three phase current shunts and the high-voltage supply input connector J3, the 24-V input supply connector J5, the three-phase motor connector J4, and the connectors J6 to J9 and J11 to an external MCU, as well as J1 and J2 to interface to a F28379D C2000 MCU controlCARD.

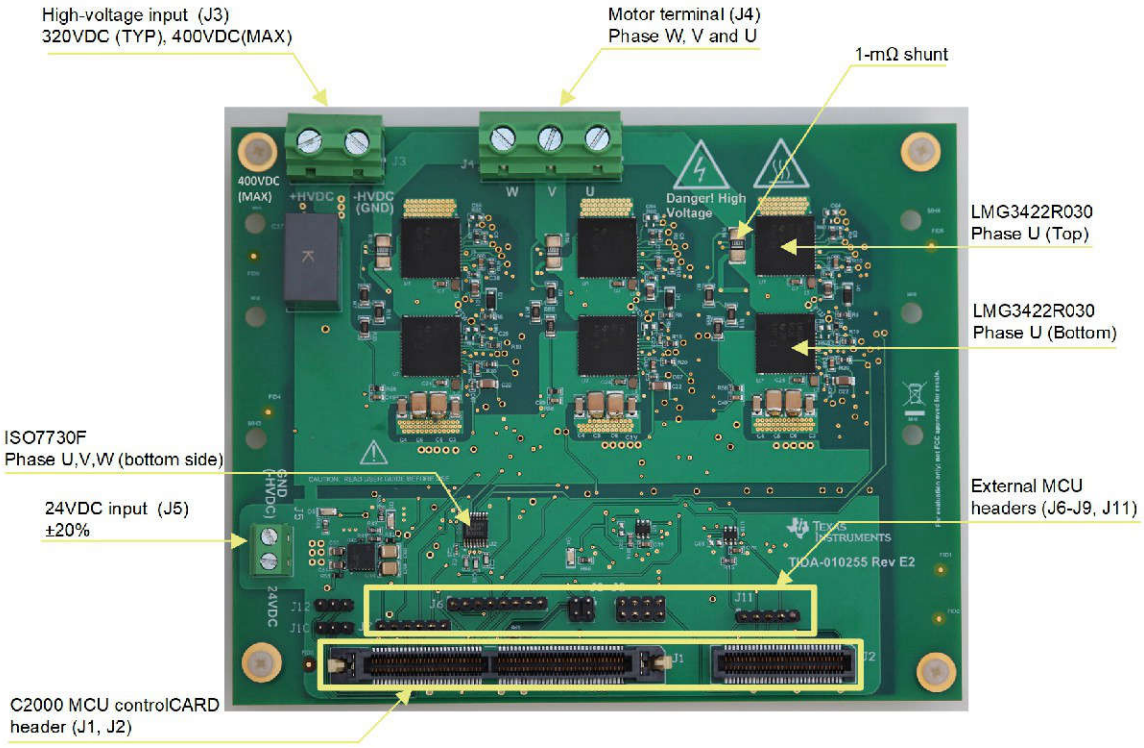



**Figure 4-1. TIDA-010255 PCB Top View**

The PCB bottom side shows the three isolated modulators AMC1306M25, the resistor dividers with the AMC1035 delta-sigma modulator for the DC-link voltage sensing and the six digital isolators ISO7741 for PWM level shifting. The 6 holes shown on the left and right allow for mounting a heat sink on the bottom-side of the PCB to connect to the six copper planes on the bottom-cooled LMG3422R030 GaN-FETs.

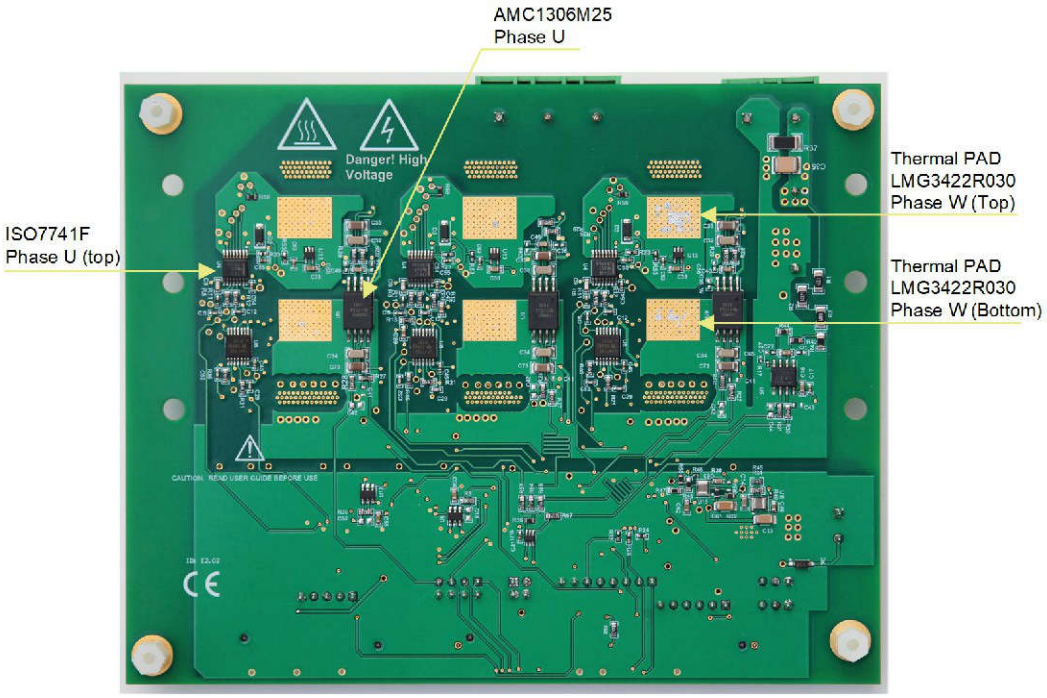



**Figure 4-2. TIDA-010255 PCB Bottom View**

### 4.1.2 MCU Interface

The TIDA-010255 offers two options to connect to a MCU:

1. Connect to a C2000 MCU controlCARD, such as the F28379D development kit for C2000™ Delfino MCU controlCARD™ to headers J1 and J2
2. Connect to an external MCU to headers J6, J7, J8, J9, and J11

The pin assignment with connectors J1 and J2 is shown in Table 4-1. The table also includes the corresponding I/O signals based on the F28379D control card. All I/O pins are 3.3-V I/O, and only the supply voltage provided to the F28379D controlCARD is 5 V.

Rows where no pin was connected (for example, pin 15 and pin 16) are not shown – to reduce size of the table. The pins and related headers J10 and J12 are marked reserved (RSVD) and are for test and debug.

**Table 4-1. C2000™ controlCARD Connector**

| J1–J2 PIN | F28379D GPIO | TIDA-010255 SIGNAL | J1-J2 PIN | F28379D | TIDA-010255 SIGNAL |
|---|---|---|---|---|---|
| 7 | GND | GND | 8 | TDI | |
| 9 | A0 | J10-2 (RSVD) | 10 | GND | GND |
| 11 | A1 | V_PHASE_W | 12 | B0 | V_PHASE_W |
| 13 | GND | GND | 14 | B1 | J10-3 (RSVD) |
| 17 | A3 | | 18 | B2 | V_PHASE_V |
| 19 | GND | GND | 20 | B3 | V_PHASE_U |
| 21 | A4 | J12-3 (RSVD) | 22 | GND | GND |
| 23 | A5 | J12-2 (RSVD) | 24 | B4 | TOP_TEMP_V |

**Table 4-1. C2000™ controlCARD Connector (continued)**

| J1–J2 PIN | F28379D GPIO | TIDA-010255 SIGNAL | J1-J2 PIN | F28379D | TIDA-010255 SIGNAL |
|---|---|---|---|---|---|
| 25 | A14 | | 26 | B5 | BOT_TEMP_V |
| 29 | GND | GND | 30 | D1 | |
| 31 | C2 | V_PHASE_V | 32 | RSV | |
| 35 | GND | GND | 36 | D3 | |
| 37 | C4 | | 38 | GND | GND |
| 45 | VREFHI | | 46 | GND | GND |
| 47 | GND | GND | 48 | 5 V | 5 V |
| 49 | EPWM1A | TOP_FET_V | 50 | EPWM3A | TOP_FET_W |
| 51 | EPWM1B | BOT_FET_V | 52 | EPWM3B | BOT_FET_W |
| 53 | GPIO-2 | | 54 | EPWM4A | TOP_FET_U |
| 55 | GPIO-3 | | 56 | EPWM4B | BOT_FET_U |
| 57 | GPIO-8 | | 58 | EPWM7A | MCU_CLK_VDC_FB |
| 59 | GPIO-9 | | 60 | EPWM7B | MCU_CLK_VDC |
| 61 | GPIO-10 | | 62 | EPWM6A | MCU_CLK_I_FB |
| 63 | GPIO-11 | | 64 | EPWM6B | MCU_CLK_I |
| 65 | GND | GND | 66 | RSV | |
| 83 | GND | GND | 84 | 5 V | 5 V |
| 89 | GPIO-40 | GPIO_EN | 90 | GPIO-44 | |
| 97 | GND | GND | 98 | 5 V | 5 V |
| 99 | SD1_D1 | VOUT_DCLink | 100 | GPIO-54 | |
| 101 | SD1_C1 | MCU_CLK_VDC_FB | 102 | GPIO-55 | |
| 103 | SD1_D2 | IOUT_W | 104 | GPIO-56 | |
| 105 | SD1_C2 | MCU_CLK_I_FB | 106 | GPIO-57 | |
| 107 | SD1_D3 | IOUT_V | 108 | GPIO-58 | |
| 109 | SD1_C3 | MCU_CLK_I_FB | 110 | GPIO-59 | |
| 111 | GND | GND | 112 | 5 V | 5 V |
| 121 | GPIO-35 | | 122 | GPIO-36 | nOC_T |
| 127 | SD2_D4 | IOUT_U | 128 | SD2_C4 | MCU_CLK_I_FB |
| 135 | GND | GND | 136 | RSV | |
| 137 | GPIO-70 | | 138 | GPIO-71 | GaN_Fault_L |
| 139 | GPIO-72 | | 140 | GPIO-73 | GaN_Fault_T |
| 145 | GPIO-78 | | 146 | GPIO-79 | nOC_L |
| 157 | GND | GND | 158 | 5 V | 5 V |
| 179 | GND | GND | 180 | 5 V | 5 V |

The pin assignments with connectors J6–J9 and J11 are shown in Table 4-2. Note that all pins are 3.3-V I/O signal level.

**Table 4-2. External MCU Connectors Assignment J6–J9, J11**

| J6 | | | | | |
|---|---|---|---|---|---|
| Pin | J6-1 | J6-2 | J6-3 | J6-4 | J6-5 |
| Signal | TOP_FET_V | BOT_FET_V | TOP_FET_W | BOT_FET_W | TOP_FET_U |
| Pin | J6-6 | J6-7 | J6-8 | | |
| Signal | BOT_FET_U | GND | GND | | |
| **J7** | | | | | |
| Pin | J7-1 | J7-2 | J7-3 | J7-4 | J7-5 |
| Signal | V_PHASE_W | V_PHASE_V | V_PHASE_U | TOP_TEMP_V | BOT_TEMP_V |
| Pin | J7-6 | | | | |
| Signal | GND | | | | |
| **J8** | | | | | |
| Pin | J8-1 | J8-2 | J8-3 | J8-4 | J8-5 |
| Signal | VOUT_DCLink | GND | IOUT_W | GND | IOUT_V |
| Pin | J8-6 | J8-7 | J8-8 | | |
| Signal | GND | IOUT_U | GND | | |
| **J9** | | | | | |
| Pin | J9-1 | J9-2 | J9-3 | J9-4 | |
| Signal | MCU_CLK_I | GND | MCU_CLK_VDC | GND | |
| **J11** | | | | | |
| Pin | J11-1 | J11-2 | J11-3 | J11-4 | J11-5 |
| Signal | nOC_T | GaN_Fault_L | GaN_Fault_T | nOC_L | GND |

## 4.2 Software Requirements

To validate the TIDA-010255, a TI internal test software was developed for the TMS320F28379D and the corresponding controlCARD was used. This software is not available for public use. For C2000 software support refer to the *MotorControl software development kit (SDK) for C2000™* and the TI E2E™ design support forum for C2000™ microcontrollers.

## 4.3 Test Setup

Table 4-3 shows the key test equipment used to validate the performance of the TIDA-010255 3-phase GaN-inverter.

**Table 4-3. Key Test Equipment**

| DESCRIPTION | PART NUMBER |
|---|---|
| Reference design | TIDA-010255 rev E2 |
| MCU | TMDSCNCD28379D - F28379D development kit for C2000™ MCU controlCARD™ |
| AC induction motor | Pro-Lift 4 kW AC induction motor, 400 V, 690 V, 1440 rpm, model: 3A112SM4 - 00410 |
| High Voltage Permanent Magnet Synchronous Motor | ESTUN, Anaheim Automation EMJ-04APA22 |
| Adjustable power supply for DC-link (320-$V_{DC}$) | TDK-Lamda GENH600-1.3 |
| Oscilloscope | Tektronix MDO4104B-3 |
| Probes | Tektronix TPP1000 |
| Power Analyzer | Tektronix PA4000 |
| Current probe | Tektronix TCP0030 |
| Thermal camera | Fluke TI40 |

### 4.3.1 Precautions

This reference design is a non-isolated hot-side MCU controlled 3-phase power stage with functional isolation for the top-side GaN-FET drivers only and operates from a supply voltage up to 400 $V_{DC}$ (MAX). Therefore, the PCB is exposed to voltages above 60-$V_{DC}$ and 25-$V_{AC}$ and hence extreme care must be exercised while testing.

This reference design is meant for exploring TI's GaN-FET technology in a lab space only and to be used by professional engineers, who are qualified to work with high voltage. A high-voltage warning symbol is added to the PCB top and bottom side. Users must make sure proper high-voltage safety precautions are observed before and while testing. Do not directly handle exposed terminals (high voltage or otherwise) while power is turned on. All connections must be done while the reference design is de-energized and not powered-up. Even during operation at room temperature around 25°C, some components and parts of the PCB surface can reach temperatures higher than 100°C. A high temperature warning symbol is added to the PCB top and bottom side. Do not touch the PCB as contact can cause burns.

After removing power from the PCB, let the PCB cool down for some time and make sure the DC-link capacitor is discharged to 0 V before handling the PCB again.

**WARNING**

Danger! High Voltage. Electric shock is possible when connecting board to live wire. Board must be handled with care only by a professional person, qualified to work with high voltage. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

**WARNING**

Hot surface! Contact can cause burns. Do not touch!

**WARNING**

Do not leave the board powered when unattended.

### 4.3.2 Test Procedure

Use the following steps for the test procedure:

1. Become familiar with the TIDA-010255 PCB, schematic and layer plots. Remember that the TIDA-010255 PCB and related interfaces are not isolated.
2. Test and validate the TIDA-010255 PCB only in an appropriate lab. Make sure the TIDA-010255 PCB is de-energized and not connected to any power supply.
3. Connect either an external MCU or a C2000 MCU controlCARD to the TIDA-010255 PCB
   a. External MCU: Interface to connectors J6-J9 and J11.
   b. C2000 controlCARD: Insert the F28379D controlCARD to the control card connector J1 and J2 on the TIDA-010255 PCB. Be careful inserting to avoid the PCB bends during the insertion.
4. When using the F28379D controlCARD, connect an **isolated** mini-USB adapter from the F28379D controlCARD JTAG connector to the USB interface of the computer.
5. Connect a 3-phase motor to terminal J4.
6. Connect the low voltage 24-$V_{DC}$ power supply to connector J5. When the power supply is connected to the TIDA-010255 PCB, it draws around 46 mA if the F28379D controlCARD is used.
7. Connect the high voltage DC source at terminal J3. The high-voltage ground terminal (-HVDC/GND) is galvanically connected to the ground of the 24-$V_{DC}$ input terminal. Do not turn on the high-voltage DC source, until the corresponding C2000 MCU software or other MCU software is downloaded and running.
8. When using the F28379D controlCARD, upload and run the TIDA-010255E2 binary firmware. This is internal test software and not publicly available.
9. Turn on the high-voltage DC supply voltage only after the software is running as expected on the selected MCU. Start with 24-V and validate the motor is running as expected. Then the high-voltage DC supply can be increased up to a nominal 320 $V_{DC}$ and absolute maximum 400 $V_{DC}$. Current limit the high-voltage DC source accordingly to prevent accidental high short circuit current and fire.
10. Monitor the surface temperature of the PCB through a thermal camera while operating the board with a load to avoid excess PCB temperatures above 105°C.

Figure 4-3 shows how the connections are made when using a F28379D C2000 MCU controlCARD. The TIDA-010255 supplies the 5 V required for the C2000 MCU controlCARD, but all interfaces are 3.3 V I/O. The software can then be uploaded to the C2000 MCU through an isolated USB JTAG connector and Code Composer Studio™ software.

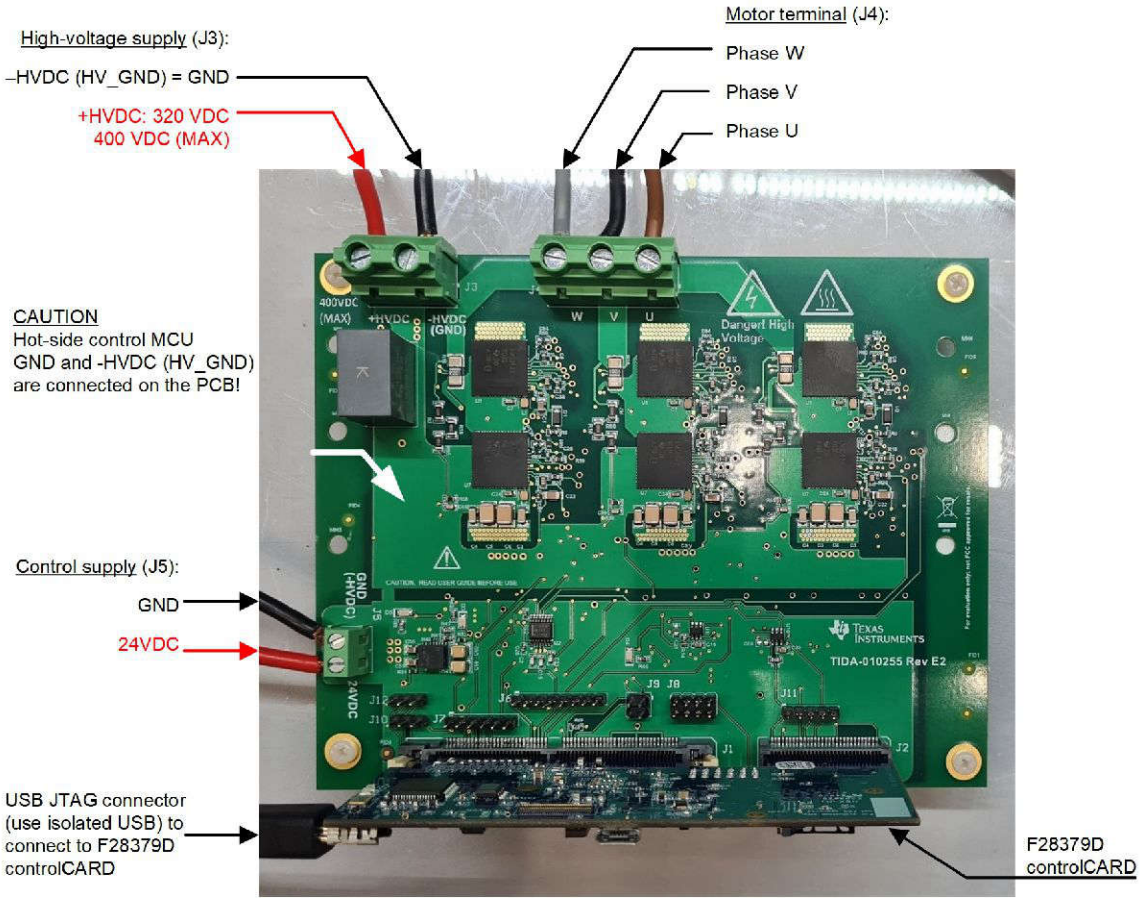



**Figure 4-3. TIDA-010255 PCB Connections**

Figure 4-4 shows the test environment for power loss and efficiency measurement with the TIDA-010255 3-phase inverter. Two power supplies are used, a high-voltage 320-$V_{DC}$ supply for the DC-link voltage and a 24-V control supply for the point-of-load supplies. The TMS320F28379D MCU on the F28379D controlCARD is configured through a laptop with Code Composer Studio (CCS) and generates a 3-phase output voltage with variable magnitude and frequency to drive an AC induction motor. The Tektronix PA4000 power analyzer is used to measure the input power, output power and the corresponding TIDA-010255 PCB power losses without a heat sink.

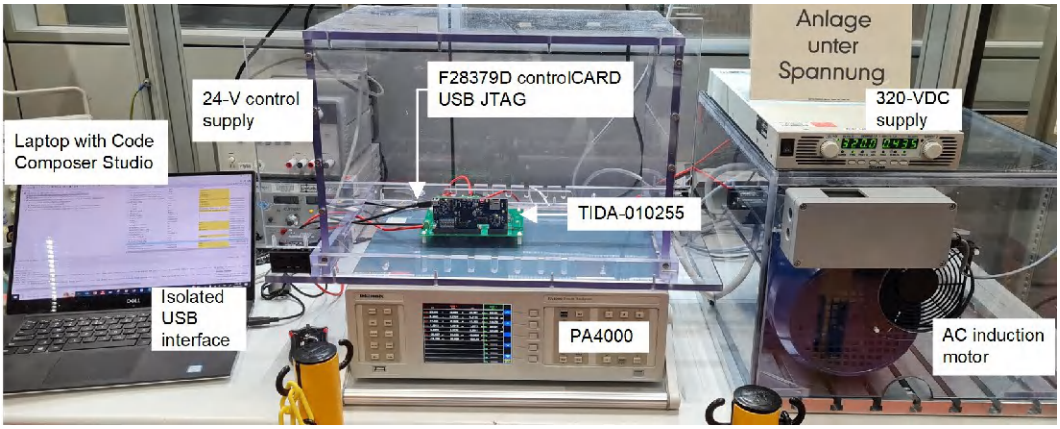



**Figure 4-4. TIDA-010255 Power Loss and Efficiency Measurement Test Setup**

## 4.4 Test Results

### 4.4.1 24-V Input Control Supply

The nominal input supply current at 24 V is dependent on the PWM frequency and using a F28379D controlCARD running at a 200-MHz system clock as shown in Table 4-4, which includes the supply current for the entire F28379D controlCARD. The typical input current of the TIDA-010255 drawn without an MCU connected is around 22 mA.

**Table 4-4. Input Supply Current at 24 V With F28379D controlCARD**

| PWM | OFF | 8 kHz | 16 kHz | 24 kHz |
|---|---|---|---|---|
| 24-V input current (TYP) | 84 mA | 87 mA | 90 mA | 93 mA |

### 4.4.2 Propagation Delay PWM to Phase Voltage Switch Node

Figure 4-5 outlines the turn-on and turn-off propagation delay from the MCU complementary PWM signal with 150-ns dead time to the phase U switch node. The turn-off time instant of the bottom GaN-FET can be identified, when the phase voltage U changes from 0 V to around –4 V. Then the bottom FET is conducting in the 3rd quadrant mode with a drain-to-source voltage $V_{DS}$ of around –4 V, as indicated with the dashed line. The effective turn-off delay is 165 ns. The effective turn-on delay of the top FET (hard switching) is around 135 ns. The effective dead time is 120 ns due to the difference in the turn-on and turn-off delay, as shown below.

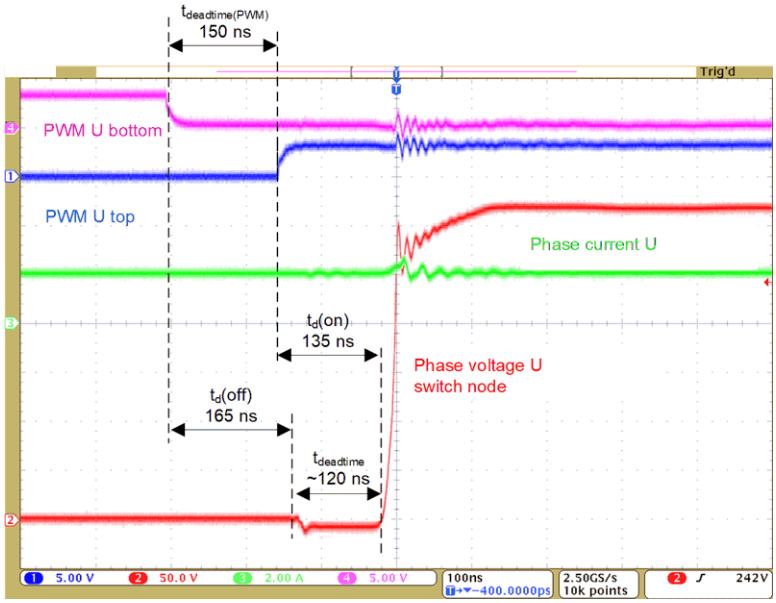



**Figure 4-5. PWM Turn On and Turn Off Propagation Delay**

### 4.4.3 Switch Node Transient at 320-$V_{DC}$ Bus Voltage

The C2000 MCU was configured to generate a 3-phase space vector with complementary PWM with 16-kHz switching frequency and 150-ns dead time. The PWM duty cycle per phase was configured to drive the corresponding phase DC current $I_U$ with $I_V = I_W = –0.5\ I_U$.

The LMG3422 switch node voltage at phase U was measured with a pigtail probe at the top of the LMG3422 source versus PGND inserted into the two vias, prepared for testing, as shown in Figure 4-6.

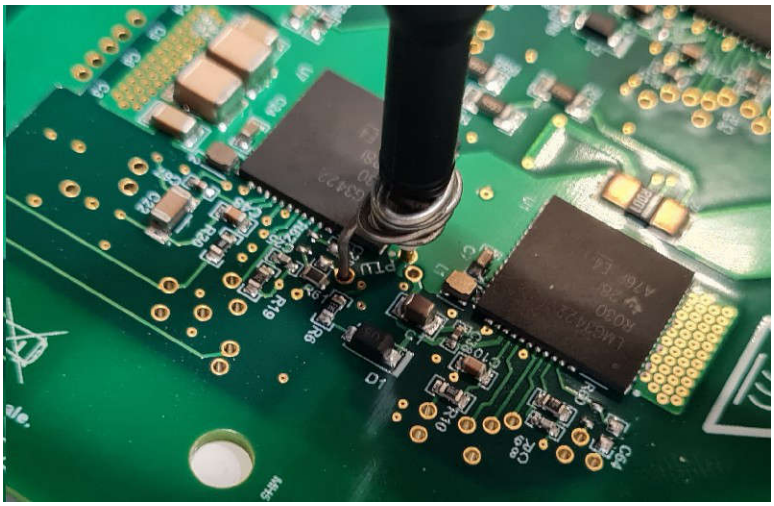


**Figure 4-6. LMG3422 Switch Node Phase Voltage Measurement**

The following figures outline the phase U switch node transient at phase currents ±1 A and ±4 A to illustrate hard-switching and soft-switching.

Observe that at ±1 A, the phase current U is not large enough to discharge (or charge) the effective output capacitance of the half-bridge during the short dead time of 120 ns; therefore, the corresponding GaN-FETs are still partially hard-switching, but at a lower drain-to-source voltage. For example with Figure 4-7, the top GaN-FET turns off and the bottom GaN-FET turns into the 3rd quadrant mode. Due to the parasitic output capacitance, the phase U voltage decline is impacted by the effective parasitic output capacitance of each half-bridge. After the 120-ns dead time, the effective parasitic output capacitance is discharged with the impressed current of 1 A from 320 V to around 250 V. Hence the bottom-side GaN-FET is still hard switched from 250 V to 0 V.

The phase current oscillations (4.5 $A_{peak}$, around 10 MHz, 500-ns duration in hard-switching) seen with Figure 4-7 through Figure 4-14 are due to the parasitic capacitance and inductance of the 1-m cable and the AC induction motor.

The oscillations significantly reduce when using a 20-cm cable, in that case with a 200 $V_{AC}$ servo motor, as shown in Figure 4-15 and Figure 4-16.

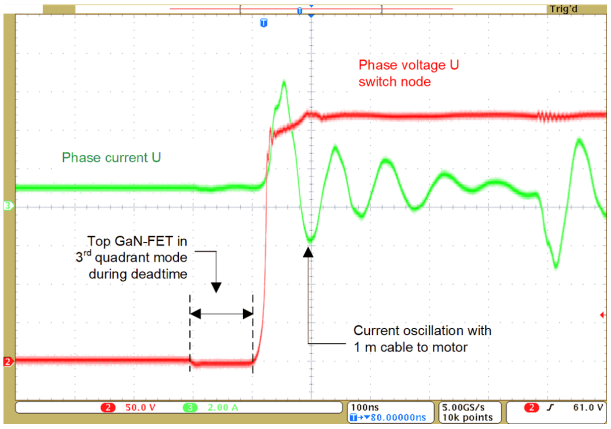



**Figure 4-7. Phase U Rising Edge Waveform at 1 A, 1-m Cable to AC Induction Motor**

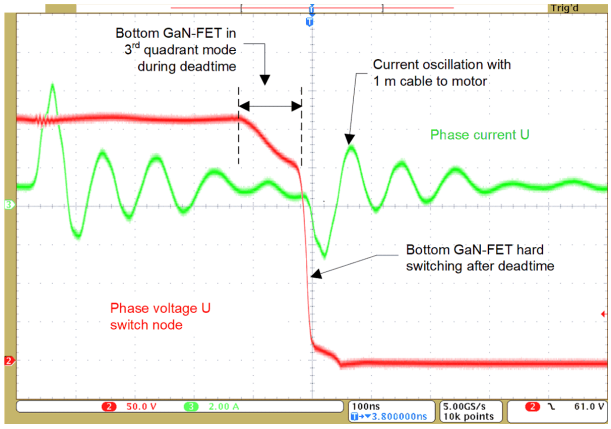



**Figure 4-8. Phase U Falling Edge Waveform at 1 A, 1-m Cable to AC Induction Motor**

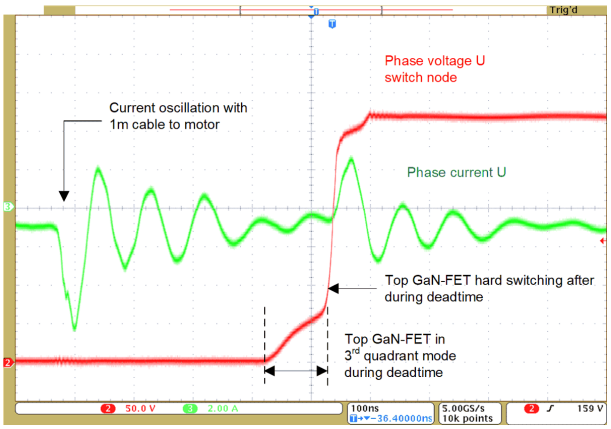



**Figure 4-9. Phase U Rising Edge Waveform at –1 A, 1-m Cable to AC Induction Motor**

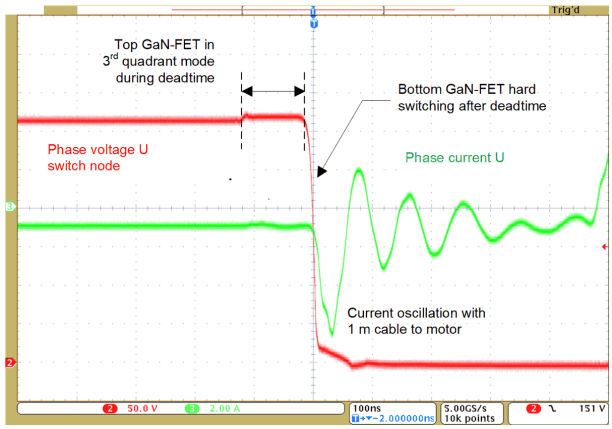



**Figure 4-10. Phase U Falling Edge Waveform at –1 A, 1-m Cable to AC Induction Motor**

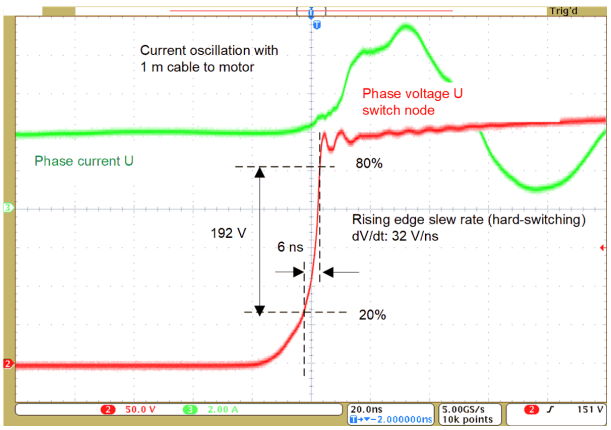



**Figure 4-11. Phase U Rising Edge Waveform at 4 A, 1-m Cable to AC Induction Motor**

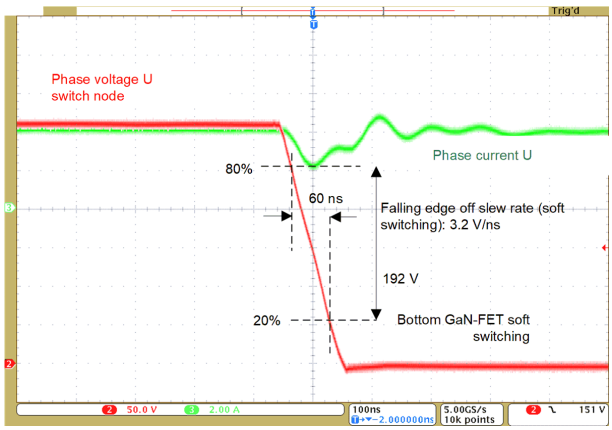



**Figure 4-12. Phase U Falling Edge Waveform at 4 A, 1-m Cable to AC Induction Motor**

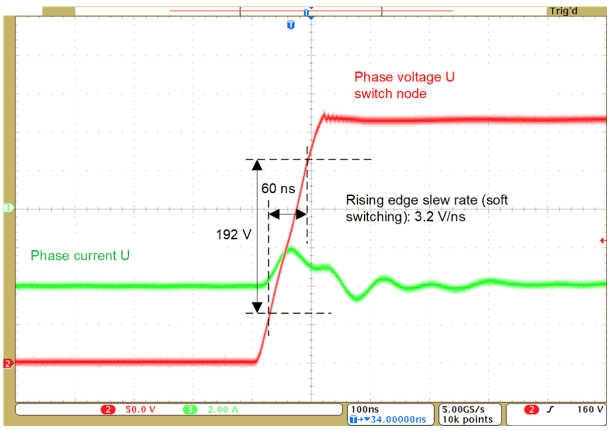



**Figure 4-13. Phase U Rising Edge Waveform at –4 A, 1-m Cable to AC Induction Motor**

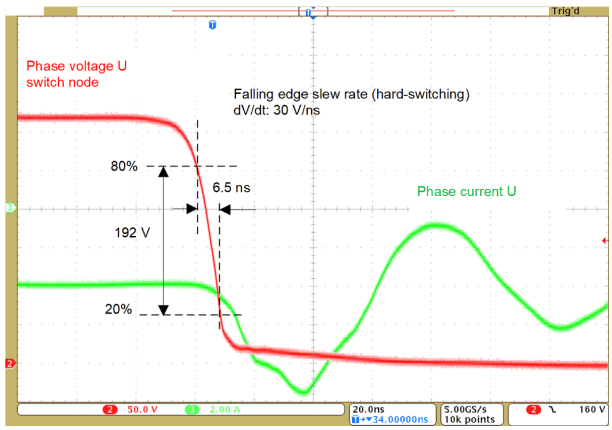



**Figure 4-14. Phase U Falling Edge Waveform at –4 A, 1-m Cable to AC Induction Motor**

The rising edge slew rate from 20% to 80% in hard-switching mode is around 32 V/ns, the falling edge slew rate from 80% to 20% in hard-switching mode is around 30 V/ns, close to the configured 30 V/ns turn-on slew rate with the LMG3422R030.

Observe that at ±4 A or higher phase currents, the phase current U is large enough to fully discharge (or charge) the effective parasitic output capacitance of the half-bridge during the short dead time, hence the corresponding GaN-FET is soft switching. From the phase voltage drop during soft-switching, the effective output capacitance of each half-bridge can be estimated using Equation 4.

$$C_{OSS,\,HB} = \frac{i_U}{\Delta V_U} \times \Delta t = \frac{4\ A}{192\ V} \times 60\ ns = 1.25\ nF \quad (4)$$

The capacitance $C_{OSS,HB}$ is basically the sum of the bottom and top $C_{O(tr)}$ of the GaN-FET and the corresponding parasitic capacitance of the PCB, motor cable, and motor. See the *Efficiency Measurements* section for further analysis.

The phase current oscillations are mainly due to motor cable and motor windings, a shorter cable leads to lower peak oscillations and higher oscillation frequency, as shown in Figure 4-15 and Figure 4-16. The peak amplitude and frequency of the parasitic oscillations were almost independent of the load current. Compared to the 1-m cable with the AC induction motor, the peak oscillation amplitude during hard-switching reduces by 80% from 5 $A_{peak}$ to 1 $A_{peak}$, the frequency increases from 10 MHz to 40 MHz, while the duration reduces from 500 ns to less than 200 ns.

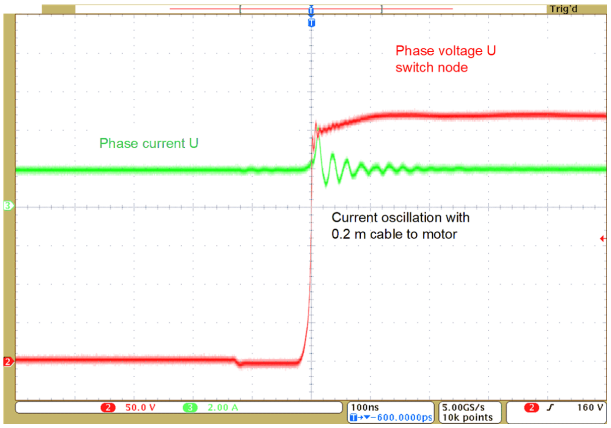



**Figure 4-15. Phase U Rising Edge Waveform at 2 A, 0.2-m Cable to PM Synchronous Motor**

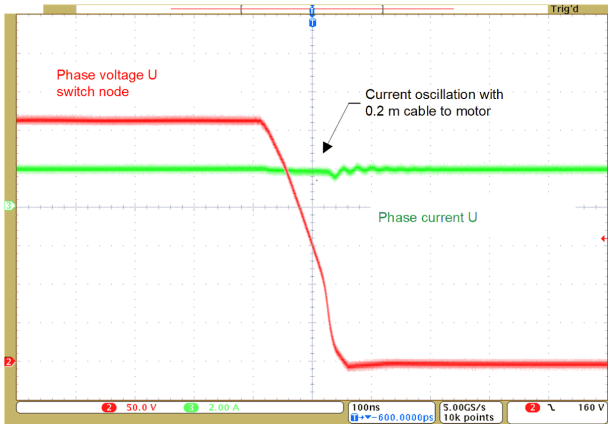



**Figure 4-16. Phase U Falling Edge Waveform at 2 A, 0.2-Cable to PM Synchronous Motor**

### 4.4.4 Phase Voltage Linearity and Distortion at 320 $V_{DC}$ and 16-kHz PWM

Figure 4-17 shows the measured phase U motor current and the low-pass filtered phase U voltage with a 1-Hz sinusoidal output voltage at 27 V driving the AC induction motor at no mechanical load. Due to the very low dead-time of 120 ns at 16-KHz PWM, there are no distortions in the phase voltage U, especially visible when the phase crosses zero.

The linearity plot in Figure 4-18 shows the high linearity between PWM duty cycle and average phase voltage and related phase current. Therefore, dead-time compensation methods are not required with LMG3422R030 GaN-FETs and BOM cost is reduced.

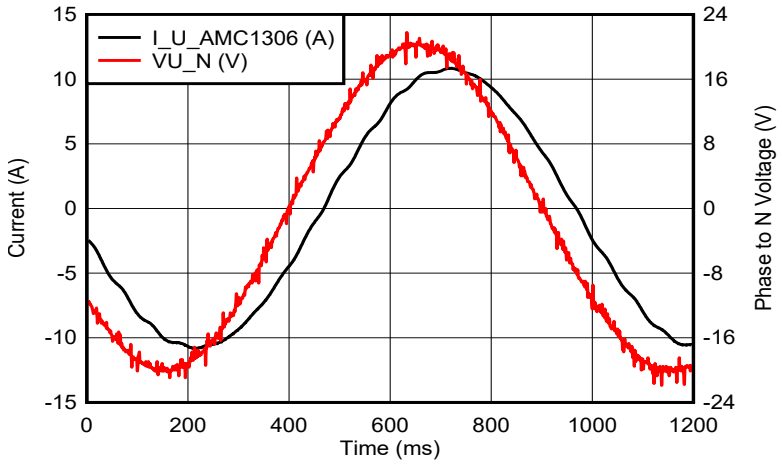



**Figure 4-17. Filtered Phase U Voltage and Current With AC Induction Motor at 16-kHz PWM and 320-$V_{DC}$ Bus Voltage**

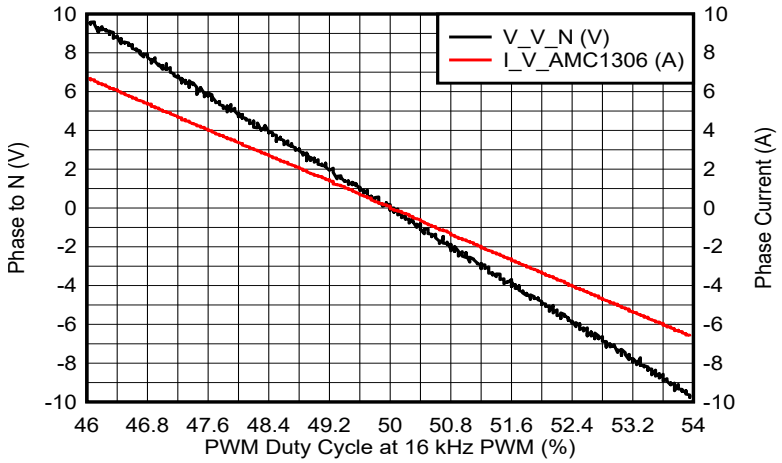



**Figure 4-18. Linearity Plot of Phase Voltage and Current Versus of PWM Duty Cycle at 16-kHz PWM and 320-$V_{DC}$ Bus Voltage**

### 4.4.5 Inverter Efficiency and Thermal Characteristic

#### *4.4.5.1 Efficiency Measurements*

The efficiency testing was done at 27°C lab temperature with a Tektronix PA4000 power analyzer. The TIDA-010255 PCB without heat sink was placed horizontal on the workbench as shown in Figure 4-4, with natural convection only. The F28379D MCU software was configured to create a 3-phase AC voltage at 1-Hz frequency with configurable amplitude. The PWM carrier frequency was set to either 16 kHz or 8 kHz.

The following figures show the TIDA-010255 PCB power losses without heat sink versus the 3-phase motor load current in $A_{RMS}$ in the steady state, when the PCB and the GaN-FETs reach their steady state temperature, typically after around 5 minutes. The power losses are dominated by the switching and conduction power losses of GaN-FET, while the phase current shunt power losses are negligible.

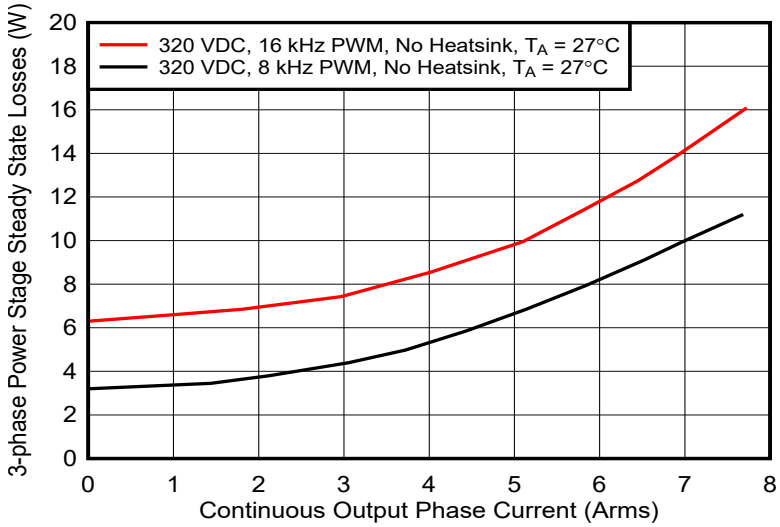



**Figure 4-19. TIDA-010025 Power Losses at 320 $V_{DC}$, 8-kHz and 16-kHz PWM versus Output Current**

The TIDA-010255 board power losses at an output current of 7.7 $A_{RMS}$ at 16-kHz PWM were 16.09 W, and 11.2 W at 8-kHz PWM.

The theoretical maximum peak efficiency at 320 $V_{DC}$ with a maximum phase-to-phase of voltage of 130 $V_{RMS}$ (Space Vector PWM with 3rd harmonics) and a power factor of 0.9 is 99.4% at 16-kHz PWM and 99.6% at 8-kHz PWM.

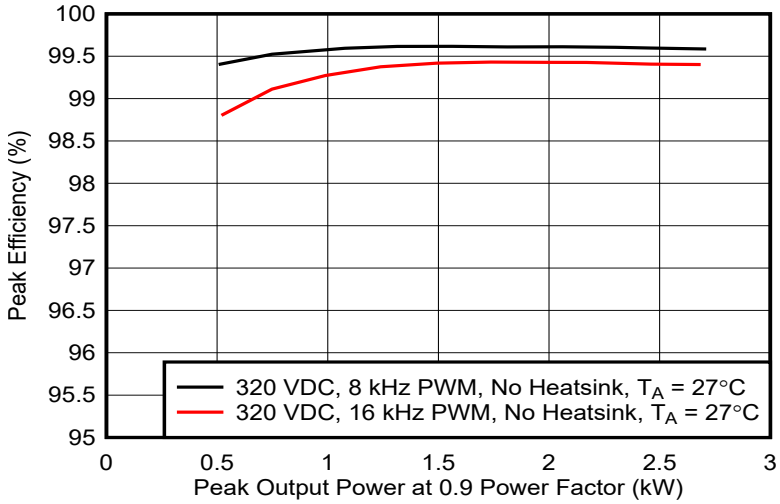



**Figure 4-20. Calculated Maximum Peak Efficiency at 320 $V_{DC}$, 8-kHz and 16-kHz PWM**

To see the effective parasitic capacitive losses, the TIDA-010255 PCB power losses were measured at zero load current with 50% PWM duty cycle and PWM switching frequencies from 8 kHz to 64 kHz, as shown in Figure 4-21. In the first test the inverter output was left unconnected. The losses at 64-kHz PWM were 21.7 W. The total losses are per Equation 5, where $C_{OSS\_HB}$ is the effective parasitic capacitance per half-bridge of around 1.1 nF, which gives around 550 pF per each of the six power switches including TIDA-010255 PCB parasitic capacitance. Assuming a 50-pF parasitic PCB capacitance, the estimated time related effective output capacitance $C_{O(tr)}$ of the LMG3422R030 from 0 V to 320 V is around 500 pF, which is around 15% higher than the 430-pF $C_{O(tr)}$ from 0 V to 400 V.

In the second test an AC induction motor with a 1-m cable was connected to explore the impact on the overall zero load current losses. Again, the PWM duty cycle was set to 50%, hence no motor current was driven. The losses at 64 kHz increased to 22.7 W. The additional parasitic load capacitance with the 1-m cable an AC induction motor was calculated around 50 pF per phase.

$$C_{OSS_{HB}} = \frac{1}{3} \times \frac{P_{NOLOAD}}{{V_{DC}}^2 \times f_{PWM}} \quad (5)$$

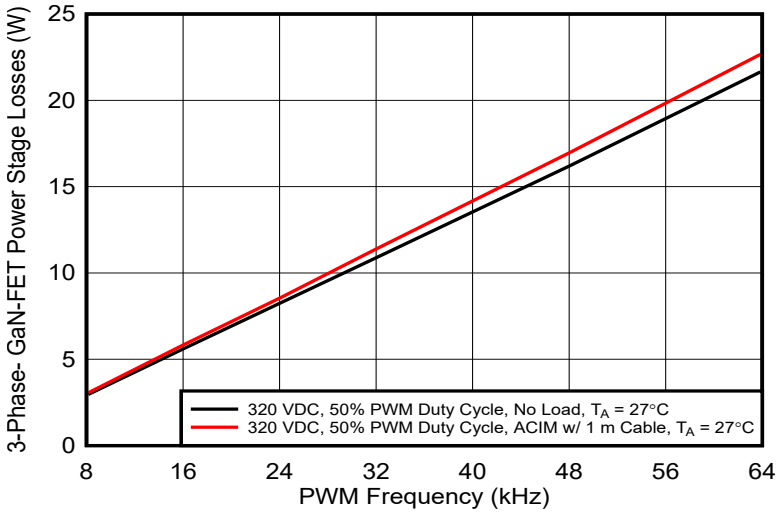



**Figure 4-21. TIDA-010025 Power Losses at 320 $V_{DC}$ Without Heat Sink versus PWM Frequency at No Load**

### *4.4.5.2 Thermal Analysis and SOA Without Heat Sink at 320 $V_{DC}$ and 16-kHz PWM*

Figure 4-22 and Figure 4-23 show the thermal tests at 27°C ambient temperature (using Fluke TI40) with the TIDA-010255 power stage running at 7.1 $A_{RMS}$ and 7.7 $A_{RMS}$ output phase current at 16-kHz PWM. The top LMG3422R030 case temperature was around 90°C (at 7 $A_{RMS}$) and 94.3°C (at 7.7 $A_{RMS}$). The six LMG3422R030 devices are quite visible. The LMG3422R030 junction temperature at phase V was measured around 98°C at 7.7 $A_{RMS}$ through the PWM temperature output with the top-side LMG3422R030, while the bottom-side LMG3422R030 was around 91°C. The bottom LMG3422R030 devices are at a lower temperature, since the thermal PAD and electrically-connected source pins were connected to the large GND plane. The top FET thermal PAD and electrically-connected source pins were connected to the individual switch node with a very small area copper plane to minimize EMI and PCB parasitic output capacitance.

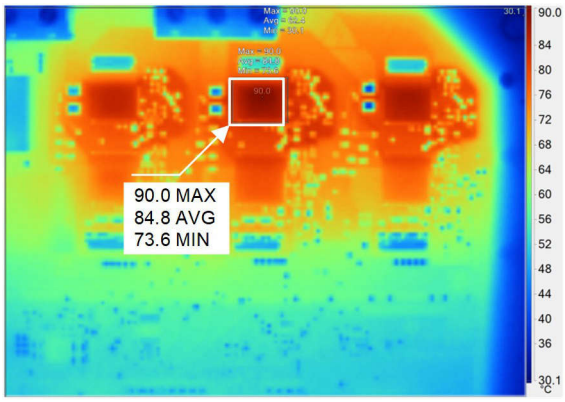



**Figure 4-22. TIDA-010255 PCB Thermal Image at 7.1-$A_{RMS}$ Load Current**

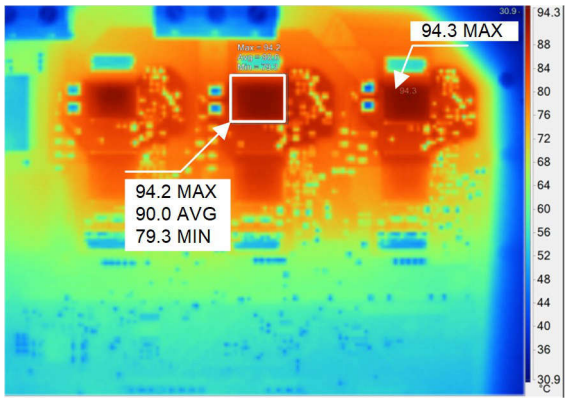



**Figure 4-23. TIDA-010255 PCB Thermal Image at 7.7-$A_{RMS}$ Load Current**

Figure 4-24 outlines the estimated safe operating area (SOA) for TIDA-0100255 without a heat sink assuming natural convection at 320-V DC-link voltage and 8-kHz PWM and 16-kHz PWM. The SOA estimation is based on the measured power losses per Figure 4-19, the LMG3422R030 thermal junction and case temperature measurements with a correction factor to consider the increased $R_{DS(on)}$ operating at $T_j$ = 125°C.

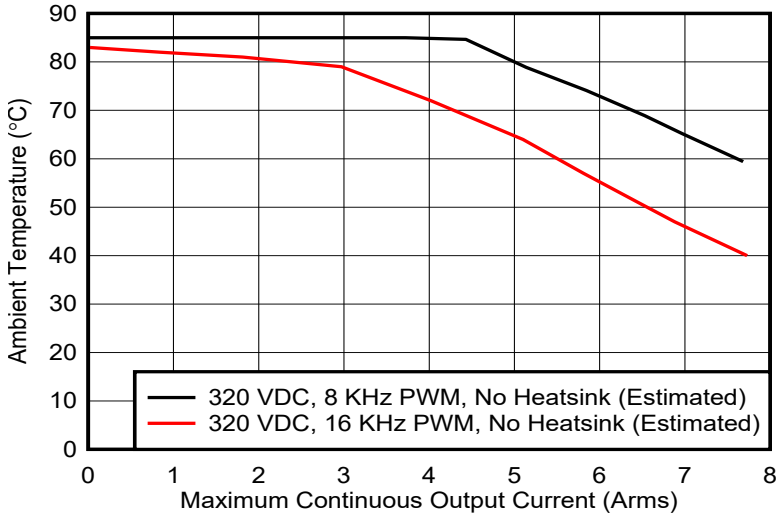



**Figure 4-24. Estimated Safe Operating Area of TIDA-010025 (Horizontal Placement, no Heat Sink) With Natural Convection**

# 5 Design and Documentation Support

## 5.1 Design Files

### 5.1.1 Schematics

To download the schematics, see the design files at TIDA-010255.

### 5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010255.

### 5.1.3 PCB Layout Recommendations

#### *5.1.3.1 Layout Prints*

To download the layout prints, see the design files at TIDA-010255.

### 5.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-010255.

### 5.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010255.

### 5.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010255.

## 5.2 Tools and Software

### Tools

| | |
|---|---|
| F28379D development kit for C2000™ Delfino MCU controlCARD™ | TMDSCNCD28379D is an HSEC180 controlCARD based evaluation and development tool for the F2837xD, F2837xS, and F2807x series in the TI MCU. controlCARDs are ideal to use for initial evaluation and system prototyping. controlCARDs are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC ) to provide a low-profile single-board controller solution. For first evaluation controlCARDs are typically purchased bundled with a baseboard or bundled in an application kit. |

### Software

| | |
|---|---|
| MotorControl software development kit (SDK) for C2000™ | MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI reference designs which are targeted for industrial drives, robotics, appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications. |

## 5.3 Documentation Support

1. Texas Instruments, *Maximize efficiency of motor drives with TI GaN technology* Video
2. Texas Instruments, *LMG342XEVM-04X User Guide* User's Guide
3. Texas Instruments, *Thermal Performance of QFN 12x12 Package for 600-V GaN Power Stage* Application Report
4. Texas Instruments, *Understanding the Third Quadrant Operation of GaN* User's Guide
5. Texas Instruments, *Achieving Better Signal Integrity With Isolated Delta Sigma Modulators in Motor Drives* Application Report

6. Texas Instruments, *Circuit Board Insulation Design According to IEC60664 for Motor Drive Application* Application Report
7. Texas Instruments, *MotorControl software development kit (SDK) for C2000™ MCUs* Tool Folder

### 5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 6 About the Author

**MARTIN STAEBLER** is a System Engineer and Senior Member Technical Staff in the Industrial Systems Motor Drive team at Texas Instruments and responsible for specifying and developing reference designs for industrial drives.

**RECOGNITION:** The author recognizes the excellent contribution from Ester Vicario to the development and validation of the TIDA-010255 reference design.

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