Design Guide: TIDM-02014

Automotive, High-Power, High-Performance SiC Traction Inverter Reference Design

Description

This reference design is an 800V, 300kW silicon carbide (SiC) based traction inverter developed by Texas Instruments and Wolfspeed®. This design provides a foundation to create a high-performance, high-efficiency traction inverter to help get to market faster.

Resources

TIDM-02014	Design Folder
UCC5880-Q1, UCC5881-Q1	Product Folder
F29H859TUQ1, TPS653860-Q1	Product Folder
UCC14240-Q1, UCC14241-Q1, UCC33421-Q1	Product Folder
AMC0386-Q1, AMC0381D-Q1	Product Folder
TCAN1043-Q1, ISO1042-Q1, ALM2403-Q1	Product Folder

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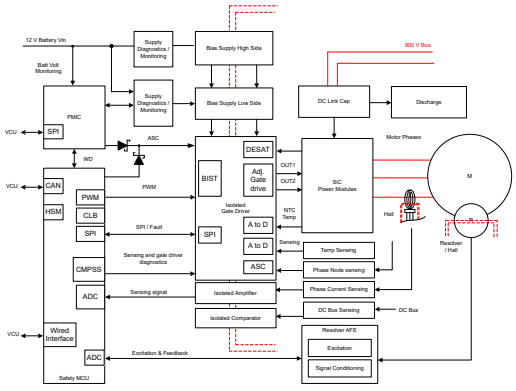
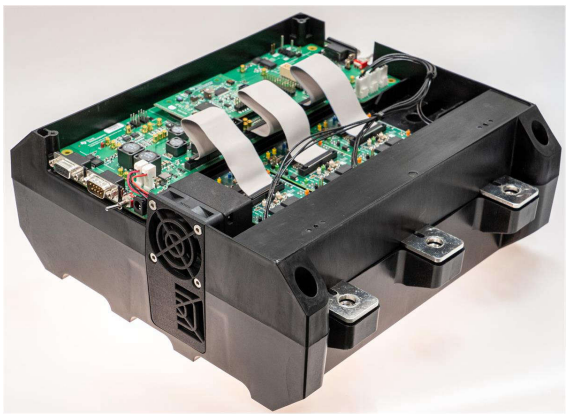
Features

- Real-time, variable gate drive strength features enable improved system efficiency by minimizing the SiC switching power losses and the accurate bias supply minimizes conductive losses
- Isolated gate drivers, bias supply modules, and highly integrated voltage sensing devices for the direct connection to the high-voltage source significantly reduce PCB area
- High-performance microcontroller (MCU) with three C29 real-time digital signal processor (DSP) cores enable motor control loop with < 2µs to help minimize torque ripple and to provide smooth speed and torque current profiles to the traction motor
- A system-on-module design with 3 × 120 high-speed, high-density connectors supports higher pin demands for MCU evaluation
- UCC5880-Q1 and F29H859TU-Q1 are Functional Safety-Compliant devices
- Enhanced system-reliability rated with reinforced capacitive isolation technology and early failure detection

Applications

- HEV and EV inverter and motor control





1 System Description

The traction inverter system is a core sub-system of an electric vehicle. The system not only contributes directly to the driver experience in terms of acceleration and speed, but also impacts the useful range of an electric vehicle. The TIDM-02014 reference design is a 800V, 300kW SiC based inverter reference design from TI and Wolfspeed that attempts to provide a starting point for designers and engineers to achieve a high-performance, high-efficiency traction inverter system.

This design demonstrates the traction inverter system technology that improves system efficiency by reducing the overshoot in available voltages with a high-performance isolated gate driver. The real-time variable drive strength of the gate driver enables inverter efficiency improvement. The isolated gate driver coupled with TI's isolated bias supply design significantly reduces the PCB size providing more than two times smaller PCB area, less than 4mm height and eliminating 30+ discrete components improving system power density. In addition, TI's high-control performance MCUs featuring tightly-integrated and remarkable real-time peripherals enable effective traction motor control even at speeds greater than 20,000RPM. A fast current loop implementation helps minimize motor torque ripple and provides smooth speed-torque profiles. The mechanical and thermal design of the system is provided by Wolfspeed.

WARNING

TI intends this reference design to be operated in a lab environment only and does not consider the reference design to be a finished product for general consumer use.

TI intends this reference design to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

High voltage! There are accessible high voltages present on the board. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

CAUTION

Do not leave the design powered when unattended.

1.1 Terminology

AFE	Analog Front End
NTC	Negative Temperature Coefficient Thermistors
LDO	Low-dropout regulator
UVLO	Undervoltage Lock Out
TVS	Transient Voltage Suppression
CMTI	Common Mode Transient Immunity
DESAT	Desaturation
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
PWM	Pulse Width Modulation
SiC	Silicon Carbide
MCU	Microcontroller Unit
BJT	Bipolar Junction Transistor
PCB	Printed Circuit Board
RPM	Revolutions Per Minute

1.2 Key System Specifications

Table 1-1 summarizes the key system specifications.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS (UNITS)	NOTES
P_{OUT}	300kW	Rated output power
V_{DSmax}	1200V	Maximum drain-source voltage
V_{DC}	800V	DC bus voltage recommended
I_{DC}	300A	DC bus current
f_{SWmax}	60kHz	Based on the gate driver bias power
I_L	360A	AC output RMS current
L_{PL}	5.3nH	Parasitic inductance including DC link capacitors and bus bar
C_{DC}	300µF	DC link capacitor
L_{DC}	3.5nH	DC bus capacitor ESL
Power Density	32kW/L	
Dimensions	28cm × 29cm × 11.5cm	
Weight	6.2kg	
Volume	9.3L	
Area	812cm^2	
P	5bar	Coolant operating pressure
ΔP	200mbar	Pressure drop

WARNING

External Connections: All external connections to the hardware must stay within the recommended operating conditions and intended usage for all hardware/components connected in the system.

- For information on the isolated gate driver, see the UCC5880-Q1 data sheet.
- For information on the microcontroller, see the F29H859TU-Q1 data sheet.
- For information on the bias supply, see UCC14240-Q1 data sheet.
- For information on the integrated modules, see the EAB450M12XM3 data sheet.
- For higher ambient temperatures, the DC-Link voltage and DC-Link current must be derated according to the included DC-Link capacitor ratings. See the 1100V / 100µF CX100µ1100d51KF6 data sheet provided by FTCAP GmbH (Mersen) for more detailed information.
- The included cold plate is a Wieland MicroCool CP3012-XP. To calculate the thermal resistance (°C/W) and pressure drop (bar) versus flow rate (liters/m), see the CP3012-XP data sheet provided by Wieland MicroCool Inc. for more detailed information.
- The included current sensor board uses the LEM LF 510-S. See the LF 510-S data sheet provided by LEM USA Inc. for more detailed information.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of this reference design with key TI components highlighted.

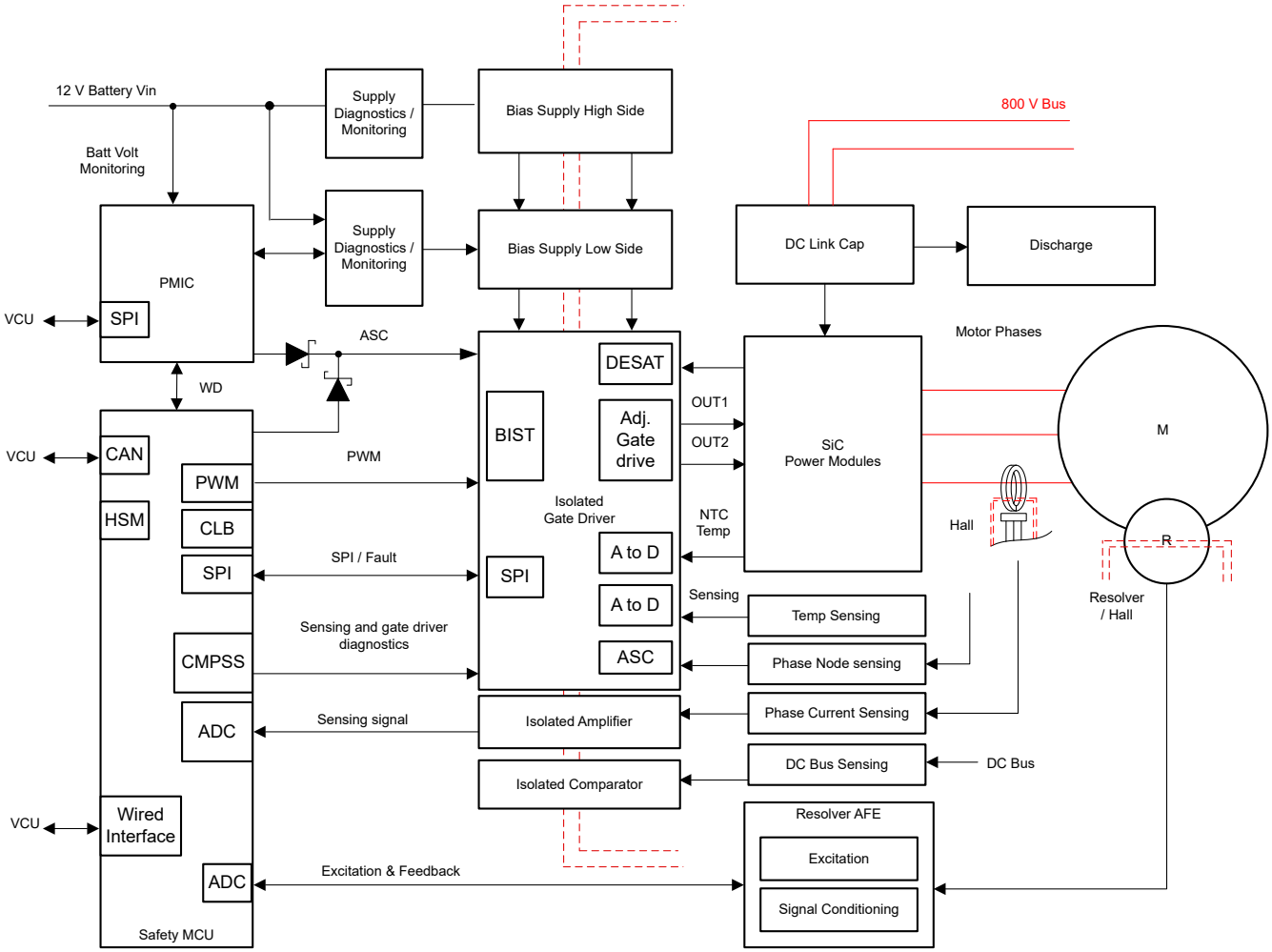


Figure 2-1. TIDM-02014 SiC Inverter System Block Diagram

2.2 Design Considerations

The primary goal of a traction system is to efficiently drive the traction motor, typically an induction or an interior permanent magnet synchronous motor (IPMSM), with a high control bandwidth. For this, the TIDM-02014 reference design features the C2000™ real-time control MCU for implementing a field-oriented control (FOC) scheme to drive the motor, achieving high real-time performance while supporting functional-safety requirements.

To achieve high-efficiency operation of the SiC inverter, the UCC5880-Q1 functional-safety-compliant isolated gate driver design is used. In addition to advanced configuration and protection features, the real-time variable gate driver strength feature of the UCC5880-Q1 enables efficiency optimization. The gate drive bias supply design features the UCC14240-Q1 bias supply device with integrated isolation transformer and post regulation. The tight regulation capability of the UCC14240-Q1 minimizes the device conduction loss during operation. With these designs, the gate-drive BOM and PCB footprint can be reduced by up to 30%.

The design philosophy for the power stage aims to maximize performance through high-ampacity, low-inductance design while minimizing the cost and complexity. To achieve this, the following five key parameters are considered:

1. Due to the high current density and relatively small size of the SiC modules, a high-performance thermal stackup is implemented to maximize heat transfer.
2. The stray inductance introduced by the bus-bar structure is minimized through the use of low-inductance, overlapping planar structures.
3. Low-inductance and high ripple rating capacitors are utilized to close the high-frequency switching loop effectively.
4. The gate driver high-speed protections and high-noise immunity features are leveraged for effective switching of the SiC modules and to provide maximum survivability under fault conditions.
5. The engineering of the power stage is aimed to minimize complexity for assembly, manufacturing, and the system cost. The inverter measures 279mm × 291mm × 115mm for a total volume of 9.3L and a power density of up to 32.25kW/L which is more than 2 × comparable Silicon (Si) based inverters.

2.3 Highlighted Products

This reference design features the following Texas Instruments devices.

2.3.1 UCC5880-Q1

The UCC5880-Q1 is a functional safety compliant isolated gate driver targeted for EV and HEV traction inverter applications. The flexibility of SPI programing of adjustable gate drive strength, blanking times, deglitches, thresholds, function enables, and fault handling allow for the UCC5880 to support a wide variety of IGBT or SiC power transistors that are used across all EV and HEV traction inverter applications. UCC5880-Q1 integrates all of the protection features required in most traction inverter applications. Additionally, the 20A gate drive capability eliminates the need for an external booster circuit, reducing overall design size. The integrated Miller clamp circuit holds the gate off during transient events and can be configured to use the internal 4A pulldown, or drive an external N-channel MOSFET. Advanced, internal capacitor-based isolation technology maximizes CMTI performance, while minimizing the radiated emissions.

2.3.2 F29H859TU-Q1

The F29H859TU-Q1 is a member of the C2000 real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics. The C29x CPU supports 32-bit and 64-bit floating- and fixed-point signal-processing running from on-chip flash or RAM. The C29x CPU is boosted by trigonometric math instructions, speeding up common algorithms key to real-time control systems. Many features are included to support a system-level ASIL-D functional safety design.

2.3.3 UCC14240-Q1

The UCC142140-Q1 integrates a high-efficiency, low-emissions isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, industrial motor drives, or other high-voltage DC/DC converters. This DC/DC converter provides greater than 1.5W of power across a 3000V_{RMS} basic isolation barrier. TI also has the newer reinforced isolation device, UCC14341-Q1 that takes in a 15V input and

similarly provides an adjustable isolated output up to 25V. For an optimized BOM, the UCC14341-Q1 can be directly connected to the 15V resolver rail that is commonly available in a traction inverter.

2.3.4 UCC33421-Q1

UCC33421-Q1 is an automotive qualified DC/DC power module with $5kV_{RMS}$ isolation rating designed to provide efficient, isolated power to isolated circuits that require a bias supply with a well-regulated output voltage. The module integrates a transformer and DC/DC controller with a proprietary architecture to provide 1.5W (typical) of isolated power with low EMI. UCC33421-Q1 integrates protection features for increased system robustness. The module also has an enable pin, synchronization capability, wide input (3.0V to 5.5V) options, and regulated 5V or 3.3V output options with headroom.

2.3.5 AMC0386-Q1

The AMC0386-Q1 is a precision, galvanically isolated delta-sigma (ΔΣ) modulator with a high-voltage, high-impedance input, and external clock. The input is designed to connect directly to a high-voltage signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference and is certified to provide reinforced isolation of up to $5kV_{RMS}$ (60s).

The AMC0386-Q1 is available with a ±600V and ±1000V linear input range. The resistive divider at the input of the AMC0386-Q1 scales down the voltage applied to the HVIN pin to a ±1V level. This signal is available on the SNSP pin, which is also the input of the analog signal chain.

The input stage of the AMC0386-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier. The output bitstream is synchronized to an external clock. Combined with a sinc3, OSR 256 filter, the device achieves 16 bits of resolution with an 84dB dynamic range and a 39kSPS data rate.

With an integrated resistive divider, low temperature drift and high lifetime stability, the AMC0386-Q1 achieves better than 1% voltage sensing accuracy including lifetime and temperature drift, without system-level calibration.

2.3.6 AMC0381D-Q1

The AMC0381D-Q1 is a precision, galvanically isolated amplifier with a high-voltage DC, high-impedance input, and fixed-gain, differential output. The input is designed to connect directly to a high-voltage signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference and is certified to provide reinforced isolation of up to $5kV_{RMS}$ (60s).

The AMC0381D-Q1 outputs a differential signal that is proportional to the input voltage. The differential output is insensitive to ground shifts and enables routing the output signal over long distances.

The AMC0381D-Q1 is available with a 600V and 1000V linear input range. The resistive divider at the input of the AMC0381D-Q1 scales down the voltage applied to the HVIN pin to a 1V level. This signal is available on the SNSP pin, which is also the input of the analog signal chain.

With an integrated resistive divider, low temperature drift and high lifetime stability, the AMC0381D-Q1 achieves better than 1% voltage sensing accuracy including lifetime and temperature drift, without system-level calibration.

2.3.7 TCAN1043-Q1

The TCAN1043-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification and the CiA 601-4 Signal Improvement Capability, CAN specification. The device reduces signal ringing at the dominant-to-recessive edge and enables higher throughput in complex network topologies. Signal improvement capability allows the applications to extract real benefit of CAN (flexible data rate) FD by operating at 2Mbps, or operating at 5Mbps or higher in large networks with multiple unterminated stubs.

The device also meets the timing specifications mandated by CiA 601-4; thus, has a much tighter bit-timing symmetry compared to regular CAN FD transceivers. This provides a larger timing window to sample the correct bit and enables error-free communication in large complex star networks where ringing and bit distortion are inherent.

2.3.8 ISO1042-Q1

The ISO1042-Q1 device is a galvanically-isolated controller area network (CAN) transceiver that meets the specifications of the ISO11898-2 (2016) standard. The ISO1042-Q1 device offers ±70V DC bus fault protection and ±30V common-mode voltage range. The device supports up to 5Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of $5000V_{RMS}$ and a working voltage of $1060V_{RMS}$. Electromagnetic compatibility has been significantly enhanced to enable system-level ESD, EFT, surge, and emissions compliance. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. While the ISO1042-Q1 device is available for both basic and reinforced isolation, this reference design uses the device featuring reinforced isolation.

2.3.9 ALM2403-Q1

The ALM2403-Q1 is a dual-power op amp with features and performance that make this device preferable for resolver-based applications. The high-gain bandwidth and slew rate of the device, along with a continuous high-output current-drive capability, make this device an excellent choice to provide the low distortion and differential high-amplitude excitation required for exciting the resolver primary coil. Current limiting and overtemperature detection enhance overall system robustness, especially when driving analog signals over wires that are susceptible to faults.

2.3.10 LM5158-Q1

The LM5158x-Q1 is a wide input range, non-synchronous boost converter that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies. The device can start up with a minimum of 3.2V. The device can operate with input supply voltage as low as 1.5V if the BIAS pin is greater than 3.2V. The internal VCC regulator also supports BIAS pin operation up to 60V (65V absolute maximum) for automotive load dump. The switching frequency is dynamically programmable from 100kHz to 2.2MHz with an external resistor. Switching at 2.2MHz minimizes AM band interference and allows for a small design size and fast transient response. The device provides an optional dual random spread spectrum to help reduce the EMI over a wide frequency span.

2.3.11 LM74202-Q1

LM74202-Q1 is a diode with integrated back-to-back FETs and enhanced built-in protection circuitry. LM74202-Q1 provides robust protection for all systems and applications powered from 4.2V to 40V. The device integrates reverse battery input, reverse current, overvoltage, undervoltage, overcurrent, and short circuit protection. The precision overcurrent limit (±5% at 1A) helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.1A and 2.23A with an external resistor. The device monitors the bus voltage for brownout and overvoltage protection, asserting the FLTb pin to notify downstream systems.

2.4 System Design Theory

2.4.1 Microcontrollers

The microcontroller, as the primary control unit, is at the heart of this reference design. The TIDM-02014 design supports the F29H859TU-Q1 device from TI's C2000™ family, and the F29H85X-SOM-EVM plugs directly into the TIDM-02014 control board.

2.4.1.1 Microcontroller – C2000™

F29H85X-SOM-EVM is an evaluation and development board for TI C2000™ MCU series of F29H85x and F29P58x devices. This system-on-module (SOM) design is an excellent choice for initial evaluation and prototyping. The SOM architecture of the EVM includes all the power, reset, and clock logic needed to operate the F29H85x device. This 360-pin SOM is intended to provide a well-filtered robust design that is capable of working in most environments. See also the *F29H85X controlSOM Evaluation Board* EVM user's guide. For evaluation of F29H85X-SOM-EVM, the XDS110ISO-EVM debug probe is required and can be purchased separately. Both of these EVMs are required to use the TIDM-02014 reference design.

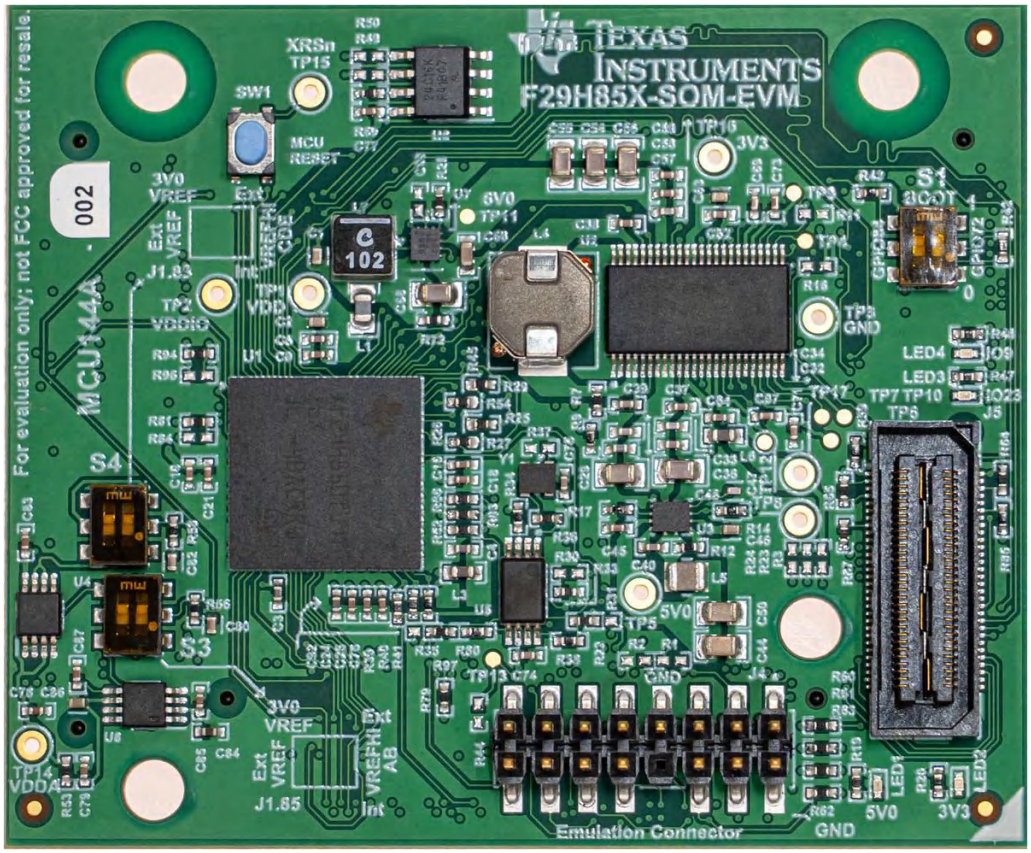


Figure 2-2. F29H85X-SOM-EVM Front

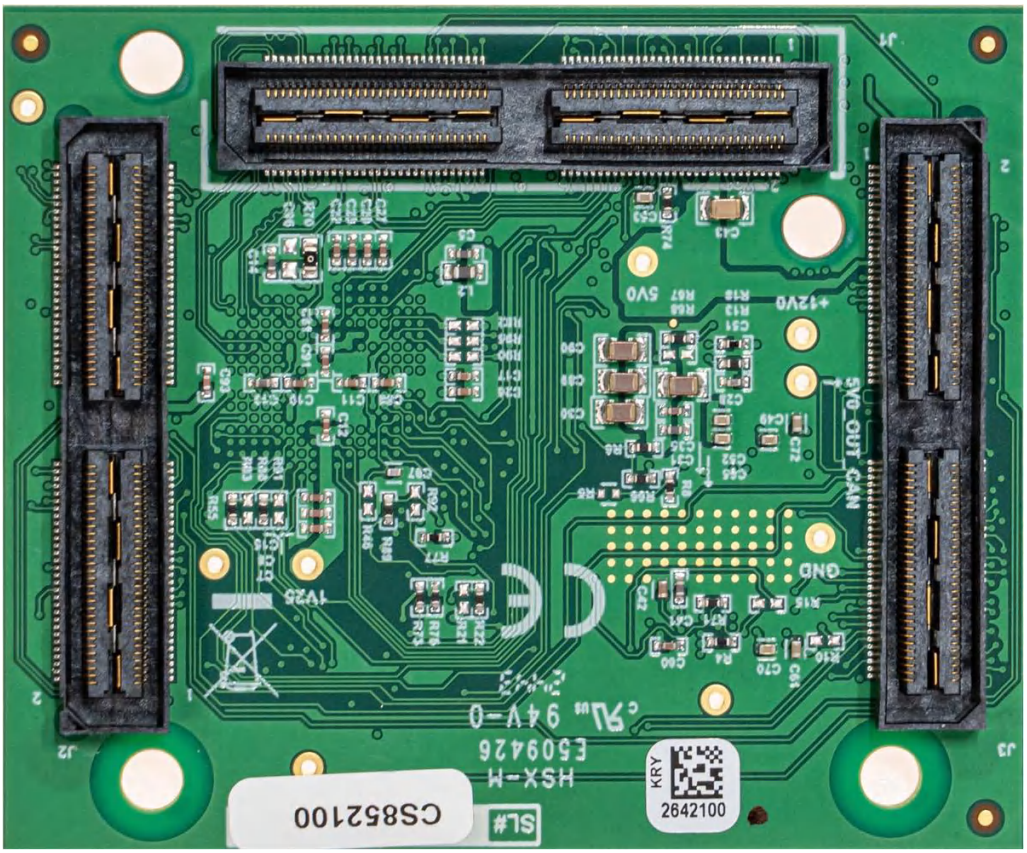


Figure 2-3. F29H85X-SOM-EVM Back

2.4.2 Isolated Bias Supply

The schematic in Figure 2-4 shows the UCC14240-Q1 DC/DC converter module operates from a single 24V (P24V) input and is configured to provide dual, +15V (VCC2), –4V (VEE2), 3kV$_{RMS}$ isolated, bias supply voltage rails to the UCC5880-Q1 isolated gate driver. VCC2 and VEE2 are programmed by resistor dividers R13, R19 and R15, R20 and are tightly regulated to within ±1.3%, providing +15V and –4V as recommended by the Wolfspeed XM3, SiC half-bridge module. Start-up is initiated when the digital host first provides the enable signal (EN_PS) required to pull the UCC14240-Q1 ENA pin to an active high state, allowing VCC2 and VEE2 to soft-start. The UCC14240-Q1 then provides an active low, LVTTL compatible, power good signal (N_PG), notifying the host that P24V is above the 21V, UVLO turn-on threshold and VCC2 and VEE2 are above 90% of the set regulation target values (VCC2 > 13.5V and VEE2 > 3.6V, respectively). This connection between the host and UCC14240-Q1 makes sure the UCC5880-Q1, gate driver has sufficient bias voltage present to safely allow inverter switching to begin.

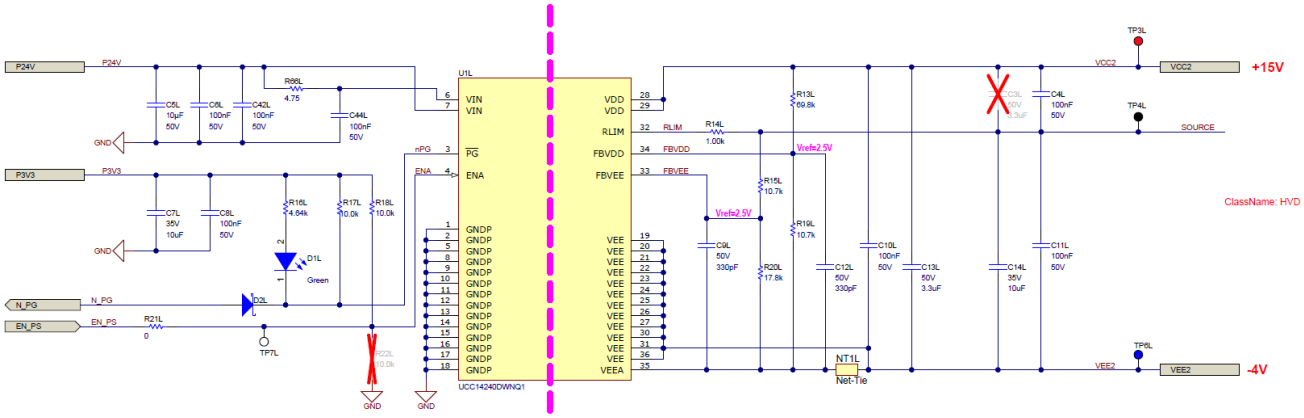


Figure 2-4. UCC14240-Q1 Bias Supply Schematic

2.4.3 Power Tree

2.4.3.1 Introduction

The control board contains a complete power supply tree to run all features on the system. The power tree provides power to:

- All onboard peripherals
- Gate-driver boards
- MCU SOM evaluation board
- Internal and external sensors

The external off-line DC adapter is assumed to be used with the board. Adapter must be specified as 12VDC nominal (8VDC to 16VDC) 3.3ADC.

Power is connected through the barrel jack connector with 2mm center pin J100 (see the PJ-037AH data sheet).

2.4.3.2 Power Tree Block Diagram

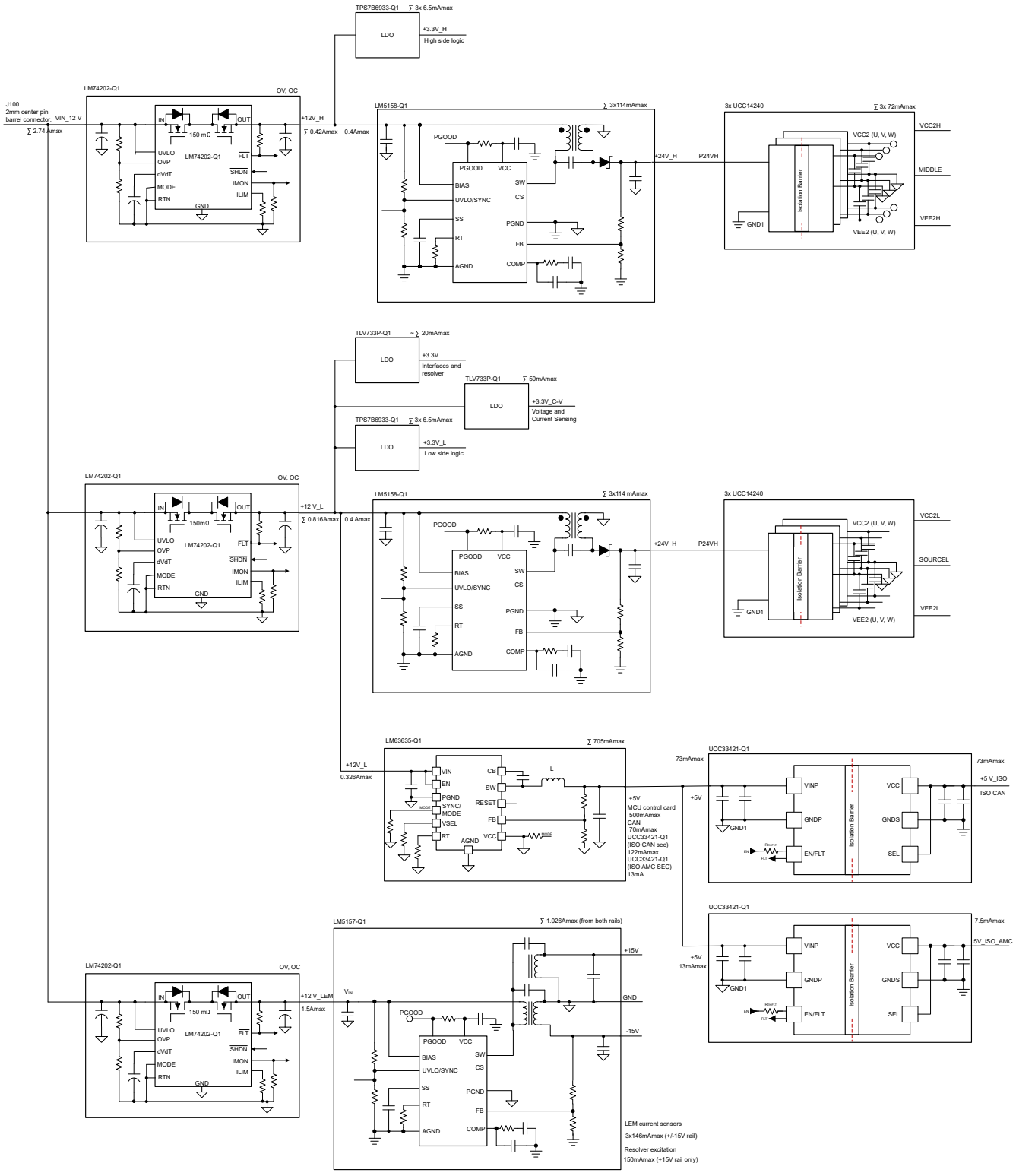


Figure 2-5. Power Tree Block Diagram

2.4.3.3 12V Distribution and Control

The 12V domain is distributed into three separate rails.

Table 2-1. 12V Distribution and Control

RAIL	REGULATOR	LOAD	MAXIMUM CURRENT
+12V_H	LM5158-Q1 based SEPIC	High-side 24V domain	0.4A
	TPS7B6933-Q1 LDO	High-side 3.3V logic	0.02A
+12V_L	LM5158-Q1 based SEPIC	Low-side 24V domain	0.4A
	TPS7B6933-Q1 LDO	Low-side 3.3V logic	0.02A
	TLV733P-Q1 LDO	High-voltage sensing and current sensing signal conditioning	0.05A
	TLV733P-Q1 LDO	Digital interfaces and resolver front-end	0.02A
	LMR63635-Q1 step-down	5V supply domain	0.81A
	UCC33421-Q1 isolated DC-DC	Isolated CAN	0.123A
	UCC33421-Q1 isolated DC-DC	Isolated voltage sensing	0.013A
+12V_LEM	LM5157-Q1 based SEPIC	LEM current sensor modules	1.5A
		Resolver excitation	

These rails are separated and protected with LM74202-Q1 ideal diodes.

The primary function of LM74202-1 is to provide overvoltage (OV) and short circuit protection. For debugging or experimental purposes, the MCU can control the LM74202-Q1 with a logic signal (Power_EN_LoadSW) when powered from a different power source, for example, through the programming USB cable.

2.4.3.4 Gate Drive Supply

Low-voltage domains of the isolated gate driver units (GDU) (UCC5880-Q1) are powered by the TPS7B6933-Q1 LDO. The high-voltage domain of the GDU is powered using UCC14240-Q1 isolated DC/DC modules. The modules selected are compact and easy to use.

The voltage generated by UCC14240-Q1 is set to total 19V (V_{CC2} = 15V and V_{EE2} = –4V). The high-voltage negative pole is a virtual ground for UCC14240-Q1.

The maximum power consumption on the high-voltage side of each UCC14240-Q1 DC/DC module can be estimated as a worst-case switching condition for f_{SWmax} = 30kHz and C_L = 100nF:

$$P2 = f_{SWmax}(V_{CC2} - V_{EE2})^2 C_L + \left(V_{CC2} - V_{EE2}\right) I_{CCq2} \quad (1)$$

The secondary quiescent current of UCC5880-Q1 can be found in the data sheet as I_{CC2q} = 15mA. Resulting secondary power consumption is then calculated as 1.368W. Assuming 50% efficiency this corresponds to 114mA of supply current on 24V input side of each UCC14240-Q1.

These UCC14240-Q1 DC/DC modules require pre-regulated 24V. The 24V pre-regulator is implemented as LM5158-Q1 based SEPIC with coupled inductors. The SEPIC topology supports appropriate input voltage range. The LM5157 and LM5158-Q1 converters are used in this case because of the versatility of the devices and – due to random spread spectrum – for the noise properties.

The component values for the power supply design are calculated using the *LM5158 Quick Start Calculator tool for SEPIC*. Table 2-2 shows the main input parameters of the supply.

Table 2-2. SEPIC Converter Design Parameters for Gate Drive Power Supply

PARAMETER	VALUE			
	MIN	NOM	MAX	UNIT
V_{INPUT}	8	12	16	V
f_{SW}		435		kHz
V_{LOAD}		24		V
I_{LOAD}		0.35		A

Each 24V SEPIC powers three UCC14240-Q1 devices; therefore, I_{LOAD} = 0.35A is listed (see Figure 2-5).

2.4.3.5 5V Supply Domain

The 5V power supply features the LM63635-Q1 step-down voltage converter. The power supply mainly powers the MCU SOM evaluation board, non-isolated CAN, and provides the power for isolated DC-DC converters which power isolated CAN and isolated voltage sensing.

LM63625-Q1 has a maximum output current of 3.25A. For the load of 705mA and efficiency of 90%, the device draws about 326mA from the 12V power rail. Figure 2-5 shows a realistic estimate of the load current in all branches.

The MCU SOM evaluation board is expected to use more power than other components. Therefore, the power budget calculations are based on estimated power consumption.

This evaluation board consumes in average 2.5W with all unused peripherals disabled. The 5V power supply domain then offers sufficient margin to support various use cases and operation profiles.

The CAN interface consumes 70mA and the isolated CAN 122mA, totaling 192mA from the 5V rail. The isolated CAN interface is powered using the UCC33421-Q1 DC/DC power module. This module provides a maximum 1.5kW of power at 5V and 5kV_{RMS} isolation. At 73mA loading on the isolated side using the ISOCAN1042-Q1 device, 122mA is expected on the primary side assuming 60% efficiency.

The secondary side of AMC0386-Q1 is powered using another UCC33421-Q1 device. For the consumption of 7.5mA with 60% efficiency, 0.013A is expected on the primary side of the DC-DC converter.

2.4.3.6 Current and Position Sensing Power

The current and position sensing (resolver) is powered from the +12V_LEM power rail. The LEM LF 510-S current transducers require symmetrical power supply of positive and negative 15V.

The current draw for one current measurement channel from ±15V power supply is defined as (for details see the LEM LF 510-S data sheet):

$$I_{CCLEM}(mA) = 44mA + 0.2\ I_{MEAS}(A) \quad (2)$$

where

- 44mA is the quiescent current of the transducer
- I_{MEAS} is the measured current

Peak measured current determines the maximum power draw. In this case, assume a maximum 509A of peak measured current (see note in the schematic diagram). This corresponds to 146mA current consumption.

A +15V rail powers the resolver excitation amplifier. The current consumption naturally depends on the resolver type. The estimated current budget for this function is 150mA from the +15V rail.

A dual-output SEPIC topology is selected to provide symmetrical 15V supply featuring the LM5157-Q1. Similar to LM5158-Q1, this wide V_{IN} converter has random spread spectrum for better noise performance. LM5157-Q1 simultaneously drives two independent SEPIC stages connected in series. To be able to use the LM5157 and LM5158 calculation spreadsheet for component calculation, the total I_{LOAD} must be determined. If an assumption is made that the V_{LOAD} = 15V, multiply the current transducer consumption by a factor of two. This represents two driven branches (creating the ±15V). I_{LOAD} can be calculated as:

$$I_{LOAD} = 150mA + 2 \times 3 \times 146mA = 1026mA \quad (3)$$

where

- The factor of three represents the three channels connected to the power supply
- 150mA represents the power budget for resolver excitation

The parameters in Table 2-3 are used for component calculation in the calculation spreadsheet.

Table 2-3. SEPIC Converter Design Parameters for Current and Position Sensing Circuits

PARAMETER	VALUE			
	MIN	NOM	MAX	UNIT
V_{INPUT}	8	12	16	V
f_{SW}		435		kHz
V_{LOAD}		15		V
I_{LOAD}		0.35		A

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

This section details the hardware and explains the different sections on the board and how to set them up for the test outlined in this design guide.

3.1.1 Hardware Board Overview

Figure 3-1 shows the assembled inverter system with the functional sections highlighted. Additional hardware details of the sections are provided.

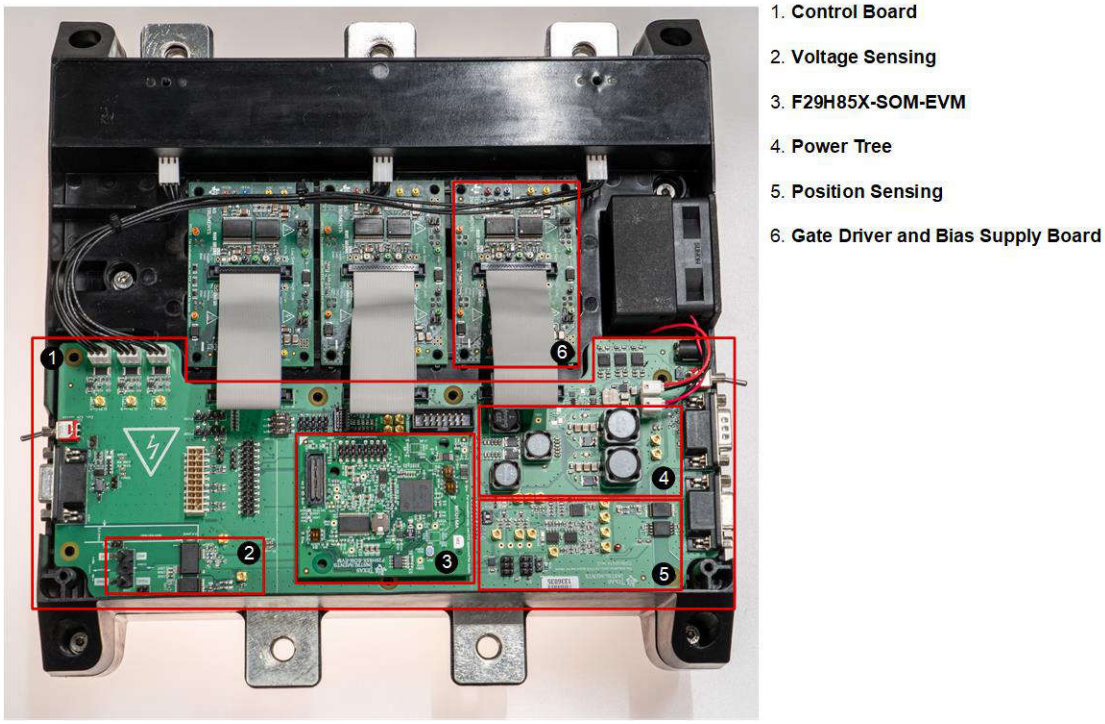


Figure 3-1. Functional Sections of TIDM-02014 Inverter System

3.1.1.1 Control Board

The control board accepts the MCU SOM evaluation board, provides auxiliary power, provides interfaces for position, voltage and current sensing, and communication. The control board also interfaces to the gate drive and bias supply board, providing power to the PWM and SPI connection between MCU and gate drivers. Since the control board accepts SOM evaluation boards, the same board can be used to test the TIDM-02014 system with TI's F29H859TU-Q1 MCU.

3.1.1.2 MCU SOM Evaluation Board – C2000™

Figure 3-2 shows the components and the corresponding functions for the F29 SOM evaluation board.

The F29H85X controlSOM Evaluation Board user's guide provides further details on configuring and debugging the board.

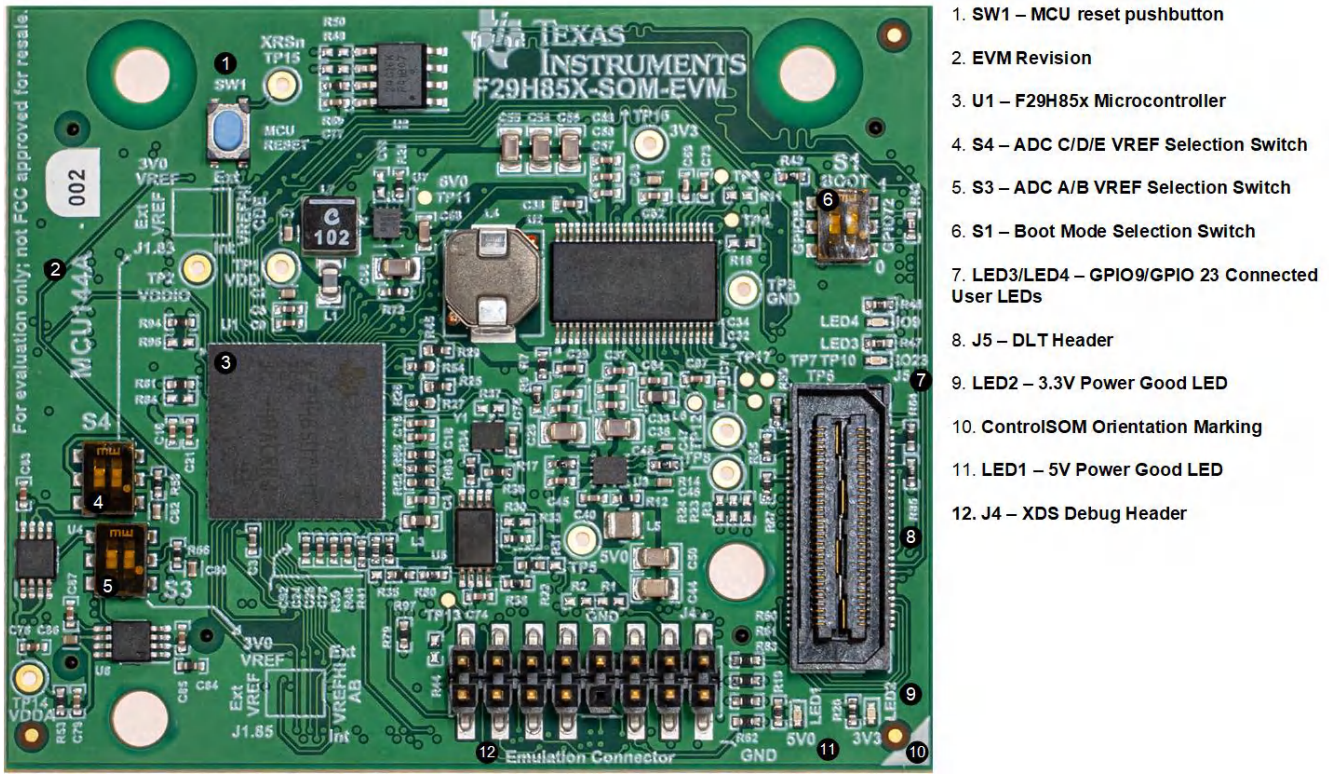


Figure 3-2. Key Components on the SOM Evaluation Board

3.1.1.3 Gate Driver and Bias Supply Board

Figure 3-3 shows the components and accessible test points on the gate drive and bias supply board. Table 3-1 describes the pinouts of the J9 connector.

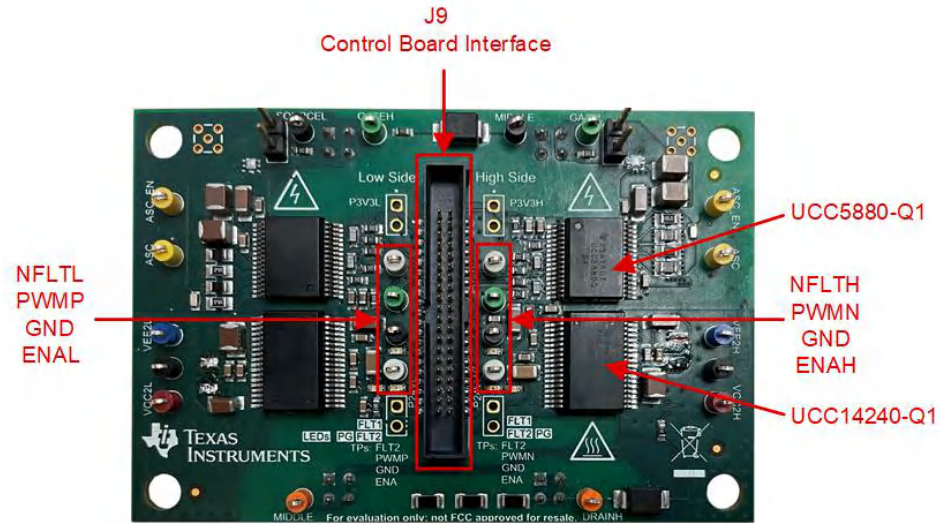


Figure 3-3. Gate Driver and Bias Supply Board

Table 3-1. Connector J9 Pinout

PIN	SIGNAL	PIN	SIGNAL
1	P3V3H_T	2	GND
3	PV3VL_T	4	GND
5	SDIL_T	6	NCSH_T
7	NCSL_T	8	SDOH_T
9	GND	10	CLK
11	GND	12	PWMN
13	GND	14	PWMP
15	GND	16	GND
17	ASCL_T	18	N_FLT2H_T
19	GND	20	N_FLT1H_T
21	GD2L_T	22	GD0H_T
23	GD1L_T	24	GD1H_T
25	GD0L_T	26	GD2H_T
27	GND	28	ASC_EN
29	N_FLT1L_T	30	ASCH_T
31	N_FLT2L_T	32	GND
33	EN_PSL_T	34	N_PGH_T
35	N_PGL_T	36	EN_PSH_T
37	P24VH_T	38	GND
39	P24VL_T	40	GND

3.1.1.4 DC Bus Voltage Sense

A voltage sense connection for the DC bus voltage is provided by a board-to-board connector between the discharge PCB and the connector on the bottom side of the controller. This allows the controller application to monitor the DC bus voltage. The full bus voltage is present at connector J8 on the controller and connected directly to the AMC0386-Q1 or AMC0381D-Q1 device. These devices have an integrated high-voltage resistor ladder and at the output provide the modulated or differential signal that goes to the MCU.

3.1.1.5 SiC Power Module

3.1.1.5.1 XM3 SiC Power Module

The XM3 module from Wolfspeed is designed to simplify SiC power modules by creating an all new package that is both high-performance and easy to use. Wolfspeed has developed a high-performance next generation module that is easy to use and is optimized in a manner that is intended to achieve the maximum performance out of all sizes of commercially available 650V to 1700V Wolfspeed C3M™ SiC MOSFETs. The module offers the capability to carry high currents (300A to > 600A) in a small footprint (53mm × 80mm) with a terminal arrangement that allows for straightforward bussing and interconnection. A low-inductance, evenly matched layout results in high-quality switching events, minimizing oscillations both internal and external to the module. The module has a stray inductance of only 6.7nH. When coupled with the low-inductance bussing and capacitors in this reference design, a total loop inductance of 12nH is obtained, which is lower than the internal stray inductance of many standard power module packages. The XM3 platform offers 40% of the volume and 45% of the footprint of a package that is typically used in the industry (as shown in Figure 3-4); therefore, offering a more compact power module for high-power density systems. Table 3-2 lists which variant of the XM3 module is included with each three-phase inverter reference design.

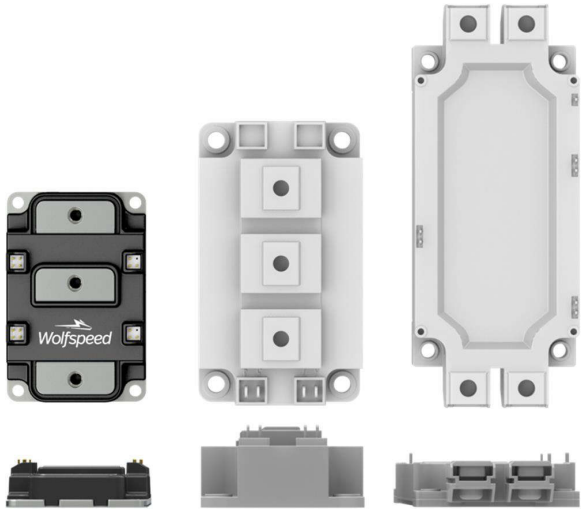


Figure 3-4. Size Comparison Between XM3 (Left), 62mm (Center), and EconoDUAL® (Right)

Table 3-2. XM3 Power Module Part Number Reference

REFERENCE DESIGN	MODULE PART NUMBER
CRD300DA12E-XM3	C4B450M12XM3
CRD250DA12E-XM3	C4B425M12XM3
CRD200DA12E-XM3	C4B400M12XM3

3.1.1.5.2 Module Power Terminals

The current loops in the XM3 power module are designed such that the loops are wide, low profile, and evenly distributed between the devices so that each has equivalent impedances across a switch position. Figure 3-5 shows that the power terminals are vertically offset in such a manner that the bus bars between the DC link capacitors and the module can be laminated all the way up to the module without requiring bends, coining, standoffs, or complex isolation. Figure 3-6 shows a representative 3-phase-inverter bussing. Ultimately this achieves a low-inductance throughout the entire power loop from the DC link capacitors to the SiC devices. A XM3 module without devices is connected to a Keysight E4990A Impedance Analyzer to extract the parasitic inductance of the package. The power loop inductance from V+ to V– is 6.7nH measured at 10MHz.

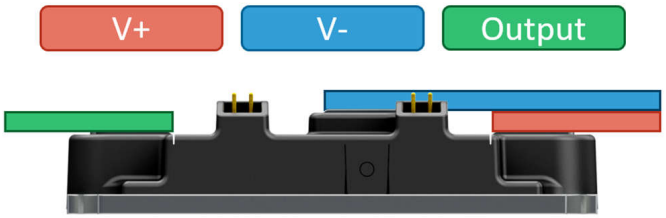


Figure 3-5. Side View of XM3 Module Showing Non-planar Power Leads

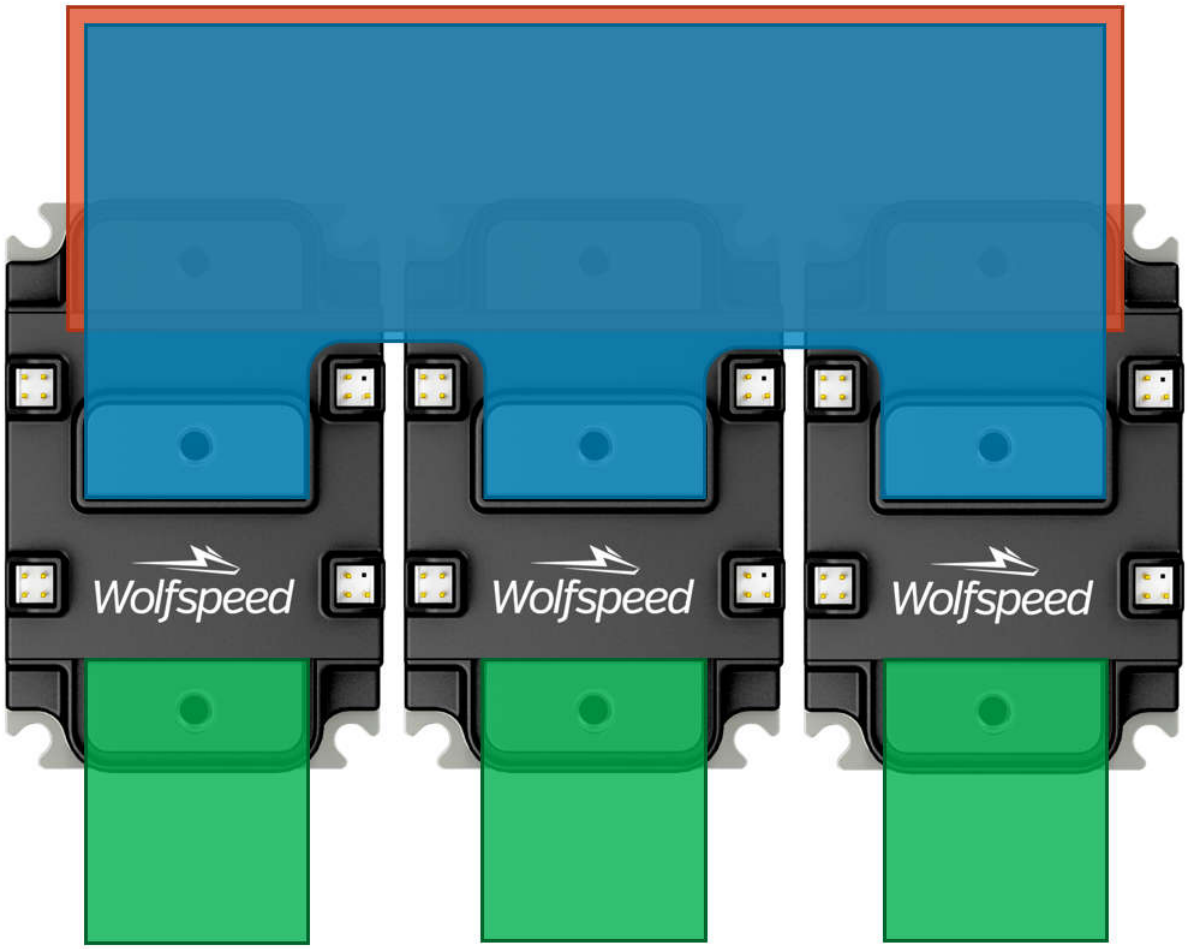


Figure 3-6. Illustration Showing Three-Phase Bussing Layout

3.1.1.5.3 Module Signal Terminals

Figure 3-7 shows the signal pins on the XM3 module consisting of four sets of male header pins grouped by function located on the left and right edge of the module. Along the left side are the gate pins for both the high-side and low-side switch positions and the associated source-Kelvin pins. In the upper right position are the *Desat / Overcurrent* pins which are internally connected to the V+ power terminal to provide a connection point for high-side gate driver protection circuitry to measure V_{DS}. In the lower right position are the pins for the internal negative temperature coefficient (NTC) temperature sensor. The NTC is located on an electrically isolated substrate pad in close proximity to the lower switch power devices and can need additional galvanic isolation according to application requirements. With the UCC5880-Q1 gate driver, the NTC measurement signal is isolated up to 5.7kV. The signal connectors on the right side both have one pin not populated so that the gate driver can be keyed to prevent improper installation.

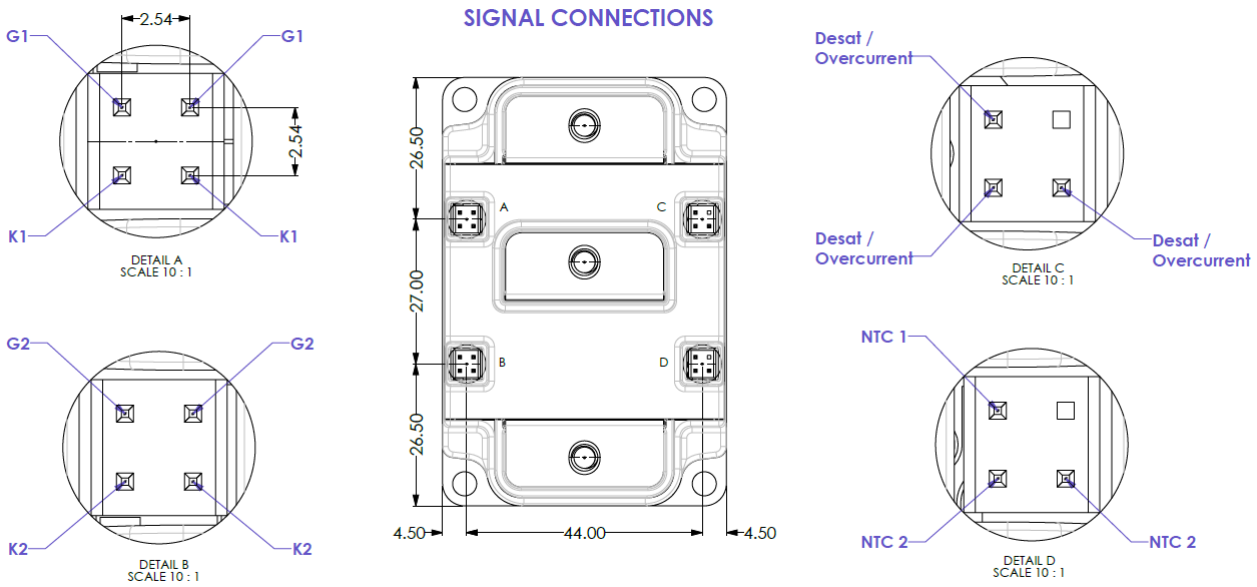


Figure 3-7. XM3 Module Signal Terminal Pinout

3.1.1.5.4 Integrated NTC Temperature Sensor

The NTC temperature sensor built into the power module is sensed and fed back to the controller through an isolated digital signal. This signal is a 50% duty cycle square wave with varying frequency. The temperature sensor is positioned as close as possible to the power devices while remaining electrically isolated from them and therefore provides an approximate baseplate temperature. The temperature reported by the NTC differs largely from the junction temperature of the SiC MOSFETs and must not be used as an accurate junction temperature measurement. There are two ways to measure the NTC feedback signal for the three XM3 modules with the controller. The first method is using the enhanced capture (eCAP) peripheral to digitally measure the frequency of the signal coming directly from the differential receivers. Figure 3-8 and Table 3-3 give the relationship of the NTC signal frequency to the NTC temperature. For the second method, the frequency signal is filtered and converted into an analog signal which can be measured by ADC on the controller. The analog voltage measures 0.38V when the frequency is 4.6kHz and 2.5V when the frequency is 30.1kHz.

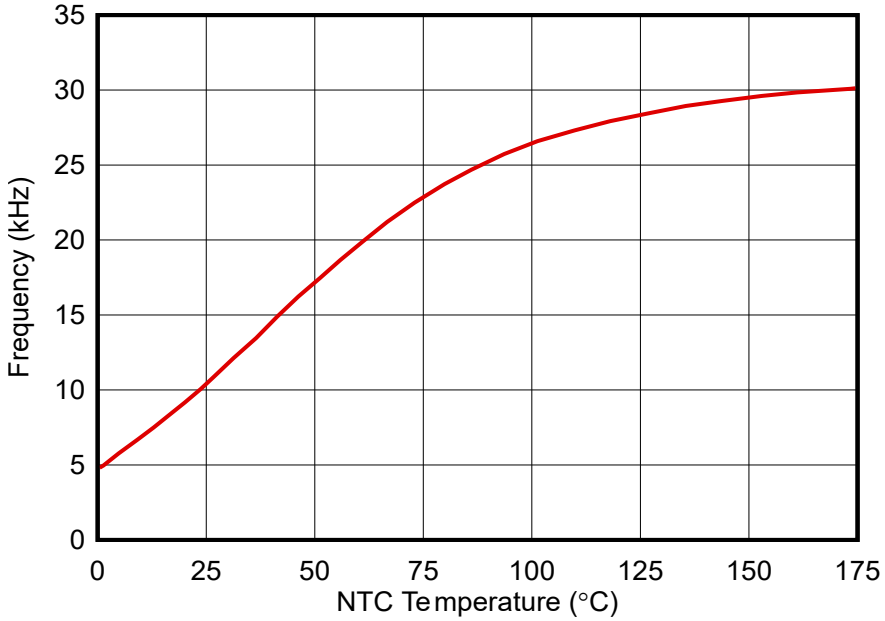


Figure 3-8. NTC Temperature vs Signal Frequency

Table 3-3. NTC Temperature, Resistance, and Frequency Correlation

NTC TEMPERATURE (°C)	NTC RESISTANCE (Ω)	FREQUENCY OUTPUT (kHz)
0	13491	4.6
25	4700	10.3
50	1928	17.1
75	898	22.8
100	464	26.4
125	260	28.3
150	156	29.5
175	99	30.1

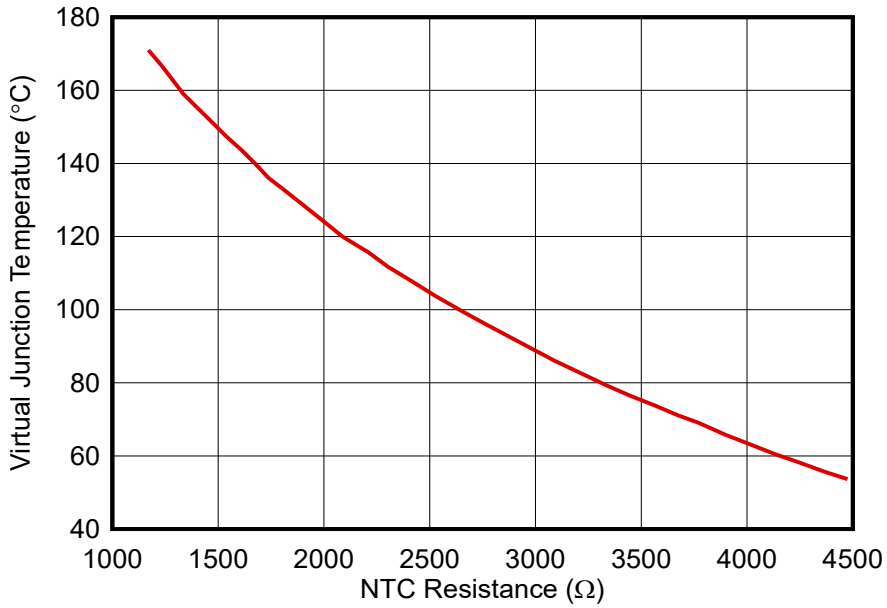


Figure 3-9. CAB450M12XM3 Virtual-Junction Temperature (T_{VJ}) vs NTC Resistance With 25°C Coolant.

Figure 3-9 shows the mapping between the NTC resistance (R_{NTC} in Ohms) of the CAB450M12XM3 module and the virtual junction temperature (T_{VJ}). Use Equation 4 to calculate the virtual junction temperature.

$$T_{VJ} = -87.12 \times \ln(R_{NTC}) + 786.14 \quad (4)$$

One additional temperature sensor is installed on the controller PCB to provide a measurement of the ambient temperature inside the reference design case. This temperature sensor consists of a 10kΩ NTC surface mount thermistor and a 10kΩ fixed resistor forming a voltage divider. As the temperature increases so does the voltage at the midpoint of the voltage divider. This voltage is low-pass filtered to remove any high-frequency noise from the slowly changing temperature. The conversion between this voltage signal, V_T, and the temperature of the thermistor (in Kelvin) is calculated with Equation 5.

$$T = \left(\frac{\ln(3.3/V_T - 1)}{3900} + \frac{1}{298.15}\right)^{-1} \quad (5)$$

3.1.1.6 Laminated Busing and DC Bus Capacitors

The vertical offset of the power terminals of the module allows the bus-bar design to remain simple and cost-effective while maintaining a low power-loop inductance. A low-inductance bus bar is utilized to interconnect the DC-link capacitors (located under the bus bar) to the power modules. Again, the offset power module terminals enable the bus-bar assembly to have no bends or standoffs, which reduces cost and maximizes overlap. The capacitors are affixed as close as possible to minimize the total loop area. As Figure 3-10 shows, the bus bars consist of one flat plate connecting V+ terminals of the modules and capacitors followed by an insulator and

then a second flat plate connecting to the raised V– terminals of the modules and the capacitors with coining or spacer for the capacitor terminal. The structure is simple enough that the product can be made with minimal fabrication which reduces the cost and lead-time.

Figure 3-10. Cross-Sectional View of Laminated Bus-Bar Structure Showing Power Loop

Optimized orientation for the capacitors is determined by measuring the inductance of three prototypes of the bussing geometry fabricated as two-layer PCBs. Between each prototype the capacitor terminals are rotated vertically, horizontally, and diagonally at 45 degrees. The horizontal orientation offered the lowest relative inductance with capacitors installed and is the orientation used for the laminated bussing.

The film capacitors serve two purposes: to close the high-frequency power loop and to provide local energy storage. To fulfill these roles the bus capacitors must be both low-inductance and have a high ripple current rating. The reference design features three Fischer & Tausche® CX100µ1100d51KF6 capacitors each rated to 100A ripple current and 100µF. A 1100V voltage rating is sufficient for operating on a 900V maximum DC bus with allowance for peak overshoots from aggressive switching rates. Each capacitor has an equivalent series inductance (ESL) of 10.5nH. Having three of these capacitors reduces the total ESL for the capacitor bank to 3.5nH which with a total measured inductance for the DC bussing and capacitors of 5.3nH means the bussing contributes 1.8nH. The 5.3nH inductance of the DC bus plus 6.7nH power loop inductance for the XM3 module results in a combined power loop inductance of 12nH which is lower than the stray inductance of many standard footprint modules alone.

3.1.1.6.1 Discharge PCB

Due to the large amount of energy storage possible in the DC bus capacitors, discharge resistors are required to bring the DC bus to a safe voltage in a reasonable amount of time. The discharge PCB mounts to the V+ and V– terminals of one of the DC bus capacitors and has high-power surface mount resistors in addition to a board-to-board connector for the DC bus voltage sense measurement on the controller. The resistors are sized to discharge the bus from a nominal voltage of 800V to less than 50V in under a minute. This requires the resistor network to dissipate a maximum of 9.4W across nine resistors with a working voltage rating of 1500V.

3.2 Test Results

This section presents results of tests performed on the system components. The results for the gate drive and bias supply are presented followed by the full inverter system.

3.2.1 Isolated Bias Supply

Figure 3-11 shows the validated UCC14240-Q1 start-up behavior.

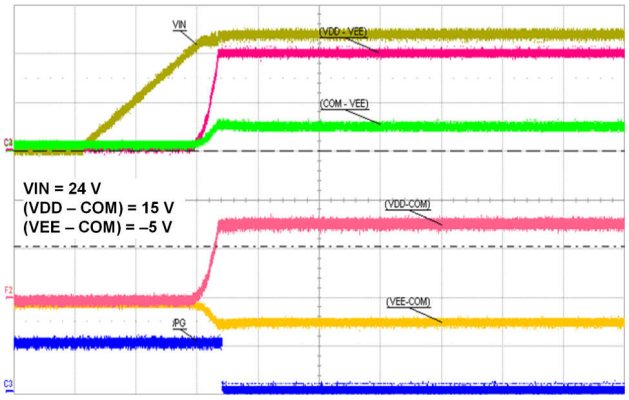


Figure 3-11. UCC14240-Q1 Power-Up Sequence

The load regulation test is performed to verify the stability of UCC14240-Q1. The electronic load is connected between VEE and VCC, with the load steps from 0mA to 80mA. Table 3-4 shows the measured output voltage.

Table 3-4. UCC14240-Q1 Load Regulation

LOAD (mA)	V_{OUT} (V)	POWER (W)
10	18.853	0.188
20	18.848	0.377
30	18.84	0.565
40	18.834	0.753
50	18.83	0.941
60	18.828	1.13
69	18.825	1.3
80	18.819	1.505

The nominal voltage value is 19V. Equation 6 is the equation for the load regulation.

$$\text{Load regulation} = \left(\frac{V_{max} - V_{min}}{V_{nom}}\right) \times 100 = 0.18\% \quad (6)$$

3.2.2 Isolated Gate Driver

Double pulse test under 800V is carried out to evaluate the switching behavior for the different adjustable gate drive strengths. The following results show the difference between weak drive (5A) and strong drive (15A). The waveforms of the gate-source voltage, drain-source voltage and drain currents are shown in the following figures. The turn off energy is measured at the end of the first pulse, while the turn on energy is measured at the beginning of the second pulse. Table 3-5 shows the measurement results.

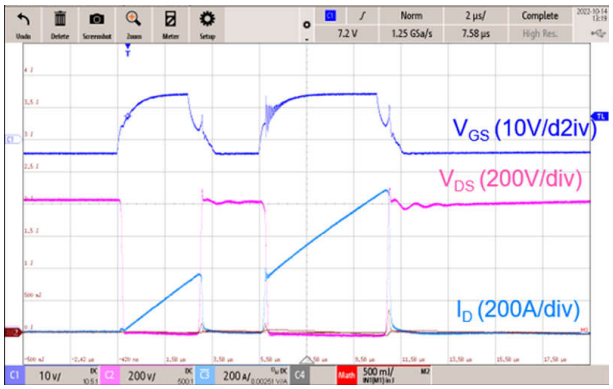


Figure 3-12. Double Pulse Test With Weak Drive Strength

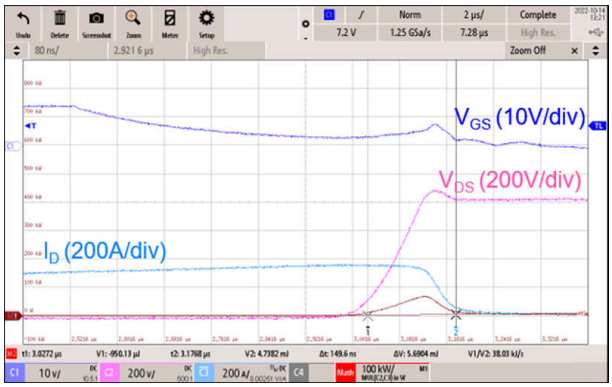


Figure 3-13. Turn-off Waveforms With Weak Drive Strength

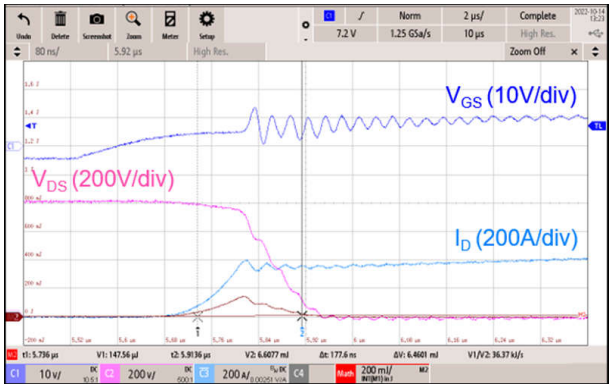


Figure 3-14. Turn-on Waveforms With Weak Drive Strength

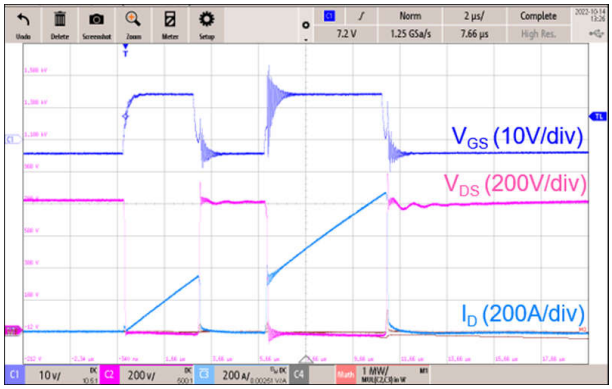


Figure 3-15. Double Pulse Test With Strong Drive Strength

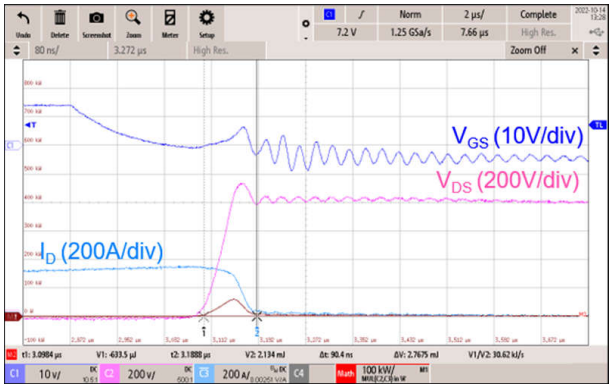


Figure 3-16. Turn-off Waveforms With Strong Drive Strength

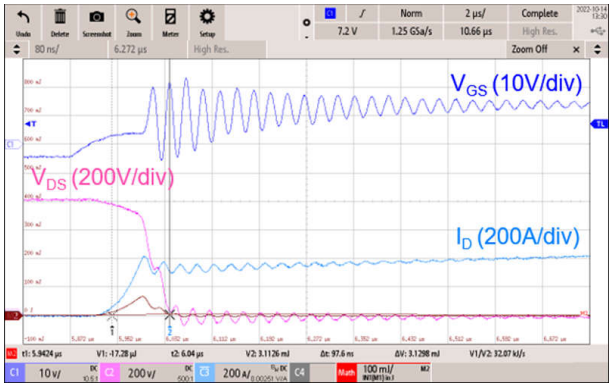


Figure 3-17. Turn-on Waveforms With Strong Drive Strength

Table 3-5. Switching Energy Measurements

	WEAK DRIVE (5A)	STRONG DRIVE (15A)
Turn-off energy	5.65mJ	2.77mJ
Turn-on energy	6.46mJ	3.13mJ

3.2.3 Inverter System

The traction inverter system is tested at the rated voltage and power levels with an inductive load. The drive strength of the UCC5880-Q1 gate driver is varied to study the impact on the efficiency of the system. The the following figures show the scope plots for the drain-source voltages (V_{ds}) and phase currents of the SiC MOSFETs. Figure 3-18 and Figure 3-19 show the test waveforms with weak gate drive strengths. Figure 3-20 and Figure 3-21 show the test waveforms with strong gate drive strengths. Table 3-6 shows the test conditions and obtained power results. In an inductive load test, the load power recirculates. Therefore, external DC supply only supplies the system losses, which is quantified as P_{loss}. Observe that with a higher drive strength, the system losses also reduce. This is primarily due to the reduction in switching losses. However, as Figure 3-20 shows, higher drive strength also increases the drain-source voltage overshoot on the SiC MOSFETs. The variable drive strength feature of the UCC5880-Q1 gate driver allows the real-time optimization of system losses.

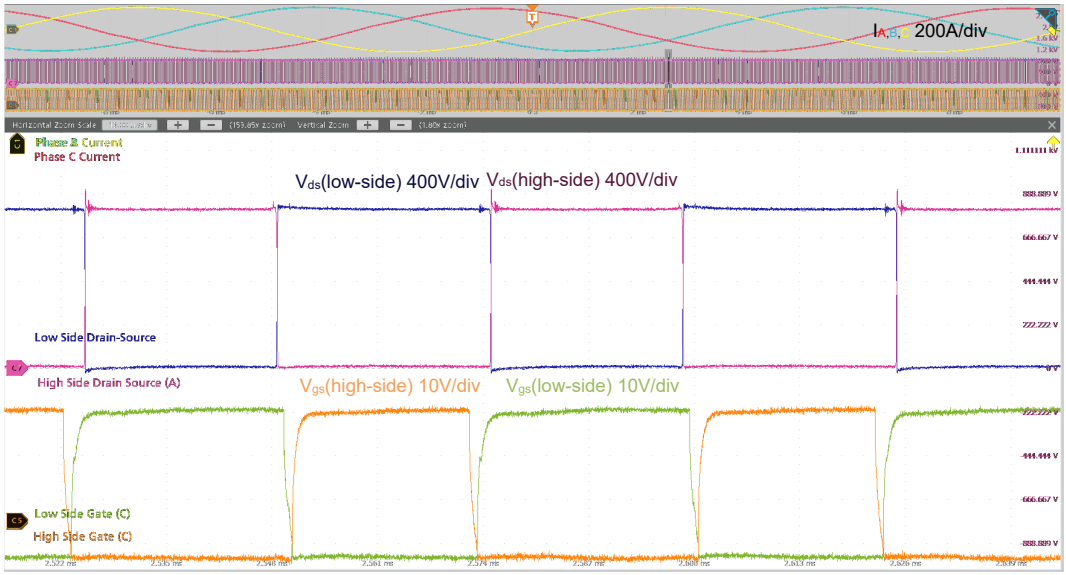


Figure 3-18. Voltage and Phase Current Waveforms With Weak Gate Drive Strength (I_{RMS} = 285A)

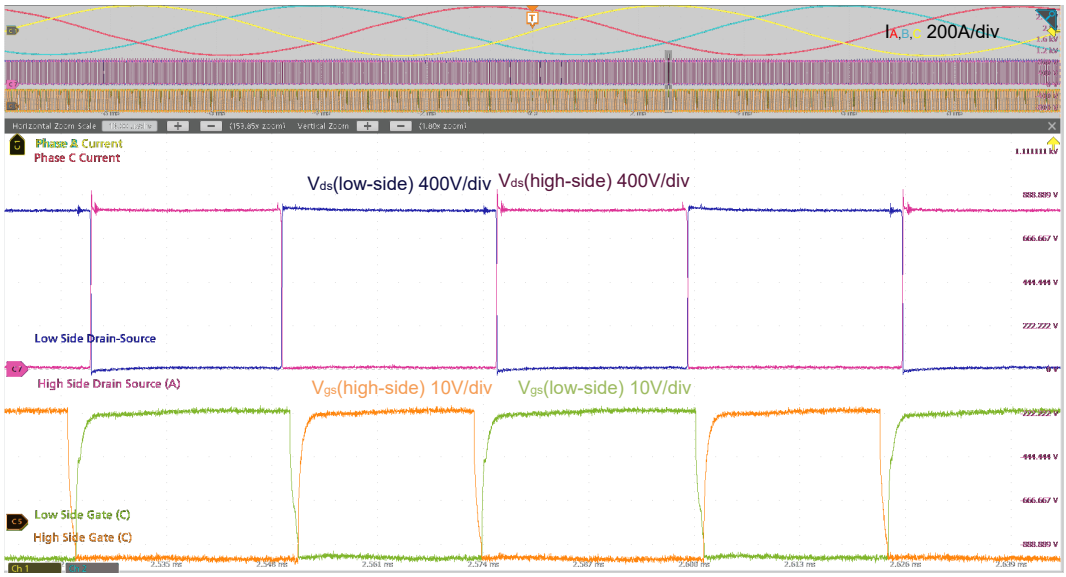


Figure 3-19. Voltage and Phase Current Waveforms With Weak Gate Drive Strength (I_{RMS} = 320A)

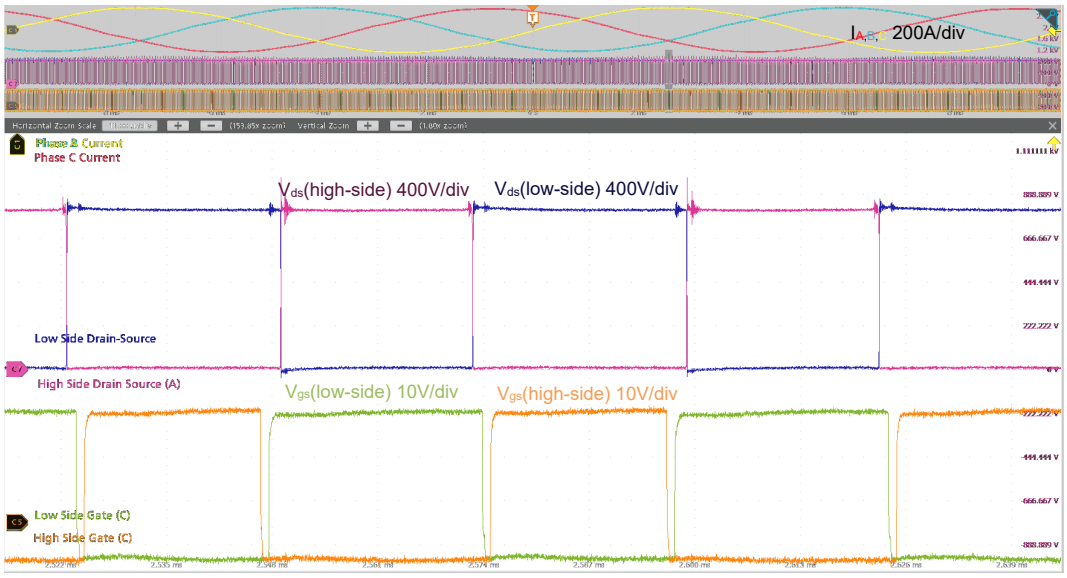


Figure 3-20. Voltage and Phase Current Waveforms With Strong Gate Drive Strength (I_{RMS} = 285A)

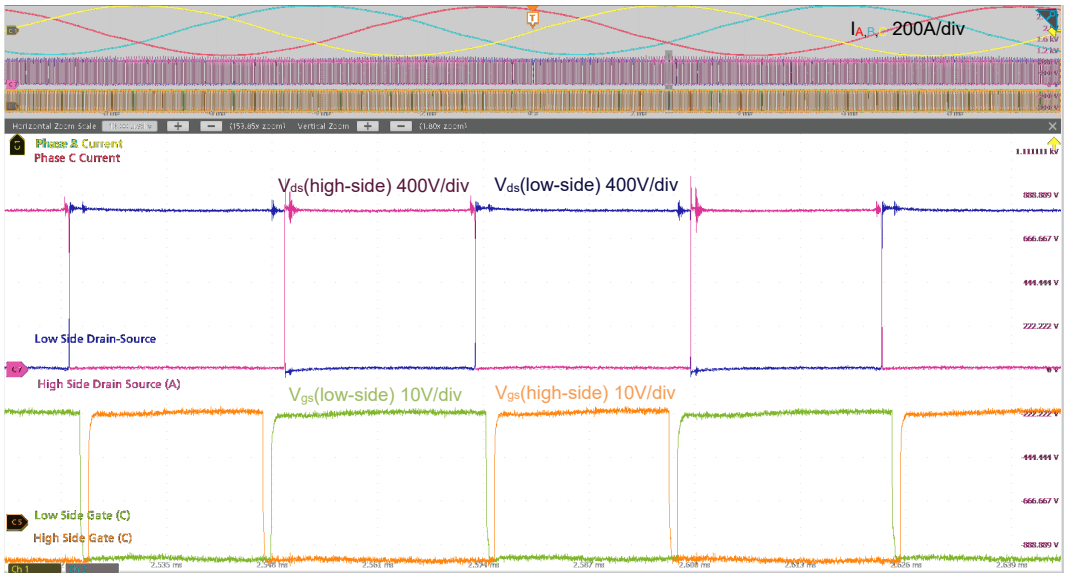


Figure 3-21. Voltage and Phase Current Waveforms With Strong Gate Drive Strength (I_{RMS} = 320A)

Table 3-6. Test Conditions and Results

GATE-DRIVE STRENGTH	DC BUS VOLTAGE	RMS CURRENT	P_{loss}
Weak	800V	285A	4.2111kW
Weak	800V	320A	5.1627kW
Strong	800V	285A	2.273kW
Strong	800V	320A	2.747kW

4 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Re-validate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDM-02014.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDM-02014.

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at TIDM-02014.

5.1.4 Altium Project

To download the Altium project files for each board, see the design files at TIDM-02014.

5.1.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDM-02014.

5.1.6 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at TIDM-02014.

5.2 Tools and Software

Tools

F29H85X-SOM-EVM	The F29H85X-SOM-EVM is an evaluation and development board for TI's C2000™ MCU F29H859TU-Q1 device. The system-on-module design with three 120-pin high-speed and high-density connectors make this EVM an excellent choice for initial evaluation and prototyping.

Software

F29-SDK	The F29 SDK provides comprehensive software packages for the development of high-performance real-time control applications. The SDK contains peripheral drivers, libraries, FreeRTOS®, No-RTOS, MCAL, CDD, tools, documentation and other packages targeting Digital Power and Motor Control applications.

5.3 Documentation Support

1. Infineon® Technologies, *Easy 1B/2B Automotive Power Modules Power Module for Hybrid- and Electric Vehicles Product Brief*
2. Texas Instruments, *Dual Isolated Outputs Fly-Buck Power Module Reference Design for Single IGBT Driver Bias Tool Folder*
3. Würth Elektronik®, *Specification Sheet: 750315445*
4. Texas Instruments, *Passing CISPR 25 Radiated Emissions Using the TPS54160-Q1 Application Note*
5. Texas Instruments, *TPS54xx0-Q1 and TPS57xx0-Q1 Design Calculation Tool*
6. Würth Elektronik®, *Specification Sheet: 760390014*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2023) to Revision A (May 2025)	Page
• Updated the design guide to reflect the reference design change to TI's F29H859TU-Q1, AMC0386-Q1, AMC0381D-Q1, and UCC33421-Q1 devices. Control card for the MCU evaluation is replaced by F29H85X-SOM-EVM	1
• Changes made throughout document to conform to the latest design guide standards.	1

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