Design Guide: TIDA-050060

Automotive 3-MP Scalable Camera Module Reference Design with PMIC and FPD-Link

Description

This reference design provides a compact and scalable camera module for automotive camera applications. It combines a 2.9-megapixel (2.9-MP) imager with a 4-Gbps serializer and four-channel power management integrated circuit (PMIC). The camera module is a two-board design to illustrate the flexibility and scalability of the power and serializer components to different image sensors. The camera PMIC enables a compact design optimized for flexibility and thermal performance by integrating three buck converters and one low-dropout regulator (LDO) with programmable output voltages and sequencing. Supervisors are integrated on each rail to further reduce the component count and overall form factor.

Resources

TIDA-050060	Design Folder
DS90UB953-Q1	Product Folder
TPS650330-Q1	Product Folder

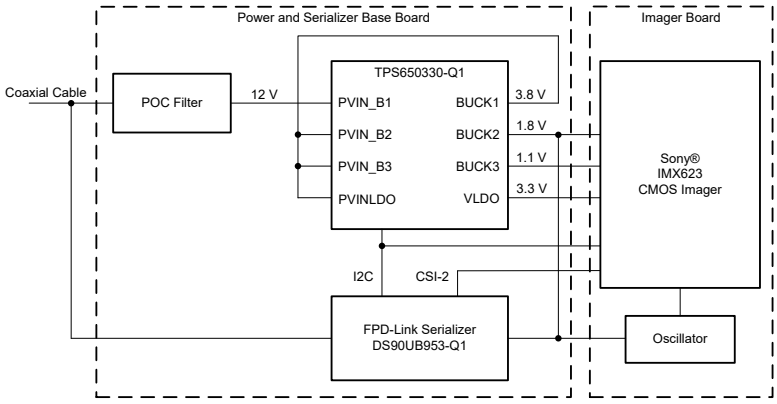
Ask our TI E2E™ support experts

Features

- 20-mm × 20-mm power and serializer PCB compatible with a variety of image sensors
- High efficiency and low noise power-supply
- High-resolution camera applications with the 4-Gbps DS90UB953 device
- 2.95-MP IMX623 imager from Sony® providing full-HD, AD 12-bit, MIPI 4-lane, RAW12, RAW14, RAW16, RAW20, RAW24
- Single Rosenberger FAKRA coaxial connector for digital video, power, control, and diagnostics
- Additional diagnostic capabilities to enable ASIL

Applications

- Camera Module without Processing
- Surround View System ECU
- Front Camera
- Rear Camera



1 System Description

Many automotive applications require small form factors that enable compact, modular, and remote systems. The growing demand for automotive vision systems also requires the flexibility of system components to meet the requirements of various image sensors to reduce the camera module design cycle and time-to-market. This reference design addresses these challenges by including a 2.9-megapixel imager, 4-Gbps serializer, and four-channel PMIC within two 20-mm x 20-mm circuit boards. The only connection required by the system is a single 50-Ω coaxial (coax) cable.

DC power, the FPD-Link front-channel, and the FPD-Link back-channel enter the board through the FAKRA coax connector. The POC filter in Figure 1-1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

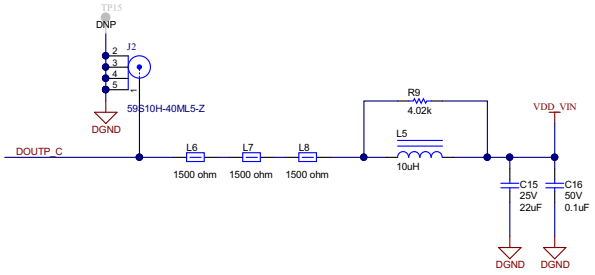


Figure 1-1. POC Filter Schematic

The DC portion is connected to the input of the TPS650330-Q1 PMIC. A dedicated mid-voltage buck regulator converts this to an intermediate 3.8 V. The two low-voltage buck regulators provide a dedicated 1.1 V for the imager and a dedicated 1.8 V shared by both the imager and serializer. An integrated high-PSRR, low-noise LDO provides a clean 3.3 V analog supply for the imager. The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and control backchannel take between the serializer and deserializer.

The output of the imager is connected through a 4-lane MIPI CSI-2 interface to the serializer. The serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coax cable.

Additionally, on the same coax cable, there is a separate low-latency, bidirectional control channel that provides the additional function of transmitting control information from an I2C port. This control channel is independent of the video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	5	9	18.3	V
P_{TOTAL}	Total power consumption	V_{POC} = 9 V	-	1	1.5	W

2 System Overview

2.1 Block Diagram

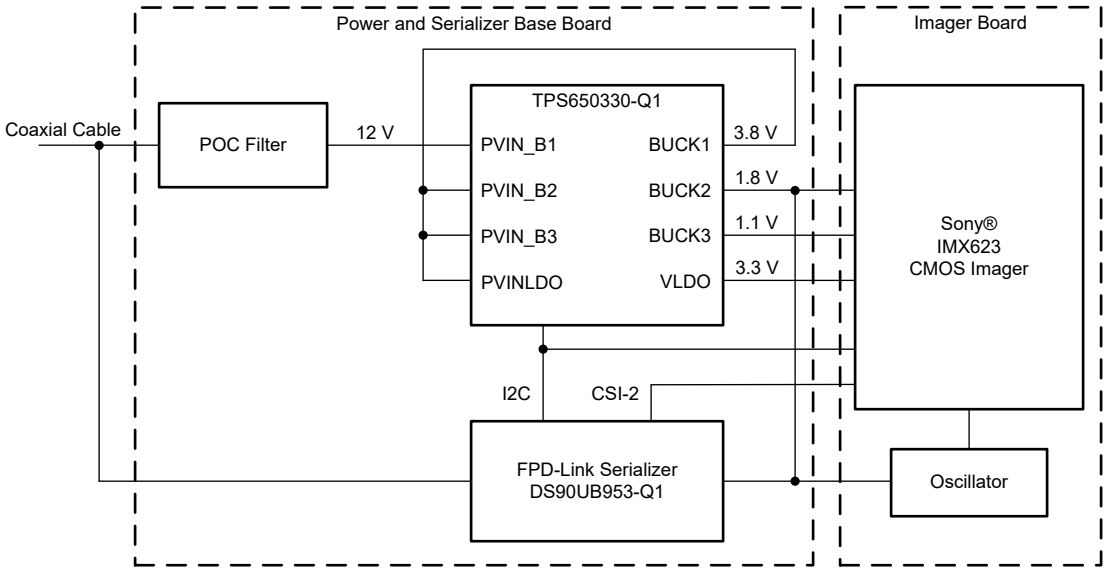


Figure 2-1. TIDA-050060 Block Diagram

2.2 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.2.1 PCB and Form Factor

The goal of this design is to combine the flexibility of a two-board solution within a compact area of 20 mm x 20 mm. The lens mounting on the imager board and FAKRA connector on the power and serializer board all fit within this area. Figure 2-2 and Figure 2-3 show the base board 3-D PCB views and Figure 2-4 and Figure 2-5 show the imager board 3-D PCB views.

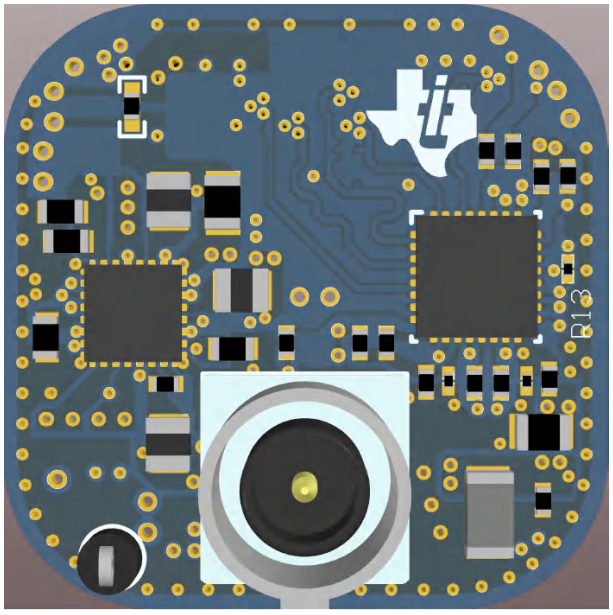


Figure 2-2. 3-D PCB Base Board (Top)

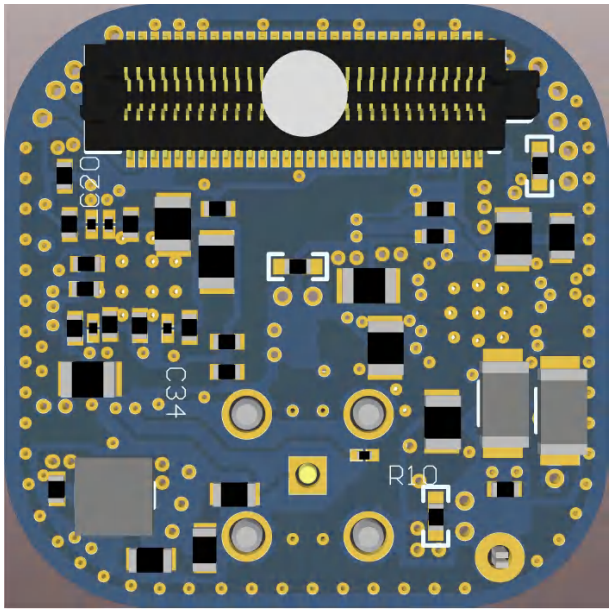


Figure 2-3. 3-D PCB Base Board (Bottom)

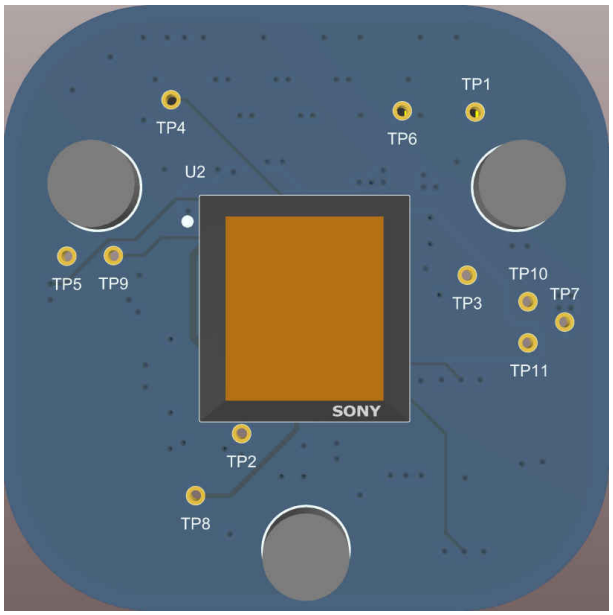


Figure 2-4. 3-D PCB Imager Board (Top)

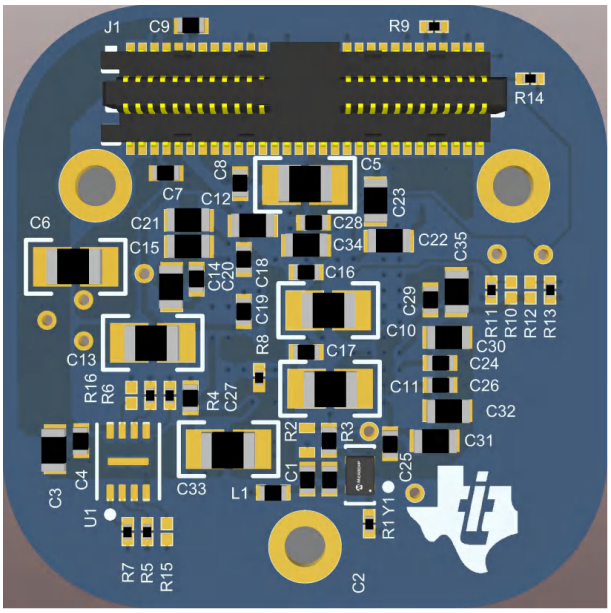


Figure 2-5. 3-D PCB Imager Board (Bottom)

Figure 2-6 and Figure 2-7 show 3-D PCB views of the assembled boards.

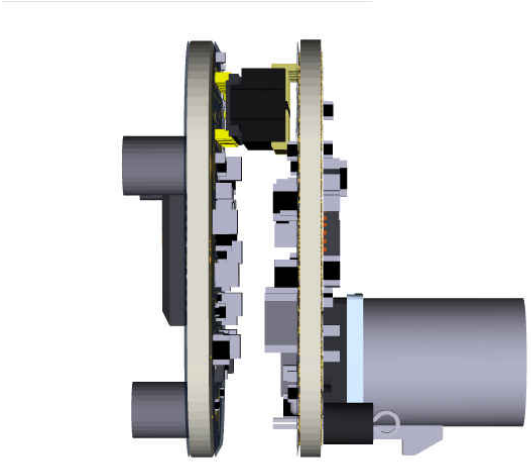


Figure 2-6. 3-D PCB Assembled Boards (Side View)

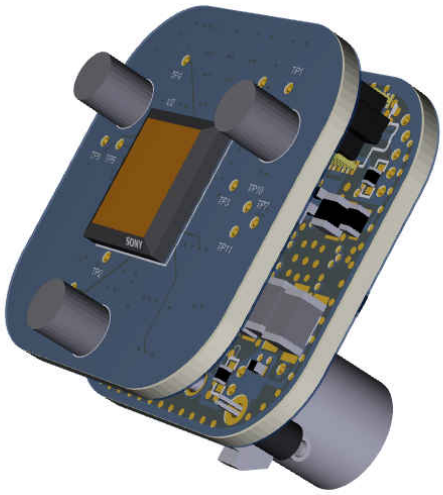


Figure 2-7. 3-D PCB Assembled Boards (Angled View)

2.2.2 Power Supply Design

2.2.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators
2. Protect the FPD-Link communication channels from noise-coupled backwards from the rest of the system

The DS90UB953-Q1 and DS90UB960-Q1 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed ("forward channel") and a lower frequency of 50 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC. To allow the forward channel and backchannel to pass uninterrupted over the POC cable, an impedance of > 2 kΩ across the 25-MHz to 2-GHz bandwidth is required. To accomplish this, an inductor is typically chosen for filtering the 25-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2-GHz frequency band. This complete filter is shown by L2 in Figure 2-8. L1 is the same inductor for the POC filter on the deserializer side. In this camera design, it is imperative for the filter to have the smallest footprint allowable. To accomplish this, the LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the lower frequency and another for the higher frequency.

For the high-frequency forward-channel filtering, this reference design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2-GHz range. This design uses three 1.5-kΩ ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore, three ferrite beads instead of two allows for more headroom across the whole frequency band. For good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized onboard for the POC inductor filtering. For more details, see the *Power-over-Coax Design Guidelines for DS90UB953-Q1* application report.

Lastly, in regards to filtering, ensuring that the FPD-Link signal is uninterrupted is just as important as providing a clean, noise-free DC supply to the system. To achieve this, AC coupling capacitors of 0.033 µF and 0.015 µF are chosen to ensure the high-speed AC data signals are passed through, but the DC is blocked from getting on the data lines.

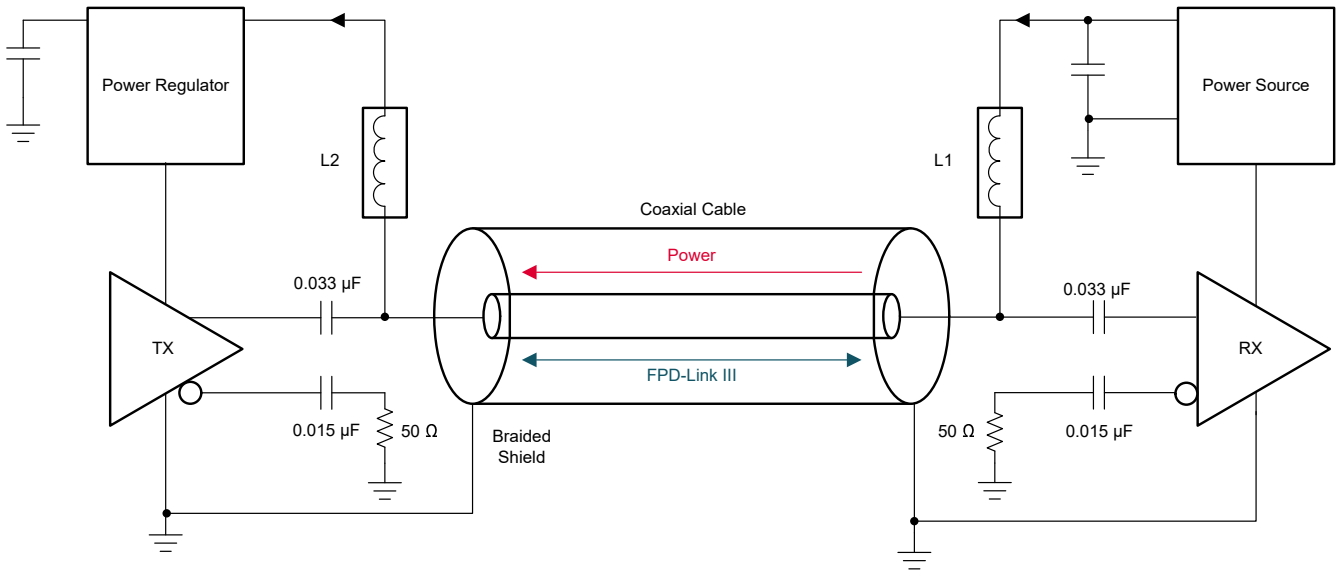


Figure 2-8. Power Over Coax

2.2.2.2 Power Supply Considerations

This reference design targets automotive applications, so there are several requirements that shape the design choices:

- The board area needs to be minimized to 20 mm × 20 mm. A fully-integrated PMIC power solution minimizes the external component count, making this requirement easier to achieve.
- Switching frequencies must be lower than 540 kHz or higher than 1700 kHz to avoid interfering with the AM radio band. Choosing a higher switching frequency prevents harmonics encroaching in the AM band, and allows for smaller external components to aid the board area requirements.
- All devices must be AEC Q100-Q1 rated.

The system input voltage is a pre-regulated 9-V supply over coax. As the PMIC integrates supervisors and monitoring, the only system components requiring power are the imager, serializer, and oscillator. Table 2-1 shows the maximum power consumption of these devices:

Table 2-1. System Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (mA)	POWER (mW)
Imager			
	3.3	79	261
	1.8	9	16
	1.1	383	421
Serializer			
	1.8	225	405
Oscillator			
	1.8	3	5
Total			
	3.3	79	261
	1.8	237	427
	1.1	383	421

2.2.2.2.1 Choosing External Components

For simplicity, the efficiency of the buck regulators is assumed to be 80% for the operating conditions listed in Table 2-1, while the efficiency of the LDO is given by Equation 1:

$$\eta_{LDO} = \frac{V_{OUT}}{V_{IN}} = \frac{3.3}{3.8} = 0.87 \quad (1)$$

Equation 2, which calculates the input power of a converter as a function of the output power and efficiency, is used to calculate the system and Buck 1 output currents.

$$P_{IN} = V_{IN} \times I_{IN} = \frac{P_{OUT}}{\eta} \quad (2)$$

$$I_{OUT,\ Buck1} = \frac{\frac{P_{OUT,\ Buck2}}{\eta_{Buck2}} + \frac{P_{OUT,\ Buck3}}{\eta_{Buck3}} + \frac{P_{OUT,\ LDO}}{\eta_{LDO}}}{V_{OUT,\ Buck1}} = 341 \quad mA \quad (3)$$

Table 2-2 shows the load capability of each regulator compared to the requirements of the camera module. The TPS650330-Q1 device is capable of supplying the system power with plenty of margin to account for variations between typical and maximum current variation.

Table 2-2. TPS650330-Q1 Capabilities vs. System Requirements

REGULATOR	OUTPUT VOLTAGE (V)	MAXIMUM CURRENT (mA)	REQUIRED CURRENT (mA)
Buck 1	3.8	1500	341
Buck 2	1.8	1200	237
Buck 3	1.1	1200	383
LDO	3.3	300	79

After determining that the TPS650330-Q1 device is suitable based on the power requirements, the external components can be chosen quickly based on the data sheet recommendations, simplifying the design process. These recommendations are shown in Figure 2-9 and Table 2-3.

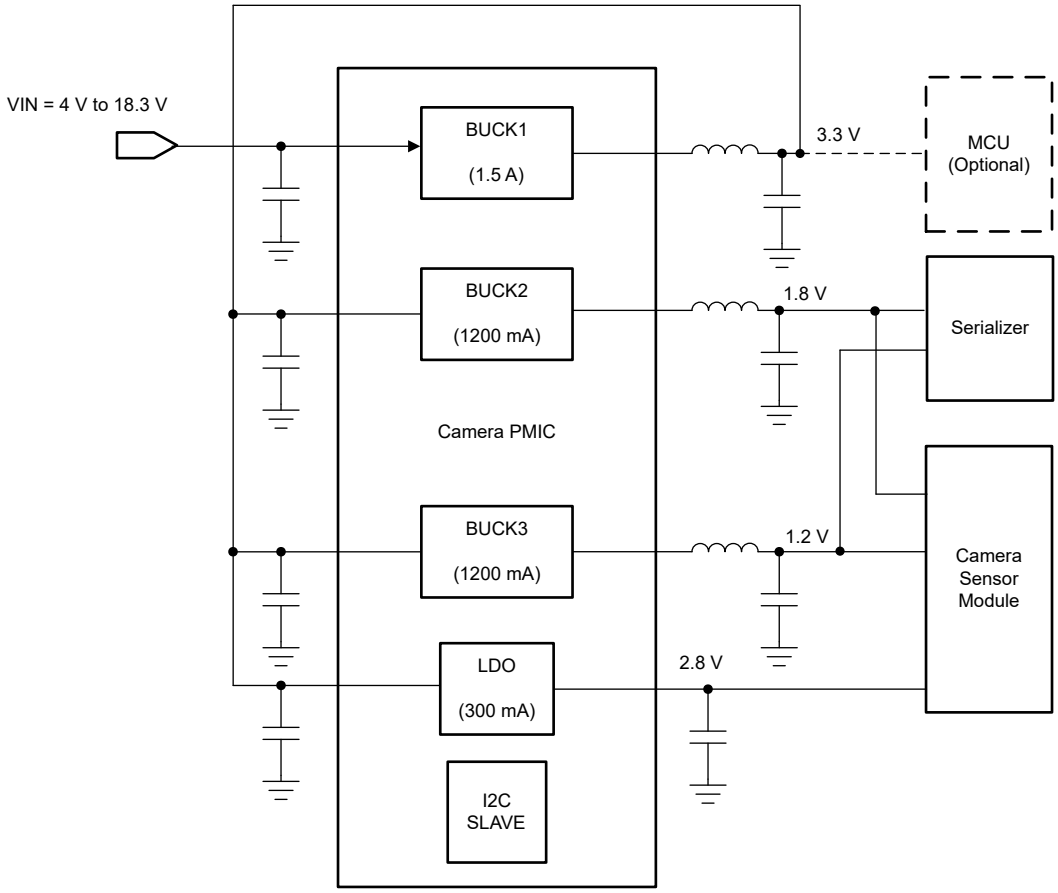


Figure 2-9. Typical Application

Table 2-3. TPS650330-Q1 Recommended Components

COMPONENT	DESCRIPTION	VALUE	UNIT
$C_{VSYS,VSYS\_S}$	VSYS and VSYS_S decoupling	10	µF
C_{PVIN_B1}	Buck 1 input capacitor	10	µF
L_{SW_B1}	Buck 1 inductor	1.5	µH
C_{OUT_B1}	Buck 1 output capacitor	10	µF
C_{PVIN_B2}	Buck 2 input capacitor	10	µF
L_{SW_B2}	Buck 2 inductor	1.0	µH
C_{OUT_B2}	Buck 2 output capacitor	10	µF
C_{PVIN_B3}	Buck 3 input capacitor	10	µF
L_{SW_B3}	Buck 3 inductor	1.0	µH
C_{OUT_B3}	Buck 3 output capacitor	10	µF
C_{PVIN_LDO}	LDO input capacitor	1.0	µF
C_{OUT_LDO}	LDO output capacitor	2.2	µF

2.2.2.2.2 Choosing the Buck 1 Inductor

With an inductance value of 1.5 µH selected, the minimum inductor saturation current must be derived to choose an appropriate inductor for the design. This is the combination of the steady-state supply current as well as the inductor ripple current. To ensure flexibility of the power and serializer base board to higher power image sensors, the inductor is chosen based on each maximum rated output current of the regulator. Equation 4 calculates inductor ripple current.

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{sw}} \right) \quad (4)$$

where

- $\Delta I_{L(max)}$ is the maximum peak-to-peak inductor ripple current
- $L_{(min)}$ is the minimum effective inductor value
- f_{sw} is the actual PWM switching frequency

The parameters for Buck 1 of this reference design are:

- V_{OUT} = 3.8 V
- $V_{IN(max)}$ = 18.3 V
- $L_{(min)}$ = 1.5 µH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 873 mA. Assuming a maximum load current of 1.5 A, use Equation 5 to calculate a minimum saturation current of 1.9 A.

$$L_{SAT} \geq I_{OUT,(MAX)} + \frac{\Delta I_{L(MAX)}}{2} \quad (5)$$

The TPS650330-Q1 device on this design uses a TDK® TFM201610ALMA1R5MTAA, which has a rated current of 3.1 A and a DC resistance maximum of 110 mΩ. Additionally, this inductor has an operating temperature from –55°C to 150°C in a very small 2.0-mm × 1.6-mm package.

2.2.2.2.3 Choosing the Buck 2 and Buck 3 Inductors

Buck 2 and Buck 3 have a recommended inductor value of 1.0 µH. When selecting a component, it is important to verify the DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly – lower DC resistance is directly proportional to efficiency. The saturation requirement of the inductor is determined by combining the steady-state supply current and the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current using Equation 4.

The parameters for the Buck 2 1.8-V rail include:

- V_{OUT} = 1.8 V
- $V_{IN(max)}$ = 3.8 V
- $L_{(min)}$ = 1.0 µH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 412 mA. Assuming a maximum load current of 1.2 A, Equation 5 can be used to calculate a minimum saturation current of 1.4 A.

The parameters for the Buck 3 1.1-V rail include:

- V_{OUT} = 1.1 V
- $V_{IN(max)}$ = 3.8 V
- $L_{(min)}$ = 1.0 µH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 340 mA. Assuming a maximum load current of 1.2 A, Equation 5 can be used to calculate a minimum saturation current of 1.4 A.

Buck 2 and Buck 3 of this design use the TDK® TFM201610ALMA1R0MTAA, which has a current rating of 3.1 A and a DC resistance of 60 mΩ. Additionally, this inductor has an operating temperature of –55°C to 150°C in a very small 2.0-mm × 1.6-mm package.

2.2.2.2.4 Functional Safety

The TPS650330-Q1 device has integrated supervisors in addition to temperature and current monitoring. The interrupt pin or status bits of this PMIC can be used to detect when a fault condition has occurred, at which point a local or remote MCU or processor can query the fault mechanism via I2C, and take the appropriate action. The TPS650330-Q1 is also pin-compatible with the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1. Each of these devices provides additional safety features, allowing the scalability of this design to camera applications requiring functional safety.

2.3 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coax cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- TPS650330-Q1: an automotive qualified, four channel PMIC optimized for camera applications. The device integrates three buck converters and one LDO, along with undervoltage monitors and overvoltage protection for each voltage rail. A fixed PWM 2.3-MHz switching frequency enables the use of small inductors with a fast transient response. The low-noise, high-PSRR LDO provides an output voltage option for sensitive analog circuits. The output voltage and sequencing settings, along with other operational settings are programmable via I2C for compatibility with a variety of imagers without the need for any additional components.

2.3.1 DS90UB953-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 device mates well with the MIPI CSI-2 video output of the IMX623 imager. Once combined with the filters for the POC, video, I2C control, diagnostics, and power can all be transmitted on a single inexpensive coax cable.

2.3.2 TPS650330-Q1

To minimize form factor, a PMIC is selected to provide the power, supervision, and sequencing requirements for the system. A power topology consisting of three buck regulators and one LDO provides a balance between power efficiency and noise performance. A 2.2-MHz operating frequency is beneficial for two reasons: it avoids the especially sensitive frequencies of image sensor circuits (typically 1 MHz or less) and it avoids interfering in the AM radio band for automotive applications. The low noise, and high PSRR LDO of the PMIC can provide up to 300 mA of current with a tight output voltage tolerance (±1%) appropriate for the analog voltage rail requirements in ADAS camera applications. The PMIC offers programmable output voltages and sequencing, allowing the same power and serializer design to be reused with a variety of imagers depending on the vision application.

2.3.3 IMX623

The Sony® IMX623 is a diagonal 7.45-mm CMOS image sensor with 2.95 effective mega-pixels. The sensor supports 12-bit ADC, MIPI 4-lane, RAW12 up to RAW24 HDR output. Other features include:

- Supports 1920 x 1536 resolution (2.95-MP) at up to 60-fps
- 120 dB dynamic range
- LED flicker mitigation
- Requires three voltage rails (3.3 V, 1.8 V, and 1.1 V)
- Can be configured using an I^2C interface or serial NOR flash
- Pin compatible family of automotive image sensors: IMX622, ISX021, ISX031

2.4 System Design Theory

The main design challenges to consider for automotive cameras are size, ease of use, and thermal efficiency. Automotive cameras are often placed in remote regions of the vehicle where area is limited, requiring an overall

compact solution. Because of this, the system is designed around having the lowest number of components with a fully-integrated PMIC power solution. As ADAS applications continue to grow in capability and complexity, the increase in demand for automotive cameras requires that ease of use, or flexibility, becomes another critical factor to reduce system design cycle and time-to-market. The choice of the DS90UB953-Q1 and TPS650330-Q1 devices are important here as they are compatible with a wide range of imagers. The choice of a two-board solution highlights this flexibility, as the power and serializer base board can be re-used with different imager boards depending on the ADAS application. Additionally, the Sony® IMX623 image sensor is selected as part of a family of pin-compatible automotive image sensors: IMX622, ISX021, and ISX031. The option for NOR flash is included on the IMX623 imager board to enable compatibility with the ISX021 and ISX031 devices. Lastly, the small size and remote placement of these cameras increases their susceptibility to heat. A power efficient system is crucial to preserve the image quality in these conditions. The TPS650330-Q1 device is optimized for efficiency with a three buck and one LDO regulator topology, enabling the support of medium and high quality imagers without sacrificing thermal performance. Due to the impact of thermals on the system performance, it is important to calculate total system efficiency as part of the design process. From the Buck 1 output power in Table 2-2 and assuming an efficiency of 85%, Equation 2 calculates a system input power of about 1.5 W. Equation 6 can then be used with the output power of Buck 2, Buck 3, and the LDO to calculate the overall system efficiency.

$$\eta_{SYSTEM} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT,\ Buck\ 2} + P_{OUT,\ Buck\ 3} + P_{OUT,\ LDO}}{P_{IN,\ Buck\ 1}} = 73\,\% \tag{6}$$

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in Figure 3-1.

Figure 3-1. Board Image

3.1.1 Hardware Setup

Figure 3-2 shows the setup to test the camera module reference design. This design includes an IMX623 image sensor, which connects to the DS90UB953-Q1 serializer over CSI-2 and I2C interfaces. The DS90UB953-Q1 serializer then connects through POC to a DS90UB954-Q1 deserializer. Note that for test setup, only one channel is used from the DS90UB954-Q1 device. The Analog LaunchPad™ GUI writes all the back channel I2C setting configurations for the IMX623, DS90UB953-Q1, and DS90UB954-Q1 devices.

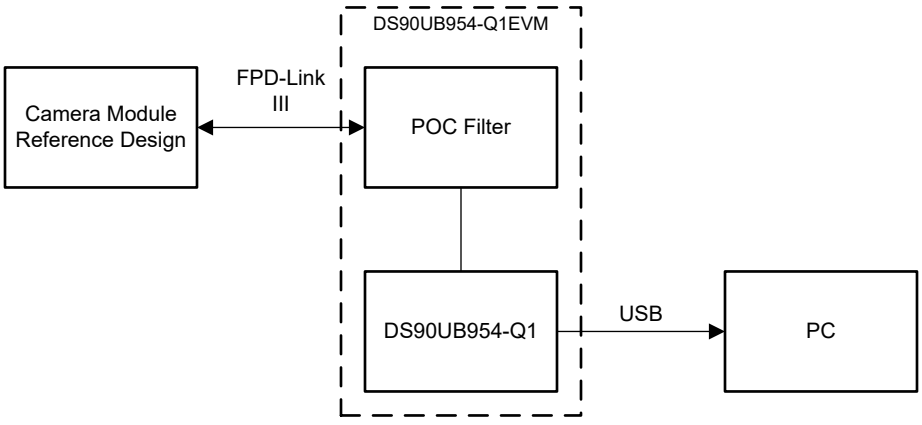


Figure 3-2. Test Setup

3.1.2 FPD-Link III I2C Initialization

With the setup in Figure 3-2 connected, the DS90UB954-Q1 EVM is supplied 12-V input power, which is regulated to 9-V with an onboard LDO and delivered through POC to power the TIDA-050060 camera module. Once all rails are established, all devices (IMX623, DS90UB953-Q1, and DS90UB954-Q1) receive power. Then, the I2C writes for initialization can begin. Note that the following writes are only showing one channel camera and may not be the mode wanted for specific multi-camera mode. The Analog LaunchPad compatible Python® script to initialize the DS90UB954-Q1 deserializer and DS90UB953-Q1 serializer are as follows:

```
# Set up Port0
board.WriteI2C(UB954, 0x4C, 0x01)

# Set up Back Channel Config (0x58)
board.WriteI2C(UB954,0x58,0x5E)

# Set up SER ID
board.WriteI2C(UB954,0x5B,UB953ID)
# Set up SER Alias ID
board.WriteI2C(UB954,0x5C,UB953)
# Set up Slave/Camera ID
board.WriteI2C(UB954,0x5D,SensorID)
# Set up Slave/Camera Alias ID
board.WriteI2C(UB954,0x65,Sensor)

# Set up CLK_OUT from 50 Mbps BC frequency
board.WriteI2C(UB953,0x06,0x22)
board.WriteI2C(UB953,0x07,0xA7)

time.sleep(0.1)

# Set GPIO1 to output, where GPIO1 = RESET
board.WriteI2C(UB953,0x0E,0x1E)

# Set GPIO1 to High - bring sensor out of power down mode
board.WriteI2C(UB953,0x0D,0x01)
```

3.1.3 IMX623 Initialization

Once the FPD-Link III setup is done for the DS90UB953-Q1 and DS90UB954-Q1 devices, the I2C initialization can now be done on the IMX623. For these writes, see the IMX623 data sheet for register settings. There are many register settings listed to configure the imager, but as long as the DS90UB953-Q1 and DS90UB954-Q1 FPD-Link III parts are configured, the I2C back channel allows access to the IMX623 registers. For this testing, the IMX623 is configured for RAW12 output at 1920 × 1536 resolution and 30-fps.

3.2 Testing and Results

3.2.1 Test Setup

The setup used to verify power supply functionality and I2C communication is the same as Figure 3-2.

3.2.1.1 Power Supplies Startup

To verify the power supply sequencing and startup behavior, each voltage rail output from the TPS650330-Q1 device was measured after applying power over coax to the system.

3.2.1.2 Power Supply Startup – 1.8 V Rail and Serializer PDB Setup

The PDB reset signal of the DS90UB953-Q1 device is connected directly to the nRSTOUT pin of the TPS650330-Q1 device . With the integrated sequencing capabilities of the PMIC, this ensures that the PDB reset line goes high after the 1.8-V supply is stable, eliminating the need for an external RC network.

3.2.2 Test Results

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supplies Start Up

Figure 3-3 shows the start-up behavior for the 3.8-V, 1.8-V, 1.1-V (DVDD), and 3.3-V (AVDD) rails.

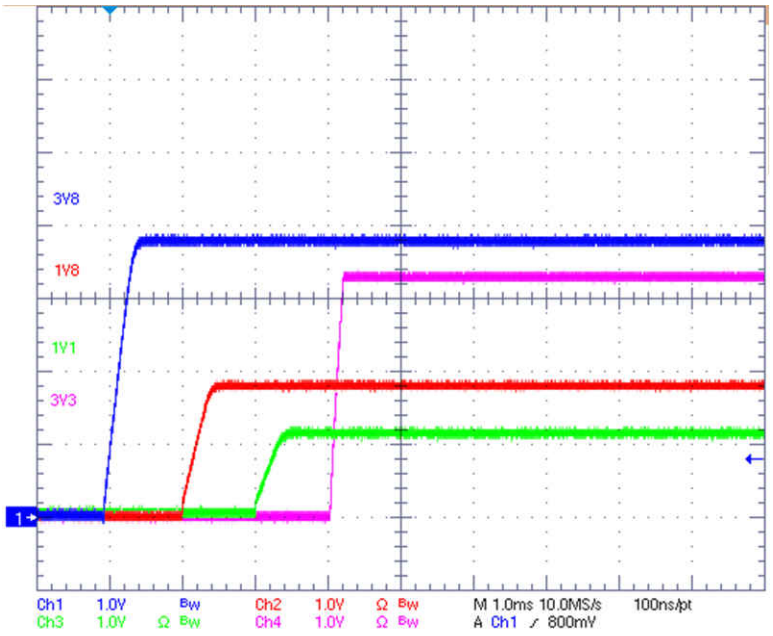


Figure 3-3. Point-of-Load Power Supply Start Up

Figure 3-4 shows the delay requirement between the 1.8-V rail and PDB reset line is met.

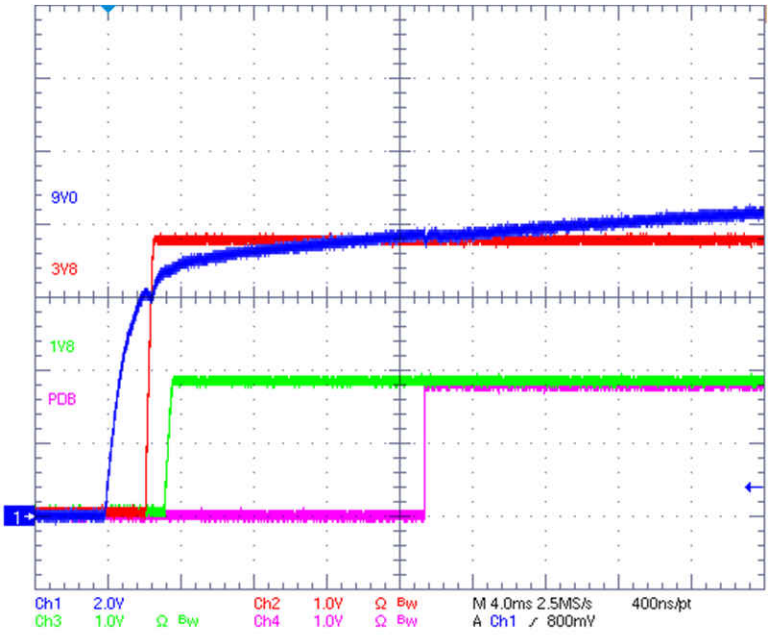


Figure 3-4. Serializer Power-Up Sequence

3.2.2.2 Power Supply Output Voltage Ripple

To achieve a quality output video stream, the output voltage ripple on the IMX623 and DS90UB953-Q1 supplies must be low so that it does not affect the integrity of the high-speed CSI-2 data and internal PLL clocks. Figure 3-5 to Figure 3-8 show the measurements for 3.8-V, 1.8-V, 1.1-V, and 3.3-V rails while the camera is streaming video. The measured peak-to-peak ripple voltages are 0.4%, 0.6%, 0.6%, and 0.1% respectively. The tight voltage accuracy allows for the video output to be successfully transmitted.

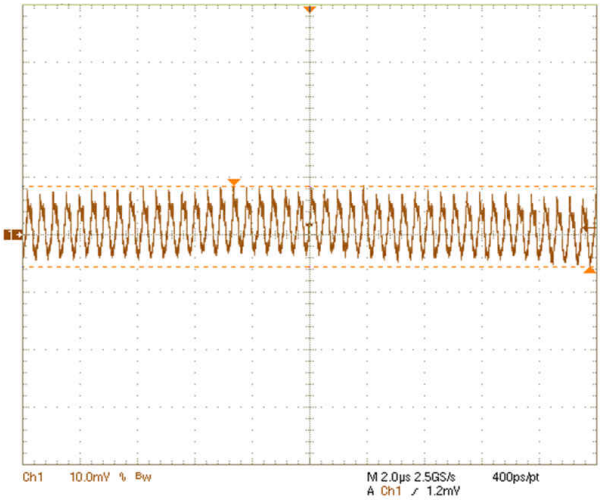


Figure 3-5. Output Voltage Ripple: 3.8 V

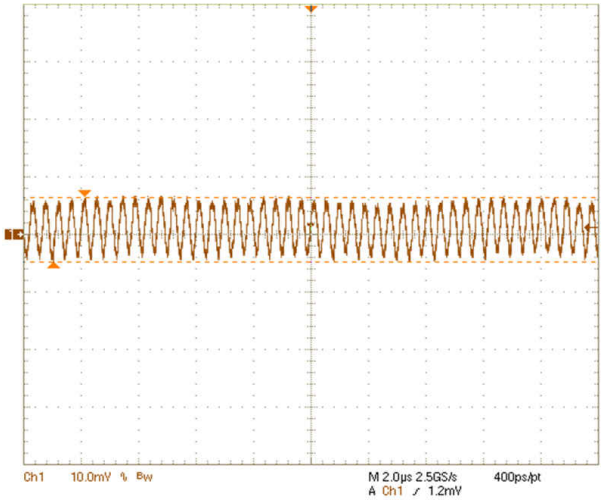


Figure 3-6. Output Voltage Ripple: 1.8 V

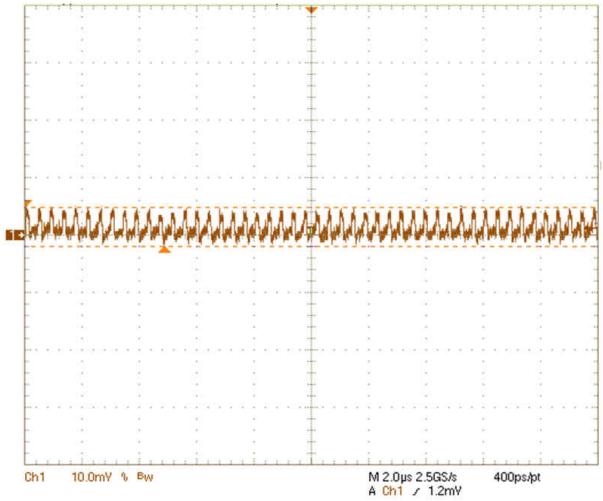


Figure 3-7. Output Voltage Ripple: 1.1 V

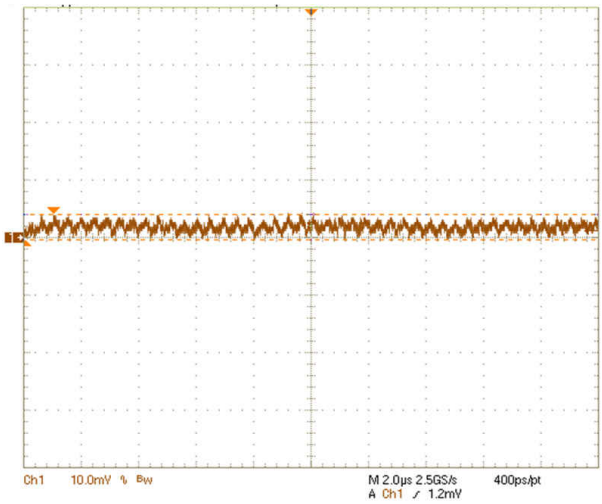


Figure 3-8. Output Voltage Ripple: 3.3 V

3.2.2.3 Power Supply Load Currents

Table 3-1 shows the currents measured for each supply voltage in this reference design. The measurements correspond to an overall system efficiency of 70%, close to the 73% derived in Section 2.4. The difference can be attributed to lower measured operating currents compared to the maximum values used in the analysis. Additionally, losses in the coaxial cable and POC filter were not factored into the analysis.

Table 3-1. Measured Supply Currents

VOLTAGE RAIL (V)	MEASURED CURRENT (mA)
9	87
3.8	180
3.3	51
1.8	139
1.1	116

3.2.2.4 I2C Communications

I2C communication between the DS90UB954-Q1 EVM and IMX623 imager over the FPD-Link III back channel can be confirmed with the Analog LaunchPad GUI. Figure 3-10 and Figure 3-11 show the established link with the serializer on RX port 0, and the corresponding register map.

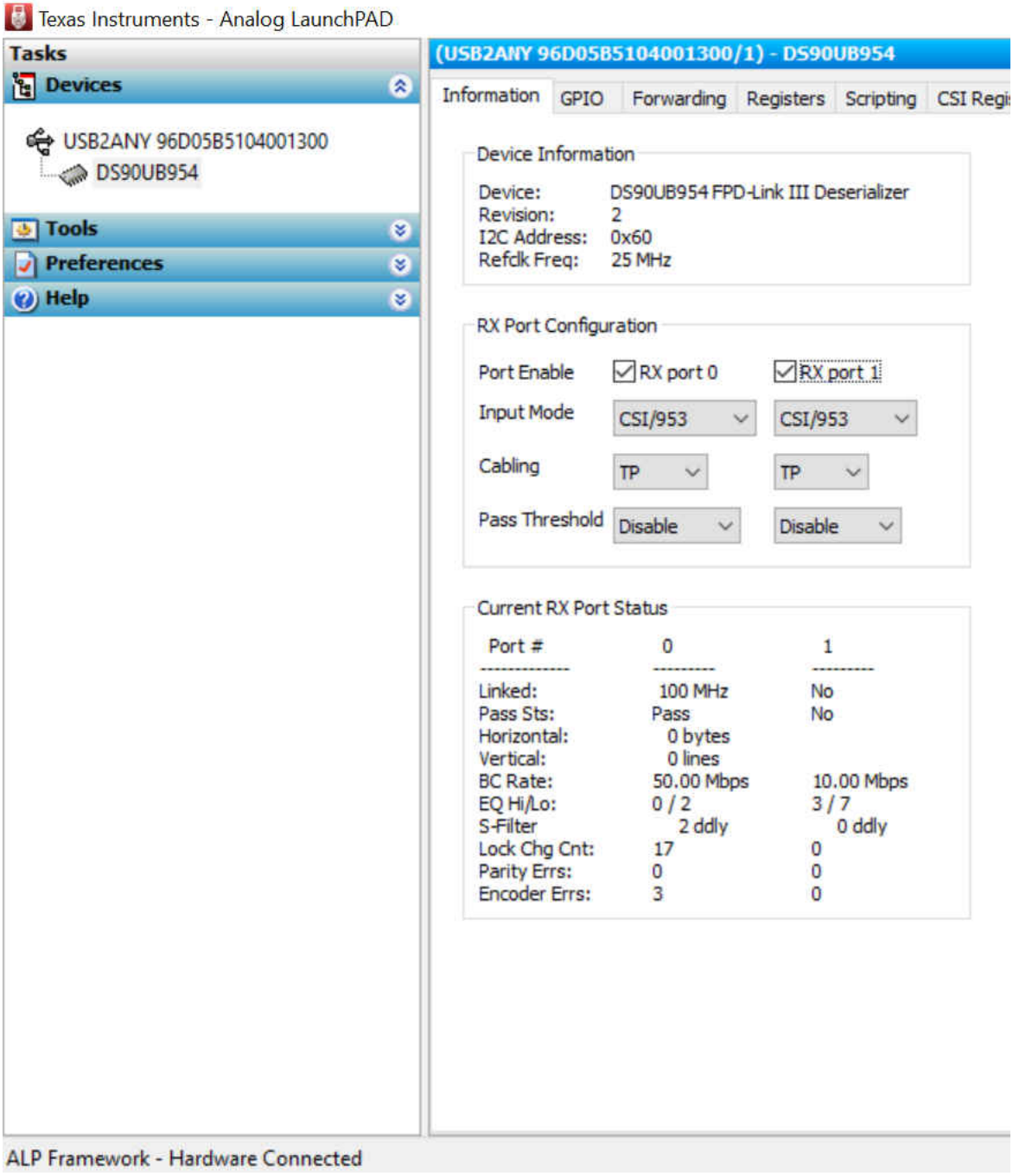


Figure 3-9. Analog LaunchPad Link Confirmation

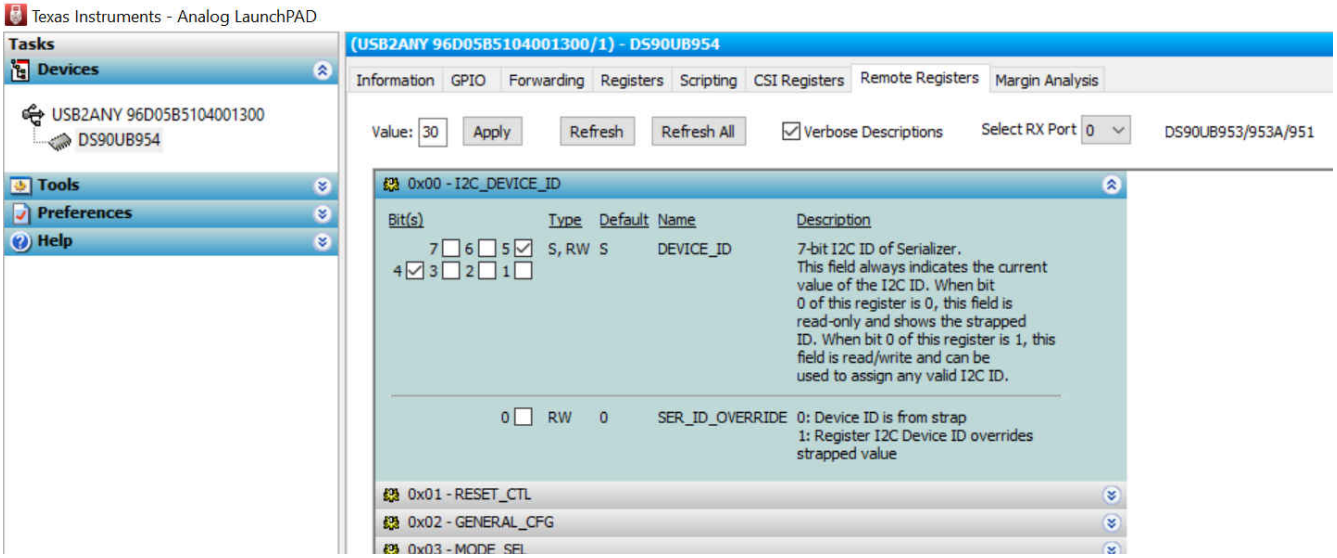


Figure 3-10. Serializer Remote Registers

Read and writes to the imager, at slave alias address 0x1A (7-bit), are confirmed with the built-in Python scripting window of the Analog LaunchPad. Register 0x8A54 reads data 0x1A, which is the expected default value for the register.

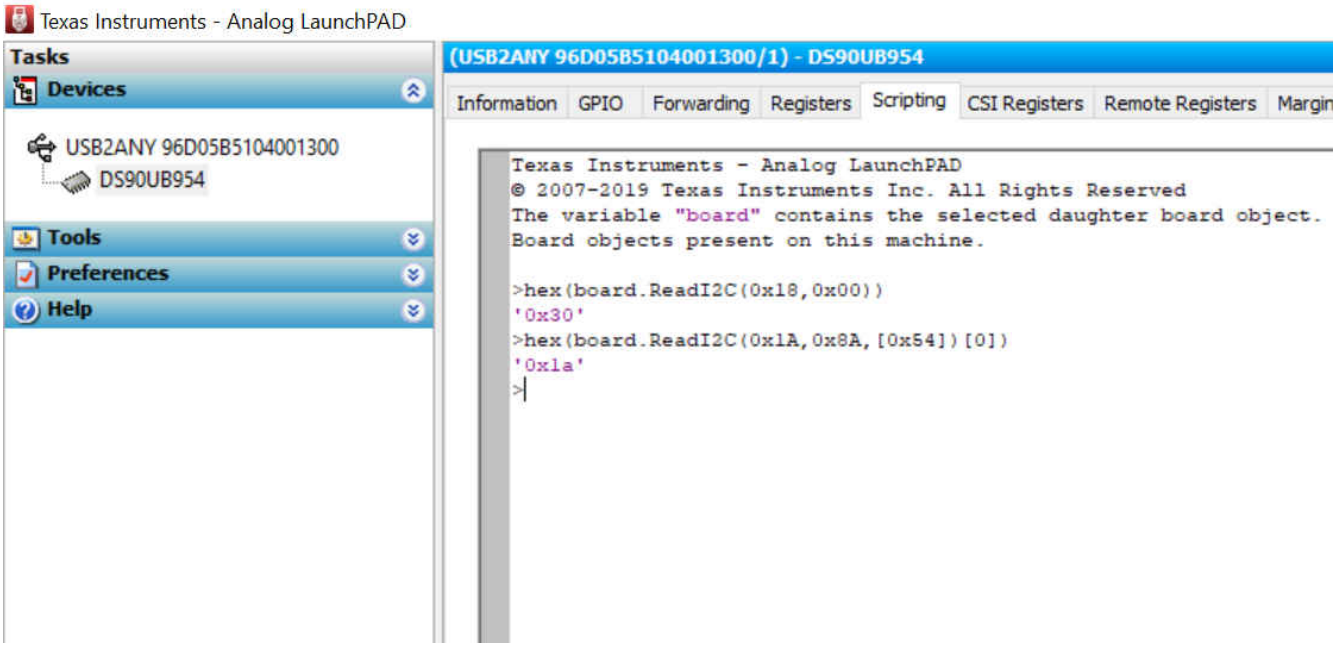


Figure 3-11. Back-Channel I2C Communication

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050060.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050060.

4.3 PCB Layout Recommendations

4.3.1 PMIC Layout Recommendations

The PMIC portion of the layout requires careful consideration to minimize both PCB area and noise. As EMI is a critical concern in automotive systems, the TPS650330-Q1 device includes a spread spectrum feature to reduce conducted and radiated emissions, allowing more flexibility with placement and layout for space-constrained applications. However, it is still recommended to follow as many best practices as possible. This includes minimizing the area traveled by switching currents between buck regulator input capacitor, inductor, and output capacitor with tight component placement and minimal return path to the PMIC thermal pad. Figure 4-1 shows an example of this for Buck 2.

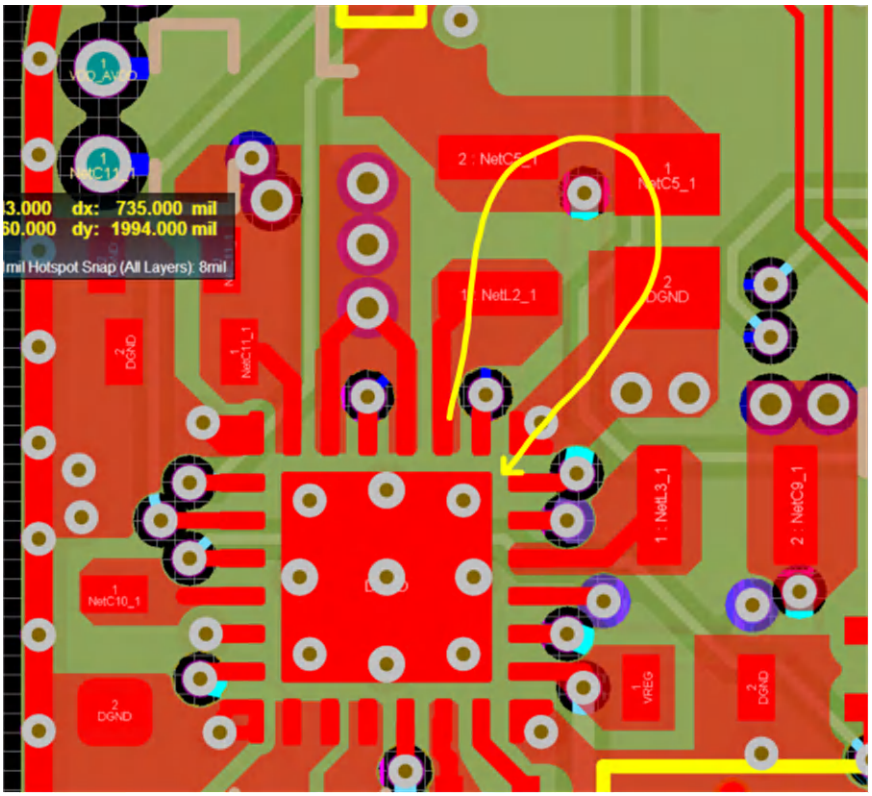


Figure 4-1. Buck 2 Layout Considerations

For the LDO, separation of input and output capacitor ground planes will reduce noise coupling from the switching rails to the sensitive analog rail. To further reduce noise coupling, the dedicated AGND pin of the PMIC is connected to the ground plane on an internal layer with a via, rather than directly to the noisier thermal pad on the top layer.

4.3.2 PCB Layer Stackup

Figure 4-2 shows the 8-layer stackup used for the PMIC and serializer board. Two signal layers are required due to the complex routing requirements introduced by I2C, GPIO, clock, and control signals between the PMIC, serializer, and header, which provide an interface with the imager. The separation between planes carrying high-speed CSI data lines should be selected to ensure a characteristic differential impedance of 100 Ω ±10%.

Figure 4-3 shows the 6-layer stackup for the imager board. This has similarly been designed around the target differential impedance of the CSI-2 traces.

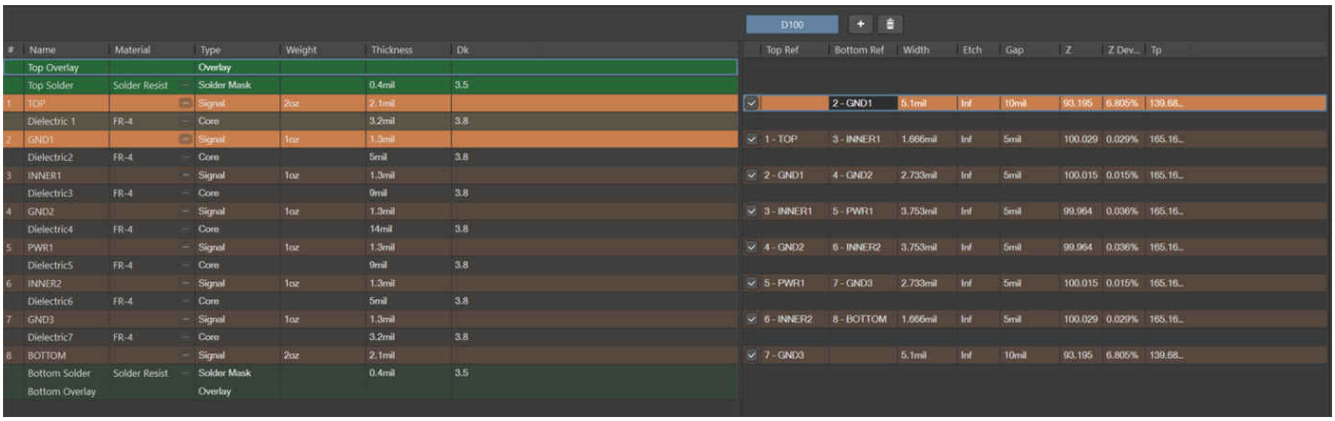


Figure 4-2. Eight-Layer Stackup PMIC and Serializer Board

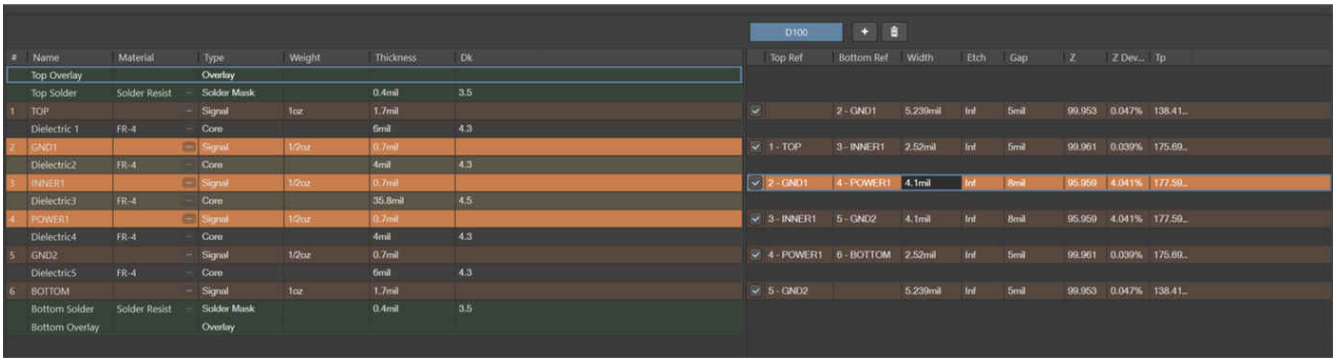


Figure 4-3. Six-Layer Stackup Imager Board

4.3.3 Serializer Layout Recommendations

Trace impedance is one critical aspect to the CSI-2 lane routing. For trace impedance to be within specifications and within range of each other, the length and width of the trace plays a factor in this. To achieve tight impedance specs, length specifications also need to be strict within the positive-to-negative differential pair length and pair-to-pair length. If the length is not matched, at these high-data switching speeds, the data can arrive at the 953 at different times and cause issues of synchronization between data and clock. The length difference between the positive and negative differential pair trace should be within 5 mils of each other. For length matching between each CSI-2 lane pair, the difference must be kept within 25 mils.

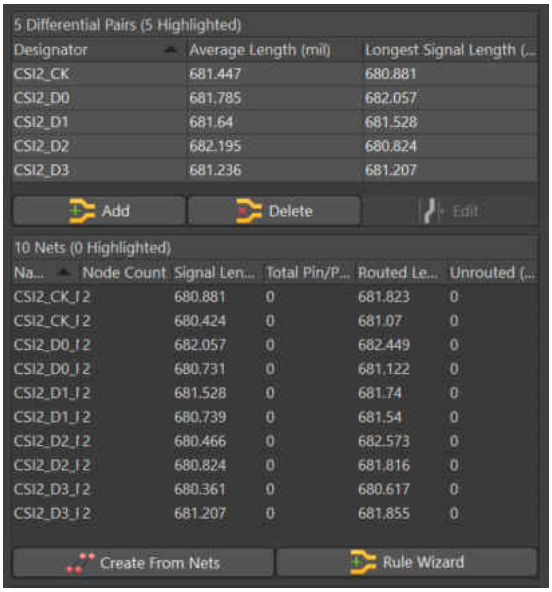


Figure 4-4. CSI Routing Matching

The last key points to address with CSI-2 routing is crosstalk and reflections. To reduce the effects of crosstalk between lanes, spacing between each differential lane must be at least three times the signal trace width. In addition, keep vias and bends on the traces to a minimum. Bends must be as equal as possible in the number of left and right bends, and the angle of the bend must be greater than or equal to 135 degrees.

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. For decoupling capacitors placed on the opposite layer of the serializer, the return path to the serializer thermal pad should be minimized. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. Figure 4-5 shows the routing of the high-speed serial line, highlighted by the yellow line. The total length of the yellow line is about ½ inch.

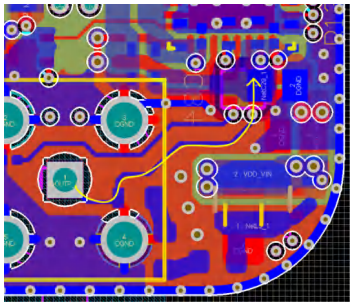


Figure 4-5. DOUT Path on Base Board

4.3.4 Imager Layout Recommendations

CSI-2 lane routing must follow the same guidelines previously outlined for the imager layout. Similarly, decoupling capacitors should be placed as close as possible to the supply pins, with smaller capacitors taking priority in terms of distance to the pin. Minimize the parasitic resistance and inductance to the ground plane with vias and wide traces.

4.3.5 Layout Prints

To download the layer plots, see the design files at TIDA-050060.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050060.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050060.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050060.

5 Related Documentation

1. Texas Instruments, *DS90UB953-Q1 FPD-Link III 4.16-Gbps Serializer With CSI-2 Interface for 2.3MP/60fps Cameras, RADAR, and Other Sensors*, data sheet
2. Texas Instruments, *TPS650330-Q1 Automotive Camera PMIC*, data sheet
3. Texas Instruments, *Power-over-Coax Design Guidelines for DS90UB953-Q1*, application note

6 Trademarks

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265