Design Guide: TIDA-010237

AC and DC Current Fault Detection Reference Design

Description

This reference design detects mA-level AC and DC ground fault currents. An auto-oscillation circuit is implemented using a DRV8220 H-bridge that drives the magnetic core in and out of saturation. In addition, an active filter circuit is implemented to identify fault current signal and level.

Resources

TIDA-010237	Design Folder
DRV8220	Product Folder
MSP430F5132, OPA202	Product Folder
INA293, SN74LVC2G74	Product Folder
TLV7011, TLV172	Product Folder

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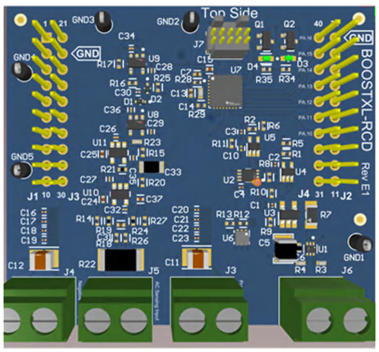
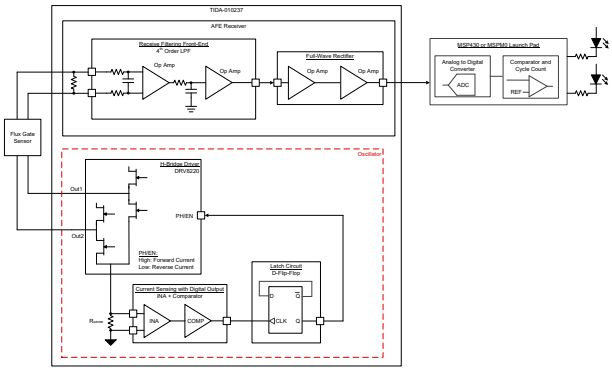
Features

- Low-cost discrete AC and DC ground fault detection circuit
- Designed to sense fault current thresholds of 6 mA DC, 30 mA_{RMS} AC based off IEC62752 and IEC62955
- Detection-to-response time < 25 ms (not including relay delay time)
- Adjustable AC and DC trip thresholds via software
- Auto-oscillation feedback circuit can drive different magnetic core materials with minimal changes to hardware
- Active low-pass filter optimized to attenuate auto-oscillation frequency and amplify fault current signal

Applications

- AC charging (pile) station





1 System Description

Electric vehicles (EVs) receive energy from the electrical grid through electric vehicle supply equipment (EVSE), more commonly known as EV chargers. To facilitate power delivery to the vehicle, the EVSE sits between the grid and the vehicle.

If a ground fault occurs, the EVSE must respond and trip a relay to disconnect power from the grid. The primary requirement in providing protection during EV charging is the ability to detect AC and DC residual currents and mitigate the risk of electrical shock. This system implements residual current detection (RCD) by monitoring the phase lines and neutral wires through a fluxgate sensor. During normal operation without a fault condition, the sum of currents equals zero. During a ground fault condition, the sum of currents is not equal to zero. This residual current indicates a system short which can be an issue at 6 mA DC and 30 mA_{RMS} according to IEC62752, IEC62955.

1.1 Key System Specifications

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT	DETAILS
INPUT CHARACTERISTICS						
Line Frequency	Line through fluxgate sensor		60, 50		Hz	
Phase Line Voltages			Universal		V	
Phase Line Current			Universal		A	
TRIP THRESHOLDS						
Residual DC Current Threshold			6		mA	Adjustable via software
Residual AC Current Threshold			30		mA_{RMS}	Adjustable via software
POINT-OF-LOAD CHARACTERISTICS						
Board positive supply voltage			+12		V	Provided by external power supply
Board negative supply voltage			–12		V	Provided by external power supply
Fluxgate sensor drive voltage	DRV8220		+12		V	H-bridge voltage to drive fluxgate sensor into saturation

2 System Overview

2.1 Block Diagram

Figure 2-1 shows an overview of connections between the fluxgate sensor, filtering circuit, and auto-oscillation circuit.

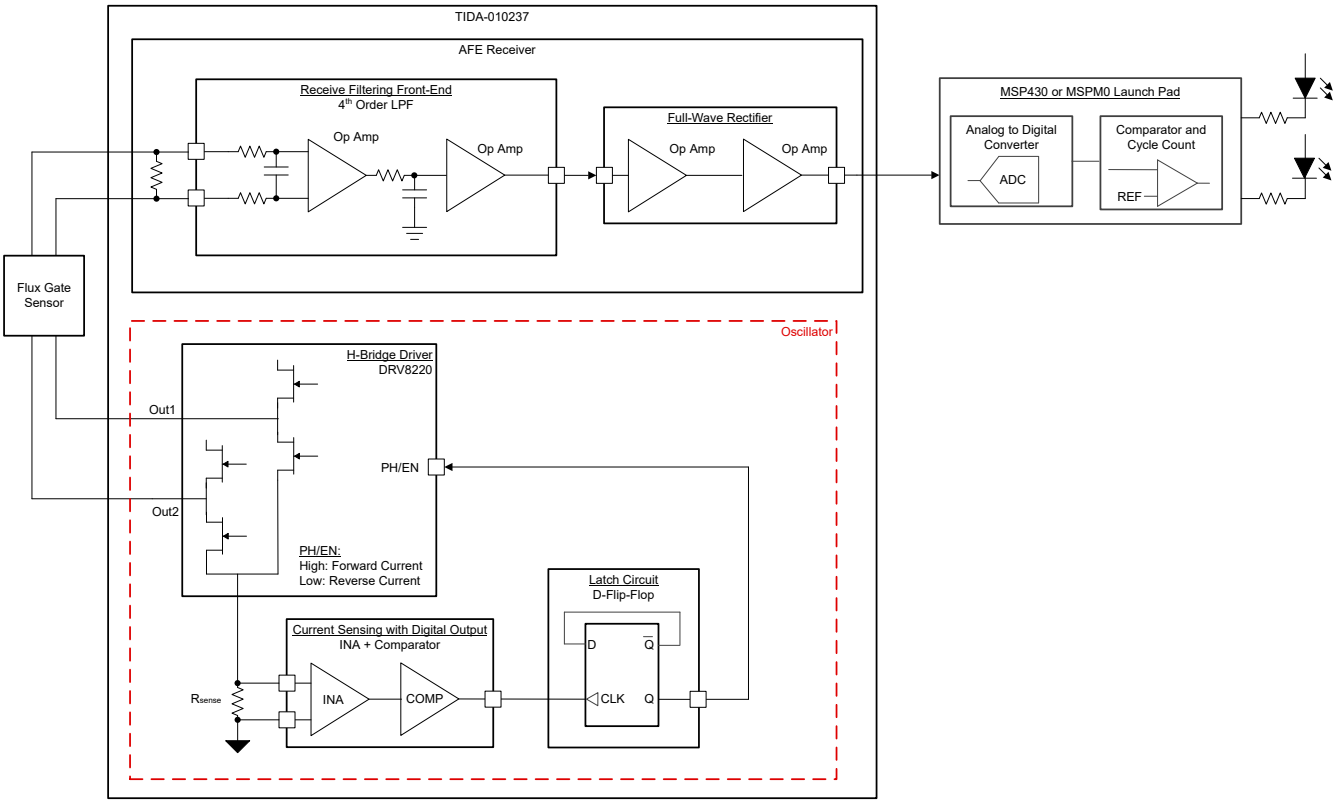


Figure 2-1. Block Diagram

2.2 System Design Theory

2.2.1 Detection Principals

If the current leaving the grid does not equal the current returning, there is a ground fault. This current is traveling somewhere unintended; therefore, risking fires or shock.

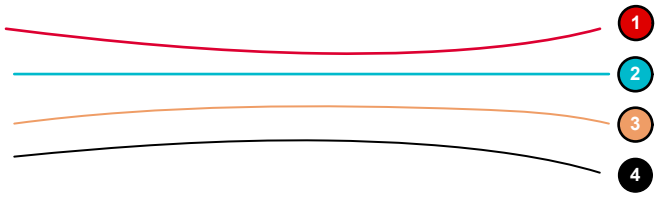


Figure 2-2. Phase Lines and Neutral

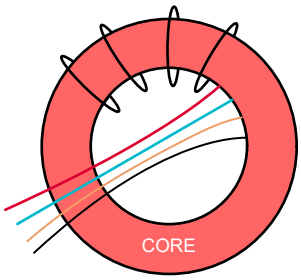


Figure 2-3. Fluxgate Sensor Frontal View

Under normal conditions:

$I_{TOTAL} = I_1 + I_2 + I_3 + I_4 = 0$ A

During a ground fault condition:

$I_{TOTAL} = I_1 + I_2 + I_3 + I_4 \neq 0$ A

For a DC fault condition: $|I_{TOTAL}| > 6$ mA

For an AC fault condition: $|I_{TOTAL}| > 30\ mA_{RMS}$

Note

The threshold values of 6 mA and 30 mA_{RMS} are adjustable via software.

2.2.2 Saturation

Saturation is a state reached when an increase in applied magnetizing *field H* cannot increase the magnetization of the material further, so the total magnetic *field B* levels off. As the H field increases, the B field approaches a maximum value asymptotically, the saturation level for the substance. The magnetic field represents the existing current through a conductor. From this idea, the excited saturable inductor is able to measure current.

The saturation point of ferromagnetic materials depends on magnetic permeability and the amount of current. The core permeability changes both by an external field and an excitation current through the coils wrapping the sensor.

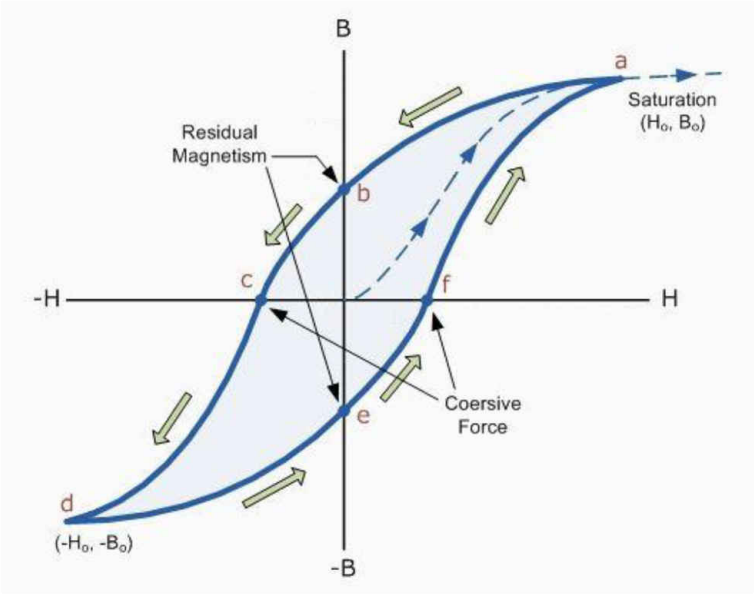


Figure 2-4. Magnetization Curve and B-H Curve

2.2.3 General Mode of Operation

Current through a wire produces a magnetic field. Explained in Detection Principals section, a ground fault produces a magnetic field. Average voltage across the fluxgate burden resistor changes proportional to the ground fault magnetic field. This average voltage is filtered and read to determine if there is a ground fault.

The core is driven into saturation with a driver circuit. Once reaching saturation, the driver circuit switches the direction of the current until the core reaches saturation again. The drive circuit continuously switches the drive current direction every time the core reaches saturation. Prior to saturation, the ambient field is channeled through the core producing a high flux due to the high permeability. At the point of saturation, the core permeability falls away to the vacuum. During the next half cycle of excitation drive current, the core recovers from saturation, and the flux due to the ambient field is once again at a high level until the core saturates in the opposite direction; the cycle then repeats.

2.3 Highlighted Products

2.3.1 DRV8220

The DRV8220 is an integrated H-bridge driver with multiple control interface options: PWM (IN1, IN2) interface, PH, EN,or half-bridge interface. To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and the capacitors.

The integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

2.3.2 OPAx202

The OPA202 (OPAx202) family of devices is a series of low-power, super-beta, bipolar junction transistor (super-β BJT), input amplifiers featuring high-level drift performance and low input bias current. The low output impedance and heavy capacitive load drive abilities allow designers to interface to modern, fast-acquisition, precision analog-to-digital converters (ADCs) and buffer precision voltage references and drive power supply decoupling capacitors. The OPAx202 achieves a 1-MHz gain-bandwidth product and a 0.35-V/µs slew rate, and consumes only 580 µA (typical) of quiescent current, making the devices a great choice for low-power applications. These devices operate on a single 4.5-V to 36-V supply, or dual ±2.25-V to ±18-V supplies.

2.3.3 TLVx172

The TLV172 operational amplifier provides high overall performance, making these devices designed for many general-purpose applications. The excellent offset drift of only 1 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}.

2.3.4 TLV7011

TheTLV701x and TLV702x devices are single-channel, micro-power comparators with push-pull and open-drain outputs. Operating down to 1.6 V and consuming only 5 µA, the TLV701x and TLV702x are designed for portable and industrial applications. The comparators are available in leadless and leaded packages to offer significant board space savings in space-challenged designs.

2.3.5 INA293

The INA293 is a high- or low-side current-sense amplifier that offers a wide common-mode range, precision zero-drift topology, excellent common-mode rejection ratio (CMRR), high bandwidth, and fast slew rate. Different gain versions are available to optimize the output dynamic range based on the application. The device is designed using a transconductance architecture with a current-feedback amplifier that enables low bias currents of 20 µA with a common-mode voltage of 110 V.

2.3.6 SN74LVC1G74

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully-specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

2.3.7 TLV767

TheTLV767 is a low quiescent current, high-PSRR linear regulator capable of handling up to 1 A of load current. Unlike typical high-current linear regulators, the TLV767 consumes significantly less quiescent current. This device is designed for high-current applications that require very sensitive power-supply rails.

This device features integrated foldback current limit, thermal shutdown, output enable, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line- and load-transient performance. This device is low noise and exhibits a very good PSRR. The operating ambient temperature range of the device is –40°C to +125°C.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware

3.1.1 Board Overview

The TIDA-010237 is in a BoosterPack™ Plug-in Module form factor to connect to an MSP430 or MSPM0 LaunchPad™ Development Kit. Figure 3-1 shows the top side of the reference design and highlights the board size that is 5 cm × 5.842 cm as well as the AC/DC Detection and Oscillator subsystems.

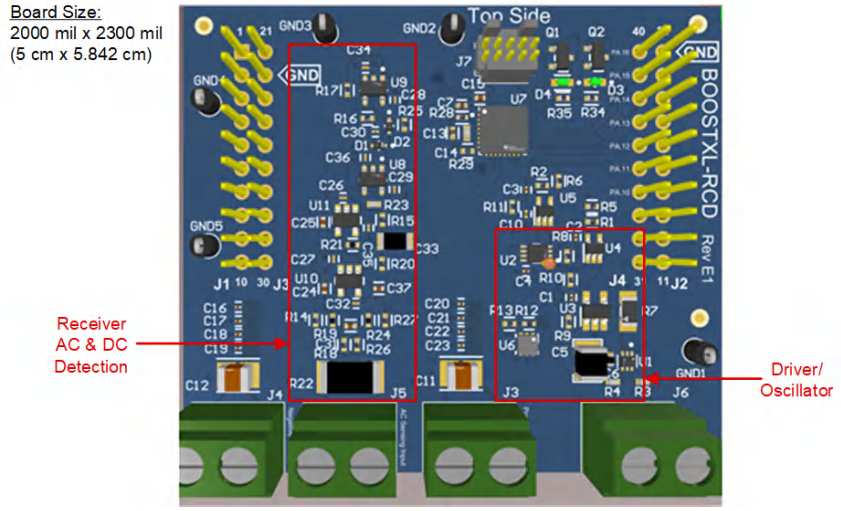


Figure 3-1. Subsystem Location on Board Hardware

Figure 3-2 highlights the connections for both the power supply and sensor to the board. The terminal header J3 and J4 are connections for an external power supply where J3 is for positive12 V and GND. Terminal header J4 is for negative 12 V and GND.

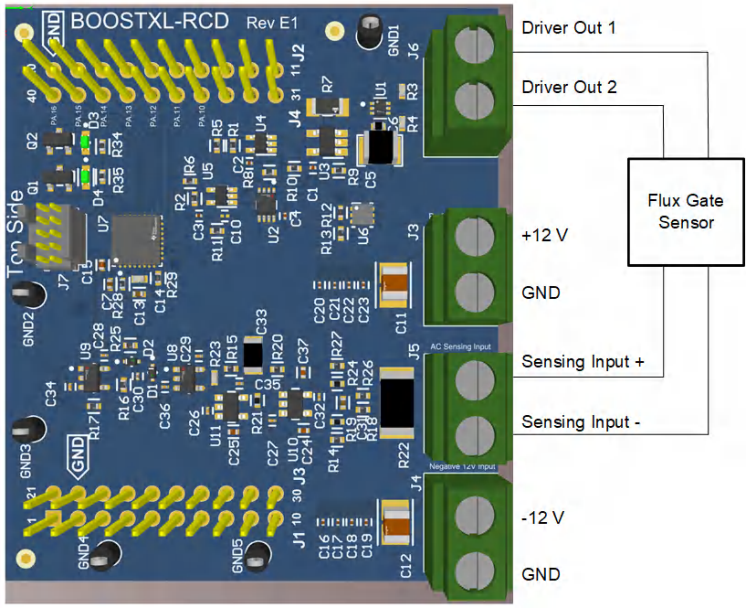


Figure 3-2. Power Supply and Sensor Board Connections

Connector J5 and J6 are for connecting the driving coil on the Hitachi nanocrystalline core. J6 connects one side of the two drive coils to the DRV8220 outputs. J5 connects the other side of the drive coil to a 1-kΩ sense resistor of the receive detection circuit.

3.1.2 Filter Stage

The three goals of filter stage are to gain the ground fault detection signal, filter the noise created by the auto-oscillation circuit, and correct a DC bias inherent to the fluxgate core.

Filter noise in the signal path from the burden resistor to the ADC. Too much noise can trigger false trips. The major source of noise is switching caused by the auto-oscillation circuit generating switching of the DRV8220. The auto-oscillation switching frequency changes with fluxgate sensor permeability, burden resistance, or adjusting the saturation detection circuit. The Hitachi nanocrystalline cores used for testing ranged from 600 Hz–800 Hz with a 1-kΩ burden resistor.

During a fault, the filter stage outputs a detectable signal read by the ADC. A fault trip occurs when the filter stage output signal passes a threshold and the MCU determines the fault type, as AC and DC faults have separate trip thresholds adjustable within software.

In this design with a gain of 20 dB, a DC fault of 6-mA outputs a 200-mV offset. An AC fault of 30-mA_{RMS} outputs a peak of 600 mV. The gain can be increased, make sure the trip threshold is below the rail of op amps.

Filter stage is designed to gain the fault signal by 20 dB and attenuate frequencies above 70 Hz. Figure 3-3 highlights the receiver circuit that consists of a differential to single-ended active low-pass filter and a full-wave rectifier. A DC offset circuit was added in place of R23 to mitigate the offset of the nanocrystalline core.

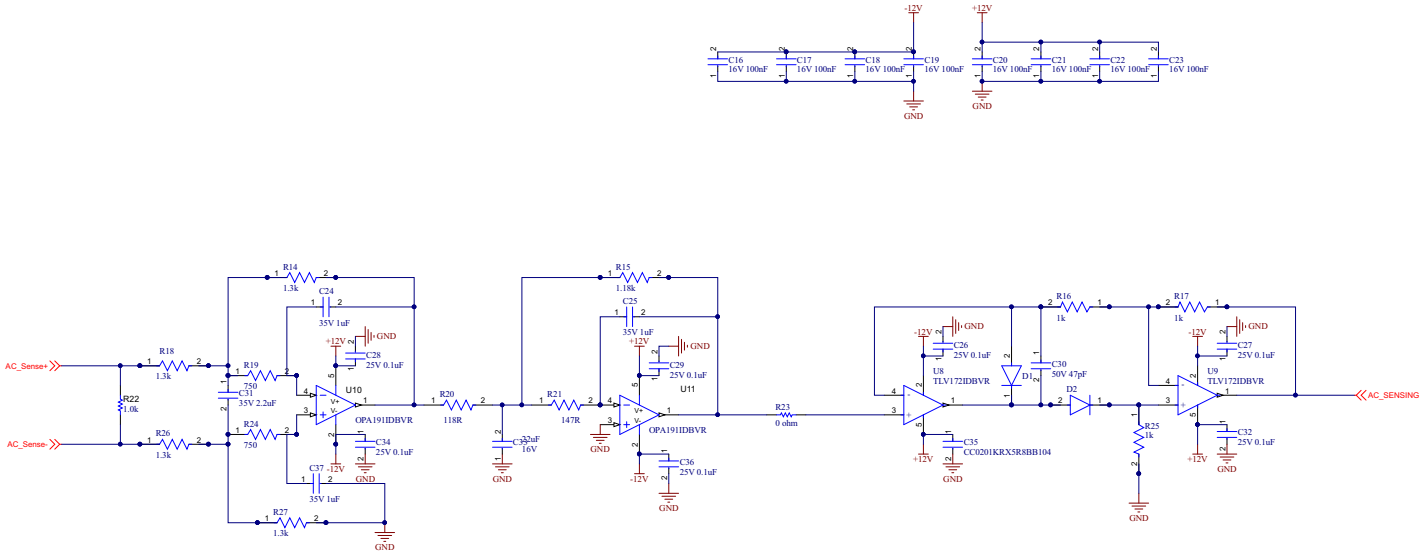


Figure 3-3. Filter Stage Schematic

The filter topology used is the MFB topology (sometimes called infinite gain or Rauch) and is often preferred due to low sensitivity to component variations. The MFB topology creates an inverting second-order stage. This inversion can be a concern in the filter application. The MFB filter circuit can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection. For this application, a fourth-order low-pass filter with a Butterworth response was used.

3.1.3 Differential to Single-Ended Converter

The differential to single-end conversion is performed by the first part of the signal chain. The first op amp converts the differential signal across the fluxgate burden resistor to a single-ended signal. This simplifies later signal conditioning and allows the ADC to read a ground referenced signal. R22 is the burden resistor across the coils of the fluxgate sensor.

Impedance matching to op amp inputs is important to minimize error. Mismatched impedance adds error to the fault detection signal. Trace from R22 to U10 can be similar to reduce error. To increase the ground fault signal, replace R18 and R26 with buffer op amps or resistors an order of magnitude larger.

A higher impedance relative to the burden resistor (R22) gives a higher ground fault signal due to the resistor divider effect.

The first filter stage in Figure 3-4 is used to convert the differential signal across the burden resistor to a single-ended signal. These interface between the burden resistor (R22) of the fluxgate sensor and the TIDA-010237.

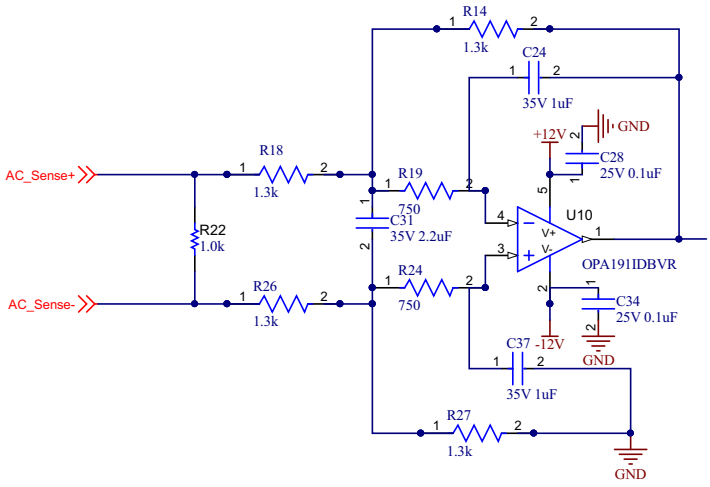


Figure 3-4. Differential to Single-Ended Schematic

3.1.4 Low-Pass Filter

The low-pass filter is optimized to attenuate auto-oscillation frequencies. The goal is to reduce noise to prevent false trips. This design has a gain of 20 dB at 0 Hz and a cutoff frequency of 70 Hz.

The auto-oscillation frequency depends on many variables: magnetic core material, burden resistance, and the auto-oscillation signal chain. This design with a nanocrystalline core material results an oscillation around 800 Hz.

The low-pass filter is optimized to attenuate noise created by the auto-oscillation circuit.

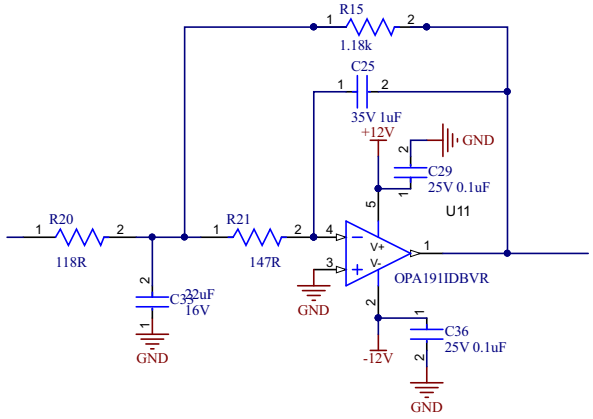


Figure 3-5. Low-Pass Filter Schematic

3.1.5 Full-Wave Rectifier

The full-wave rectifier only flips negative voltage to positive. The full-wave rectifier allows the same trip threshold for negative and positive fault current. The other reason for using the full-wave rectifier is to convert the negative polarity of the signal to positive voltage within the input range of the ADC of the MCU and prevent Electrical Overstress (EOS).

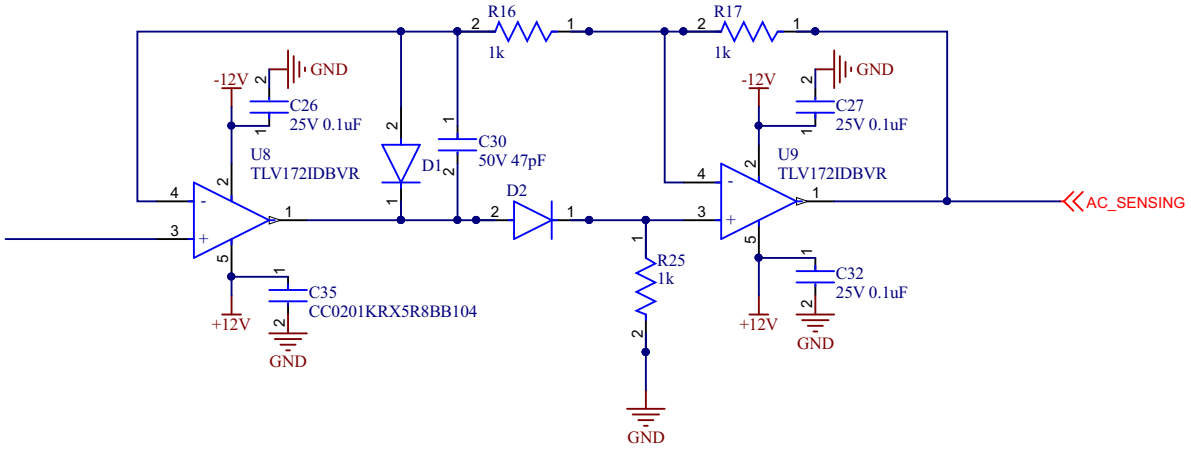


Figure 3-6. Full-Wave Rectifier Schematic

This precision full-wave rectifier can turn alternating current (AC) signals to single polarity signals. The op amps, U8 and U9, buffer the input signal and compensate for the voltage drops across D1 and D2 allowing for small signal inputs. The circuit is used in this application to quantify the absolute value of input signals which have both positive and negative polarities.

This topology was chosen over other full-wave rectifier topologies for the simplicity while achieving the desired performance. U1A and U1B control the biasing of D1 and D2 to change the signal path based on the polarity of the input signal achieving the full-wave rectification. The input impedance of the circuit is set by the termination resistor R4 and can be set to match the source impedance or as high as the input impedance of the U1A amplifier.

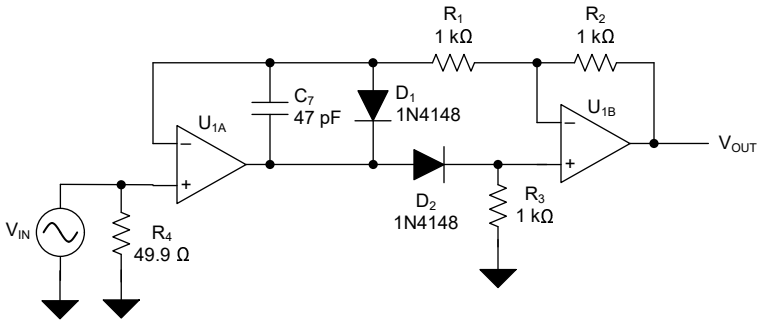


Figure 3-7. Circuit Schematic

Figure 3-8 and Equation 1 show the circuit schematic and transfer function for positive input signals. Positive input signals reverse-bias D1 and forward-bias D2 make the components act like an open circuit and short circuit respectively. In this configuration, the U1A amplifier drives the non-inverting input of U1B such that the voltage at the inverting input of U1A is equal to V_{IN}. Because current does not flow into the high-impedance inverting input of U1A, there is no current through R1 or R2 and U1B acts as a buffer. U1A must therefore also act as a buffer and V_{OUT} is simply equal to V_{IN}.

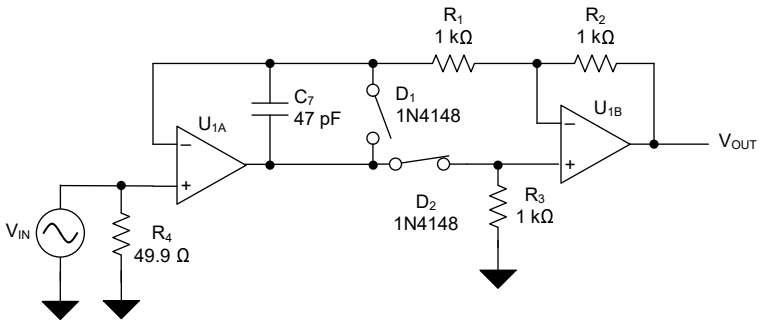


Figure 3-8. Simplified Circuit for Positive Input Signals

$$V_{OUT} = V_{IN} \quad (1)$$

Figure 3-9 and Equation 2 show the circuit and transfer function for negative inputs. Negative input signals forward bias D1 and reverse bias D2. Therefore, U1A drives U1B like a standard inverting amplifier while R3 biases the non-inverting node of U1B to GND. In this configuration, the output is now positive for negative input signals achieving the full-wave rectification.

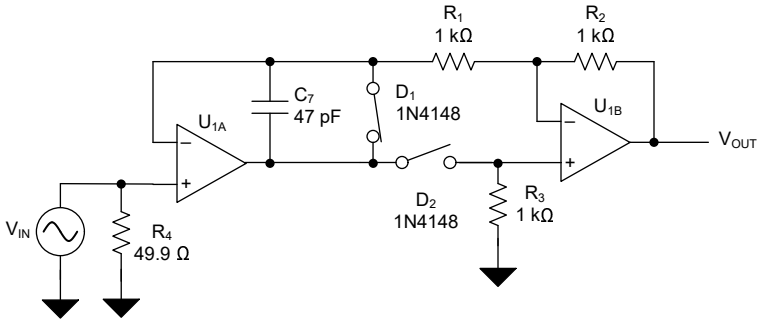


Figure 3-9. Simplified Circuit for Negative Input Signals

$$\frac{V_{OUT}}{V_{IN}} = \left(-\frac{R_2}{R_1}\right) \quad (2)$$

$$\frac{V_{OUT}}{V_{IN}} = -1\frac{V}{V} \quad (3)$$

3.1.6 DC Offset Circuit

In place of 0 Ω R23, a DC offset circuit was used. The auto-oscillation duty cycle was found to be 50.10% at steady state with no fault condition. For the best case, the duty cycle is 50.00% with no fault condition. This duty-cycle shift resulted in a consistent 200-mV DC offset evident on the final output of the filter stage. The DC offset is an issue,because thresholds for positive and negative fault current are not the same. By zeroing the AC_SENSING output, both negative and positive ground fault current have the same threshold. This offset is due to the magnetic core and can vary depending on material used.

Figure 3-10 shows the schematic for the dual-supply, inverting amplifier circuit configuration.

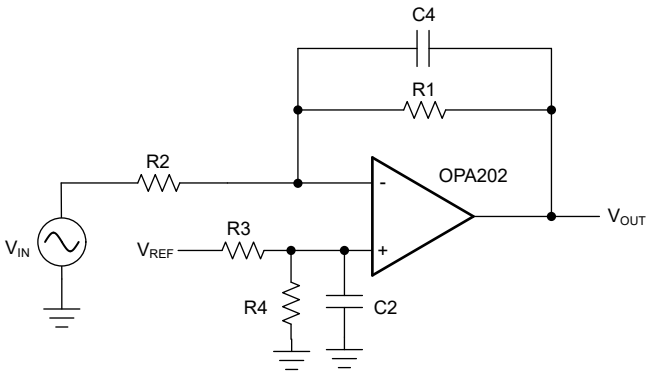


Figure 3-10. Dual-Supply, Inverting Amplifier Circuit Schematic

The inverting op-amp configuration takes an input signal that is applied directly to the inverting input terminal and outputs a signal that is the opposite polarity as the input signal. The benefit of this topology is that the topology avoids common-mode limitations. The load resistance for this topology is equal to R2. The values of the resistors in the feedback network determine the amount of gain to amplify the input signal.

Equation 4 displays the transfer function for the dual-supply, inverting amplifier circuit configuration with level shifting input shown in Figure 3-10.

$$V_{OUT} = \left(-\frac{R_1}{R_2}\right)V_{IN} + \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_4}{R_3 + R_4}\right)V_{REF} \quad (4)$$

Capacitor C2 filters noise that can be introduced from the V_{REF} input. Equation 5 calculates the cutoff frequency due to C2.

$$f_{C\_Vref} = \frac{1}{2\pi \times R_3//R_4 \times C_2} \quad (5)$$

Capacitor C4 provides the option to filter the output. The cutoff frequency of the filter can be calculated using Equation 6.

$$f_{C\_Vout} = \frac{1}{2\pi \times R_1 \times C_4} \quad (6)$$

3.1.7 Auto-Oscillation Circuit

The Auto-Oscillation sub-circuit detects when the fluxgate sensor reaches saturation, then reverse the current direction. When saturation is reached, current sense voltage exceeds the comparator threshold, which causes the D-type flip-flop to flip control signals to the DRV8220 H-bridge. This drives the fluxgate sensor core to saturation in the opposite direction.

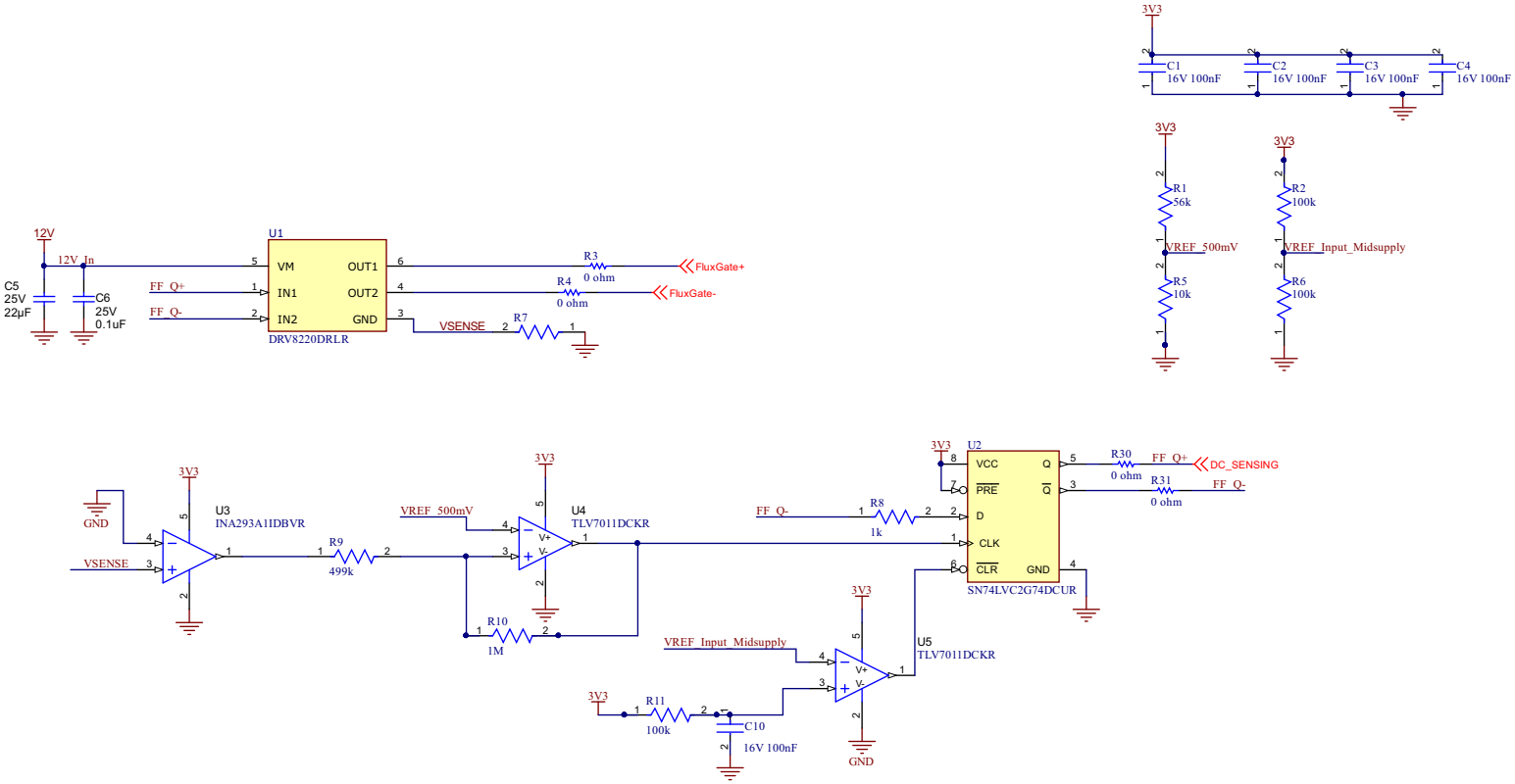


Figure 3-11. Auto-Oscillation Circuit Schematic

This circuit monitors the current flowing through the fluxgate and reverses drive current direction once saturation is reached. The auto-oscillation circuit is needed to detect DC faults.

The phase lines and neutral wires go through a fluxgate sensor. During normal operation without a fault condition, the sum of currents equals zero.

During a ground fault condition, the sum of currents is not equal to zero. During a DC fault, there is an imbalance of current flowing through the line and current returning through the neutral wire. The fluxgate is blind to steady DC current. An oscillating drive current is pushed through the fluxgate sensor coil. This DC fault current produces a magnetic field which opposes fluxgate drive in one direction, and assists fluxgate drive in the opposite direction; resulting in a duty cycle shift. Under normal conditions, the duty cycle of the switching is 50%. During a DC fault, the duty cycle shifts.

The oscillation frequency depends on the signal chain between R7 to pin 1 of the DFF. Match the current sense amplifier gain and VREF voltage to make sure the core is driven to saturation. Driving the core deeper into saturation reduces noise, removing the need for degaussing. When the core is fully saturated, all material within the core is magnetically aligned. When all material is aligned, there are no stray fields within the material to contribute noise.

3.1.8 DRV8220 H-Bridge

The DRV8220 drives current through the magnetic core to saturate the core. This device is the smallest, most cost-effective device capable of driving enough current.

The DRV8220 is an integrated motor driver with four N-channel power FETs, charge pump regulator, and protection circuitry. The device can supply up to 1.76 A of output current, operating on a supply voltage from 4.5 V to 18 V. The driver offers robust internal protection including undervoltage lockout, output overcurrent, and device overtemperature.

The low-side current sense resistor (R7) detects current through the DRV8220. The current spikes when the core reaches saturation, which is read by the saturation detection circuit.

The output of the DRV8220 is controlled by pins 1 and 2. The state of these pins determines which direction current flows through the magnetic coil. When the saturation detection circuit threshold is passed, the control signals to pins 1 and 2 flip, which flips the DRV8220 output.

DRV8220 output 1 and 2 are used to drive are used to drive the fluxgate sensor coil to saturation. The low-side current sense resistor is used by the saturation detection circuit to know when saturation is reached.

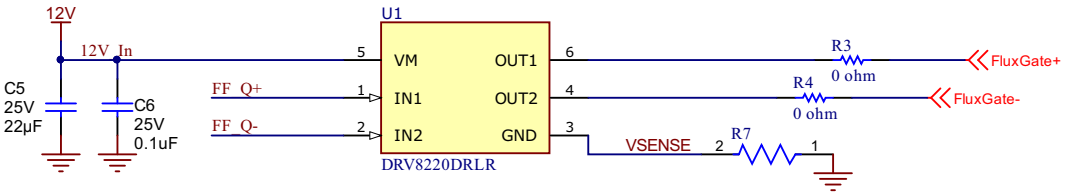


Figure 3-12. DRV8220 Schematic

The current through VSENSE peaks when the core reaches saturation.

3.1.9 Saturation Detection Circuit

The saturation detection circuit is made of the low-side current sense resistor (R7), current sense amplifier INA293, and comparator TLV7011. The comparator outputs high when the fluxgate sensor coil saturation is reached.

This circuit is used to determine when the fluxgate sensor has reached saturation.

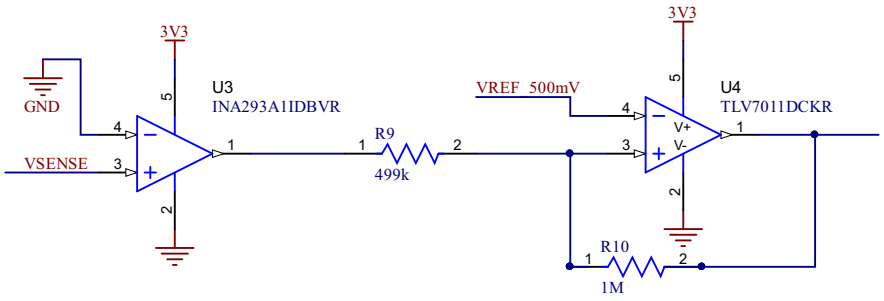


Figure 3-13. Saturation Detection Schematic

V_{SENSE} is read from the low-side shunt resistor of the DRV8220. V_{SENSE} gives the current through the fluxgate sensor coil. This signal is gained by current sense amplifier INA293, with a fixed gain of 20 V/V. The gained signal is compared to a reference voltage V_{REF} of 500 mV which is sourced from a resistor divider. When the current sense signal passes the V_{REF} voltage, the core has saturated and the DRV8220 must swap output directions. The output of comparator TLV7011 feeds into a DFF which is explained more in the H-Bridge Controlled by DFF section.

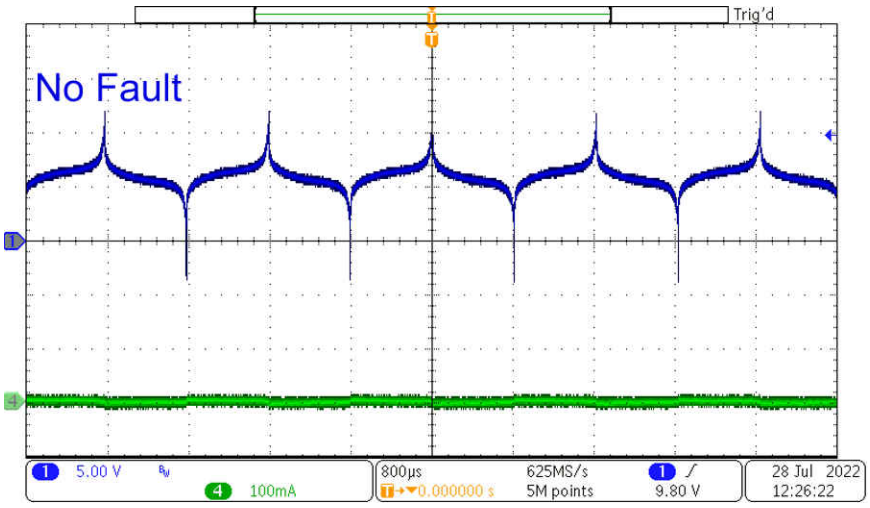


Figure 3-14. Burden Resistor Going Into Saturation

3.1.10 H-Bridge Controlled by DFF

The digital flip-flop uses the output logic to control the DRV8220 output current direction. The flip-flop circuit changes output Q with each positive CLK edge.

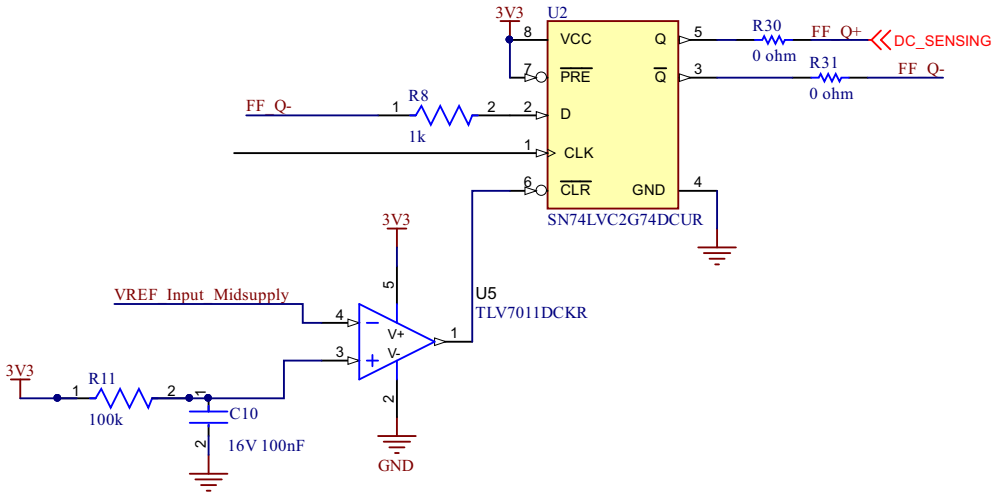


Figure 3-15. DFF SN74LVC2G74 Circuit

Inverted output !Q is connected to input data D, so each positive clock edge inverts the outputs.

3.1.11 MCU Selection

For this design, the MSP430F5132 MCU was originally chosen for the high clock speed required for timer capture DC fault detection. Use a lower-cost MCU instead, since a high clock speed was a requirement for duty cycle detection using the timer capture method. The timer capture method directly measured duty cycle changes by triggering a timer on each duty cycle edge, so a high clock speed was required. This timer capture method is used in many existing RCD modules. With testing, it was determined that a lower BoM cost is achieved by reading DC fault with an ADC instead of using the timer capture method.

The most important specification of MCU choice is the integrated ADC.

The ADC must have an effective resolution small enough to consistently differentiate between a fault. This design sees a 200-mV filter output during a 6-mA DC fault, and 600-mV maximum filter output during an 30-mA_{RMS} AC fault[1]. This design uses a 10-bit ADC with a full scale range of 1.5 V integrated in the MSP430F5132 MCU.

[1] These fault threshold values can be increased by increasing the gain of the filter stage.

The ADC needs a sample speed faster than 2000 samples per second. The software stores the low value read by the ADC and uses the low value to determine if an AC or DC fault occurred. The ADC must sample quickly enough to consistently detect a low value during an AC waveform to differentiate AC versus DC fault.

The largest source of noise is the ADC reference voltage error. This design has a total reference voltage error of 1.5%. This is the most significant source of error. The fault detection signal needs to be gained enough to make this error insignificant.

3.1.12 Move Away From Timer Capture

Timer capture is a method to read the DC fault by reading duty cycle shifts from the auto-oscillation circuit. This is a common measurement technique in RCD modules. With a DC fault condition, the duty cycle of the DRV8220 shifts as the B-H curve or magnetization curve loop shifts. The DC fault current through the core causes saturation slightly quicker in one direction than the other. This translates into a measurable shift in duty cycle.

This approach was sensitive to noise in components, oscillators, and magnetic cores. This approach is found to require more expensive components with less delay, and faster MCU clock speeds. There was a large inconsistency of duty cycle shift dependent on which magnetic core was used. In many cases, the jitter caused by noise blinded the signal, causing false trips.

Reading a DC fault with an ADC on the output of the filter path resulted in a lower cost BoM and more accurate readings over a broader selection of fluxgate sensor material types.

3.1.13 Differentiating DC and AC From the Same Signal

DC fault and AC fault have different trip thresholds. In this design, a DC fault of 6 mA translates to 200-mV input to ADC. An AC fault of 30 mA_{RMS} translates to 600-mV input to ADC. To avoid false trips, the system must differentiate an AC fault signal from a DC fault signal.

The MSP430F5132 MCU monitors the voltage with an integrated ADC to determine which type of fault is seen. The fault type is determined in software by saving the highest and lowest values read by ADC. The MCU compares the highest and lowest ADC readings to the trip thresholds.

3.1.14 Fluxgate Sensor

Fluxgate sensors measure magnetic fields by periodically saturating a piece of ferromagnetic core material in alternating directions. When an external magnetic field is present, the periodic saturation is offset and measured. Fluxgate performance is limited by intrinsic magnetic noise of the core as the core saturates.

A ground fault creates a magnetic field due to the imbalance of current through line and return current through neutral.

Magnetics are created by current going through a wire. When equal current flows in opposite directions, the sum of magnetic fields cancels out. To detect mA levels of fault current, a soft magnetic material that has a high permittivity and low coercivity is needed. The Hitachi core used for this design is FT-3K70T F2520C which is a nanocrystalline core. For questions on magnetic core selection and availability see *Amorphous and Nanocrystalline* at Hitachi Metals.

3.2 Software Requirements

When the MSP430F5132 ADC detects an AC or DC fault, a GPIO outputs high to trip a relay. When the ADC detects a fault is has been cleared and is below a set threshold, the GPIO outputs low to reset the relay.

3.2.1 Software Description for Fault Detection

The MSP430F5132 internal ADC polls a filtered signal.

When a voltage greater than DC trip threshold is detected, the MSP430 enters a monitor mode. The highest and lowest readings determine whether a DC fault or AC fault has occurred. While in monitor mode, the highest and lowest values are saved over a detection window greater than 10 ms. The detection window needs to be more than 10 ms to make sure 0 V is detected if an AC fault occurs.

The code sequence is as follows:

1. MCU samples ADC
2. DC trip threshold is passed[2]
3. Wait the duration of the detection window in milliseconds. A time of 13 ms was found to be most consistent to detect a zero during an AC fault. The window must be larger than 10 ms to detect a zero of a 50-Hz AC fault[3]
4. Save the highest and lowest recorded values
5. If the lowest value is greater than the DC trip threshold, a DC fault occurred.
6. If the lowest value is near zero and the highest value is greater than the AC trip threshold, an AC fault occurred
7. Trip type, AC or DC, is saved. GPIO output high.
8. When the fault condition clears below hysteresis, GPIO returns low. Relay is reset via GPIO low.

If the lowest ADC reading is greater than the DC trip threshold, a DC fault occurred and the system trips the relay.

If the lowest ADC reading is zero, and the highest reading is greater than the AC trip threshold, an AC fault occurred and the system trips the relay.

This is how the software differentiates between the two fault types. The software must differentiate AC versus DC because the trip thresholds are different for each.

[2] Use whichever threshold is lower: AC or DC. In this design, DC trip threshold is lower.
[3] Ten ms is half the period of 50 Hz. Because the AC fault is full-wave rectified, half the period makes sure a zero is detected and successfully detects an AC fault.

3.3 Test Setup

3.3.1 Ground-Fault Simulation

Faults were simulated with an additional wire running through the magnetic toroidal core with the 3 phase and neutral line. The additional wire was connected to a separate power supply and controllable load to control the fault current amplitude and confirm circuit trip levels of 6-mA DC or 30-mA_{RMS}. In addition to threshold testing, the GPIO of the MCU was measured to confirm when the system detected a fault and determine system response time.

3.4 Test Results

3.4.1 Linearity Over Temperature

The design was tested from –40°C to 105°C, and measurements were taken at the output of the 4th order low-pass filter to measure output voltage versus fault current. The fault current input range was –10 mA to +10 mA. Figure 3-16 shows the output voltage of the active filters versus the fault current at different temperatures. The temperature drift is at a worst case of ±0.8 mA.

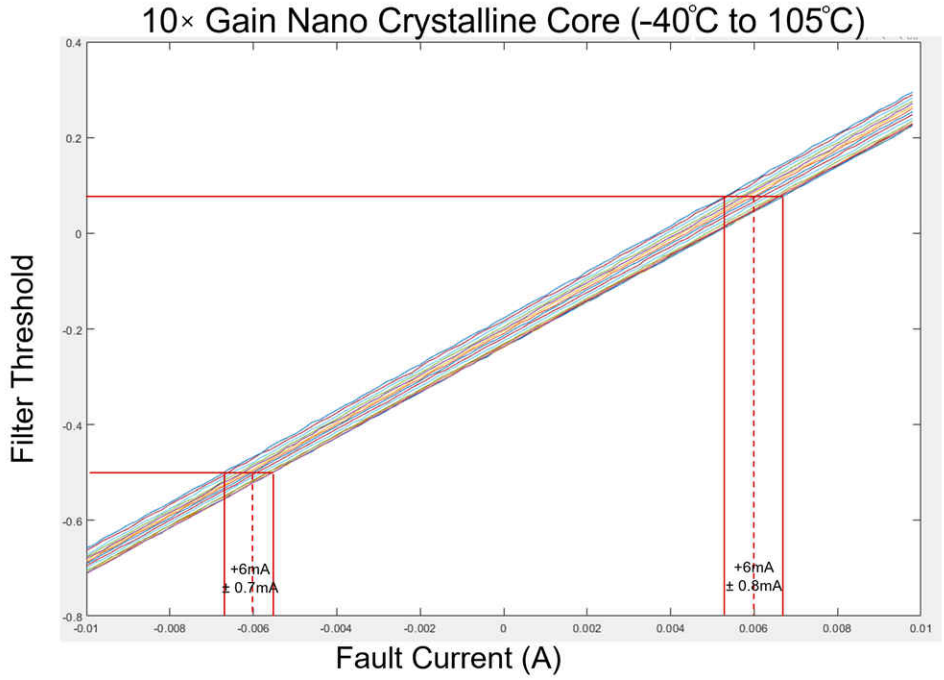


Figure 3-16. Filter Output vs Fault Current

3.5 Fault Response Results

Response time was measured for both AC and DC faulty currents. In Figure 3-17, the TIDA-010237 is sensing a 30 mA_{RMS} and resulted in a response time of approximately 18 ms.

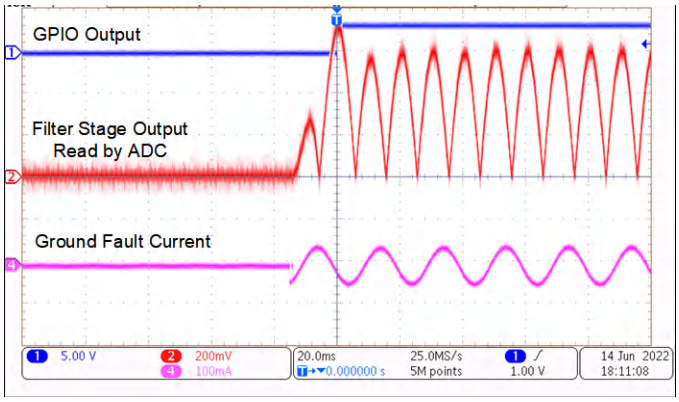


Figure 3-17. System Response to 30-mA_{RMS} Fault Current

In Figure 3-18, the TIDA-010237 is sensing 6 mA and resulted in a response time of approximately 24 ms.

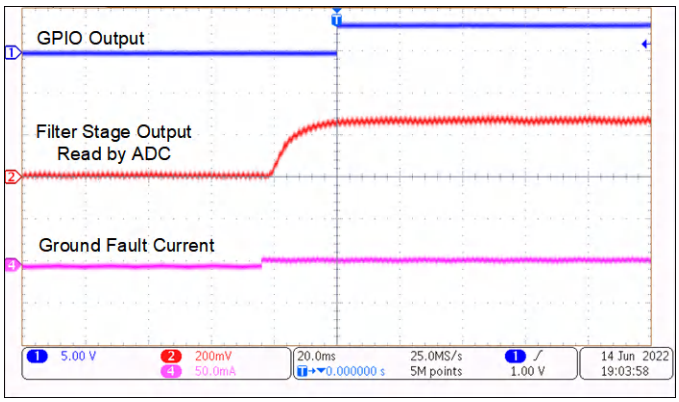


Figure 3-18. System Response to 6-mA Fault Current

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010237.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010237.

4.2 Documentation Support

1. Texas Instruments, *Precision Full-Wave Rectifier, Dual-Supply* design guide
2. Texas Instruments, *DIYAMP-SOIC-EVM* user's guide
3. Texas Instruments, *DRV8220 18-V H-Bridge Motor Driver with PWM, PH/EN, and Half-Bridge Control Interfaces and Low-Power Sleep Mode* data sheet
4. Texas Instruments, *OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers* data sheet
5. Texas Instruments, *TLVx172 36-V, single-supply, low-power operational amplifier for cost-sensitive systems* data sheet
6. Texas Instruments, *INA293 –4 V to 110 V, 1.3-MHz, Ultra-Precise Current Sense Amplifier* data sheet
7. Texas Instruments, *SN74LVC1G74 Single Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset* data sheet
8. Texas Instruments, *TLV767 1-A, 16-V Precision Linear Voltage Regulator* data sheet

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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5 About the Author

ERROL LEON graduated with BSEE and MSEE from Cal Poly San Luis Obispo in 2015. Works with Texas Instruments Grid Infrastructure team with a focus on electric vehicle charging and smart meter. Has experience with analog front end signal chains, PLC, and communication protocols.

CAMERON WUTZKE graduated with BSEE from University of Washington in 2019. Works with Texas Instruments Grid Infrastructure team with a focus on electric vehicle charging. Has experience with embedded systems and analog front-end signal chains.

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