Design Guide: TIDA-010191

Space-Grade, Multichannel, JESD204B 15-GHz Clock Reference Design

Description

Digital beamforming, typically requires a data converter per antenna, and each converter needs a clock with a defined phase relationship. This reference design shows how to generate ultra-low noise MHz to GHz clock signals with defined and adjustable phase relationship that supports JESD204B and 10 ps board-to-board skew.

Resources

TIDA-010191	Design Folder
ADC12DJ3200-SP	Product Folder
ADC12DJ3200EVM	Tool Folder
LMK04832-SP	Product Folder
LMX2615-SP	Product Folder
TSW14J57EVM	Tool Folder

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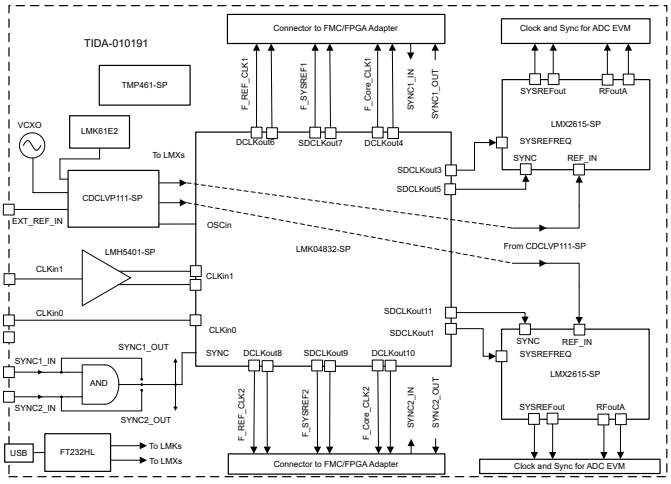
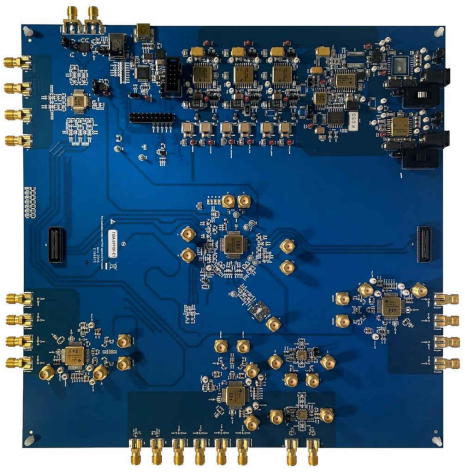
Features

- Up to 15-GHz sample clock generation
- Multichannel JESD204B-compliant clock design
- Less than 10-ps clock skew between channels
- Low-phase noise (< 100 fs) clocking for RF sampling ADC and DAC
- Configurable phase synchronization to achieve low skew in multichannel system
- Radiation hardened high-speed ADC, clocking, RF amplifiers, and point-of-load power devices

Applications

- Communications payload
- Radar imaging payload
- Command and data handling (C and DH)





1 System Description

Phased-array antennas and digital beamforming (DBF) are key technologies with the ability to boost the performance of many satellite applications such as spaceborne radar imaging and broadband satellite communication systems. Digital beamforming unlike analog beamforming, typically requires a set of data converters per antenna element which in turn need precise synchronization. Digital beamforming enables performance improvement and increased flexibility, allowing for new operating modes. One example of this is high-resolution synthetic aperture radar (SAR), a novel radar technique first used in a space-based application by NASA-ISRO in the NISAR project under the name SweepSAR. Beamforming is also a core building block of the 5G mobile broadband universe. In this context, it makes minimal difference whether the 5G transmission is ground-based or spaceborne. Similar to radar applications beamforming in 5G benefits as well from going digital and the clocking requirements are very similar between both application areas.

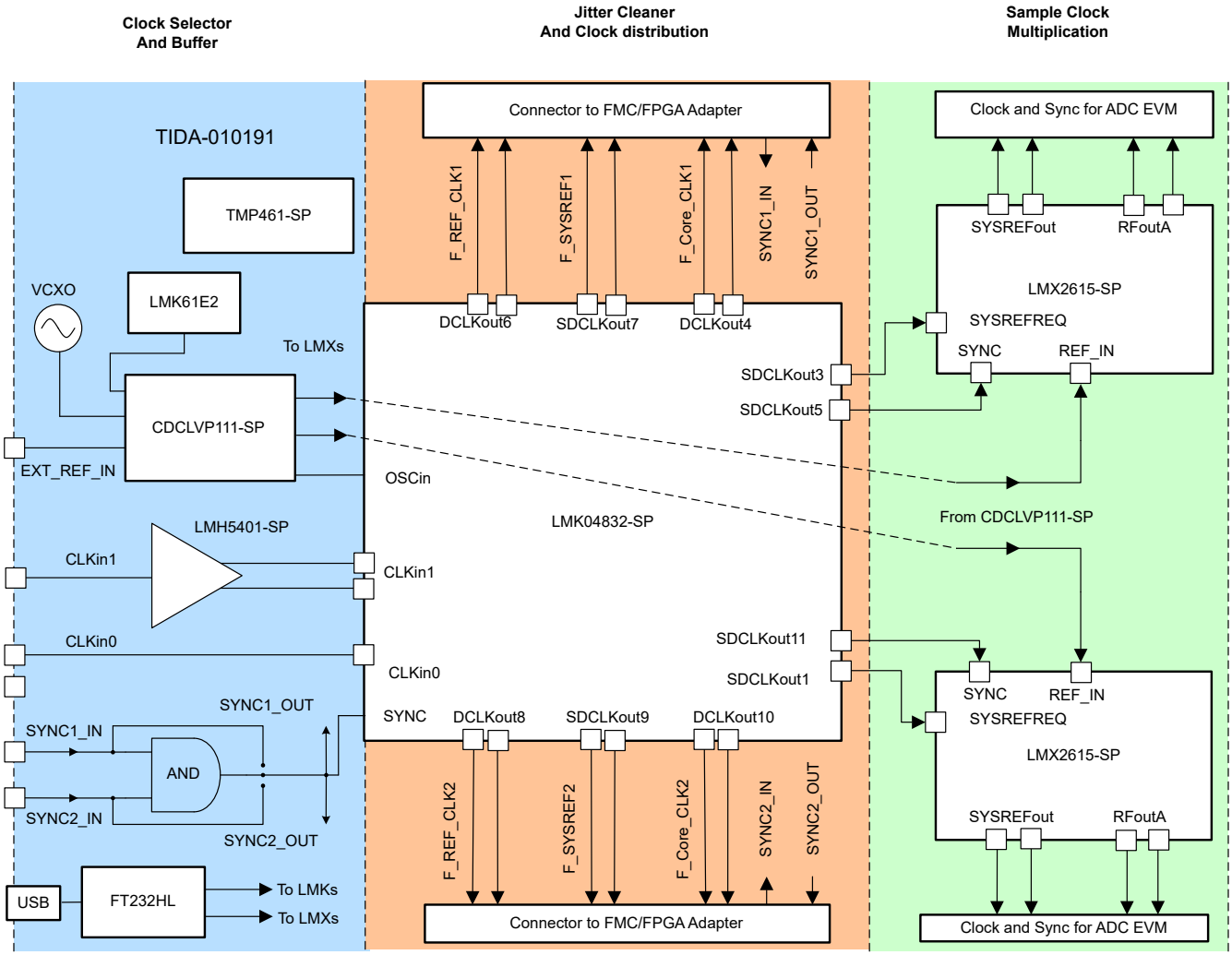


Figure 1-1. Clock Subsystem

The focus of this reference design is on the clocking subsystem for the high-speed GSPS JESD204B-enabled ADC12DJ3200QML-SP data converter. The design demonstrates a multichannel, phase-synchronized clocking platform that can be used in applications with precise synchronization requirements across elements. In the minimal form, the design has two high-speed channels for demonstration purposes. Figure 1-1 shows the block diagram of the design. The clock system divides into three main parts: input clock selector and clock reference buffer CDCLVP111-SP, jitter cleaner and clock distribution LMK04832-SP, and sample clock multiplier LMX2615-SP. The heart of the system is the LMK04832-SP. This device removes the jitter from the incoming clock and creates a stable clock framework. The LMK04832-SP also sources the FPGA clocks and the SYSREF signals. For the input clock of the LMX2615-SP clock multiplier, the reference design can be configured to either

use a clock output of the LMK04832-SP or an output of the input clock reference buffer CDCLVP111-SP. When the incoming clock has already very-low phase noise, then connecting the LMX2615-SP to the CDCLVP111-SP gives the lowest possible output phase noise for the ADCs. The LMX2615-SP can then take this base clock and use fractional multiplication techniques to generate an up to 15-GHz sampling clock tunable to sub-Hertz accuracy. The system also routes the SYSREF through to the ADC subsystem.

The design features three LMX2615-SP devices but only two of them are used for the technical analysis in this document. Therefore, the diagrams also show only two RF PLL synthesizers. The third LMX2615-SP can, for example, be used as the source for the local oscillator input of a down converter to support higher input frequency bands or other superheterodyne principles.

1.1 Key System Specifications

The objective of the design is to demonstrate the high-speed clocking design for a multichannel, RF sampling receiver signal chain. This design focuses on the space-grade low-noise clock design performance based on the LMX2615-SP and LMK04832-SP and their impact on multichannel synchronization and SNR of ADC12DJ3200QML-SP. The data capture is done by the TSW14J57EVM, which is interfaced with the ADC12DJ3200EVMCVAL using the FMC+ adapter card. Table 1-1 lists the key system-level specifications for the multichannel signal chains from the clocking design perspective.

Table 1-1. Key System Parameters

PARAMETER	SPECIFICATIONS	CONDITIONS
Dev_Clk phase noise	–111.5 dBc / Hz at 10-kHz offset –115.3 dBc / Hz at 100-kHz offset –121.9 dBc / Hz at 1-MHz offset –146.3 dBc / Hz at 10-MHz offset –150.9 dBc / Hz at 40-MHz offset	at 7 GHz
	–104.9 dBc / Hz at 10-kHz offset –111.4 dBc / Hz at 100-kHz offset –121.9 dBc / Hz at 1-MHz offset –146.0 dBc / Hz at 10-MHz offset –153.0 dBc / Hz at 40-MHz offset	at 9 GHz
	–100.8 dBc / Hz at 10-kHz offset –107.2 dBc / Hz at 100-kHz offset –114.3 dBc / Hz at 1-MHz offset –140.4 dBc / Hz at 10-MHz offset –151.0 dBc / Hz at 40-MHz offset	at 15 GHz
SNR (dBFS) (dual-channel mode) (JMODE3)	55.5	at a 997-MHz ADC input signal
	55	at a 2482-MHz ADC input signal
	53	at a 4997-MHz ADC input signal
Multichannel clock time skew	< 10 ps	at a 997-MHz ADC input signal
		at a 2482-MHz ADC input signal
		at a 4997-MHz ADC input signal

2 System Overview

2.1 Design Block Diagram

Figure 2-1 shows the block diagram of the measurement setup consisting of the high-speed multichannel clock design interface with ADC12DJ3200EVMCVAL evaluation modules and TSW14J57EVM capture cards. ADC12DJ3200EVMCVAL is interfaced with the TSW14J57EVM data capture board through an FMC+ adapter board. ADC DCLK and SYSREF are provided directly from the TIDA-010191 clocking board through length-matched cables with SMA connectors.

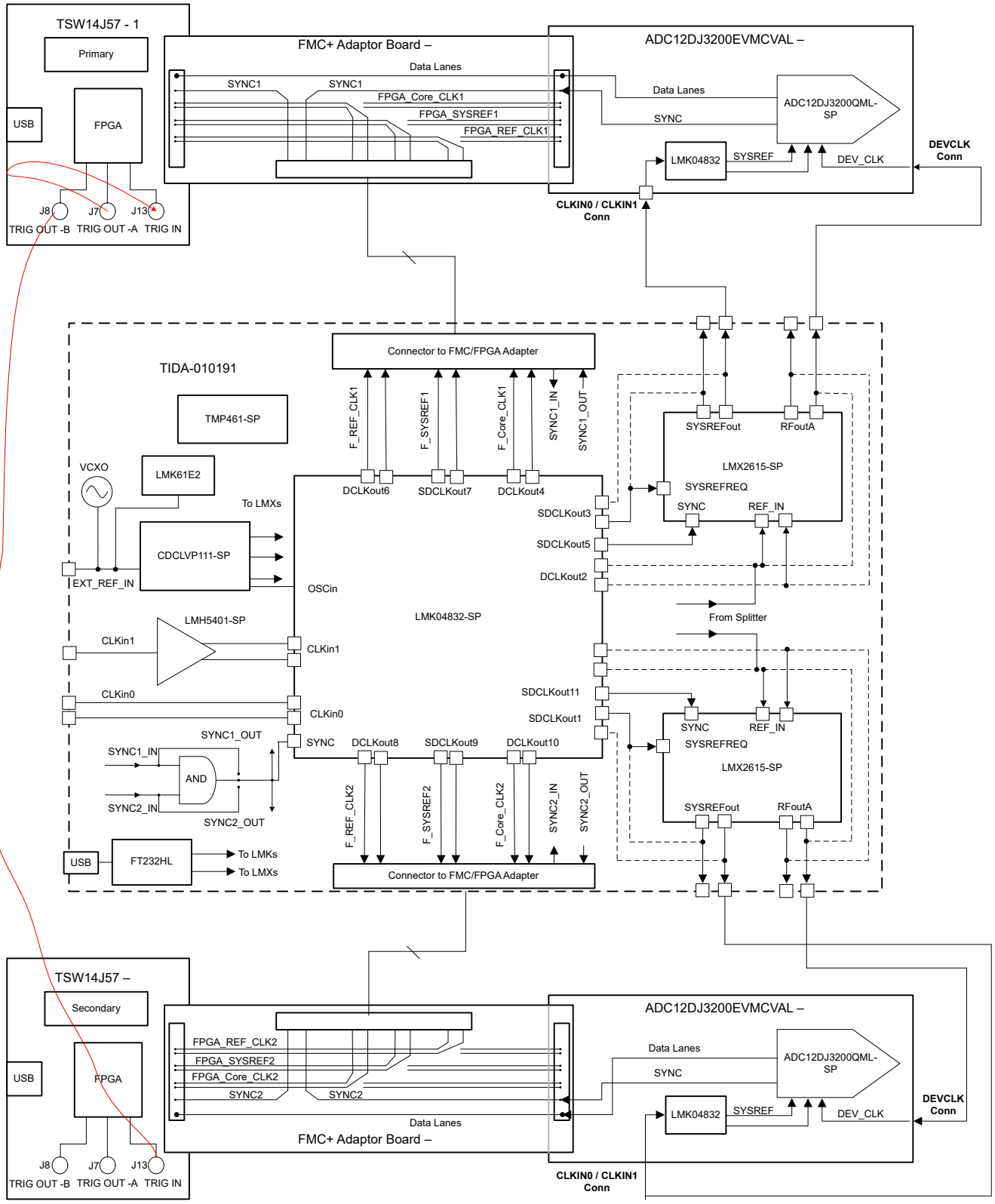


Figure 2-1. Measurement System Setup

2.2 Highlighted Products

2.2.1 LMK04832-SP

The LMK04832-SP is a high-performance clock conditioner with JEDEC JESD204B support for space applications. The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high-performance outputs for traditional clocking systems.

The LMK04832-SP can be configured for operation in dual-PLL, single-PLL, or clock-distribution modes with or without SYSREF generation or reclocking. PLL2 can operate with either internal or external VCO. The high performance combined with features like the ability to trade off between power and performance, dual VCOs, dynamic digital delay, and holdover allows the LMK04832-SP to provide flexible high-performance clocking trees. The LMK04832-SP is a 10.9-mm × 10.9-mm, 64-pin CFP package.

2.2.2 LMX2615-SP

The LMX2615-SP is a high-performance wideband phase-locked loop (PLL) with integrated voltage controlled oscillator (VCO) and voltage regulators that can output any frequency from 40 MHz and 15.2 GHz without a doubler, which eliminates the need for ½ harmonic filters. The VCO on this device covers an entire octave so the frequency coverage is complete down to 40 MHz. The high-performance PLL with a figure of merit of –236 dBc/Hz and high-phase detector frequency can attain very low in-band noise and integrated jitter.

The LMX2615-SP allows users to synchronize the output of multiple instances of the device. This means that deterministic phase can be obtained from a device in any use case including the one with a fractional engine or output divider enabled. The device also adds support for either generating or repeating SYSREF (compliant to JESD204B standard), making the device a very good low-noise clock source for high-speed data converters. This device is fabricated in Texas Instruments' advanced BiCMOS process and is available in a 64-lead CQFP ceramic package.

2.2.3 CDCLVP111-SP

The CDCLVP111-SP clock driver distributes one differential clock pair of LVPECL input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP111-SP can accept two clock sources into an input multiplexer. The CDCLVP111-SP is specifically designed for driving 50-Ω transmission lines. When an output pin is not used, leave the pin open to reduce power consumption. If only one of the output pins from a differential pair is used, the other output pin must be identically terminated to 50 Ω.

The V_{BB} reference voltage output is used if single-ended input operation is required. In this case, connect the V_{BB} pin to CLK0 and bypassed to GND via a 10-nF capacitor. For high-speed performance, the differential mode is strongly recommended. The CDCLVP111-SP is characterized for operation from –55°C to 125°C.

2.2.4 ADC12DJ3200QML-SP

The ADC12DJ3200QML-SP device is an RF-sampling, giga-sample, analog-to-digital converter (ADC) that can directly sample input frequencies from dc to above 10 GHz. In dual-channel mode, the ADC12DJ3200QML-SP can sample up to 3200 MSPS. In single-channel mode, the device can sample up to 6400 MSPS. Programmable tradeoffs in channel count (dual-channel mode) and Nyquist bandwidth (single-channel mode) allow development of flexible hardware that meets the needs of both high channel count or wide instantaneous signal bandwidth applications. Full-power input bandwidth (–3 dB) of 7 GHz, with usable frequencies exceeding the –3-dB point in both dual- and single-channel modes, allows direct RF sampling of L-band, S-band, C-band, and X-band for frequency agile systems.

The ADC12DJ3200QML-SP uses a high-speed JESD204B output interface with up to 16 serialized lanes and subclass-1 compliance for deterministic latency and multidevice synchronization. The serial output lanes support up to 12.8 Gbps, and can be configured to trade off bit rate and number of lanes. Remarkable synchronization features, including noiseless aperture delay (t_{AD}) adjustment and SYSREF windowing, simplify system design for synthetic aperture radar (SAR) and phased-array MIMO communications. Optional digital down converters (DDCs) in dual-channel mode allow for reduction in interface rate (real and complex decimation modes) and digital mixing of the signal (complex decimation modes only).

2.3 Design Steps

A signal chain that uses multiple data converters must have clocks that are synchronized to make sure all of the sampling instances of the data converters are aligned. However, in the case of a JESD204B-based data converter, the following requirements for device synchronization are critical for performance:

- Low-phase noise ADC sampling clock (DEVCLK) generation
- Phase align device clocks at each data converter
- Generate and capture SYSREF signal with appropriate timing margin
- Achieve deterministic latency with appropriate elastic buffer release point

There is no need for length matching the SERDES lanes between ADCs and FPGAs. The synchronization methodology of JESD204B absorbs delay variations.

2.3.1 Multiple JESD204B Synchronization Requirements

In a JESD204B system environment, data transfer from the JESD204B TX block to the RX block happens in multiframes. These multiframes are aligned to the edges of the local multiframe clock (LMFC), which is internal to the JESD204B RX and TX block. The concept of the LMFC and the associated alignment requirements are critical in applications that require deterministic latency and multiple device synchronization. To achieve deterministic latency, multiple device synchronization, or both is to make sure that the LMFC of each JESD204B device in the JESD204B system environment are aligned. The LMFC for each of the JESD204B devices is aligned through the SYSREF signal, which is globally generated from a common source throughout the JESD204B system. Once the LMFCs of all devices in the system are aligned, the devices are synchronized and data transfer happens at the same rate and at the same instant. Figure 2-2 shows the typical setup for synchronization of multiple JESD204B devices. Such synchronization of the clock sources requires:

1. Phase-align device clocks, sampling clocks (DCLK) at each ADC12DJ3200-SP device
2. In-phase SYSREF to each DCLK to meet SYSREF setup and hold time of the ADCs
3. In-phase FPGA CLK and FPGA SYSREF, if using multiple FPGAs in a system

In this design the ADC12DJ3200-SP is operating in JMODE3 with the highest sampling clock of 3.2 GHz. Based on the ADC12DJ3200-SP data sheet calculation, the required FPGA clock is 160 MHz and the SYSREF frequency is 20 MHz. These are generated by the proposed clocking design TIDA-010191.

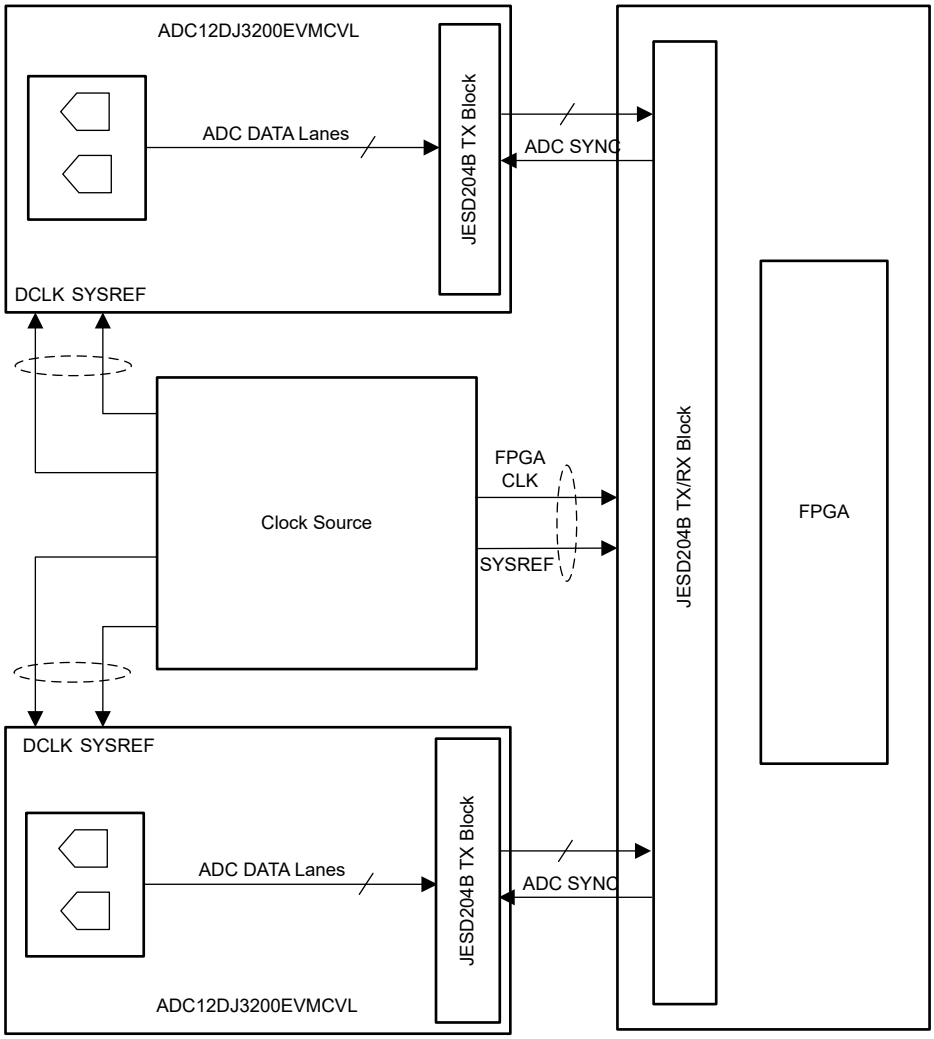


Figure 2-2. Typical Setup for Synchronization of Multiple JESD204B, and JESD204C Devices

2.3.2 Clock Tree Design

2.3.2.1 Clock Frequency Plan

A JESD204B-compliant clock output from the board is given to ADC12DJ3200QML-SP. Because SNR of the ADC is directly affected by clock jitter, the ADC is used to analyze the performance of the clocking board. The ADC12DJ3200QML-SP can go up to a 3.2-GHz clock frequency. The LMK04832-SP is configured in single PLL mode (PLL2) to generate SYSREF_REQ and SYNC signals to LMX2615-SP devices. The LMK04832-SP on this reference design is also used to provide an FPGA reference clock, a core clock, and SYSREF to the TSW14J57 capture card through the FMC+ adapter board. The clock reference and core clock frequency are both 160 MHz and the SYSREF frequency is 20 MHz. The adapter board also provides the interface between the data converter EVM and the capture card while also connecting the ADC data lanes to the FPGA.

ADC12DJ3200EVMCVAL operates in dual-channel mode (JMODE3) where input to only one channel is provided and output from the corresponding ADC core is captured. An input reference frequency of 100 MHz is provided to the LMX2615-SP RF PLL clock synthesizer device by LMK61E2 via CDCLVP111-SP. The phase-detector frequency is also changed to 100 MHz. Various input signals are available at the ADC input for SNR measurement and results are shown in Section 4, Testing and Results.

Table 2-1. Loop-Filter Configuration

CLOCK REFERENCE	LMK04832-SP CLOCK PLL2 MODE	LMX2615-SP PLL SYNTHESIZER	ADC CLOCKING	FPGA CLOCKING
Clock Reference Selected	List Clock Inputs/Outputs	Clock Inputs and Clock Outputs	Clocks Inputs/Outputs	Clocks Inputs/Outputs
Other Options: 1. VCXO 2. Programmable Oscillator (LMK6E12) – 100 MHz 3. External reference	Input REF (OSCin) – 100 MHz Output clocks: CLKout1 – LMX2615-1 SYSREF_REQ1 (20 MHz) CLKout3 – LMX2615-2 SYSREF_REQ2 (20 MHz) CLKout4 – FPGA2 REFCLK CLKout5 – LMX2615-1 SYNC1 CLKout6 – FPGA2 CORECLK CLKout7 – FPGA2 SYSREF CLKout8 – FPGA1 CORECLK CLKout9 – FPGA1 SYSREF CLKout10 – FPGA1 REFCLK CLKout11 – LMX2615-2 SYNC2	LMX2615-1: Input REF (OSCin) – 100 MHz SYNC - SYNC1 SYSREFREQ - SYSREF_REQ1 Output clocks: RFoutA1 – ADC1 CLK RFoutB1– ADC1 SYSREF LMX2615-2: Input REF (OSCin) – 100 MHz SYNC – SYNC2 SYSREFREQ – SYSREF_REQ2 Output clocks: RFoutA2 – ADC2 CLK RFoutB2 – ADC2 SYSREF	Sampling Clock: 3.2-GHz SYSREF – 20 MHz	FPGA REFCLK – 160 MHz FPGA CORECLK – 160 MHz FPGA SYSREF – 20 MHz

2.3.2.2 Clock Tree Components

Figure 2-3 shows a simplified block diagram of the TIDA-010191 clock tree with the configuration options. This clock tree includes the multiple sections like, reference generation, clock reference buffer, clock distribution and PLL synthesizer to generate low noise, and high-performance JESD204B-compliant clocks.

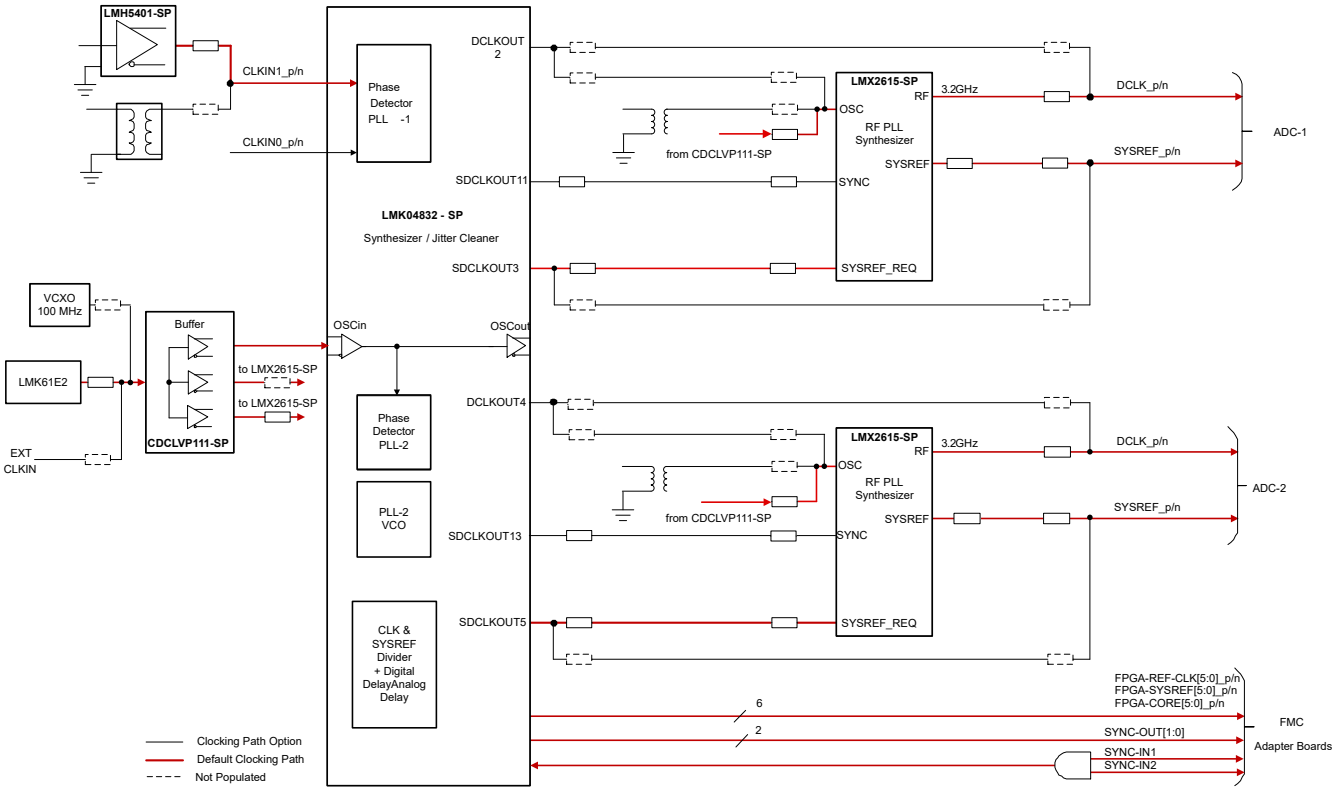


Figure 2-3. TIDA-010191 Clock Path Configuration Options

2.3.2.2.1 Clock Reference

There are two options for the clock reference input:

- The first and preferred option is an external clock reference. The external clock reference allows connection to the desired target clock of the final design and also minimizes the potential effect of the clock reference during characterization of the clock signal path performance. For the tests in this document, an oscillator (100 MHz) from Wenzel is used as a very low phase noise clock source.
- The second option is to use an onboard clock reference from an industrial grade oscillator. This design uses the programmable clock generator LMK61E2. This device helps with evaluating the sub-system without need of extensive test equipment. LMK61E2 is intended for testing purposes only and has no defined radiation performance.

2.3.2.2.2 Clock Reference Buffer

For clock distribution there exist multiple potential topologies to get the primary clock to the individual clock devices and clock multipliers. Two of them are shown in the diagram Figure 2-4 as options A and B. In option A the primary clock is replicated in the system clock device and then fanned out into the individual multipliers. In option B the fan-out is done before the system clock and all clock devices and multipliers get their individual copy of the primary clock from there.

In this design option B was chosen because there the number of sequential stations in the clock path is smaller and less noise is expected from that.

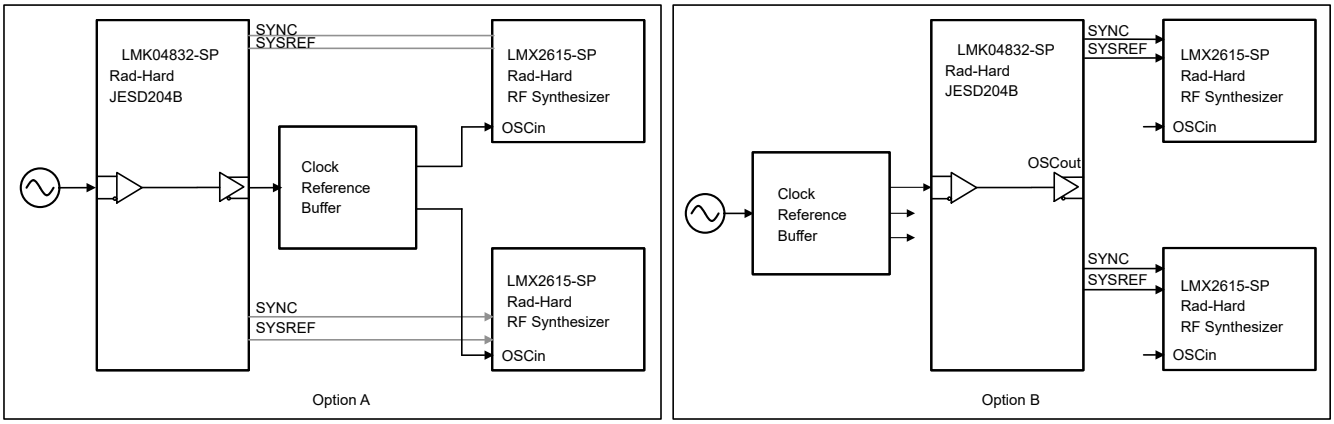


Figure 2-4. Clock Distribution Options A and B

For buffering the clock reference, the CDCLVP111-SP is an good choice because this device has all important parameters characterized and documented in the data sheet. From the various device alternatives, this device provides the lowest noise adder.

The reference design has also some provision for a purely passive clock distribution by using a 1:4 power splitter as shown in Figure 2-5. It is then possible to compare both designs. This comparison was not part of the measurements for this reference design.

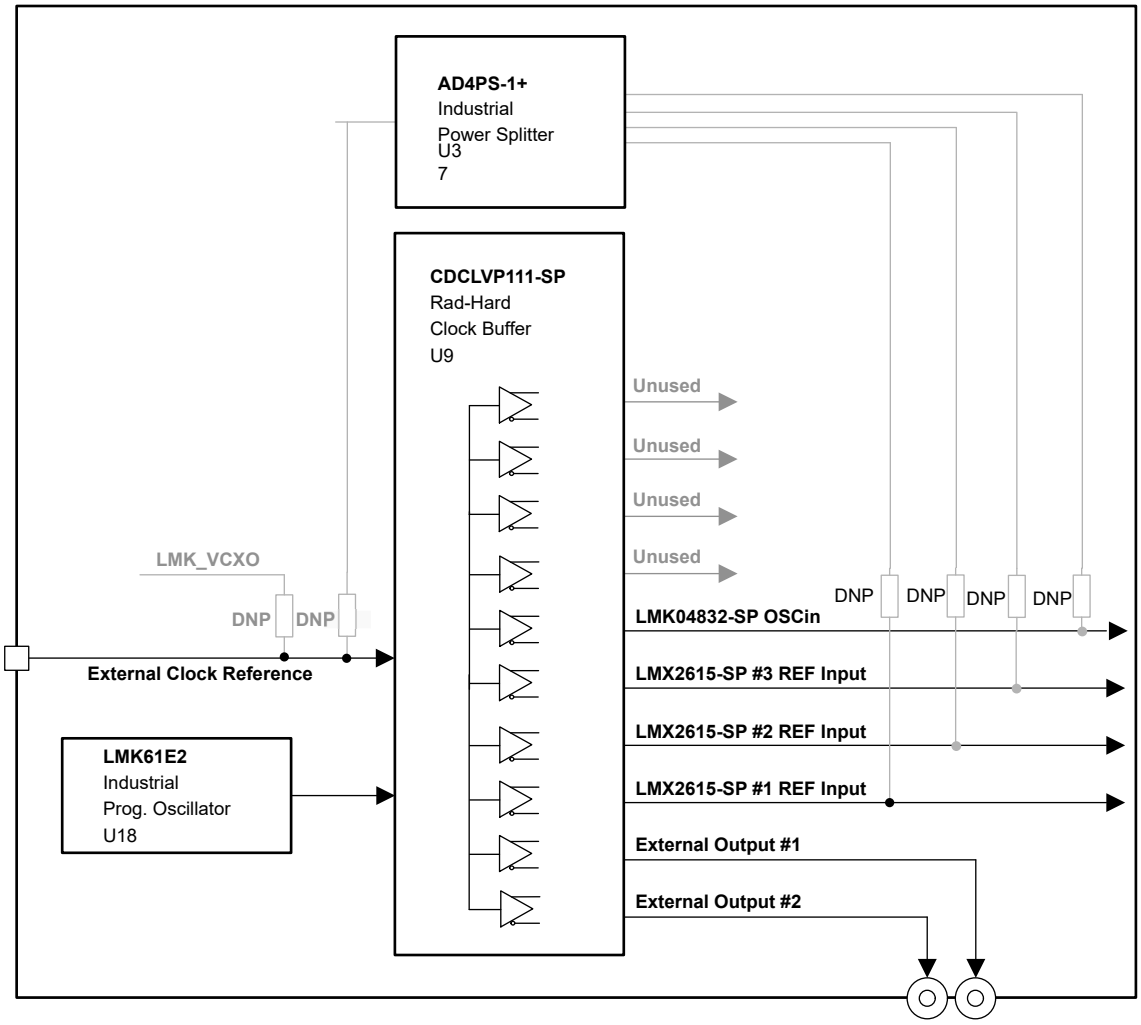


Figure 2-5. Passive Clock Distribution Using Power Splitter

2.3.2.2.3 Clock Distribution

Multichannel JESD204B designs need various clocks that are low-noise and high-frequency device clocks that are used to clock data converters, FPGA clocks, SYSREFs, and SYNC control signals for synchronizing multiple PLL synthesizer. In this design, the system clock device LMK04832-SP is used to generate the FPGA clocks, FPGA SYSREF signals, primary SYSREF signals for the data converters, and SYNC signals to multiple LMX2615-SP devices. Primary SYSREF signals are feeding to SYSREF_REQ inputs of the LMX2615-SP devices and act as primary SYSREF controlled through LMK04832-SP.

The LMK04832-SP is operating in PLL2 single-loop mode with 100-MHz input at OSCin and generates in-phase clocks out after internal SYNC and resetting the dividers. LMK04832-SP generates FPGA clocks at 160 MHz and SYSREF at 20-MHz frequencies using the internal VCO running at 3.2 GHz.

2.3.2.2.4 Frequency Synthesis

This reference design has two options to generate high-speed clocks with LMK04832-SP or LMX2615-SP, based on the jitter performance requirement. LMX2615-SP has better phase-noise performance compared to the LMK04832-SP. Hence, LMX2615-SP is used in this design to generate high-frequency clock at 3.2 GHz. Both LMX2615-SP devices receive the in-phase reference clocks of 100 MHz through the clock buffer CDCLVP111-SP and operate in VCO sync mode to synchronize their outputs and SYSREF repeater mode to route the control signal from LMK04832-SP through. LMX2615-SP requires a positive edge at the sync input to align the output clock phase to a defined position. This signal comes from the LMK04832-SP on SDCLKout in pulse mode. Similar to generating the SYSREF out from the LMX, the device is operating in SYSREF repeater mode and getting the input at SYSREF_REQ input from the LMK device.

2.3.2.3 Phase Delay Adjustment Options

Make the clocking design flexible enough to control the delay between the device clocks to maintain the SYSREF setup and hold time and provide the consistent low skew between the channels. LMX2615-SP has a SYSREF delay step of 9 ps and has a MASH SEED feature to provide the delay on the device clocks.

To adjust the delay between the DCLK and having a deterministic latency, use the MASH SEED feature in the LMX2615-SP. If there is a skew between the SYSREF clock signals, then adjust the SYSREF through the SYSREF delay to minimize the skew.

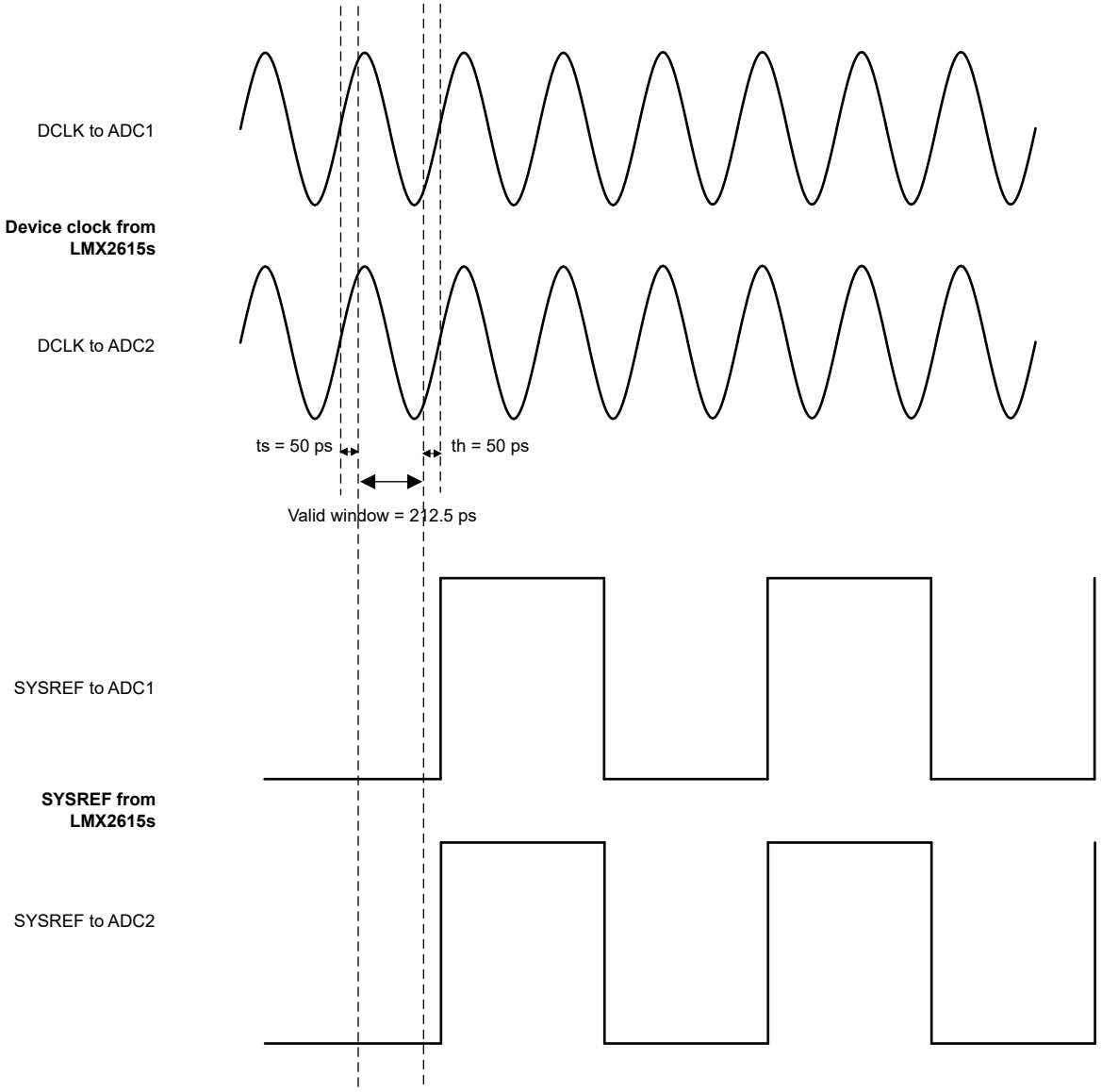


Figure 2-6. Clock and SYSREF Alignment

The ADC12DJ3200-SP has an aperture delay (tad) feature, which can also provide the delay at the input clock and adjust the skew, but in this design the delay is adjusted by the input clock itself.

2.3.2.4 Phase-Noise Optimization

Analog signal chain performance depends on the phase noise and jitter performance of the clock, which can affect the SNR, ENOB, and SFDR, of the data converter. Therefore, optimize the phase noise of the clock to having the lowest jitter.

The LMX2615-SP optimized-loop filter can be programmed to minimize phase noise with the PLLatinum™ simulation tool. In this design, the loop filter are kept the same as LMX2615-SP EVM components.

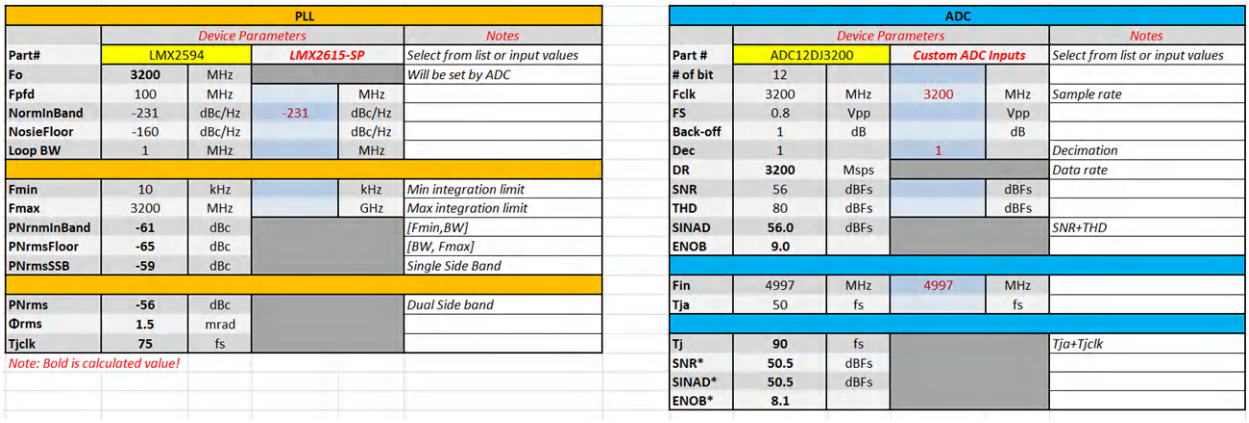
Table 2-2. LMX2615-SP Design Parameters

PARAMETER	VALUE
VCO Gain	132 MHz/V
Loop Bandwidth	285 kHz
Phase Margin	65 deg
C1_LF	390 nF
C2_LF	68 nF
C3_LF	Open
C4_LF	1.8 nF
R2	68 Ω
R3_LF	0 Ω
R4_LF	18 Ω
Charge Pump Gain	15 mA
Phase Detector Frequency	200 MHz
VCO Frequency	Designed for 15 GHz, but works over the whole frequency range

The ADC SNR degrades due to external clock jitter and internal ADC aperture jitter. SNR of the ADC, limited by the total jitter, is calculated as:

$$\mathrm{SNR(ADC)} = -20 \times \log\left(2 \times \pi \times f_{\mathrm{input}} \times \mathrm{t_{jitter}}\right)\mathrm{dBc} \quad (1)$$

To calculate the SNR performance of the ADC12DJ3200-SP over the clocking performance, TI provides a tool with the Jitter and SNR Calculator for ADCs (JITTER-SNR-CALC). Figure 2-7 is a screen-shot with the calculation results:



PLL

	Device Parameters				Notes
Part#	LMX2594		LMX2615-SP		Select from list or input values
Fo	**3200**	MHz			Will be set by ADC
Fpfd	100	MHz		MHz	
NormInBand	-231	dBc/Hz	-231	dBc/Hz	
NosieFloor	-160	dBc/Hz		dBc/Hz	
Loop BW	1	MHz		MHz	
Fmin	10	kHz		kHz	Min integration limit
Fmax	3200	MHz		GHz	Max integration limit
PNrnmInBand	**-61**	dBc			[Fmin,BW]
PNrmsFloor	**-65**	dBc			[BW, Fmax]
PNrmsSSB	**-59**	dBc			Single Side Band
PNrms	**-56**	dBc			Dual Side band
Φrms	**1.5**	mrad			
Tjclk	**75**	fs			

Note: Bold is calculated value!

ADC

	Device Parameters				Notes
Part #	ADC12DJ3200		Custom ADC Inputs		Select from list or input values
# of bit	12				
Fclk	3200	MHz	3200	MHz	Sample rate
FS	0.8	Vpp		Vpp	
Back-off	1	dB		dB	
Dec	1		1		Decimation
DR	**3200**	Msps			Data rate
SNR	56	dBFs		dBFs	
THD	80	dBFs		dBFs	
SINAD	**56.0**	dBFs			SNR+THD
ENOB	**9.0**				
Fin	4997	MHz	4997	MHz	
Tja	50	fs		fs	
Tj	**90**	fs			Tja+Tjclk
SNR*	**50.5**	dBFs			
SINAD*	**50.5**	dBFs			
ENOB*	**8.1**				

Figure 2-7. Screen-Shot Jitter to SNR Tool

Figure 2-8 and Figure 2-9 show the relevant SNR plots.

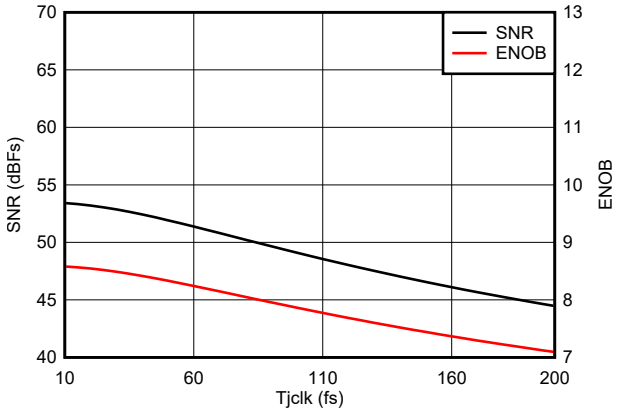


Figure 2-8. SNR vs T_J

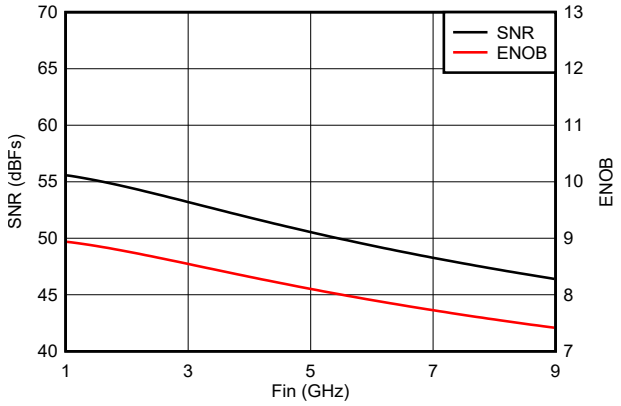


Figure 2-9. SNR vs F_{IN}

2.3.2.5 Single-Event Effects (SEE) Considerations

In this reference design the ADC12DJ3200QML-SP RF Sampling ADC is the target data converter for which to provide a clock tree. For more information about the single event upset (SEU) and how to handle SEUs, see the ADCDJ3200QML-SP data sheet: *ADC12DJ3200QML-SP 6.4-GSPS, Single-Channel or 3.2-GSPS, Dual-Channel, 12-Bit, RF-Sampling Analog-to-Digital Converter (ADC)*.

JESD204B outlines that SYSREF can be configured in different modes, continuous (also known as periodic), gapped periodic, or one-shot signal. Continuous mode allows for continuous output which designers sometimes need to avoid due to crosstalk from SYSREF to the device clock. However, the ADC12DJ3200QML-SP data sheet recommends always using a continuous SYSREF to quickly recover internal clocks and counters that can experience SEUs.

To minimize concerns of crosstalk from SYSREF to the device clock, set the period to be long enough to limit spurious performance degradation caused by coupling, but short enough to recover within the system requirements. SYSREF helps both the transmitter (ADC12DJ3200QML-SP) and receiver (FPGA or ASIC) recover after an SEU. See the single event upset (SEU) section of the *ADC12DJ3200QML-SP* data sheet for additional recommendations.

In the design, the core in the clock tree (LMK04832-SP, LMX2615-SP), as well as the target data converter (ADC12DJ3200QML-SP) are free of Single-Event Functional Interrupts (SEFI) to a LET ≥ 80 MeV·cm^2/mg. Table 2-3 provides an overview for a summary for the radiation performance of these devices.

Table 2-3. Summary for the Radiation Performance

PARAMETER	ADC12DJ3200QML-SP	LMK04832-SP	LMX2615-SP	CDCLVP111-SP
TID LDR Characterization [krad(Si)]	N/A	100	100	75
TID HDR Characterization [krad(Si)]	300	100	100	100
TID RLAT/RHA [krad(Si)]	300	100	100	—
SEL Immunity [MeV·cm^2/mg]	120	120	120	69.2
SEFI Immunity [MeV·cm^2/mg]	120	120	120 (Pin Mode)	—
SEE Characterization [MeV·cm^2/mg]	120	120	120	65.3

For additional device-specific information refer to the Single-Event Effects (SEE) reports, typically available in the TI.com product folders.

2.3.2.6 Expanding Clock Tree for MIMO Systems

In this reference design the focus is in providing clocking and synchronization to two ADC12DJ3200QML-SP RF sampling ADCs, however, most systems typically have a need to provide clocking and synchronization to multiple high-speed data converters, in many instances a combination of many ADCs and DACs.

To scale the clocking tree for multichannel systems with more than two channels, consider a variety of clock architectures, such as a *Tree* or *Daisy Chain* configurations as illustrated in Figure 2-10.

In a daisy chain configuration, first the clocking board receives a high-frequency reference signal from an external clock source and generates the synchronized high-frequency clocks; then distributing the same reference signal to the next clocking board, along with the SYNC signals, to synchronize the two clocking boards. Conversely, in a clock tree configuration, one primary board (for example, LMK04832EVM-CVAL) receives a high-frequency reference signal from an external clock source, which is distributed to the secondary boards (clocking boards) along with the SYNC signals for synchronizing the secondary devices.

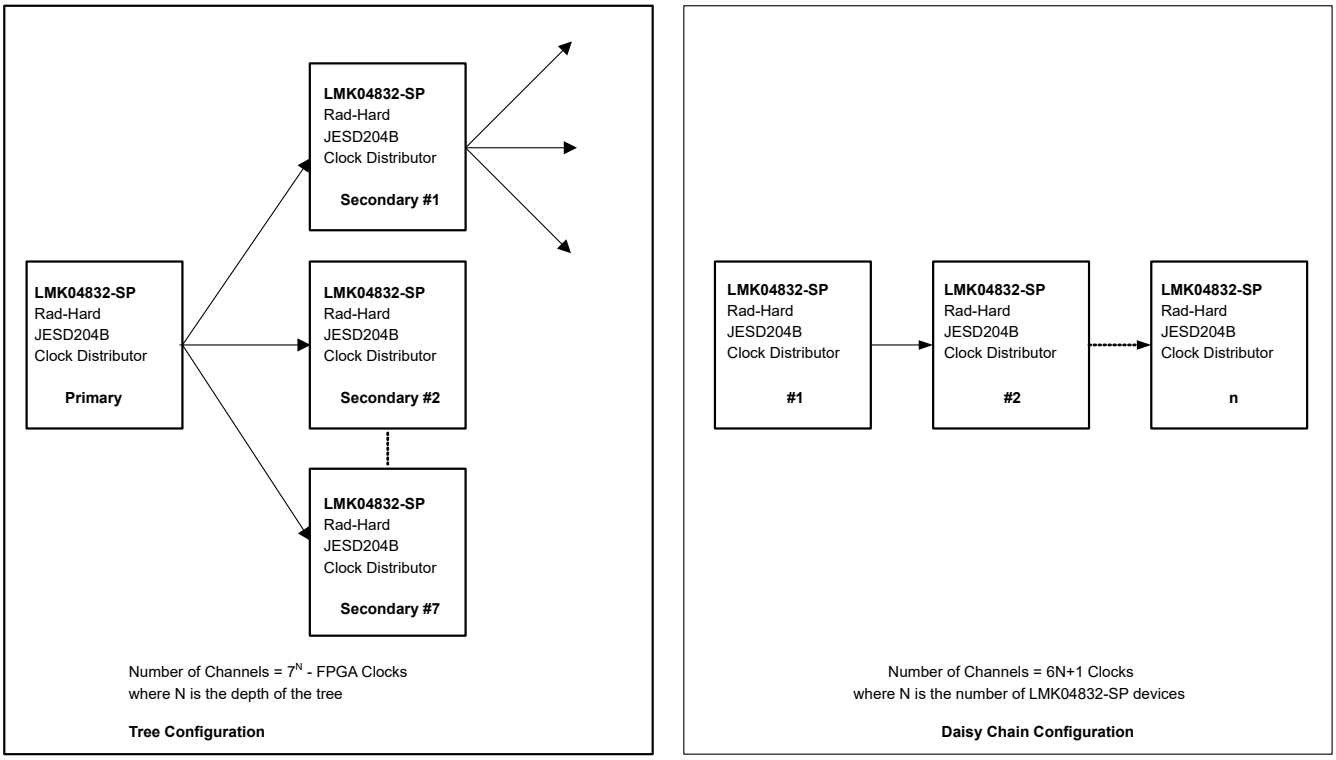


Figure 2-10. Clock Distribution Configuration Examples

Examples of these configuration are shown in the following industrial-grade reference designs:

- Daisy Chain: High Channel Count JESD204B Daisy Chain Clock Reference Design for RADAR and 5G Wireless Testers (TIDA-01024)
- Tree: High Channel Count JESD204B Clock Generation Reference Design for RADAR and 5G Wireless Testers (TIDA-01023)

2.3.3 Power Management

As part of the reference design, a primarily radiation-hardened power clock tree was developed to provide power for the key elements of the clocking tree. Additionally, there is a portion of the tree using an industrial-grade device to provide power to the programming interface, which does not imply any radiation performance assurance. The following sections describe product selection as well as design choices.

2.3.3.1 Power Design Considerations

Low-noise power supply is critical to the performance of the analog front end. Figure 2-11 shows the noise coupling paths from the power supply to the analog front end. Figure 2-11 also shows the impact of the power-supply noise on the output spectrum of the data converter. As previously mentioned, the data converter spectrum has two components due to power supply noise:

- Direct-coupled frequency component
- Modulated frequency component

Consider the following for a robust design:

- Reduce the noise at the source
- Eliminate or minimize the coupling path
- Desensitize the load to noise

In the analog front end, the clock power rails and the analog power rails of data converters need low-noise power supply. Take necessary precautions in terms of using a post regulator for the DC/DC converter or appropriate filtering of the DC/DC converter output.

The DC/DC converter followed by an LDO has tradeoffs in terms of size and thermal performance. If there are multiple switch-mode power supplies synchronizing, these can reduce beat frequencies and EMI.

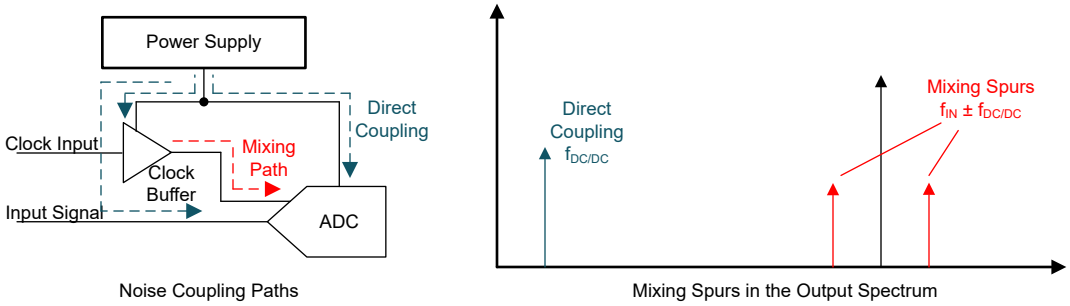


Figure 2-11. Noise Coupling

2.3.3.2 Radiation Hardened (Rad-Hard) Power Tree

Clocking devices used in this reference design primarily require a 3.3-V supply voltage. Providing a low noise 3.3-V supply is a main focus for the power tree (see Figure 2-12). Furthermore, the power supply needs to meet radiation requirements typical for multi-year missions in GEO orbits. In this specific case all of the power tree integrated circuits (ICs) are rad-hard and meet or exceed the following radiation specifications:

- Total Ionizing Dose (TID) Characterization = 100 krad (Si)
- Radiation-Hardness-Assured (RHA) / RLAT = 100 krad (Si)
- Neutron Displacement Damage (NDD) Characterization = 1×10^{13} n/cm^2 (1 MeV equivalent)
- SEL, SEB, and SEGR Immune to LET = 75 MeV/cm^2/mg
- SET, SEFI Characterized to LET = 75 MeV/cm^2/mg

Note

Because this reference design focuses on selecting appropriate semiconductor devices, discrete components (for example, resistors, capacitors, diodes, inductors, and so forth) are used irrespective of space-qualification.

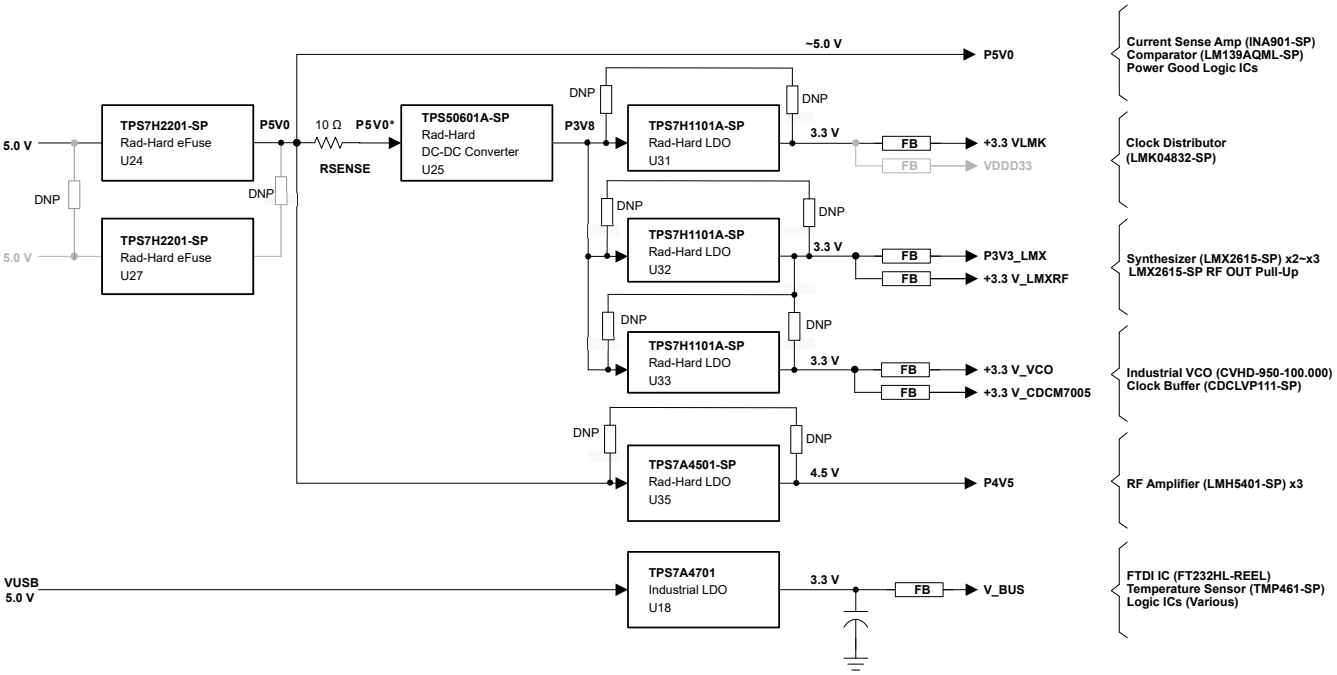


Figure 2-12. Power Tree

Figure 2-12 shows the power tree. From left to right, the power tree demonstrates three types of rad-hard power devices. First the TPS7H2201-SP eFuse provides an integrated option to provide overcurrent and overvoltage protection functions. Next, the TPS50601A-SP DC/DC buck converter does the efficient conversion from 5.0 V down to 3.8 V. This leaves 500-mV headroom for the 3.3-V LDOs so that LDO can perform with excellent AC performance. The TPS7H1101A-SP then does the conversion from 3.8 V down to 3.3 V. The LDO responsible for the 4.5-V supply of the differential amplifiers, the TPS7A4501, runs directly off the 5-V supply because at that low current the use of a switch mode converter is not needed.

2.3.3.2.1 Radiation-Hardness-Assured (RHA) Load-Switches

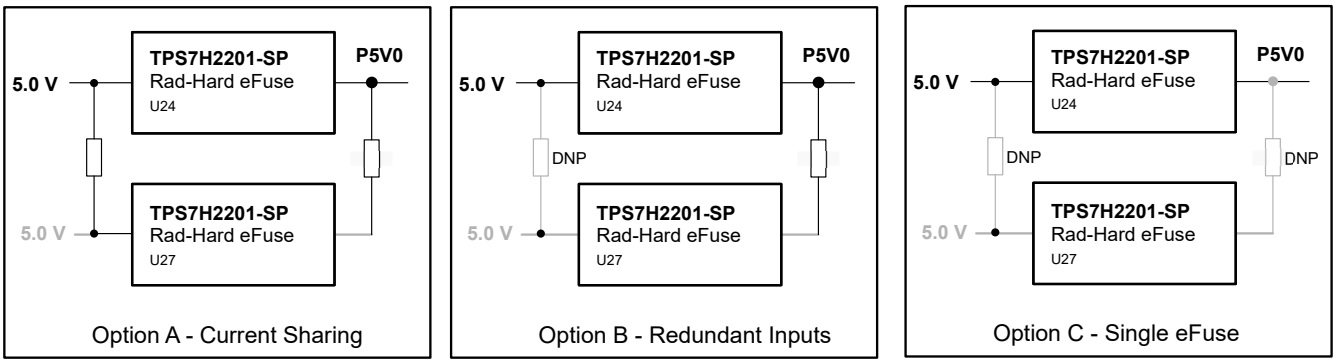


Figure 2-13. eFuse Configuration Options

eFuse Design Specifications:

- Redundant architecture
- V_{IN} = 5 V
- Ioutmax = 6 A

R_{IL} (Ω) = 45500 / (I_L (A)) = 7.58 kΩ; standard value 7.59 kΩ

Calculations were also made accounting for a 10% drop in supply (4.5 V). The following calculations show that with an R_{TOP} of 100 kΩ, that R_{BOTTOM} is 11.66 kΩ; modified to a standard value of 11.5 kΩ.

$$R_{BOT\_EN}\ (k\Omega\ ) \geq 47 / (V_{UVLO\_TRIP} - 0.47) \quad (2)$$

where

- V_{UVLO_TRIP} = 4.5 V, resulting in R_{BOT_EN} = 11.66 kΩ

Standard value chosen R_{BOT_EN} = 11.5 kΩ

$$V_{IHEN} \times (R_{EN\_TOP} + R_{EN\_BOT}) / R_{EN\_BOT} \geq V_{IN} \quad (3)$$

where

- V_{IHEN} = 0.61 V, R_{EN_TOP} = 100 kΩ, R_{EN_BOT} = 11.5 kΩ

Resulting in: 5.914 V ≥ V_{IN}.

The overvoltage protection (OVP) feature of the device can be configured using a resistor divider from V_{IN} connected to the OVP pin. The trip voltage for the OVP has to be less than the absolute maximum V_{IN} voltage. A voltage at the OVP pin greater than V_{OVPR} trips the OVP feature and turns off the FET and a voltage less than V_{OVPF} keeps the FET on.

$$R_{BOT\_EN}\ (k\Omega) \geq 63 / (V_{OVP\_TRIP} - 0.63) \quad (4)$$

where

- V_{OVP_TRIP} = 6.5 V, resulting in R_{BOT_EN} = 10.7 kΩ

$$V_{OVPF} \times (R_{EN\_TOP} + R_{EN\_BOT}) / R_{EN\_BOT} \geq V_{IN} \quad (5)$$

where

- V_{OVPF} = 0.5 V, R_{EN_TOP} = 100 kΩ, R_{EN_BOT} = 10.7 kΩ

Resulting in: 5.17 V ≥ V_{IN}.

The switch is controlled by an on and off input (EN).

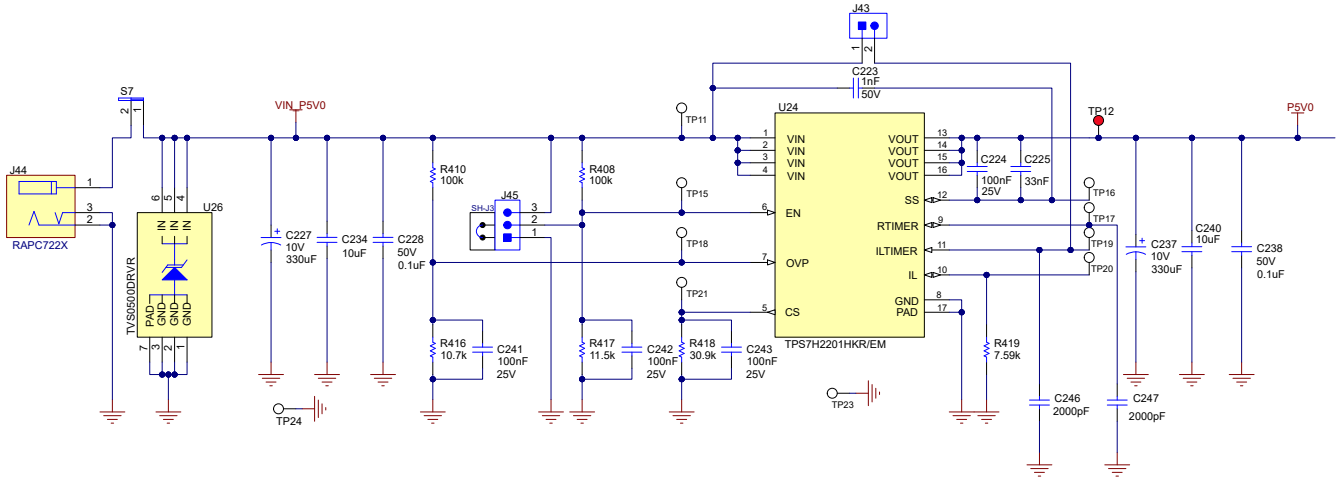


Figure 2-14. One Branch of Redundant eFuse

2.3.3.2.2 Radiation-Hardness-Assured (RHA) DC/DC Buck Converter

For supplying accurate power to all 3.3-V devices, a buck converter as pre-regulator is used. This reduces heat generation in the LDOs by reducing the drop voltage. Highly noise-reduced clock generation demands for low-noise power supply and a cascade of buck converter and LDO or set of LDOs is capable of providing this.

Converter Design Specifications:

- V_{IN} = 5 V
- V_{OUT} = 3.8 V
- I_{outmax} = 4 A
- F_{sw} = 500 kHz
- R_{TOP} = 10 kΩ, R_{BOT} = 2.64 kΩ

$$R_{BOTTOM} = V_{REF} / (V_{OUT} - V_{REF}) \times R_{TOP} \quad (6)$$

where

- V_{REF} = 0.804 V
- V_{OUT} = 3.8 V
- R_{TOP} = 10 kΩ
- R_{BOTTOM} = 2.683 kΩ
- Std Value = 2.64 kΩ

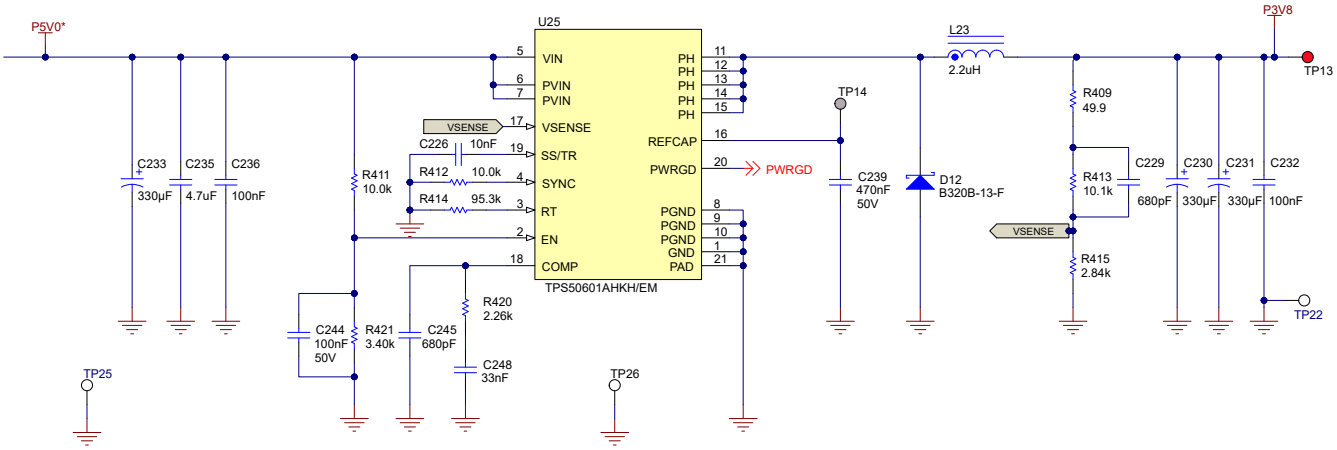


Figure 2-15. Buck Pre-Regulator

The compensation values were determined in WEBENCH® Power Designer and verified via simulation with the average model in TINA-TI.

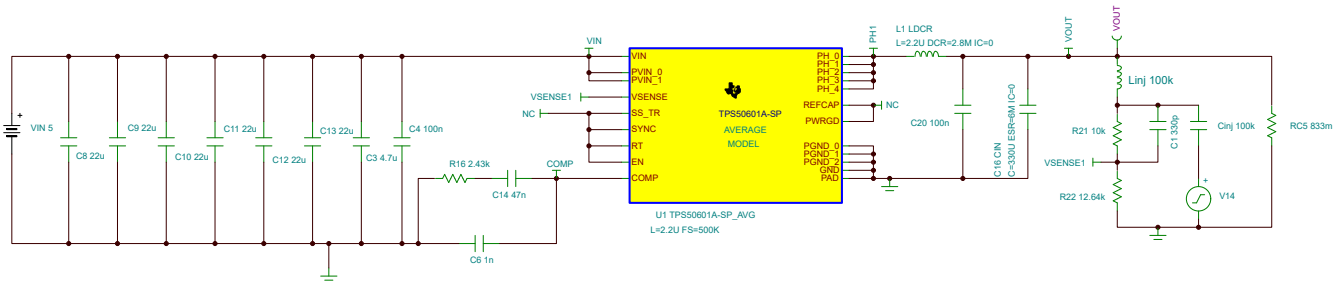


Figure 2-16. Simulation Bench for the TPS50601A Buck Regulator

Figure 2-17 illustrates that the resulting phase margin from the simulation was 57.86°.

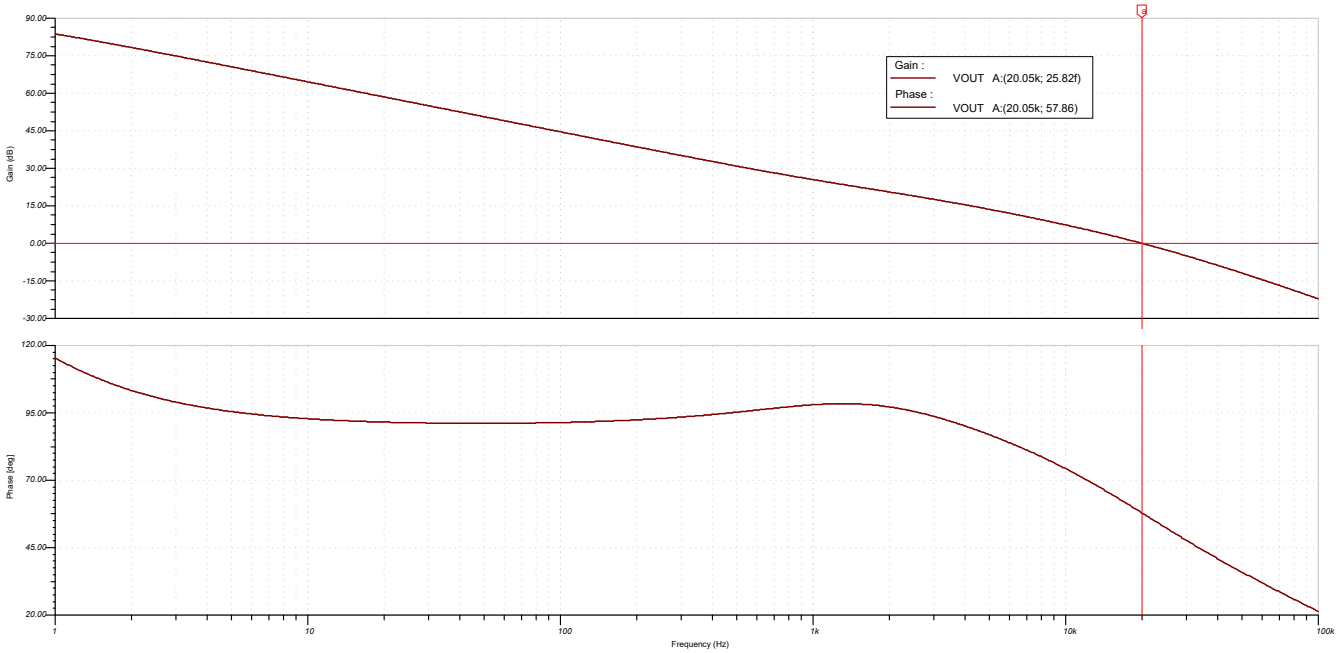


Figure 2-17. Phase and Gain of TPS50601A With Selected Passives

Use the equations in the section discussing *small signal model for frequency compensation* from the *TPS50601A-SP Radiation Hardened 3-V to 7-V Input, 6-A Synchronous Buck Converter* data sheet to recalculate the device loop compensation component values to the desired specifications.

2.3.3.2.3 Radiation-Hardness-Assured (RHA) Low-Dropout (LDO) Regulators

In the portfolio of RHA LDOs are two particularly well-designed devices for this application: the TPS7A4501-SP and the TPS7H1101-SP.

The TPS7A4501-SP has the smaller current capability of both devices, namely 0.75 A but this device provides better power-supply ripple rejection. In this design the TPS7A4501-SP is used as a regulator for devices with lower power consumption and demand for clean power supply. The LMH5401-SP fully-differential amplifiers get power through this path, and are utilized as clock buffers and a clean supply reduces the added clock jitter.

The TPS7H1101-SP powers the 3.3-V rails of the clock synthesizers LMX2615-SP, the central clock distribution, and jitter cleaner circuit LMK04832-SP, the CDCLVP111-SP, and the clock termination resistor networks. The required amount of current exceeds the capabilities of the TPS7A4501-SP and the TPS7H1101-SP when the 3-A current delivery is selected. The calculations for both LDOs are given in Section 2.3.3.2.3.1 and Section 2.3.3.2.3.2.

2.3.3.2.3.1 3.3-V Linear Regulator

LDO Design Specifications:

- V_{IN} = 3.8 V
- V_{OUT} = 3.3 V
- I_{outmax} = 2 A
- R_{TOP} = 51.1 kΩ, R_{BOT} = 11.5 kΩ

$$V_{OUT} = ((R_{TOP} + R_{BOTTOM}) \times V_{FB})/R_{BOTTOM} \quad (7)$$

where

- V_{FB} = 0.605 V, V_{OUT} = 3.3 V, R_{TOP} = 51.1 kΩ

$R_{BOTTOM} = R_{TOP} / ((V_{OUT} / V_{FB} – 1))$ = 11.47 kΩ; Std Value = 11.5 kΩ

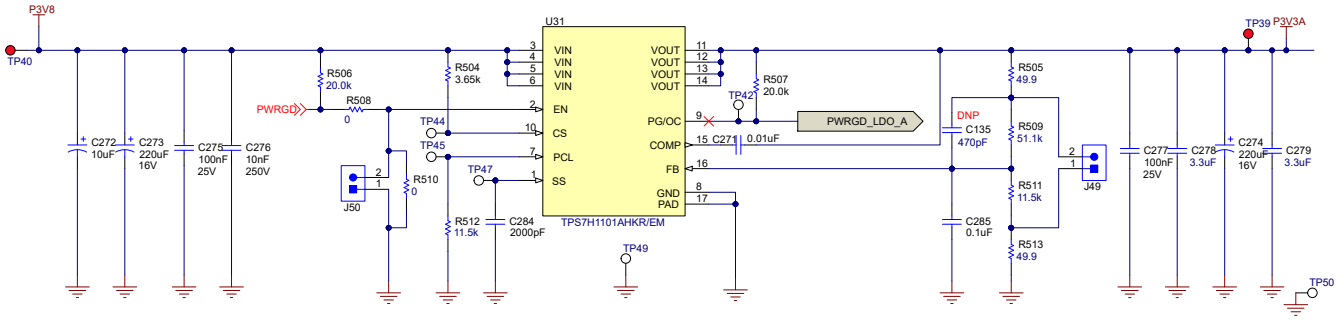


Figure 2-18. 3-A LDO for 3.3 V With TPS7H1101

The enable pins of the LDO were tied to the TPS50601A-SP Power Good pin for power sequencing. Since the output current of the LDOs is greater than 1 A, a minimum dropout voltage of 500 mV was determined to keep the spectral noise of the device relatively low.

2.3.3.2.3.2 4.5-V Linear Regulator

LDO Design Specifications:

- V_{IN} = 5 V
- V_{OUT} = 4.5 V
- I_{outmax} = 0.75 A
- R_{TOP} = 8.71 kΩ, R_{BOT} = 3.25 kΩ

$$V_{OUT} = ((R_{TOP} + R_{BOTTOM}) \times V_{FB}) / R_{BOTTOM} \quad (8)$$

where

- V_{FB} = 1.21 V
- V_{out} = 4.5 V
- R_{BOT} = 3.25 kΩ

$R_{TOP} = V_{out} / V_{FB}\ R_{BOT} – R_{BOT}$ = 8.84 kΩ; Std Value = 8.66 kΩ after subtracting R547 value of 49.9 Ω.

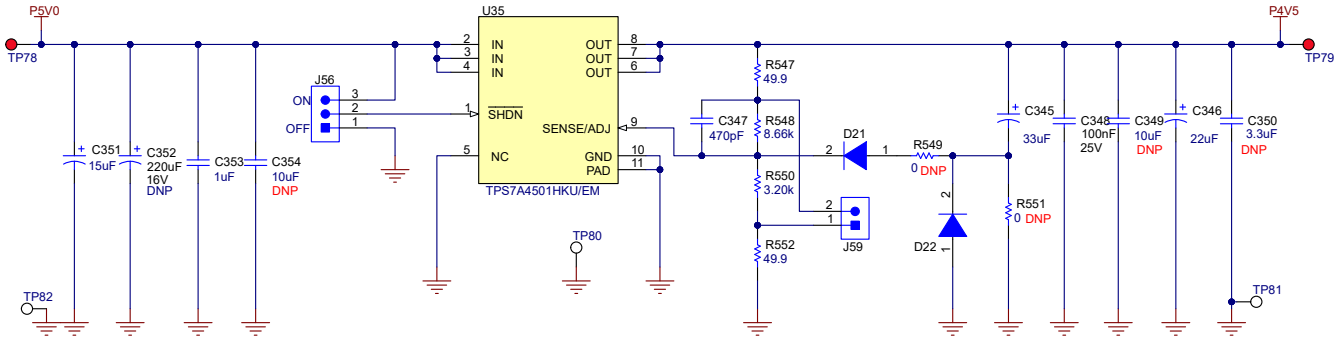


Figure 2-19. 0.75-A LDO for 4.5-V Supply With TPS7A4501

2.3.3.3 Overcurrent Detection Circuit

The total amount of current required for the application is variable and depends on the configuration. To predict potential brownout situations from misconfigurations, a current-sense amplifier and an overcurrent comparator are installed. The INA901-SP is designed to sense a high-side (positive rail) shunt resistor and convert the current into a voltage for further analysis. The device can be tapped at TP37. The sensitivity is 1 V per Ampere of total system current.

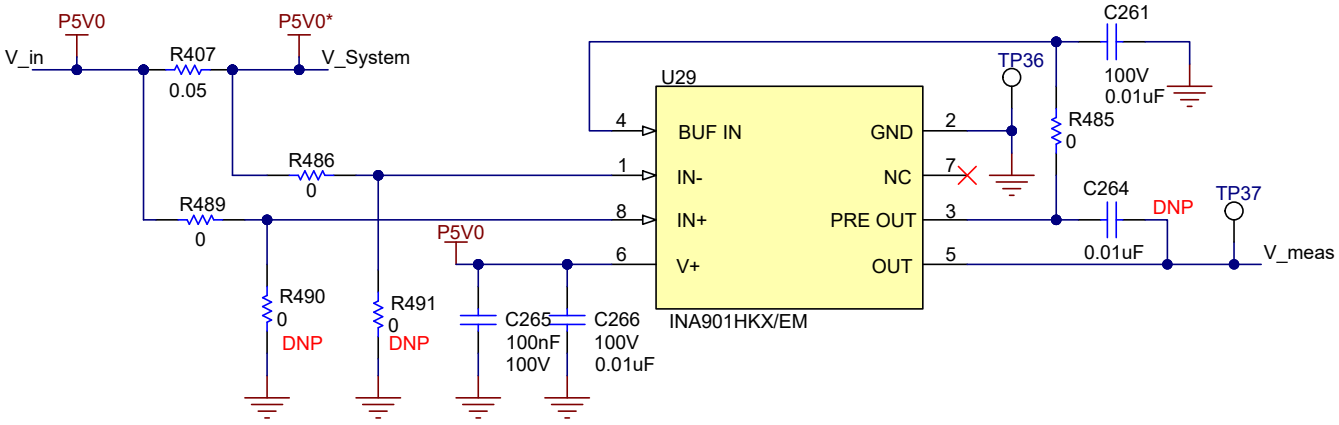


Figure 2-20. Power Supply Current Sensing

3 Getting Started Hardware and Software

3.1 Hardware Configuration

3.1.1 Clocking Board Setup

Figure 3-1 shows the multichannel TIDA-010191 clocking board.

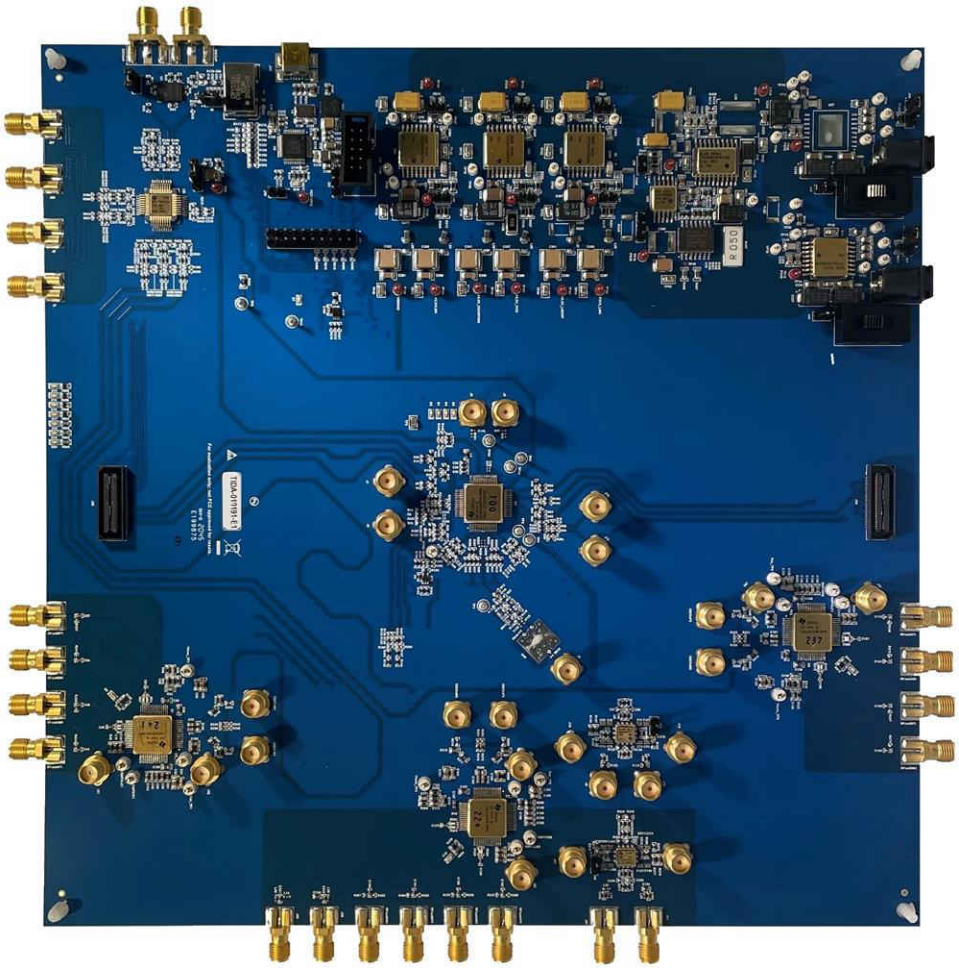


Figure 3-1. TIDA-010191 Clocking Board

3.1.1.1 Power Supply

The board has two +5-V supply options. Power connector J44 is the primary supply input and J47 is the redundant supply input. In the current board redundancy is not implemented and U27 (the second eFuse) is unpopulated. Power needs to be inserted into the primary connector J44. Set the power supply to +5 V with a 2-A current limit.

3.1.1.2 Input Reference Signals

Use the following options when setting up the input reference signals:

- Option 1: The onboard reference LMK61E2 (U2) is powered up using the jumper J16 and factory programmed to generate a 156-MHz LVDS output. U2 can be programmed to generate different clock frequencies using the I2C interface. The clocking board has a CDCLVP111-SP clock buffer (U9) to select the reference input from U2 or external reference, Y1, and distribute to the clocking devices on the board. U9 can select the LMK61E2 reference using the short jumper at pin 2-3 of the jumper J30. Isolate the power supply to Y1 by removing the short jumper at J8.
- Option 2: Connect the external reference signal to the OSCin_P and OSCin_N connectors. While connecting the external reference, power down the Y1 by removing the short jumper at J8 and remove C87. For external

reference enable to clocking devices from reference buffer device U13, place the short jumper at pin 1-2 of J30. At the same time, isolate the power supply to U2 by removing the jumper J16.

- Option 3: The onboard VCXO Y1 is powered on using the jumper J8 and outputs a 100-MHz signal to the CLK0_P pin input of clock buffer (U9) by removing R39 and connect 50 Ω at OSCin_N connector. Place the short jumper at pin 1-2 of J30 and distribute the reference to clocking devices. At the same time, isolate the power supply to U2 by removing the jumper J16.
- Option 4: Use one of the previous options, when LMK04832-SP works in single PLL mode (PLL2). When LMK04832-SP is operating in distribution mode or dual PLL mode, connect the external reference to J6 or J10 or J5 depending on the operating input frequencies. Next, choose between the LMH5401-SP based active balun (U6) or onboard passive balun (U40). Finally, select the path to CLKin1 pins of the U1 by placing C79 and C80 or C38 and C3. While operating in distribution mode, power down the Y1 by removing jumper J8. In distribution mode, when the input frequency is higher than 3 GHz, then the external clock input through the J5 connector can be fed to Fin0 pins of the LMK04832-SP and connect the external clock through R553 and R554 and remove R555 and R556.

3.1.1.3 Input sync Signal

Connect the external sync signal at external J2 and J3 connectors to reset the LMK04832-SP dividers. The same inputs can be used for additional reference for PLL1 of the LMK04832-SP.

3.1.1.4 Output Signals

The following list describes the output signal connectors:

- RFoutAP1, RFoutAM1, RFoutAP2, and RFoutAM2 connectors generate the DCLK and are connected to the phase-noise analyzer to measure phase noise and are connected to ADC EVMs as external clocks and measure SNR
- RFoutBP1, RFoutBM1, RFoutBP2, and RFoutBM2 connectors generate the low-frequency SYSREF signals interface with ADC EVMs
- Connectors J32 and J33 generates the FPGA CLKs and SYSREFs for two TSW14J57 capture cards

3.1.1.5 Programming Interface

Connect the USB mini cable to the onboard USB connector J17 and test the PC to program the TIDA-010191 clocking board devices using the TIDA-01019x software graphical user interface (GUI).

3.1.1.6 FMC+ Adapter Board Setup

The FMC+ adapter board interfaces with ADC12DJ3200EVMCVAL EVM and TSW14J57EVM to pass through the data lanes and has connections to take FPGA clocks, FPGA SYSREFs, and SYNC from the TIDA-010191 clocking board or ADC12DJ3200EVMCVAL EVM. Follow the schematic in Figure 3-2 to connect the FPGA clocks and SYSREFs from the clocking board.

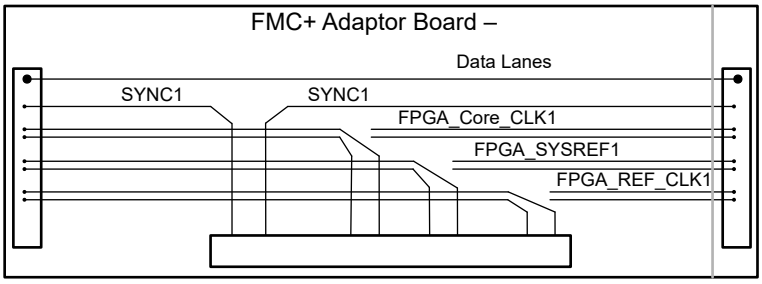


Figure 3-2. FMC Adapter

3.1.1.7 ADC12DJ3200 EVM Setup

See the *ADC12DJ3200EVMCVAL Evaluation Module* user's guide for the ADC12DJ3200EVMCVAL hardware setup procedure.

The ADC12DJ3200EVMCVAL has both internal as well as external options for clocking the ADC. Selecting the DEVCLK is based on the placement of capacitors on the shared pads. Connect C49 and C52 and remove C50

and C51 for the external DEVCLK. Connect the external SYSREF for the ADC remove R67 and place R70 and provide the SYSREF at connector J22 from the TIDA-010191 clocking board.

3.1.1.8 TSW14J57EVM Setup

Follow the *TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card* user's guide for the TSW14J57 EVM hardware setup procedure.

3.1.1.9 Multichannel Synchronization Setup

Figure 3-3 shows the multichannel synchronization setup, where the TIDA-010191 clocking board is connected with two ADC12DJ3200EVMCVAL and two TSW14J57EVM through FMC+ adapters. This setup requires 3 sets of length-matched cables to interface between them.

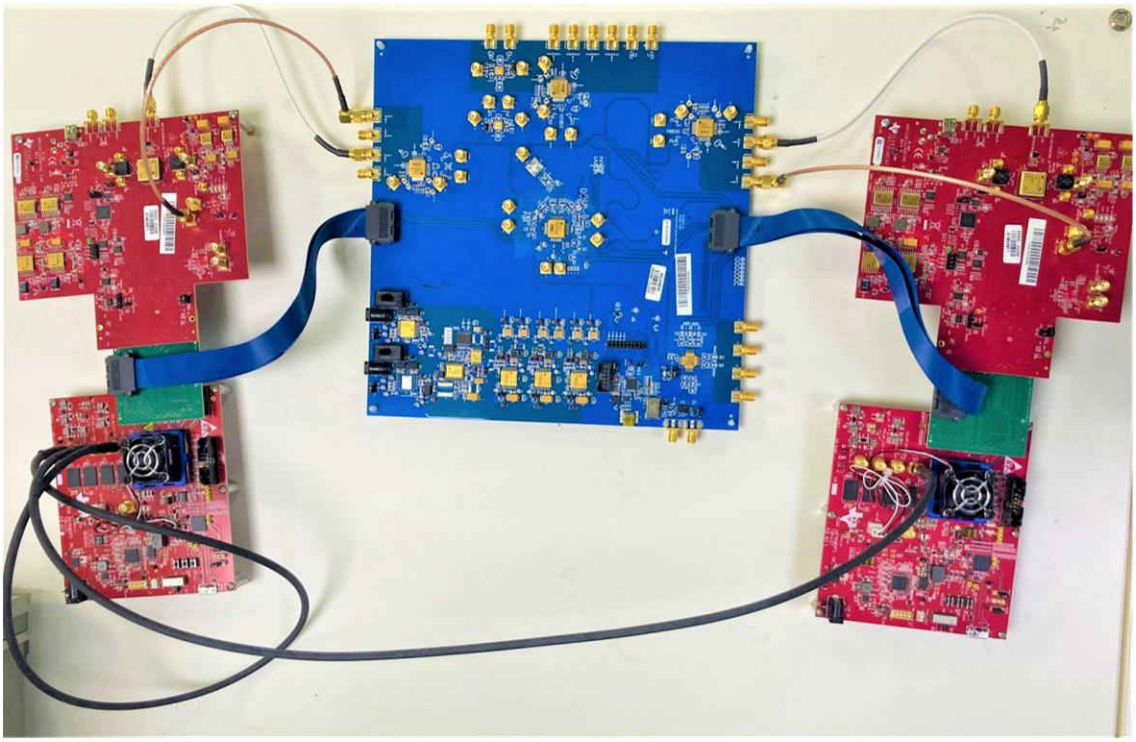


Figure 3-3. Photo of the Setting

3.2 Software

3.2.1 Software Required

This reference design uses the following software:

- HSDC TIDA01019x GUI (to program the TIDA-010191 clocking board)
- ADC12DJ3200EVM-CVAL GUI (to program ADC12DJ3200EVMCVAL)
- HSDC Pro (TSW14J57EVM GUI)

3.2.2 Clocking Board Programming Sequence

TIDA-010191 clocking board includes the FTDI device, which needs to be programmed once to support the software GUI. An FTDI utility FT-prog is installed from the web. The product description is set to TIDA01019x as shown in Figure 3-4.

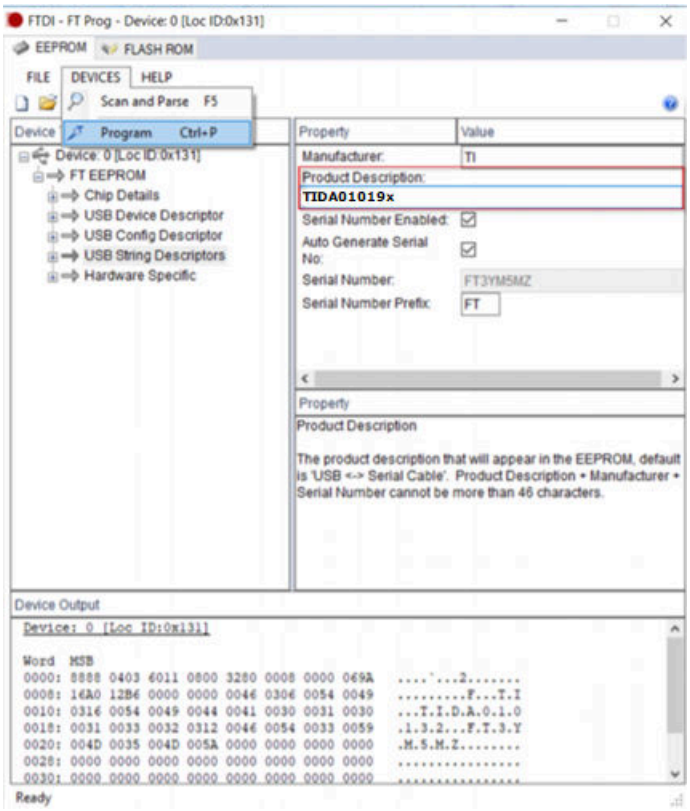


Figure 3-4. Screenshot of the FTDI Setup

Clocking board devices are programmed by HSDC TIDA01019x GUI and can be downloaded from the TIDA-010191 tool page.

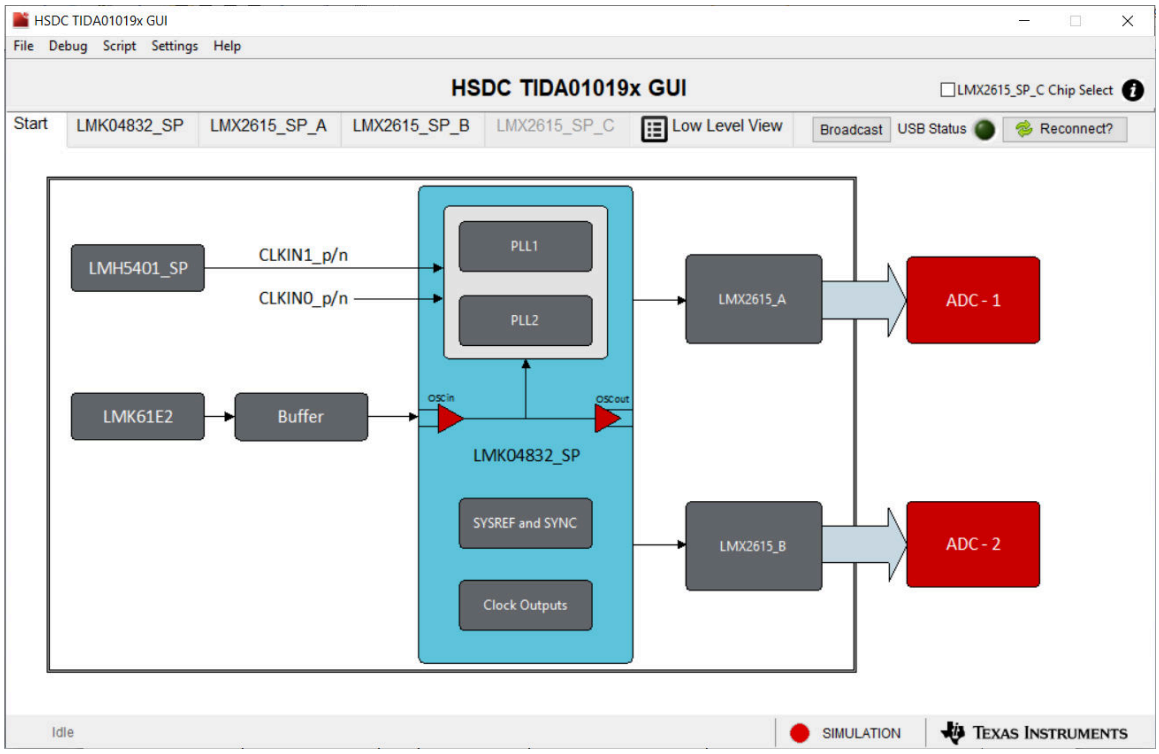


Figure 3-5. Clock GUI

All devices are configured by loading the configuration files in the low level view page.

- To measure LMX2615-SP phase noise, configure the following:
  - External reference at 100 MHz provided through Wenzel source
  - The LMX2615-SP devices are taking a reference via CDCLVP111-SP. The LMX2615-SP is programmed for a 100-MHz reference and 200-MHz phase detector frequency at various frequencies to measure the phase noise
- To measure clock skew, configure the following:
  - The LMK61E2 is programmed at 100 MHz. Configure the file in the low level view page
  - The LMK04832-SP is programmed in single PLL mode with 100-MHz reference and generates 20-MHz SYSREF frequency and provides the SYSREFREQ and SYNC signals to both LMX2615-SP devices
  - Both LMX2615-SP devices are programmed with the common configuration file at a 100-MHz phase detector frequency and generate a 3.2-GHz RFoutA and SYSREF in repeater mode at 20-MHz SYSREFout (RFoutB) from both devices
- To measure the ADC12DJ3200-SP SNR and skew between multiple ADC EVMs, configure the following:
  - The LMK61E2 is programmed at 100 MHz. Configure the file in the low level view page
    - LMK61E2_100M.cfg
    - LMK61E2_EEPROM_Write.cfg
  - The LMK04832-SP is programmed in single PLL mode with 100-MHz reference and generates 20-MHz SYSREF frequency and provides the SYSREFREQ and SYNC signals to both LMX2615-SP devices. The device also generates the FPGA clocks and FPGA SYSREFs for TSW14J57 capture cards
    - Load LMK04832-SP_160MFCLK_20MSYSREF_100MREF.cfg
  - Both LMX2615-SP devices are programmed with the common configuration file at a 100-MHz phase detector frequency and generate a 3.2-GHz RFoutA and SYSREF in repeater mode at 20-MHz SYSREFout (RFoutB) from both devices
    - LMX2615-SP_AB_3.2G_100MREF_SYSREF_Repeater.cfg

3.2.3 ADC12DJ3200CVAL EVM Programming Sequence

Download the ADC12DJ3200EVM-CVAL GUI from TI.com to program the ADC12DJ3200EVMCVAL. The ADC12DJ3200-SP and LMK04832-SP are devices configured for SNR measurement in the ADC12DJ3200EVMCVAL, as shown in Figure 3-6. The LMK04832 is programmed in distribution mode for the CLKin1 drive to configure SYSREF directly. The ADC12DJ3200EVMCVAL is put into JMODE3 mode to use in dual-channel mode at full Nyquist zone of the device. The EVM is setup in external clock source selection mode, with a sampling frequency of 3200 MSPS and load configuration files in the low level view page of the ADC12DJ3200EVM-CVAL.

Obtain the updated ADC12DJ3200EVM-CVAL configuration files for ADC12DJ3200EVM-CVAL synchronization measurement from the HSDC TIDA01019x GUI software folder.

```
C:\Program Files (x86)\Texas Instruments\HSDC TIDA01019x GUI\Configuration Files\ ADC12DJ3200EVM-CVAL GUI files
```

Use the following programming sequence for ADC EVM configuration after the clocking board program:

1. Load ADCEVM_LMK04832_CLKin1_SYSREF_bypass.cfg
2. Load ADC12DJxx00_JMODE3_SRC_EN.cfg
3. Load LMK_LMX_SYSREF_OFF.cfg in HSDC TIDA01019x GUI
4. Load ADC12DJxx00_JMODE3_SRC_clear.cfg

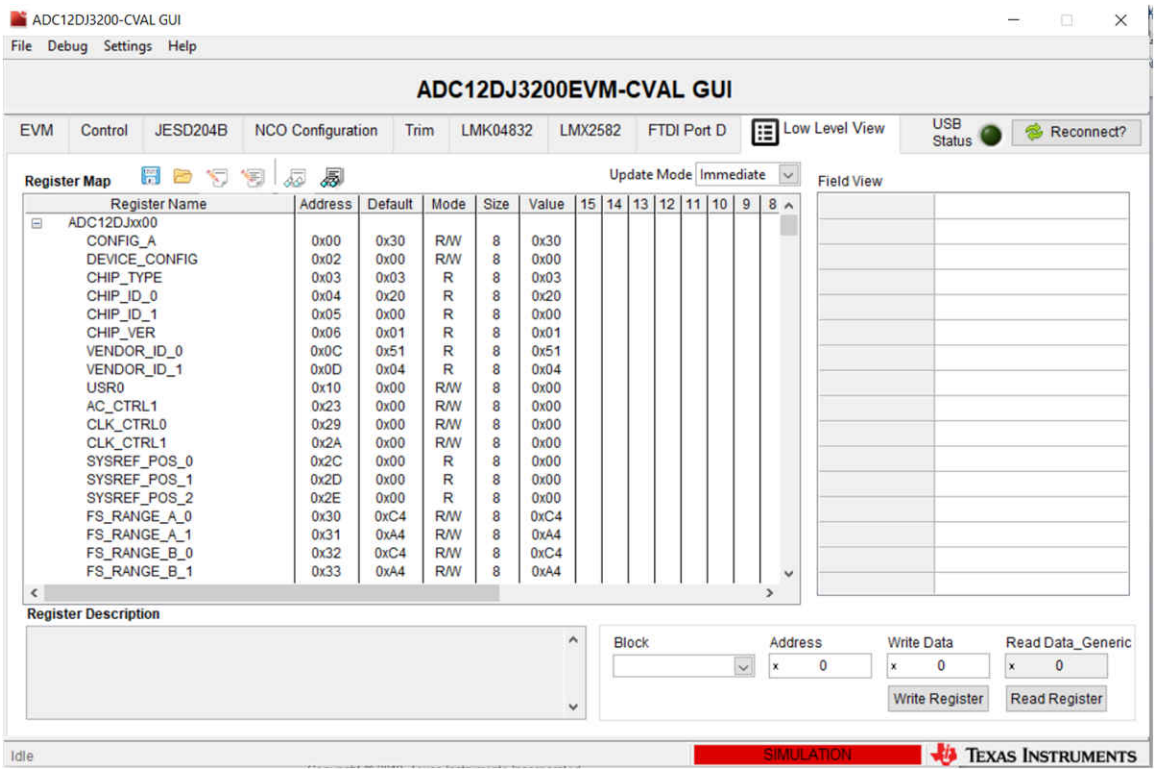


Figure 3-6. ADC12DJ3200 EVM Programming

3.2.4 TSW14J57EVM Evaluation Programming Sequence

The HSDC Pro software interfaces with the TSW14J57EVM to capture and analyze the digital data from the ADC12DJ3200-SP in SNR measurement and skew measurement.

To operate the TSW14J57EVM tools in primary and secondary mode for skew measurement, follow the README note available in the HSDC TIDA01019x GUI software folder. Next, include the updated firmware, .ini files, and other settings in HSDC Pro GUI folder.

Follow the *TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card* user's guide for HSDC Pro setup and to capture and analyze the data. The following steps show how to configure the HSDC Pro GUI for capturing the data and operating in primary and secondary mode.

1. Select ADC12DJxx00_JMODE3_F&K_1_32_sysref.ini to interface with the ADC12DJ3200EVM-CVAL GUI for JMODE3
2. Set the ADC sampling frequency to 3.2 GHz
3. Set the ADC input target frequency
4. For SNR measurement, click on the *Capture* tab and the data is captured on the screen
5. For skew measurement, configure one HSDC Pro in primary mode (Test Options) and another in secondary mode.

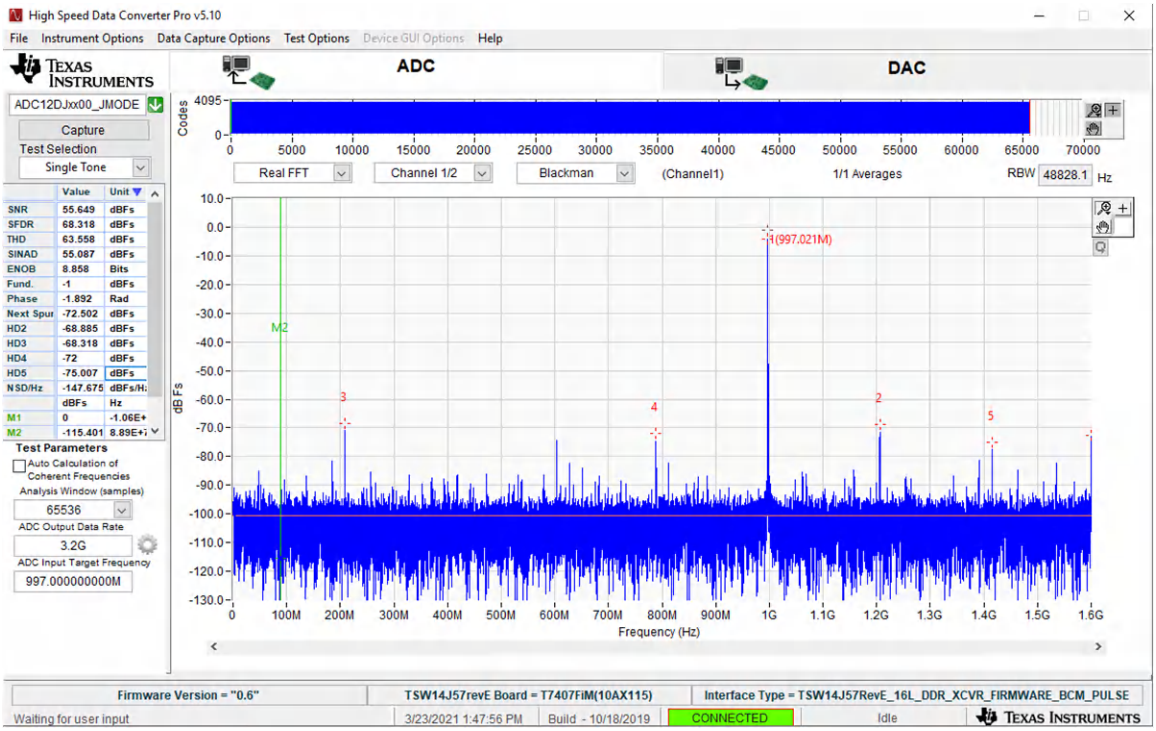


Figure 3-7. First Test of the Setup by Capturing a Spectrum

4 Testing and Results

4.1 Test Setup

Figure 4-1 through Figure 4-4 show the test setup for LMX2615-SP phase noise, clock skew, SNR measurement, and channel-to-channel skew measurement, respectively.

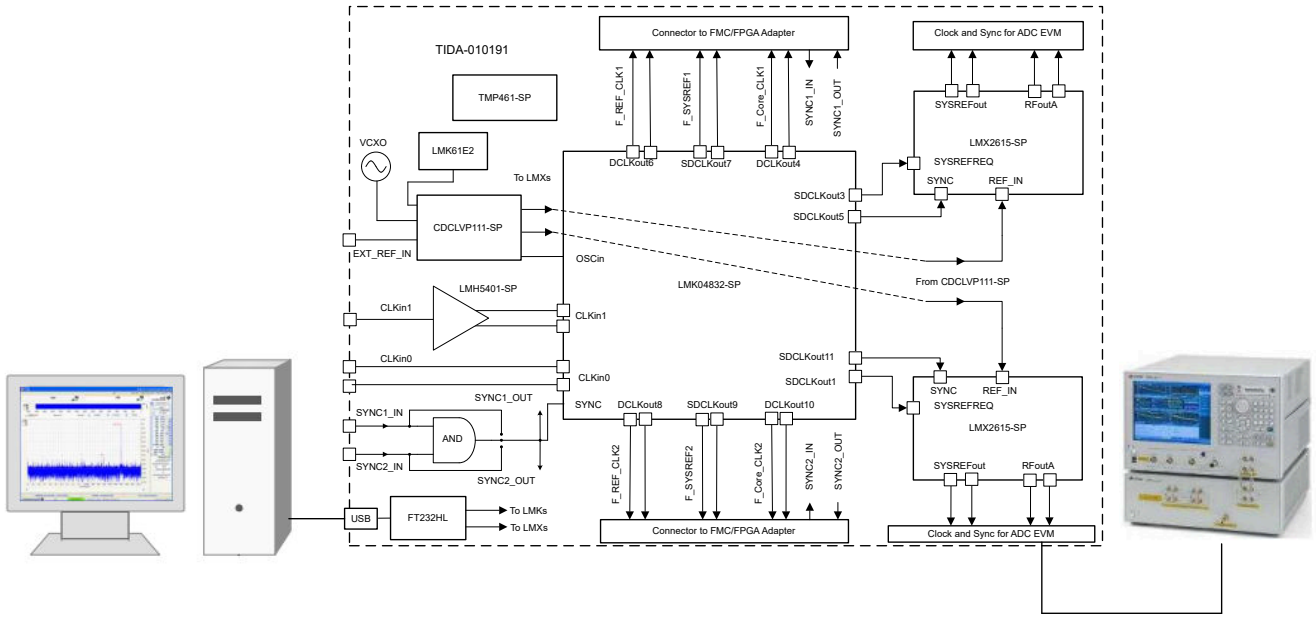


Figure 4-1. Test Setup for Phase Noise Measurement

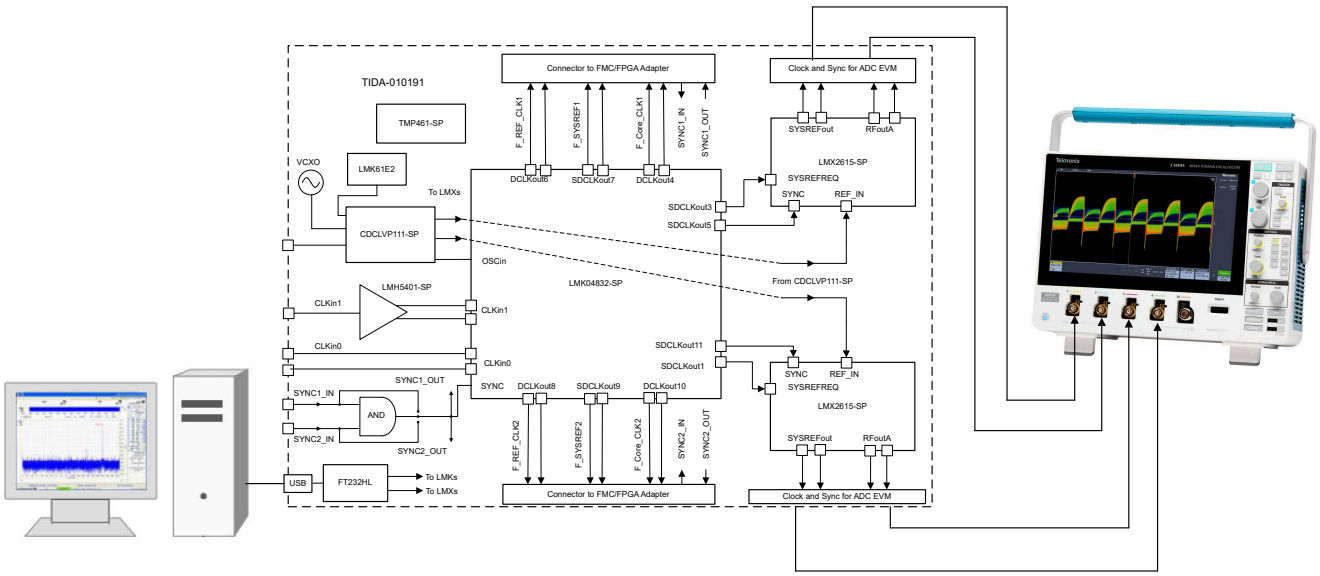


Figure 4-2. Test Setup for Multichannel Clock Skew Measurement

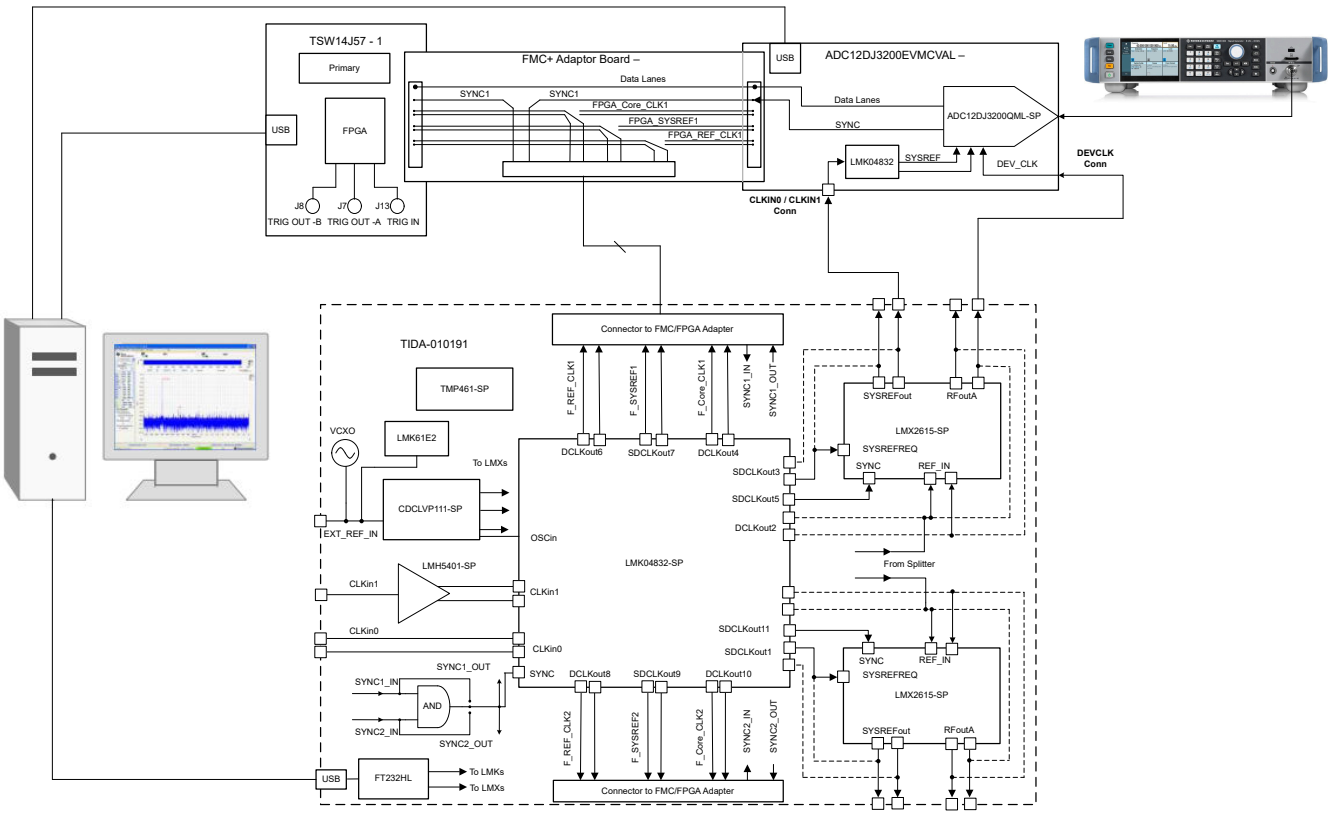


Figure 4-3. Test Setup for SNR Measurement

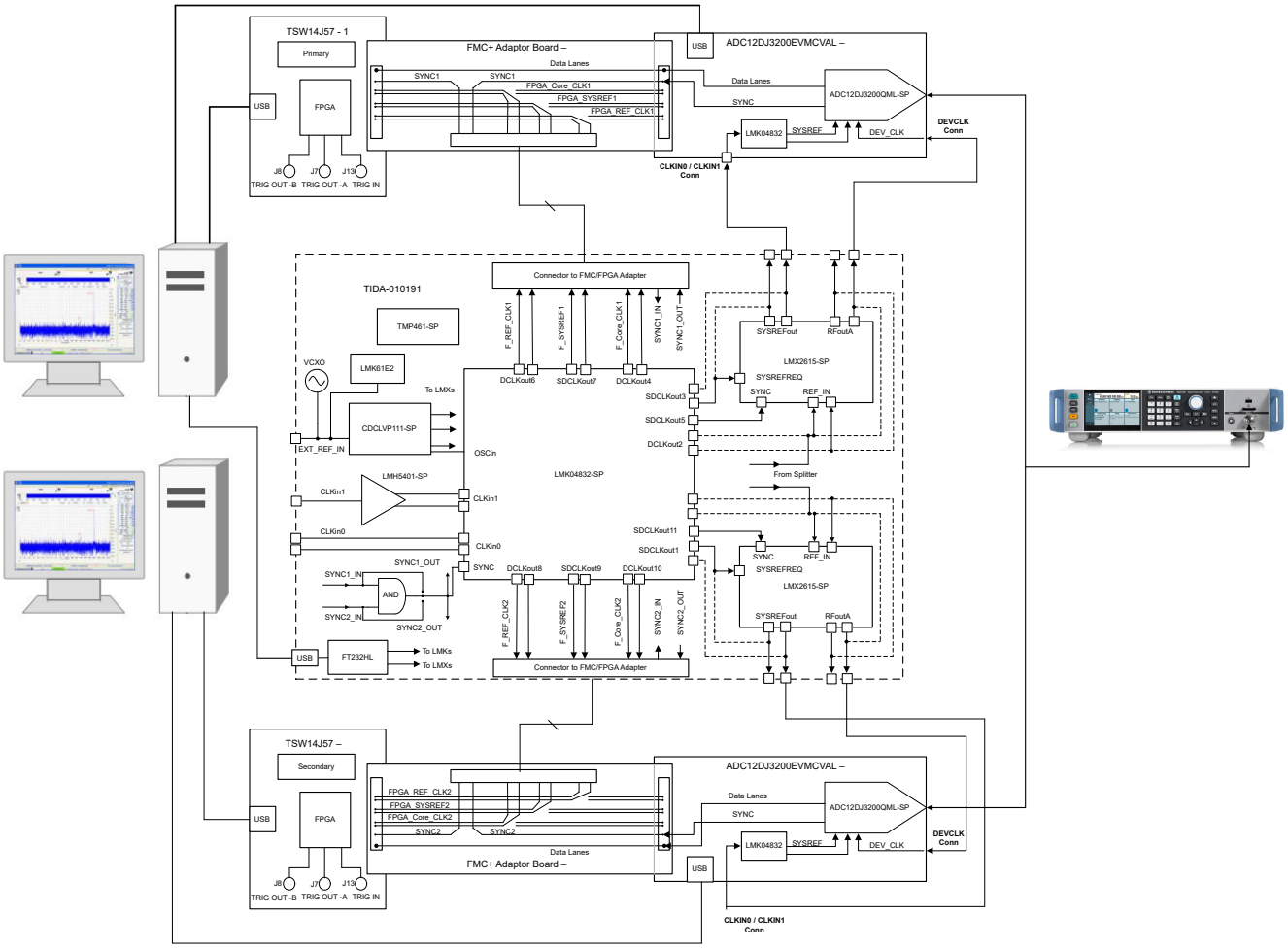


Figure 4-4. Test Setup for Channel-to-Channel Skew Measurement

4.2 Results

4.2.1 Phase Noise Measurement Results

TIDA-010191 clocking board LMX2615-SP devices show almost the same results since both are identical on the board. Table 4-1 shows the measured phase noise performance of the LMX2615-SP at various clock frequencies in the clock board. Measured phase noise plots are shown in Figure 4-5 through Figure 4-7.

Table 4-1. Measured Phase Noise

OUTPUT FREQUENCY (GHz)	CONDITION	LMX2615-SP DATA SHEET PHASE NOISE (dBc/Hz)	TIDA-010191 MEASURED PHASE NOISE (dBc/Hz)
3.5	10-kHz offset	–111.5	–112.2
	100-kHz offset	–115.3	–114.4
	1-MHz offset	–121.9	–120.6
	10-MHz offset	–146.3	–146.7
	40-MHz offset	–150.9	–151.5
9.0	10-kHz offset	–104.9	–110
	100-kHz offset	–111.4	–111.8
	1-MHz offset	–121.9	–122.3
	10-MHz offset	–146	–147
	40-MHz offset	–153	–154

Table 4-1. Measured Phase Noise (continued)

OUTPUT FREQUENCY (GHz)	CONDITION	LMX2615-SP DATA SHEET PHASE NOISE (dBc/Hz)	TIDA-010191 MEASURED PHASE NOISE (dBc/Hz)
15.0	10-kHz offset	–100.8	–106.1
	100-kHz offset	–107.2	–107.7
	1-MHz offset	–114.3	–114
	10-MHz offset	–140.4	–140.8
	40-MHz offset	–151	–149

Figure 4-5. Phase Noise at 7-GHz Carrier Frequency

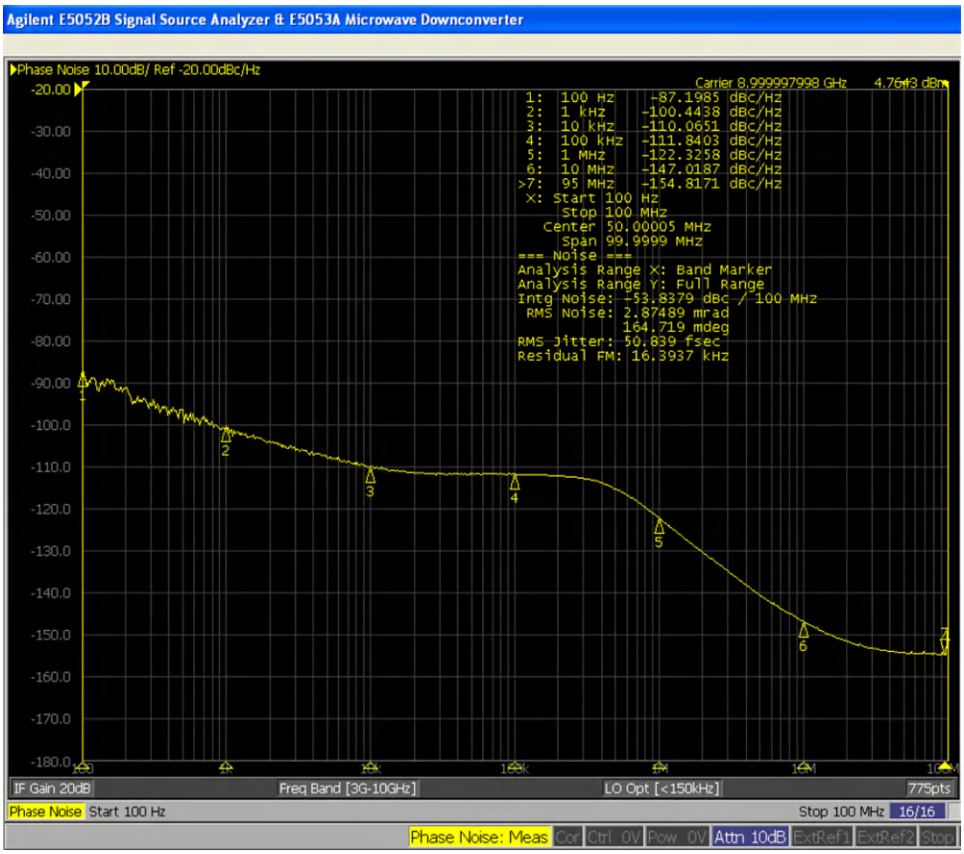


Figure 4-6. Phase Noise at 9-GHz Carrier Frequency

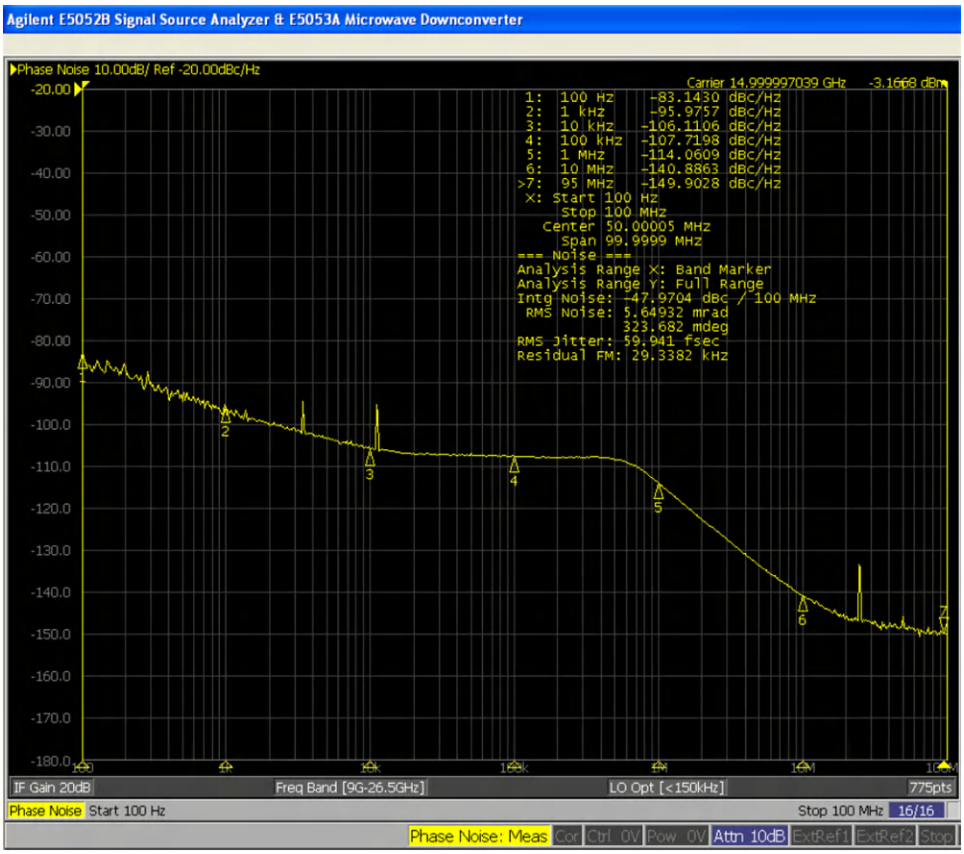


Figure 4-7. Phase Noise at 15-GHz Carrier Frequency

4.2.2 Multichannel Clock Phase Alignment

As explained in Section 3.2.3, synchronized clocks are critical for multichannel systems. This section shows the measured phase aligned clocks and SYSREFs that are generated from both LMX2615-SP devices at a 3.2-GHz device clock and 20-MHz SYSREF. The minimum skew have between the clocks, reflects the minimum channel-to-channel skew in multichannel systems. In this test, the TIDA-010191 clock board shows the clock skew less than 5 ps. As a result, can reduce the channel-to-channel skew in multichannel systems. Figure 4-8 shows the multichannel clock skew measured results from two LMX2615-SP devices at the device clocks and SYSREF signals.

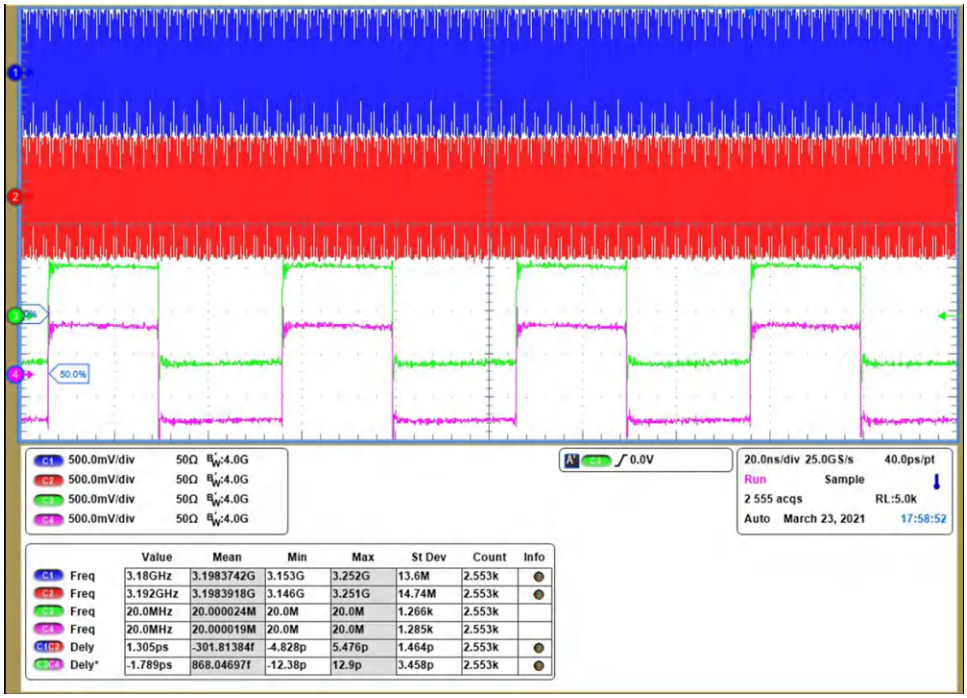


Figure 4-8. Scope-Shot Multichannel Clock Phase Alignment

4.2.3 Signal Chain Performance

Table 4-2 shows the measured SNR performance of the ADC12DJ3200-SP at various frequencies for –1-dBFS differential inputs and dual channel mode (JMODE3). The comparison between the measured SNR with the ADC12DJ3200EVMCVAL onboard clocks and with TIDA-010191 clocks shows almost similar performance. Figure 4-9 through Figure 4-11 show the spectral results at a 3200-MHz sampling frequency in single-channel mode.

Table 4-2. SNR Measurement

INPUT FREQ (MHz)	ADC DATA SHEET SNR (dBFS)	ADC12DJ3200EVM ONBOARD CLOCK MEASURED (dBFS)	TIDA-010191 MEASURED (dBFS)
997	55.5	55	55.6
2482	55	53.4	53.9
4997	53	51.4	50.4

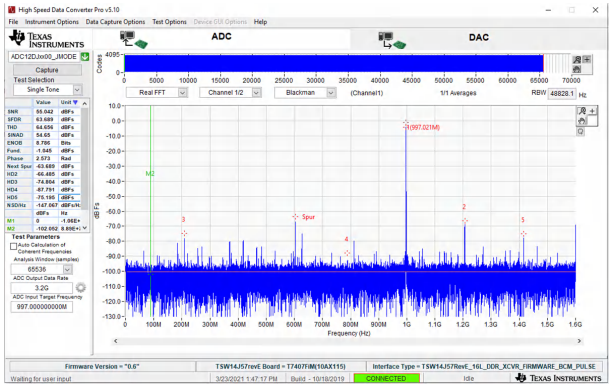


Figure 4-9. Noise Floor at 99-MHz Carrier Frequency

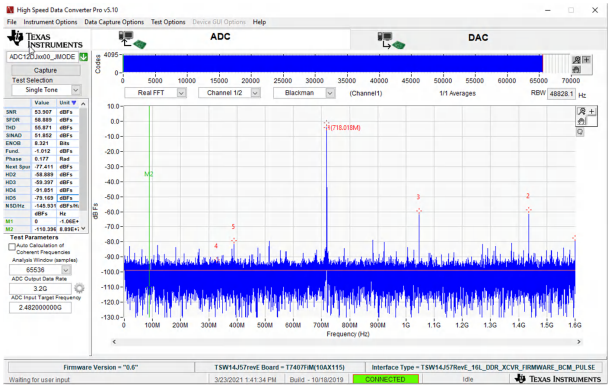


Figure 4-10. Noise Floor at 718-MHz Carrier Frequency

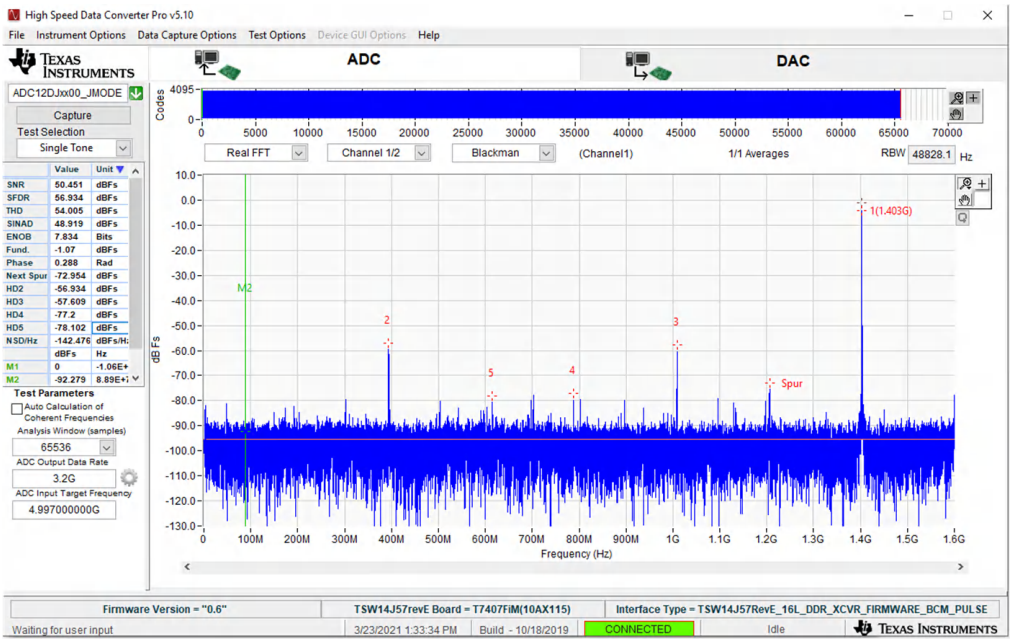


Figure 4-11. Noise Floor at 1403-MHz Carrier Frequency

4.2.4 Channel-to-Channel Skew Measurement

Figure 4-12 and Figure 4-13 show the time skew between two ADC12DJ3200EVMCVAL channels at different input frequencies. This skew is evaluated by calculating the phase difference between signals captured from each ADC. These measurements were taken at a 3.2-GHz sampling frequency and the measured time skew was < 5 ps for each input frequency.

Figure 4-12 shows the plot of the output samples of the two ADCs for a 997-MHz input, this plot is in the first Nyquist zone for a 3200-MHz sampling clock. Figure 4-13 is the plot of the output samples for a 2482-MHz input, which is in the second Nyquist zone for a 3200-MHz sampling clock. The 2482-MHz input signal aliases to 882 MHz.

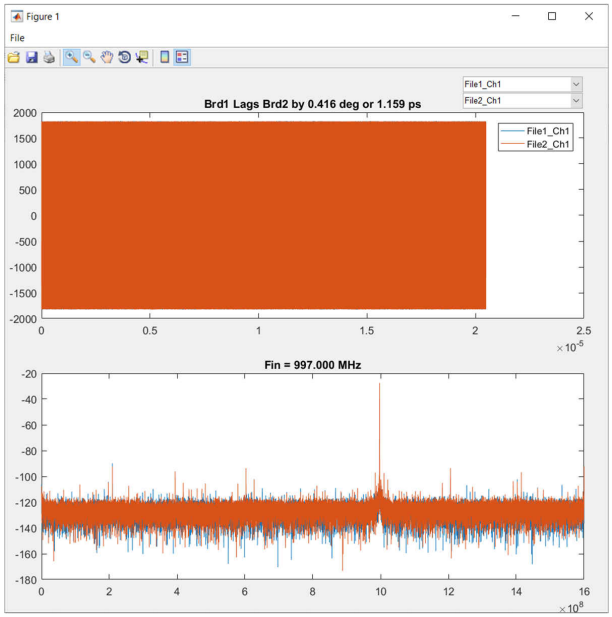


Figure 4-12. Board Skew at 997 MHz

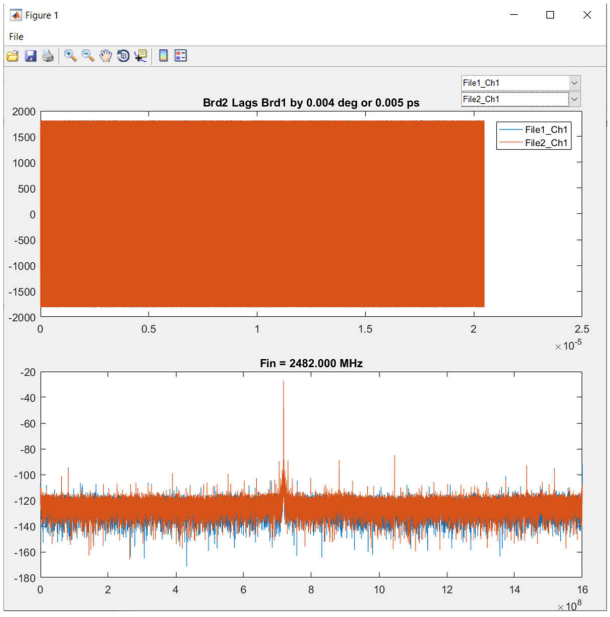


Figure 4-13. Board Skew at 2482 MHz

4.3 Summary and Conclusion

The TIDA-010191 design is a space grade multichannel JESD204B compliant clocking reference design that can be used for spaceborne radar imaging and broadband satellite communication systems. This TI Design demonstrates a high-performance (low phase noise) clock generation, using the LMX2615-SP and LMK04832-SP devices. This design also demonstrates the multichannel configurable phase synchronized clocks with skew of less than 10 ps. Finally, the ADC12DJ3200EVMCVAL onboard clock is replaced with TIDA-010191 outputs to demonstrate the impact on system performance. The system SNR is close to the ADC12DJ3200EVMCVAL performance and clock skew at less than 5 ps. The system shows deterministic latency behavior for every power ON cycle with the analog input channel-to-channel skew at less than 10 ps.

5 Design and Documentation Support

5.1 Design Support

TI helps you designing by giving you access to the complete design. Altium design files (complete project), schematics, Gerber files, bill of materials (BOM), layout plots and assembly drawings can be found in the TIDA-010191 product folder on ti.com. Corresponding engineering support is available on TI's E2E forum.

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010191.

5.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010191.

5.2 Documentation Support

1. Texas Instruments, *ADCxxDJxx00 Evaluation Module* user's guide
2. Texas Instruments, *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card* user's guide

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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