Design Guide: TIDA-050045

Type 3 IEEE802.3bt-ready Active Clamp Forward Converter PoE Powered Device Reference Design

Description

This reference design showcases a Type-3, Class 6, 51-W active clamp forward converter for powered devices (PD) through PoE. The TPS23730 PD controller provides detection and classification while also containing a PWM controller. This design takes in a 37-V to 57-V PoE input, and outputs a 5-V rail for applications such as IP network cameras and wireless access points.

Resources

TIDA-050045	Design Folder
TPS23730	Product Folder
TLV431	Product Folder

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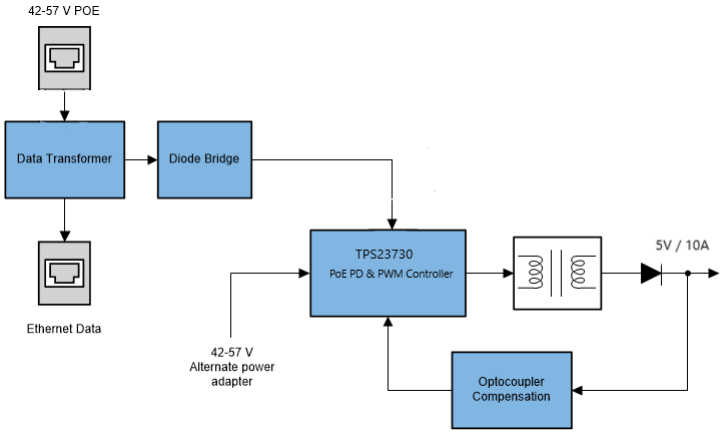
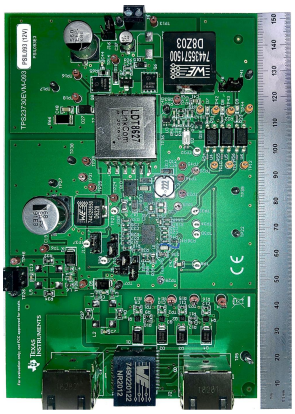
Features

- Supports Power Levels for IEEE802.3bt Type 3
- Isolated Active Clamp Forward Design
- Frequency Dithering for EMI Reduction
- Soft-Start Control with Advanced Startup
- Soft-Stop Shutdown
- Hiccup Mode Overload Protection
- Automatic Maintain Power Signature (MPS)
- Integrated Low 0.3-Ω Power Switch Supports 60 W of PSE Power

Applications

- Wireless Access Points





1 System Description

The IEEE802.3bt standard allows the implementation of >25-W PoE designs on a compliant, uniform standard over all four data pairs of the Ethernet connector. This Type-3, 50-W PoE flyback converter design is intended for users to develop such end products for various cost sensitive communication and industrial applications that require over 25 W of power on a 5-V rail. The design files include Schematics, Bill of Materials (BOMs), Altium files, Gerber Files and Fabrication Files.

This isolated active clamp forward design has an input voltage range of 37 V - 57 V for PoE and an optional auxiliary 37-V to 57-V power supply path which will be prioritized if enabled. The output of this design is 5-V at 10-A (50 W) which provides higher power than the previous sub-25-W IEEE802.3at standard allowed.

The TPS23730 soft-stop feature minimizes stress on switching power FETs and predictability of the shutdown procedure, allowing FET BOM cost reduction. Programmable spread spectrum frequency dithering (SSFD) is provided to minimize the size and cost of EMI filter. This design also has hiccup mode protection enabled, which provides excellent thermal protection during faults.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS
PoE Input voltage range	37 V - 57 V
Adaptor input voltage range	37 V - 57 V
Output voltage	5 V
Output current (PoE input)	10 A
Output current (adapter input)	10 A
PoE PD Classification	Class 6
PoE Efficiency	91.5%
Converter Efficiency	94%

2 System Overview

2.1 Block Diagram

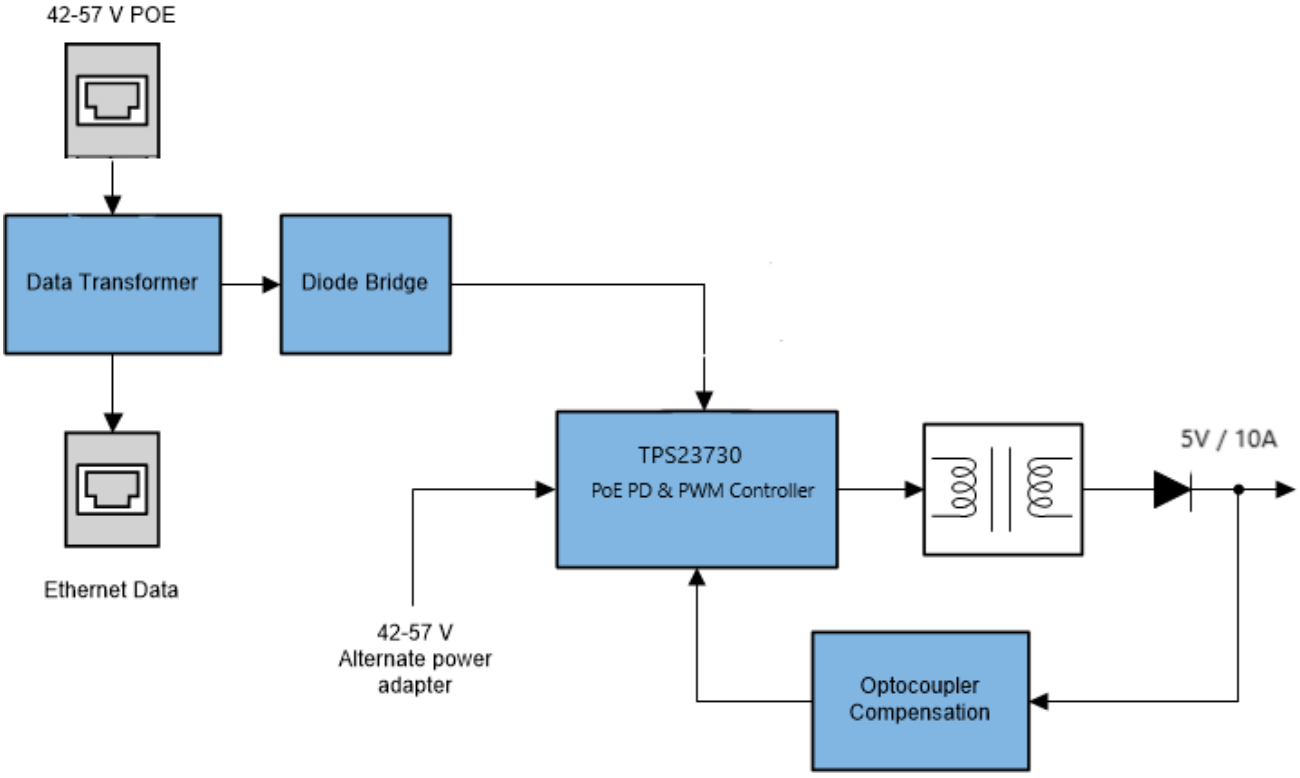


Figure 2-1. TIDA-050045 Block Diagram

2.2 Highlighted Products

2.2.1 TPS23730

The TPS23730 is an IEEE802.3bt compliant powered device (PD) interface that supports Type-3 PoE. All basic functionality such as detection, classification, inrush current limit (200 mA) and automatic maintain power signature (MPS) are integrated into a small form factor. A 0.3-Ω internal switch supports Type-3 up to 60 W of continuous power from the PSE which allows beyond 1.2 A through the PD during normal operation.

A critical TPS23730 feature to the design of this application is the soft-stop function. The soft-stop feature minimizes stress on switching power FETs, allowing FET BOM cost reduction. Soft-stop action consists in discharging in a controlled way the output capacitor of the converter, sending back the energy to the input bulk capacitor.

Another feature of the TPS23730 is the advanced startup function. This function allows for a smaller VCC capacitor, bootstrap circuitry is not needed, and it accounts for PSE inrush timing requirements.

The TPS23730 also features an auxiliary power detect (APD) input that allows an auxiliary supply to power the load. In scenarios where both PoE and the auxiliary supply are present, the TPS23730 allows the auxiliary supply to take priority over PoE.

The TPS23730 also contains several protection features such as thermal shutdown, current limit foldback and a robust 100-V internal switch.

2.2.2 TLV431

The TL431LI is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between V_{REF} (approximately 1.24 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

2.3 System Design Theory

2.3.1 IEEE802.3bt Introduction

PoE hardware classification allows the Power Sourcing Equipment (PSE) to determine the power requirements of a Powered Device (PD) before supplying power. This classification processes assists with power budgeting and efficiency. Prior to the IEEE802.3bt standard, the IEEE802.3at standard allowed up to 30 W of power sourced at the PSE and 25.5 W of power at the PD for Class 4 across two pairs of the Ethernet cable.

Table 2-1. IEEE802.3at Power Types and Classes

CLASS	TYPE	NUMBER OF PAIRS	POWER SOURCED AT PSE	MINIMUM POWER AT PD
0	1	2	15.4 W	13.0 W
1	1	2	4 W	3.84 W
2	1	2	7 W	6.49 W
3	1	2	15.4 W	13.0 W
4	2	2	30 W	25.5 W

The IEEE802.3bt standard utilizes all four pairs of the Ethernet connector and increases the maximum power the load can consume as well as the power the PSE can supply. Two new types are established under the IEEE802.3.bt standard: Type 3 (60-W PSE) and Type 4 (90-W PSE). With this increased power rating, various end equipment's such as surveillance cameras and access points can incorporate more features such as analytics, rotation and heaters. Table 2-2 highlights the IEEE802.3bt types and classes.

Table 2-2. IEEE802.3bt Power Types and Classes

CLASS	TYPE	NUMBER OF PAIRS	POWER SOURCED AT PSE	MINIMUM POWER AT PD
0	1 or 3	2	15.4 W	13.0 W
1	1 or 3	2 or 4	4 W	3.84 W
2	1 or 3	2 or 4	7 W	6.49 W
3	1 or 3	2 or 4	15.4 W	13.0 W
4	2 or 3	2 or 4	30 W	25.5 W
5	3	4	45 W	40.0 W
6	3	4	60 W	51.0 W
7	4	4	75 W	62.0 W
8	4	4	90 W	71.3 W

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

This Type-3, Class 6 PoE reference design can be configured in multiple modes of operation. This section will cover the setup required to evaluate this design.

3.1.1 Hardware

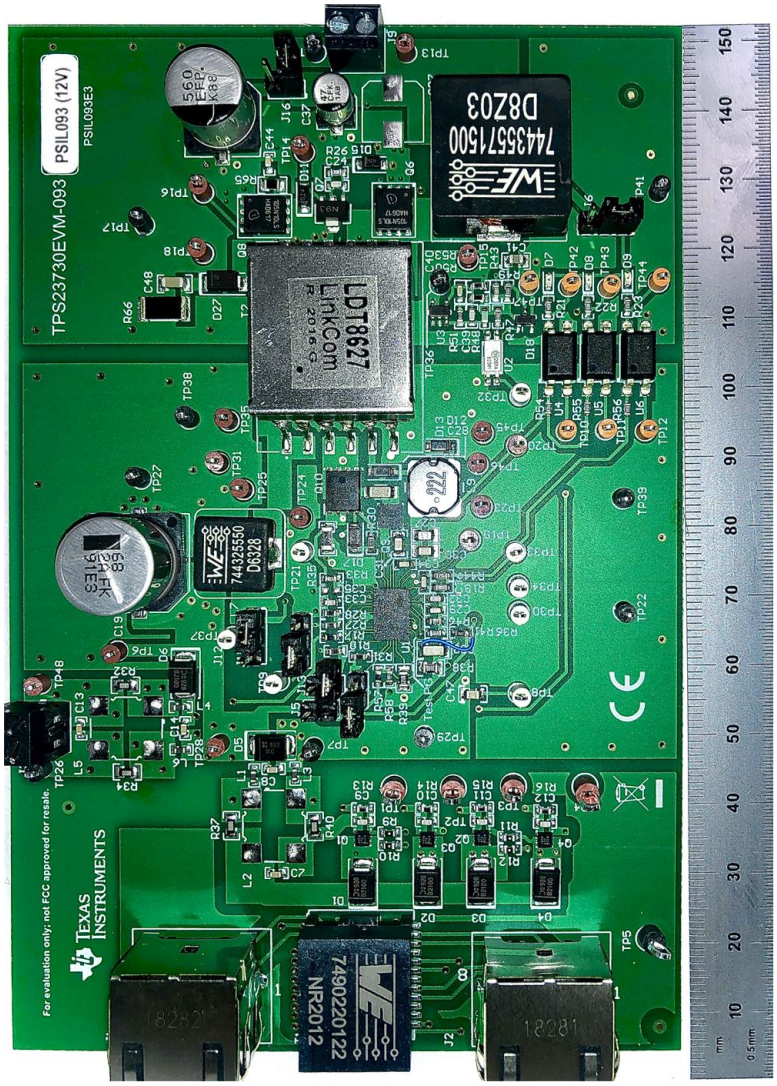


Figure 3-1. TIDA-050045 Reference Board (Top)

Table 3-1. Table of Jumpers and Connectors

TYPE	LABEL	CONNECTOR/JUMPER	DESCRIPTION
Input	Ethernet Power	J1	Data output after data transformer
	Ethernet Data	J2	Input connector for PoE
	Adaptor Input	J3	37-V to 57-V adaptor input. J4 jumper must be connected to enable adaptor power delivery
PD Configuration	APD Divider	J4	Enable to allow adaptor power delivery
	PPD	J5	Enable to provide lower input voltage turn on*. Range is around 19-V to 32V.
	DTHR	J8	Spread Spectrum Frequency Dithering control
	EMPS	J9	Automatic MPS control
	SCDIS	J10	TPL serial code setting
	TPL / TPH / BT Output	J11	TPH / TPL / BT output control
Output	V_{OUT}	J6	5-V output of design

3.2 Testing and Results

This section describes the test setup and test results for the TIDA-050045 board.

3.2.1 Test Setup

The jumpers and connectors configurations are shown in Table 3-2.

Table 3-2. TIDA Jumper and Connector Configuration

TYPE	LABEL	JUMPER/CONNECTOR	VALUE
Input	Ethernet Power	J1	Open
	Ethernet Data	J2	Power supply with voltage from 37-V to 57-V
	Adaptor Input	J3	Open for PoE tests. Connected to 37-V to 57-V power supply for adaptor tests
PD Configuration	APD_Connect	J4	Connected to pins 2 & 3
	PPD	J5	Open
	DTHR	J8	Connected
	EMPS	J9	Connected
	SCDIS	J10	Open
	TPH / TPL / BT Output	J11	Connected to pins 1 & 2 for LED's
Output	V_{OUT}	J11	Connected to electronic load. At full load, resistor load is 0.1 Ω.

3.2.2 Test Results

The following section provides the performance and test results of this design.

3.2.2.1 Efficiency

Figure 3-2 shows the efficiency performance at 48 V for PoE and DC/DC only.

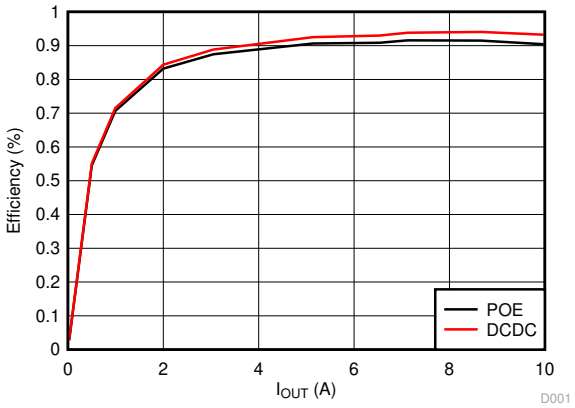


Figure 3-2. 48-V Efficiency for PoE and DC/DC Converter

3.2.2.2 Control Loop Gain/Stability

The loop gain margin, phase margin and crossover frequency are listed below along with the Bode plot 48 V at full load.

Gain Margin: –14.9 dB

Phase Margin: 56.8°

Crossover Frequency: 16.6 kHz

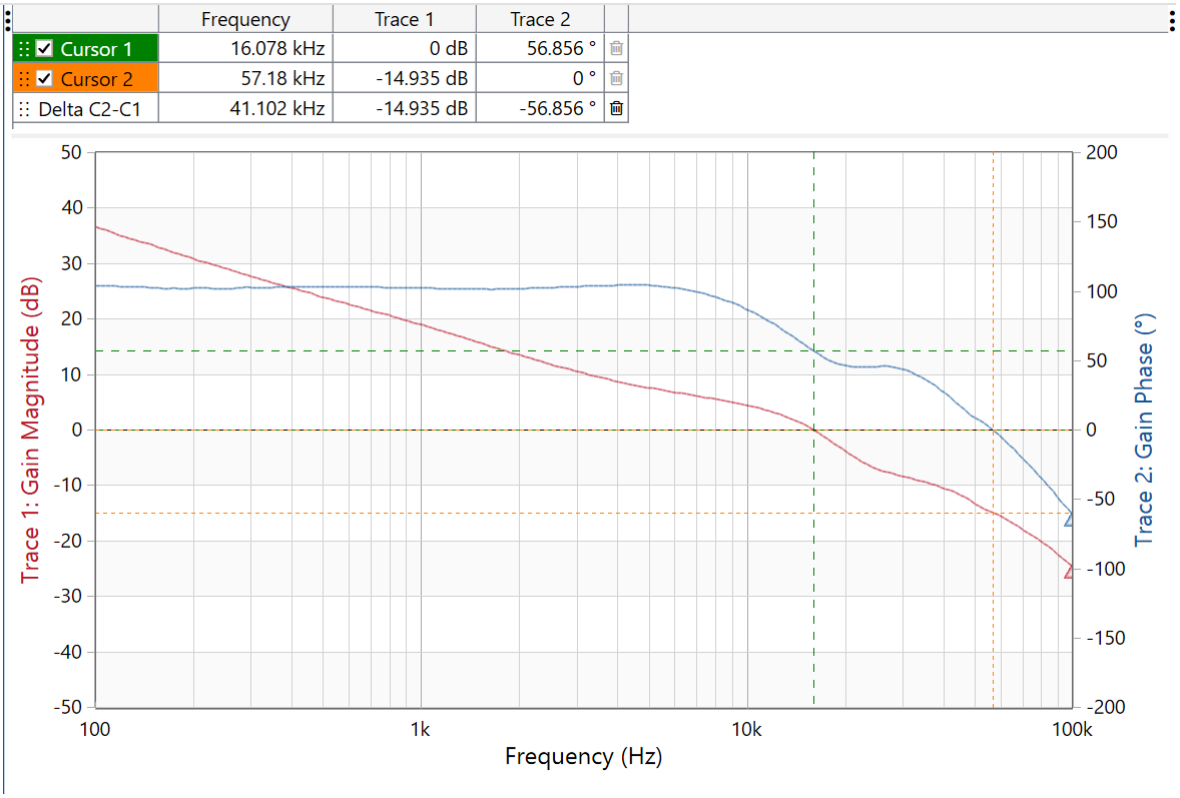


Figure 3-3. Loop Gain and Phase Margin at 48 V

3.2.2.3 Load Transient

Figure 3-4 shows the 5-V output voltage (at J6) when the load current pulses between 1 A and 10 A. The input voltage is 48-V at J2.

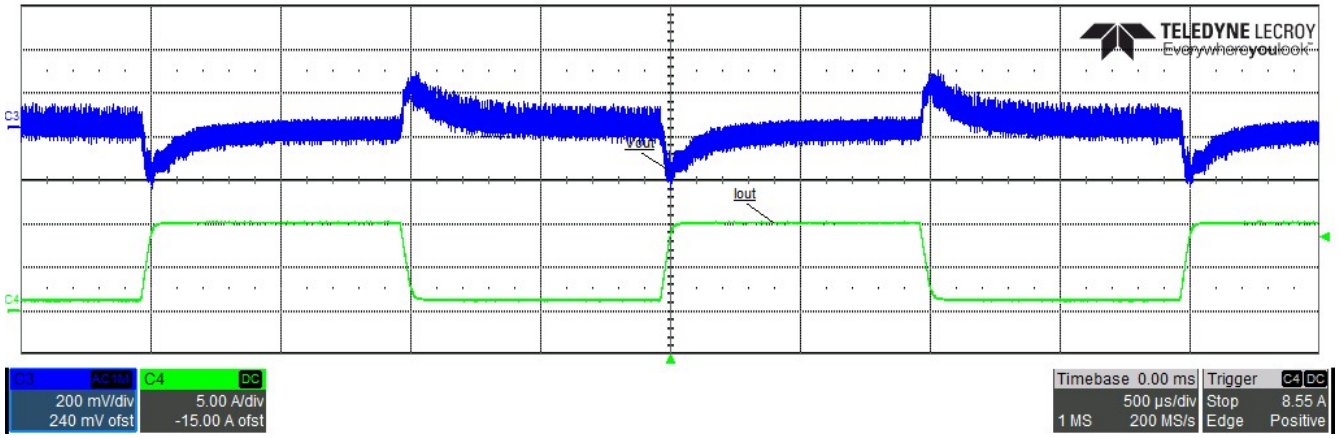


Figure 3-4. 1-A to 10-A Load Step, 48 V_{IN}, 200 mV/div, 500 us/div

Figure 3-5 shows the 5-V output voltage (at J6) when the load current pulses between 5 A and 10 A. The input voltage is 48-V at J2.

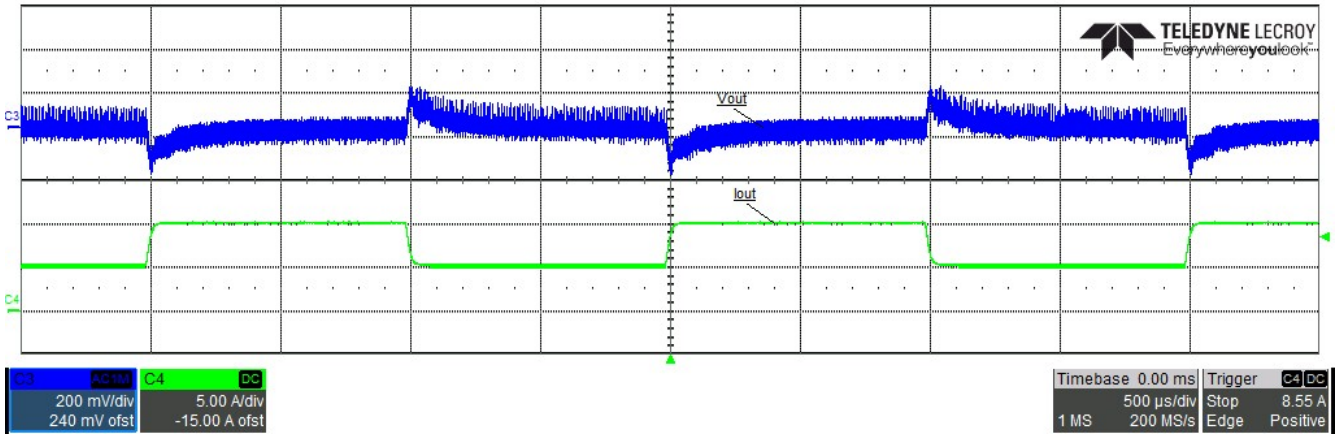


Figure 3-5. 5-A to 10-A Load Step, 48 V_{IN}, 200 mV/div, 500 us/div

3.2.2.4 Input and Output Ripple

The input ripple shown in Figure 3-6 and output ripple shown in Figure 3-7 were measured with an input voltage of 48-V (at J2), an output load of 10 A (at J6) and no band limiting.

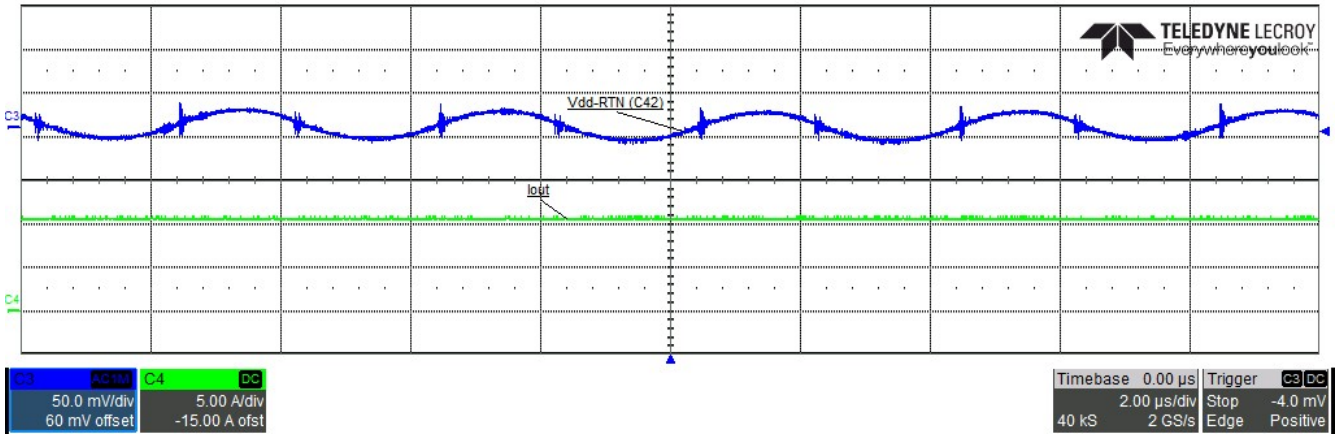


Figure 3-6. Input Ripple, 50 mV-div, 2 µs-div

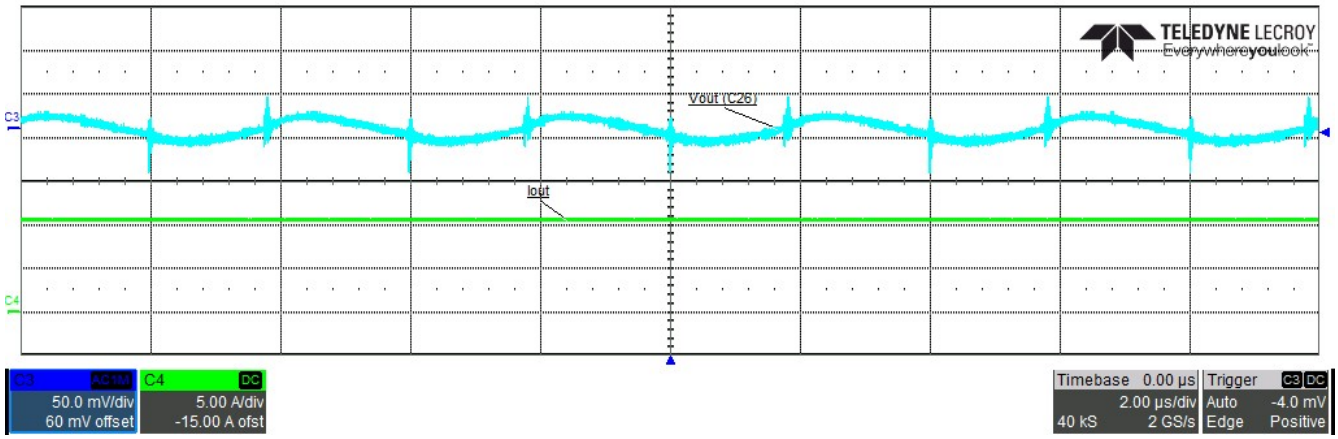


Figure 3-7. 5-V Output Ripple, 50 mV-div, 2 µs-div

3.2.2.5 Switching Waveforms

Figure 3-8 shows the V_{DS} voltage of secondary parallel MOSFET (Q6) and Figure 3-9 shows the primary synchronous MOSFET (Q8) at a 10 A load. The input voltage is 48-V. Figure 3-10 shows the VDS and Vgs voltage of primary switching MOSFET (Q11) and Figure 3-11 shows the VDS and Vgs voltage across the primary synchronous MOSFET (Q10) at a 10 A load.

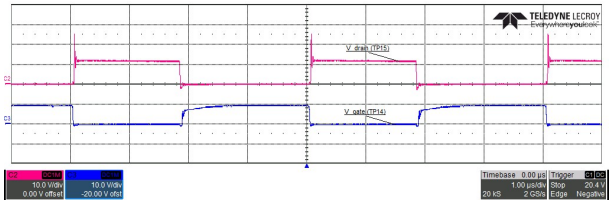


Figure 3-8. Secondary Parallel MOSFET Voltage, 10-A Load, 50 V-div, 1 µs-div

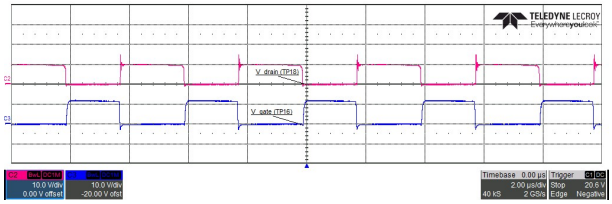


Figure 3-9. Secondary Series MOSFET Voltage, 10-A Load, 50 V-div, 1 µs-div

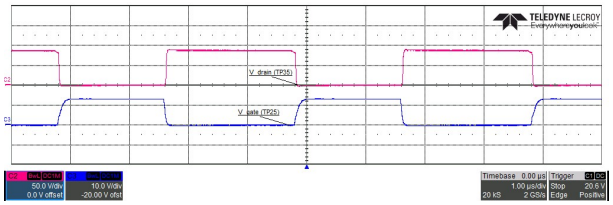


Figure 3-10. Primary MOSFET Voltage, 10-A Load, 50 V-div, 1 µs-DIV

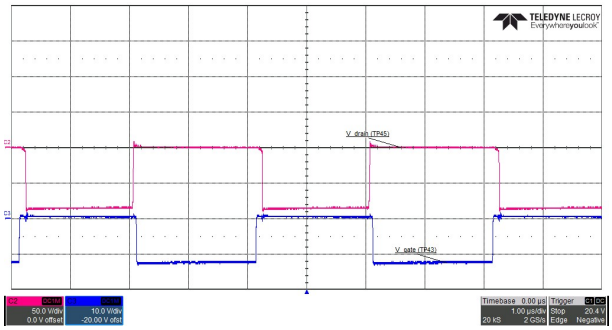


Figure 3-11. Primary Synchronous MOSFET Voltage, 10-A Load, 50 V-div, 1 µs-DIV

3.2.2.6 Start Up Response

Figure 3-12 and Figure 3-13 shows the 5-V output start up waveform after the application of 48 V at the PoE input (J1). The output was loaded to 10 A Figure 3-12 and 0 A Figure 3-13. Both waveforms include the output voltage (yellow), VCC (pink), VOUT (blue) and output current (green).

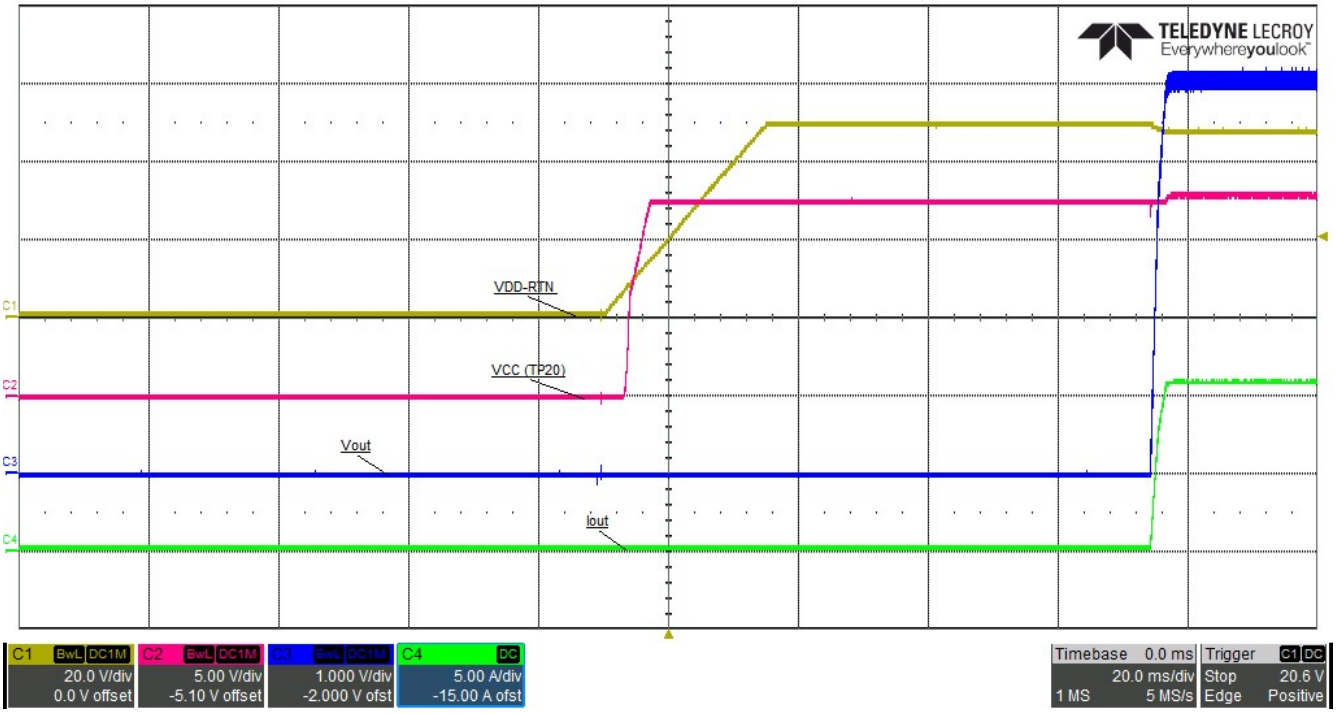


Figure 3-12. Startup Waveforms at 10-A Load, 20 ms-div

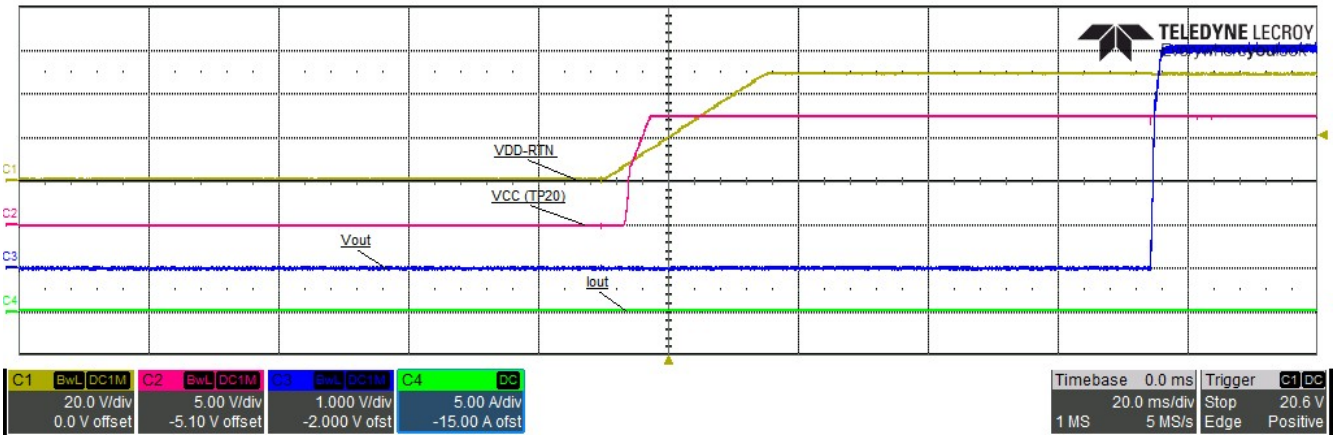


Figure 3-13. Startup Waveforms at 0 A Load, 20 ms-div

3.2.2.7 Soft-Stop Response

The TPS23730 has a soft stop feature that enables a controlled discharge of the output bulk capacitance. Please refer to SLVAEY9 for more information. Figure 3-14 and Figure 3-15 show the 5-V output waveform after the input voltage is removed.

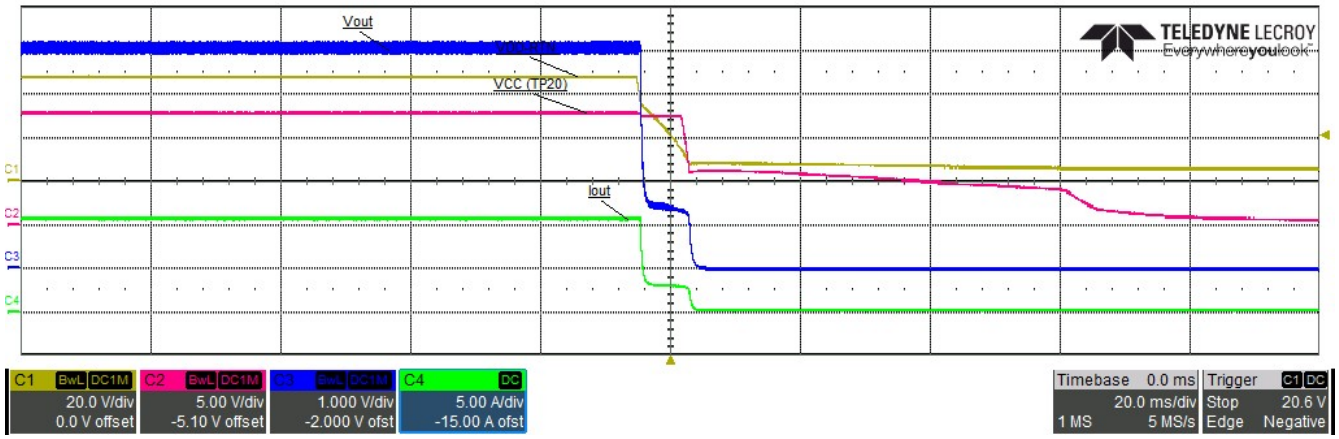


Figure 3-14. Shutdown Waveform 10-A Load

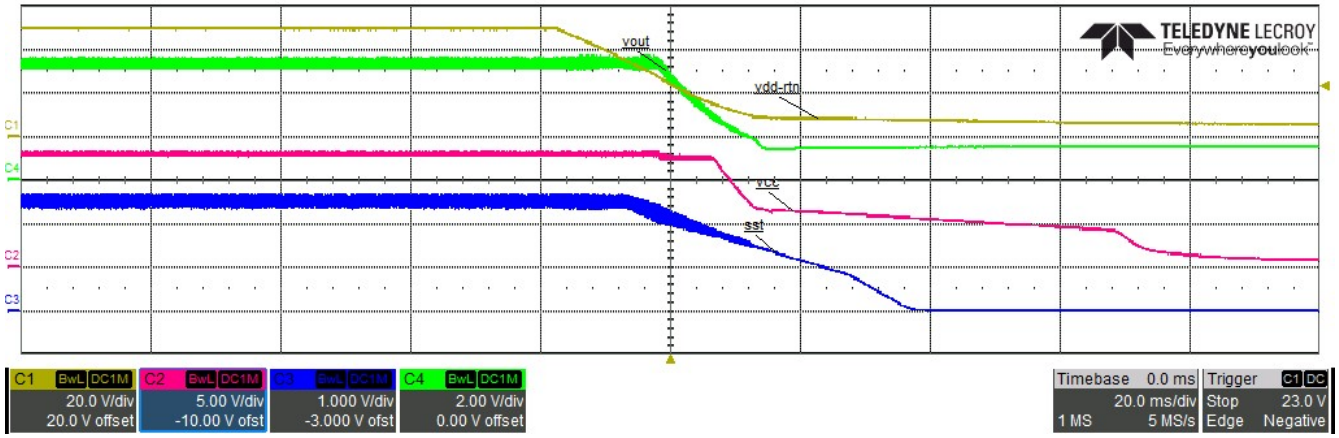


Figure 3-15. Shutdown Waveform 0-A Load

Figure 3-16 and Figure 3-17show the primary MOSFET Q11 during shutdown

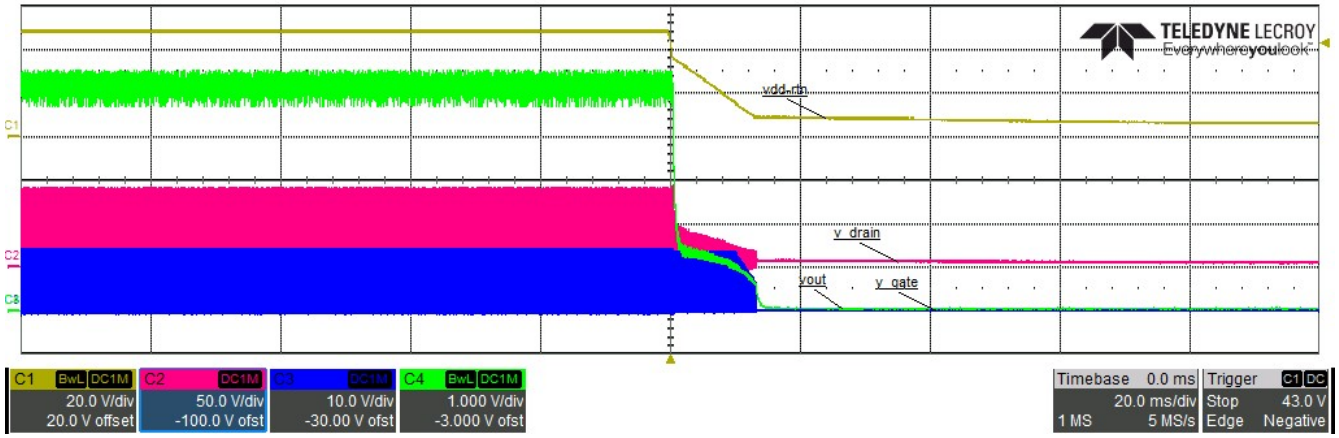


Figure 3-16. Shutdown Waveform Primary MOSFET with 10-A Load

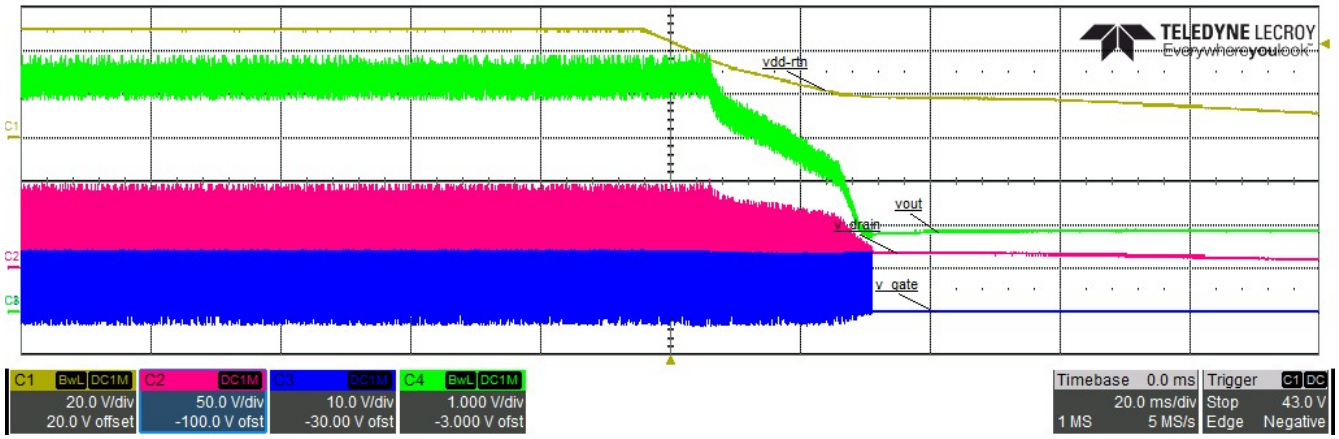


Figure 3-17. Shutdown Waveform Primary MOSFET with 0-A Load

Figure 3-18 and Figure 3-19 show the primary sync MOSFET Q10 during shutdown

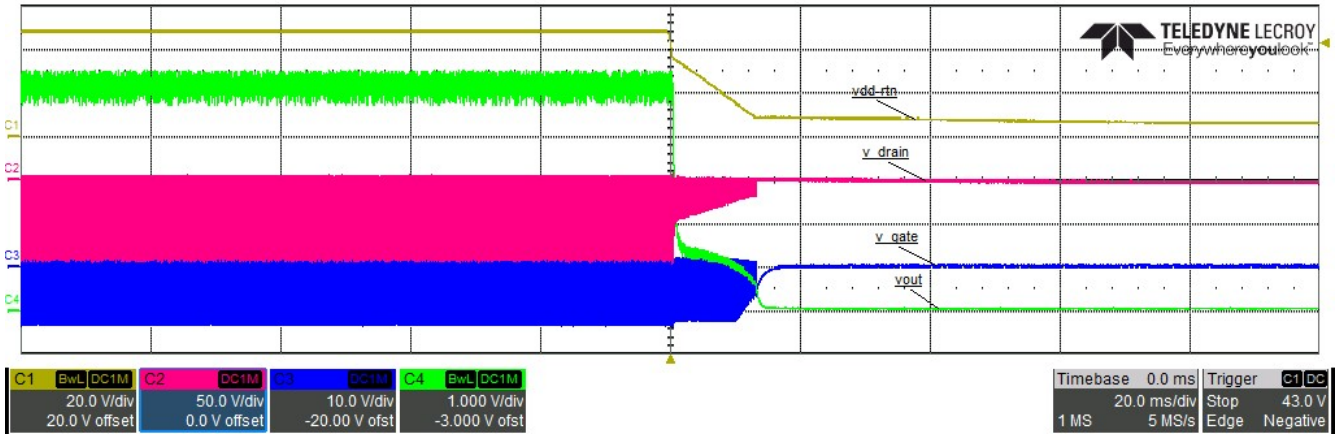


Figure 3-18. Shutdown Waveform Synchronous MOSFET with 10-A Load

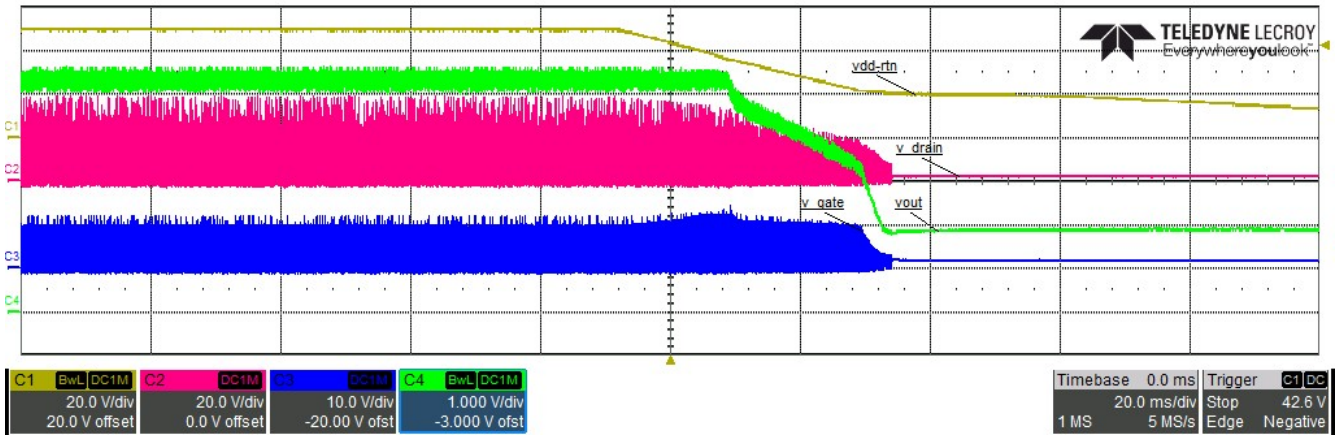


Figure 3-19. Shutdown Waveform Synchronous MOSFET with 0-A Load

Figure 3-20 and Figure 3-21 show the secondary series MOSFET Q8 during shutdown

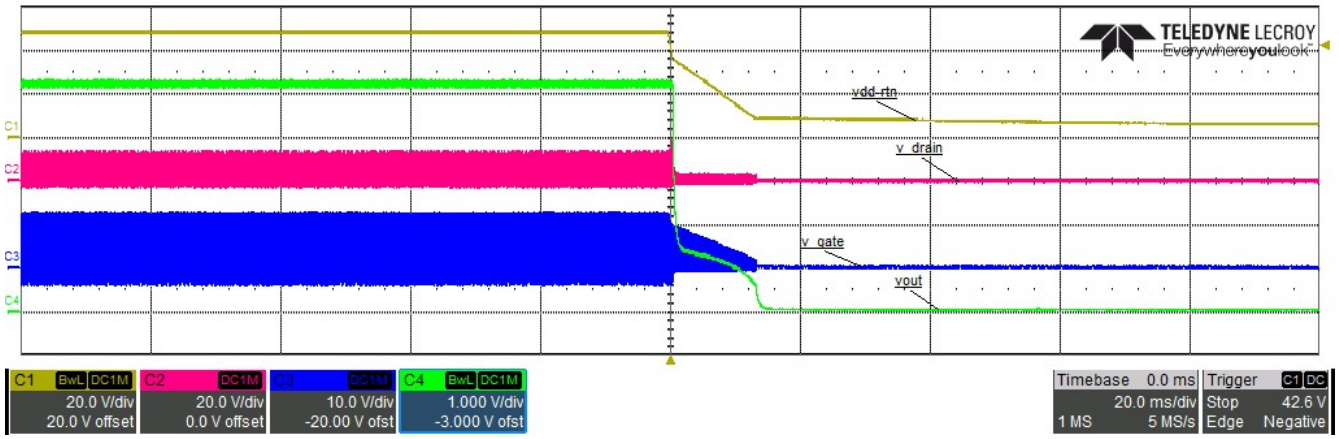


Figure 3-20. Shutdown Waveform Secondary Series MOSFET 10-A Load

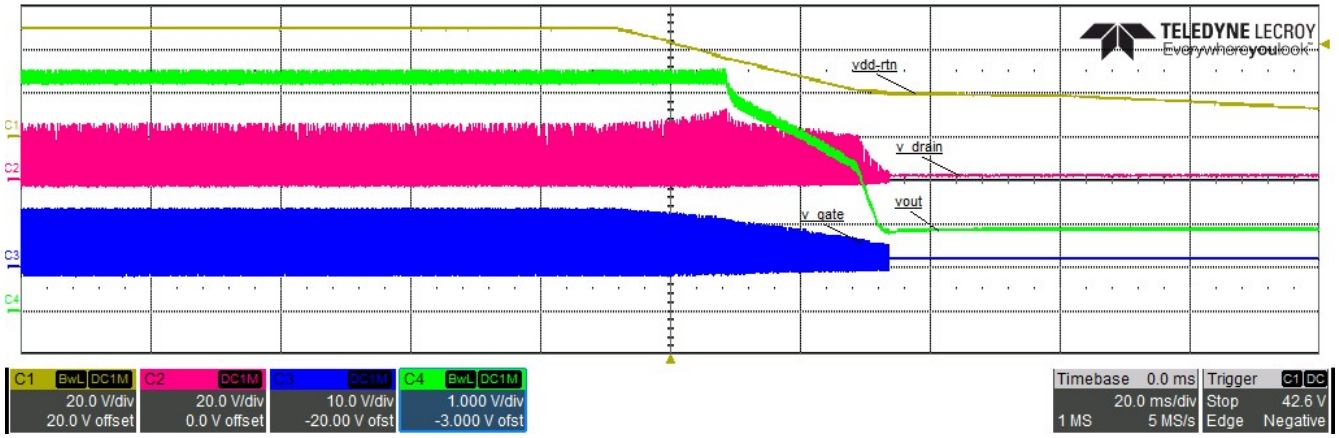


Figure 3-21. Shutdown Waveform Secondary Series MOSFET 0-A Load

Figure 3-22 and Figure 3-23 show the secondary parallel MOSFET Q6 during shutdown.

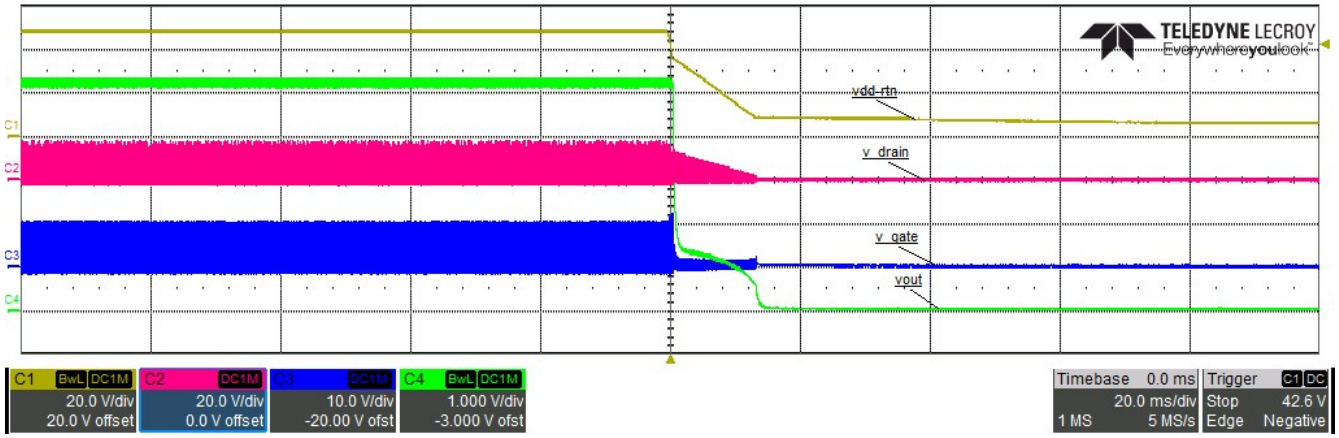


Figure 3-22. Shutdown Waveform Secondary Parallel MOSFET with 10-A Load

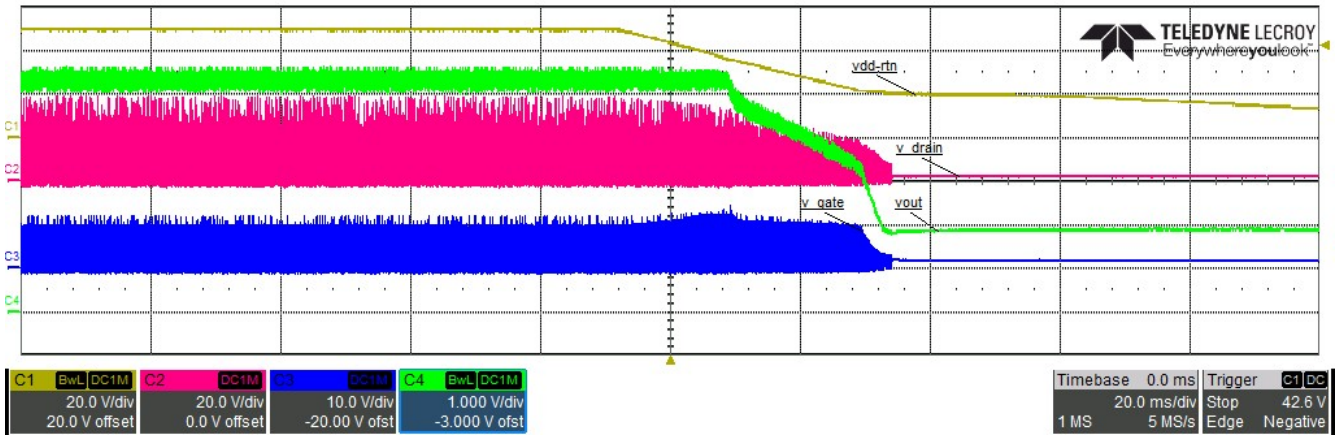


Figure 3-23. Shutdown Waveform Secondary Parallel MOSFET 0-A Load

3.2.2.8 Output Short Circuit Response

Figure 3-24 shows system response to a hot short at the 5-V output (J6). Output voltage (yellow), VCC (pink), VOUT (blue) and output current (green) are all shown in Figure 3-24.

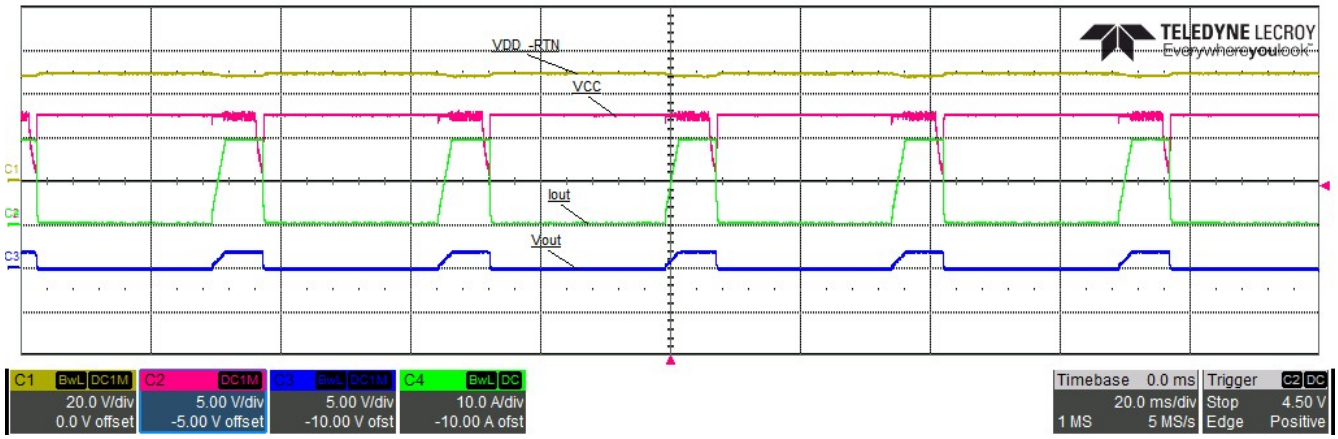


Figure 3-24. Short Circuit Hiccup Response, 20 ms-div

3.2.2.9 Thermal Performance

Top of board and bottom of board thermal measurements were taken at full PoE load (10-A), Figure 3-25 and Figure 3-26 shows the resulting thermals at full PoE load of 10A.

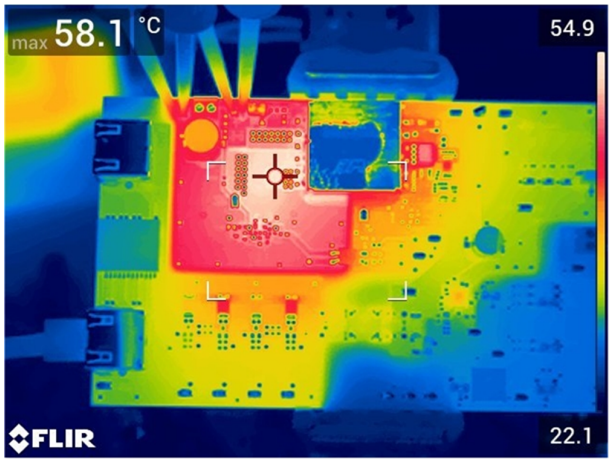


Figure 3-25. 10-A Load, Top of Board

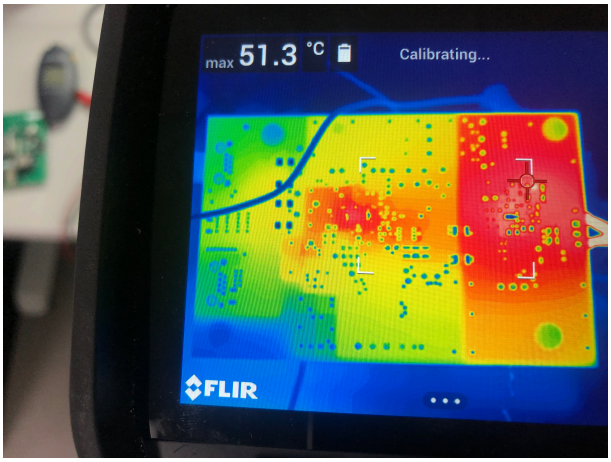


Figure 3-26. 10-A Load, Bottom of Board

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050045.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050045.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050045.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050045.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050045.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050045.

5 Related Documentation

1. Texas Instruments, *TPS23730 IEEE 802.3bt Type 3 PoE PD with High Efficiency DC-DC Controller data sheet*
2. Texas Instruments, *TLV431x Low-Voltage Adjustable Precision Shunt Regulator data sheet*

5.1 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Altium Designer® is a registered trademark of Altium LLC or its affiliated companies.
All other trademarks are the property of their respective owners.

6 Terminology

PD	Powered Device
PSE	Power Sourcing Equipment
PoE	Power Over Ethernet

7 About the Author

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