Design Guide: TIDEP-01020

Automotive Domain Controller for Gateway, Assisted and Automated Driving Systems Reference Design

Description

Decentralized vehicle architectures on the road today use individual ECUs that lack processing power and high-speed interfaces to handle the complex tasks and data movement needs of newly emerging automotive architectures. Higher level functions require the correct combination of DMIPS, data bandwidth and power efficiency. The DRA829V and TDA4VM processors in our Jacinto™ 7 processor family provide necessary performance, power, and automotive interfaces needed for these architectures.

This automotive reference design can enable domain-based architectures while showcasing the performance capabilities of DRA829V and TDAV4M SoCs. This 8-layer PCB design is optimized to reduce cost and time-to-market, making it a great way to evaluate Jacinto 7 processors with a fully functional domain controller board while enabling automotive connectivity interfaces including Ethernet, CAN-FD, and PCIe. Note: This DRA829/TDA4VM SoCs 8-layer reference design is tailored toward customers focused on cost, power, and size optimization rather than full entitlement of features; the design focuses only on a subset of the capabilities of the DRA829/TDA4VM SoCs. For superset features, please refer to the DRA829V Jacinto Automotive Processors, Silicon Revision 1.0 data sheet. For engineers who want to unlock more capabilities of the DRA829V or TDA4VM processors, please note that we also have a 10-layer PCB design for that purpose.

Resources

TIDEP-01020	Design Folder
DRA829, TPS6594-Q1, 941AS-Q1	Product Folder
DP83TC-Q1, TCAN1043-Q1, TCAN1042-Q1	Product Folder
TAS6421-Q1, TPA6304-Q1	Product Folder

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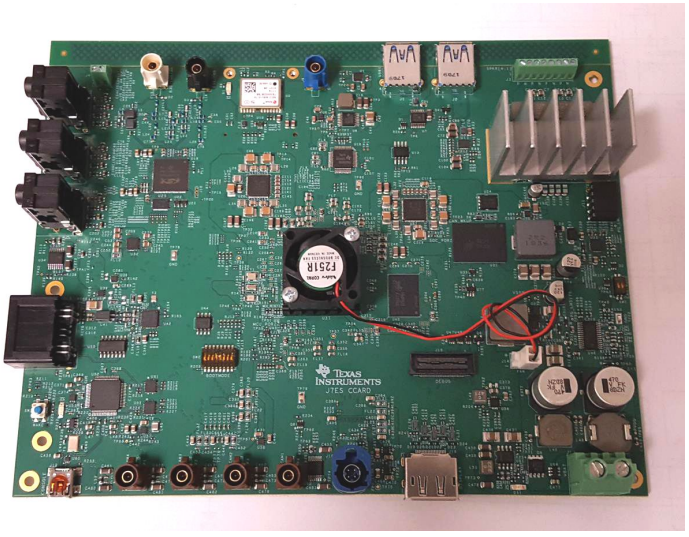
Features

- DRA829 and TDA4 SoCs as domain controller
- Optimized design on 8-layer PCB
- Auto Connectivity (Ethernet, PCIe, CAN-FD)
- Multiple camera input for rear-view, driver monitoring or surround view
- Multiple high resolution display output
- Multi-zone audio input and output
- Dual-tuner for DAB/HD/AM/FM radio and diversity
- Connectivity (BT, WiFI, GPS, GNSS)

Applications

- Advanced Driver Assistance Systems (ADAS)
- Automotive Infotainment and Cluster
- Automotive Gateway
- ADAS Domain Controller



1 System Description

This 8-layer reference design is based on the DRA829 and TDA4VM automotive applications processor, a highly optimized and scalable device that meets increasing compute and data bandwidth requirements of the automotive industry. The DRA829/TDA4VM Integrates an optimal mix of performance, low power, and data bandwidth to meet evolving market trends. DRA829/TDA4VM is based off a heterogeneous architecture which integrates connectivity, a variety traditional automotive (CAN-FD) and high-speed peripherals (PCIe, USB3.x, Gigabit Ethernet), safety and security (via integrated HSM). Integrated PCIE and Ethernet switches enable increased data movement with low software overhead and lower BOM.

The reference design supports multiple external high-resolution displays. The design also enables 4x camera input for rear-view camera, driver monitoring system(DMS) or surround view(SRV) applications. A dual tuner is used to support AM/FM/HD/DAB and diversity, expanding use to both European and American markets. 4 zone audio output and 4 zone audio input allows for seamless surround sound and speech recognition. With increasing use of connectivity functions and FOTA in the automotive space, the design includes a module that enables enable BT and WiFI. Telematics is also showcased in the design via GPS and GNSS capabilities.

This reference design serves as a starting point for OEMs and Tier1 to easily and quickly create a fully functional DRA829/TDA4VM solution in the automotive space. Leveraging this design can substantially decrease development costs and time to market.

1.1 Key System Specifications

Table 1-1. Key System Specifications Table

SYSTEM	SPECIFICATION
SoC	DRA829/TDA4VM
Power	12 V
Display	• eDP connector • DSI output with FDPLink support
Backlight	Supported via PWM
Camera	4x 2Mpixel camera input for DMS/SRV
Radio	Dual tuner to support AM/FM/HD/DAB and diversity
Audio	• 4 zone audio output • 4 zone audio input (2x Line In, 2x Mic) • Warning Chimes
Auto Connectivity	• Ethernet, CAN Wakeup, CAN-FD, USBSS
Connectivity	• BT • WiFI
Telematics	• GPS • GNSS
Memory	• 8 GB of LPDDR4 at 3733 MT/s • 32 GB eMMC/UFS eMMC Flash • 64 MB OSPI
Wakeup	Via CAN, PMIC

2 System Overview

2.1 Block Diagram

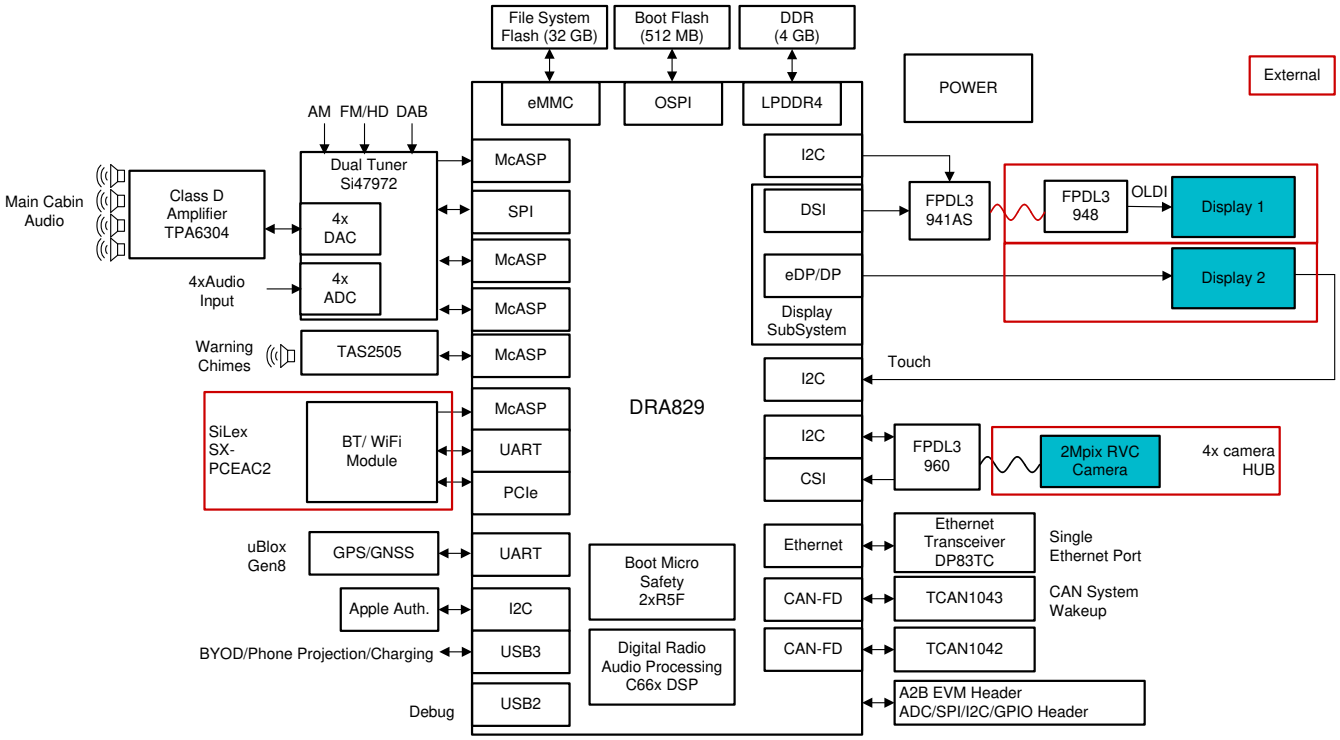


Figure 2-1. TIDEP-01020 Block Diagram

2.2 Design Considerations

- Showcase DRA829/TDA4VM domain controller SoC features
- Demonstrate optimized system reference design
- Cost-optimized automotive Q100 parts where possible to minimize total system BOM

2.3 Power Considerations

The Power Tree Design is shown in Figure 2-2 and Figure 2-3.

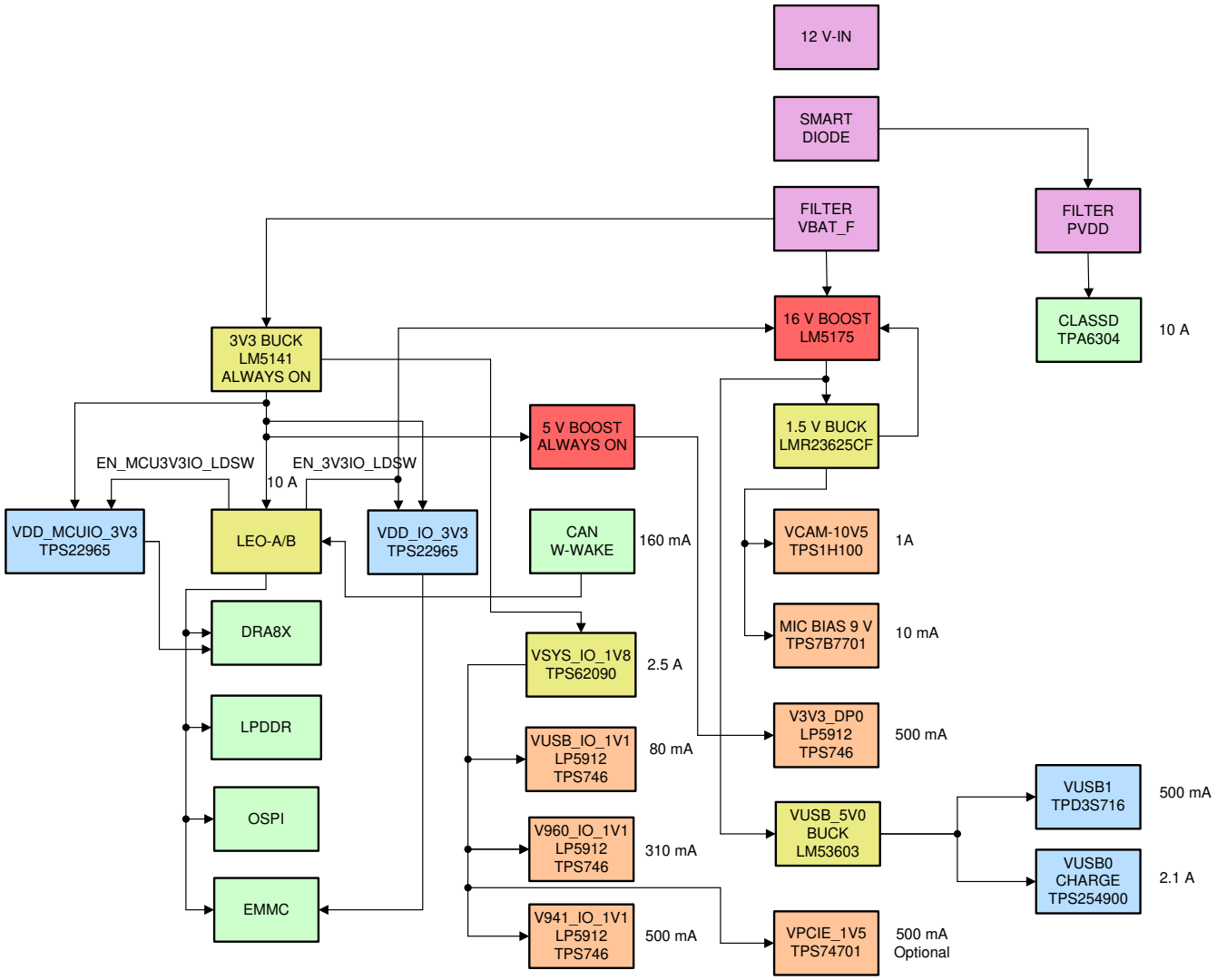


Figure 2-2. Power Tree 1

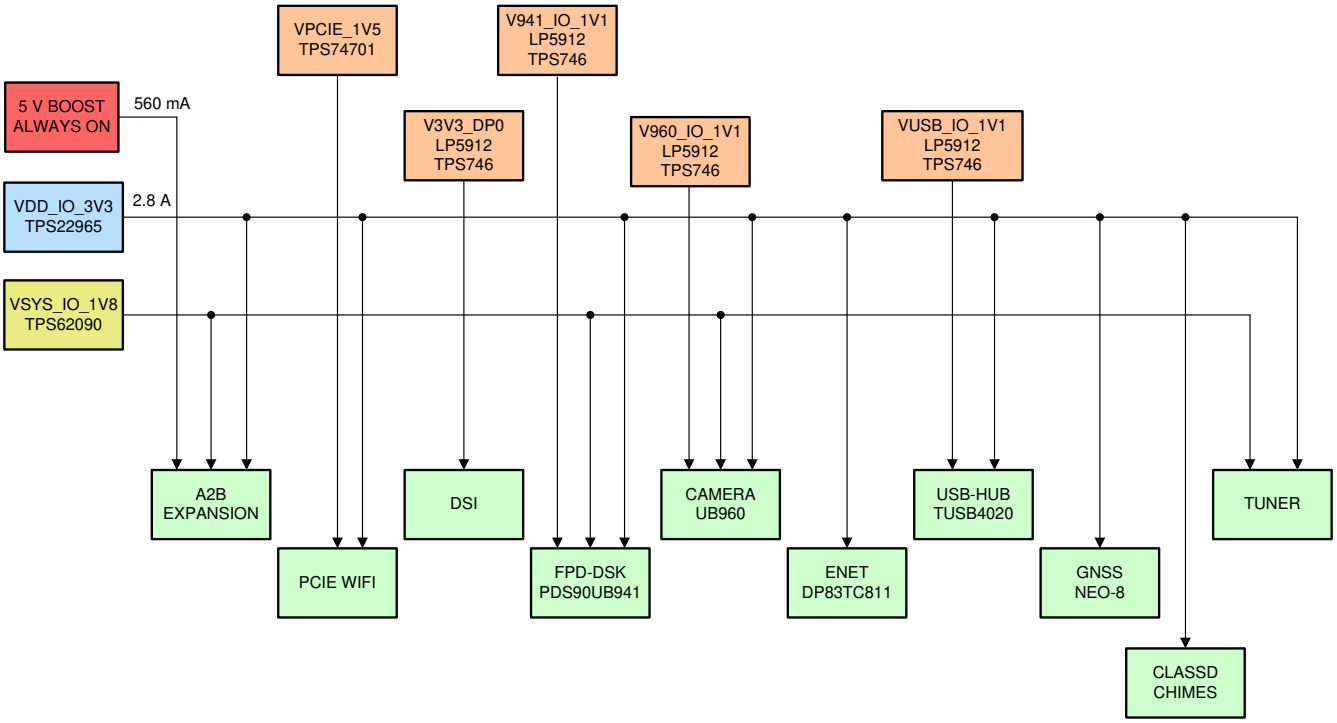


Figure 2-3. Power Tree 2

2.4 Highlighted Products

2.4.1 Processor

The reference design is based on the DRA829/TDA4VM SoC. The DRA829/TDA4VM is a heterogeneous automotive processor with dual ARM Cortex-A72 cores and six ARM R5Fs to support a variety of processing and real-time applications. The SoC also has integrated 4-port PCIE and 8-port Ethernet switch allowing for high data bandwidth communication in gateway applications.

2.4.2 Power Supply

The reference design is based off of a 12V input and uses dual TPS6594x-Q1 in the power topology. The TPS6594x-Q1 is a PMIC that integrates optimized power management, ASIL-D features, and wakeup functionality into a chip.

2.4.3 Display

This reference design supports multiple high resolution display outputs based on DSI and eDP interfaces. eDP interface can drive multiple displays in a daisy-chain using Multi Stream Transport (MST).

2.4.4 FPDLink Serializer

The reference design uses the DS90UB941AS-Q1 to serialize DSI output from the DRA829/TDA4VM automotive processor to FPD-Link III format. This enables serial transmission over long distances and signal is deserialized on receiving end.

2.4.5 Input/Cameras

The reference design uses the DS90UB960-Q1 hub to receive serialized sensor data from up to four independent video streams and is aggregated into the CSI-2 input of DRA829/TDA4VM processor. The DS90UB960-Q1 receives data from sensors such cameras supporting full HD 1080p/2MP resolution at 60-Hz frame rates.

2.4.6 Ethernet

The Ethernet interface is supported on this reference design to enable transfer of data content from other subsystems. A DP83TC811R-Q1 Ethernet Phy is used to interface with the DRA829/TDA4VM automotive processor where content sent over the Ethernet interface is processed.

2.4.7 CAN

This reference design supports the CAN interface using a TCAN1043 and TCAN1042. The TCAN1043 transceiver supports CAN-FD functionality and meets the requirements of the ISO 11898-2. The device has wakeup pin support enabling DRA829/TDA4VM wakeup without need for an external MCU. CAN wakeup integration details as follows:

- Mode 1: OFF
- Mode 2: Wakeup
  - CAN module is in standby mode. Signal can wake up CAN which in turns on PMIC and rest of the board.
- Mode 3:ON
  - CCARD is ON and fully functional

The TCAN1042 transceiver supports CAN-FD functionality and meets the ISO 11898-2:2016 and ISO 11898-5:2007 Physical Layer Standards

2.4.8 Class-D Amplifier

This reference design supports 4-zone audio output with the TPA6304-Q1 four-channel Class-D Burr-Brown audio amplifier. This reference design supports single zone audio output for warning chimes with a TAS6421 Class-D amplifier. Both devices implement a 2.1 MHz PWM switching frequency that enables a cost optimized solution in a very small PCB footprint while offering exceptional sound quality with up to 40 kHz audio bandwidth.

2.4.9 Other Products

2.4.9.1 Radio Tuner

The reference design uses the Si47972 Dual tuner to support AM/FM/, HRC MRC, DAB, phase diversity and weatherband++. AM/FM & phase diversity + HD MRC functionality is targeted for North America and AM/FM & phase diversity + DAB functionality is targeted for Europe.

2.4.9.2 Bluetooth/WiFi

The reference design uses the SX-PCEAC2 module for dual band 802.11 a/b/g/n/ac and Bluetooth support. The module supports high performance up to throughputs of 867 Mbps and connects to the DRA829/TDA4VM processor via a mini-PCIE form factor.

2.4.9.3 GPS/GNSS

The reference design uses the U-Blox GPS Neo M8U/M8L MX8030 chipset for GPS and GNSS functionality.

2.4.9.4 Memory

The reference design uses two 4GB MT53D1024M32D4DT memory banks for a total of 8 GB of onboard LPDDR4 memory running at 3733 MT/s. For on-board NAND flash, the design uses the MTFC32GAPALNA which is 32 GB of NAND flash connected to DRA829/TDA4VM's eMMC interface. To support fast booting over OSPI, the board uses the MT35XU512ABA1G12 for 64 MB of NOR Flash.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This reference design is a hardware-only design and end-users will need to develop their own software tailored to their system. Resources are provided below on basic hardware setup and software references.

3.1.1 Hardware

The board requires a 12V DC power supply to power up. To fully utilize all hardware interfaces on the reference design, it is recommended that following external parts should be connected:

3.1.2 Software

There is no official software development kit (SDK) available for this design. SDK for DRA829/TDA4VM EVM is available at https://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X and can be used as starting point to port this hardware if desired.

3.2 Testing and Results

3.2.1 Test Setup

Diagnostic tests were run on the board after power up (12 V DC power brick) with no external components attached (no displays, speakers, or cameras)

3.2.2 Test Results

The following tests were run on board.

Table 3-1. Test Results

SYSTEM	SPECIFICATIONS
Power	Validated. Powers up drawing about 250mA@12V and runs up to 1.2A@12V when tests are running.
CCS connect	Validated
Boot Mode Settings	Validated
UART Consoles	Validated
DDR	LPDDR4 at 3733 MT/s validated
eMMC	Validated
OSPI	Validated
SDCARD	Validated
I_2C	Validated with PMIC, ID-EEPROM, UB941, TAS6304, TAS2505
GPIO	Validated
LEDs	Validated

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDEP-01020.

For the 10-layer board, please see the following TIDEP-01020.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP-01020.

For the 10-layer board, please see the following TIDEP-01020.

4.3 PCB Layout Recommendations

To download the layer plots, see the design files at TIDEP-01020.

For the 10-layer board, please see the following TIDEP-01020.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDEP-01020.

For the 10-layer board, please see the following TIDEP-01020.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP-01020.

For the 10-layer board, please see the following TIDEP-01020.

5 Related Documentation

1. Texas Instruments, *Jacinto™ TDA4x / DRA829 Processors Technical Reference Manual*
2. Texas Instruments, *DRA829 Applications Processor Data Sheet*
3. Texas Instruments, *DRA829Vx Evaluation Module*
4. Texas Instruments, Software Development Kit for DRA8x and TDA4x Jacinto Automotive Processors

5.1 Trademarks

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (October 2020)	Page
• Updated Description	1

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