Design Guide: TIDA-010122

Reference Design Synchronizing Data Converter DDC and NCO Features for Multi-channel RF Systems

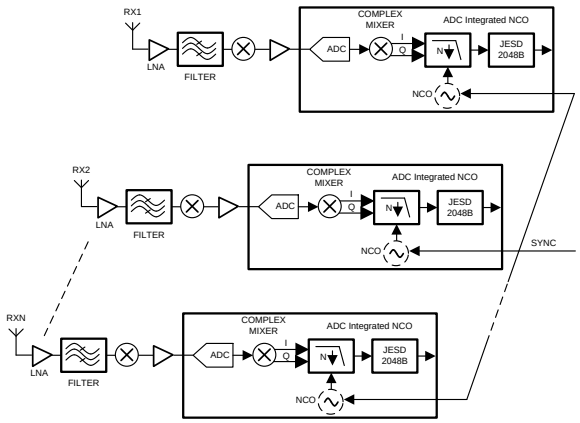
Description

This reference design provides the solution for synchronization design challenges associated with emerging 5G adapted applications like massive multiple input multiple output (mMIMO), phase array RADAR, and communication payload. The typical RF front end contains antenna, low noise amplifier (LNA), mixer, local oscillator (LO) in analog domain and analog-to-digital converter, numerical controlled oscillator (NCO) and digital down converter (DDC) in digital domain. To achieve overall system synchronization these digital blocks need to be synchronize with system clock. This reference design uses ADC12DJ3200 data converter, achieve less than 5-ps channel-to-channel skew across multiple receiver with deterministic latency by synchronizing on chip NCO with SYNC~ and uses Noiseless Aperture Delay Adjustment (t_{AD} Adjust) feature to further reduce skew.

Resources

TIDA-010122, TIDA-01027	Design Folder
ADC12DJ3200, TPS259261	Product Folder
LMK04828, LMX2594, LMK61E2	Product Folder
LMH6401, LMH5401	Product Folder
TSW14J57EVM	Tool Folder

TI E2E™ Community — ASK Our E2E™ Experts

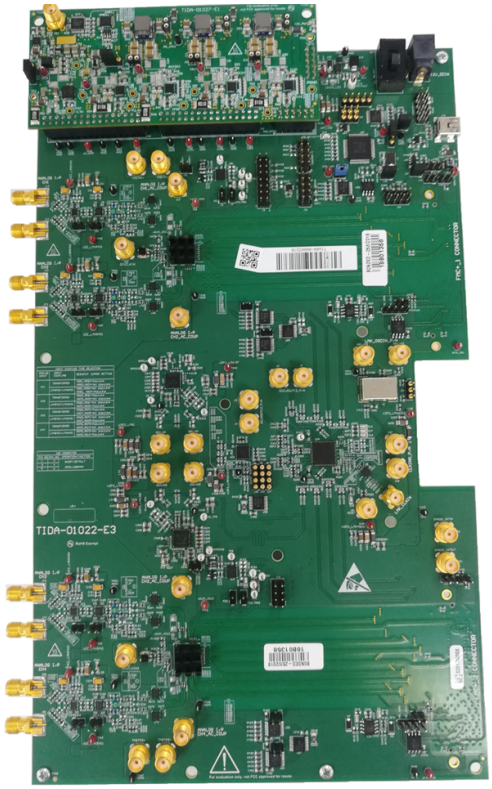


Features

- 4-channel, 3.2-GSPS, 6-GHz high-speed analog front end
- On-chip NCO synchronization allows synchronization across multiple ADCs using SYNC~
- Multi-channel JESD204B complaint clock
- JESD204B supporting 8, 16, or 32 JESD lanes and data rates up to 12.8 Gbps per lane
- Companion power reference design with a > 85% efficiency at 12-V input
- Includes theory, calculations, component selection, PCB design and measurement results

Applications

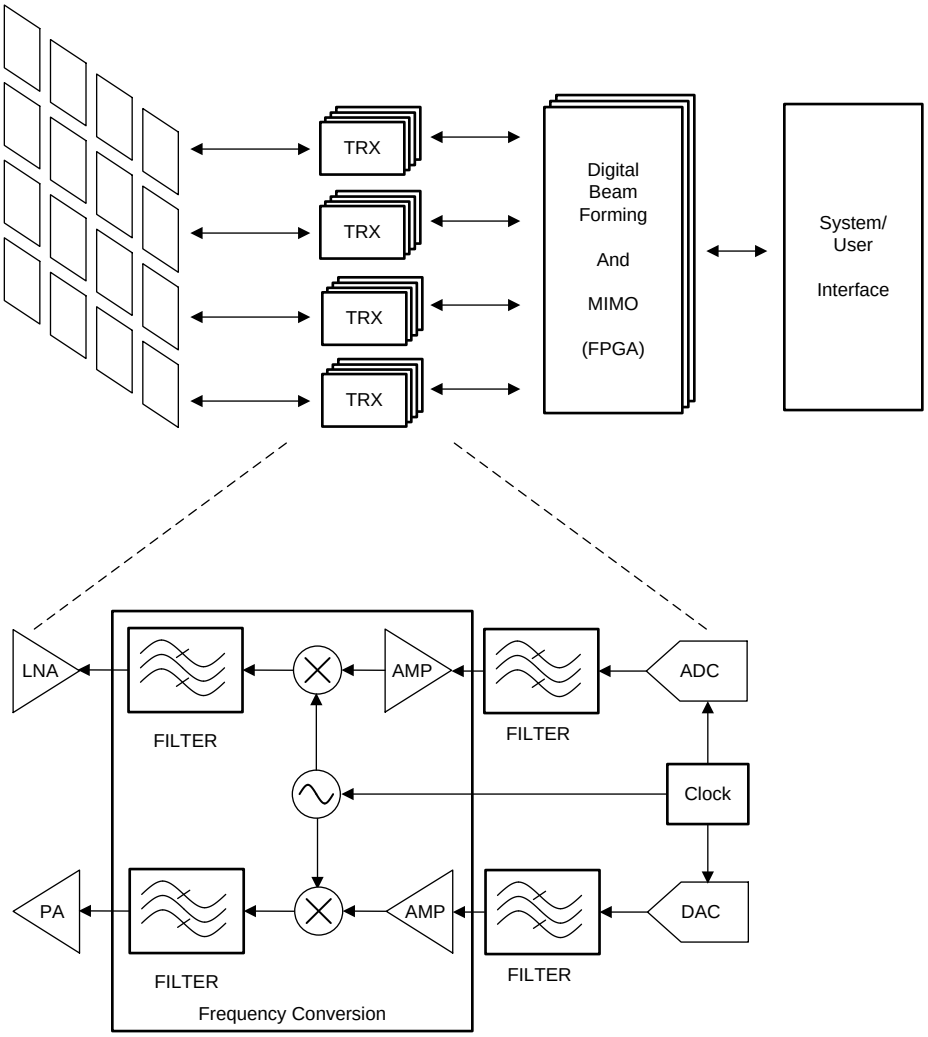
- RADAR
- Communications payload
- Wireless communications test equipment
- Vector signal transceiver (VST), vector signal analyzer (VSA), and vector signal generator (VSG)



1 System Description

Emerging network communication systems like 5G technology (5G NR), WLAN 802.11ax standards use massive Multiple input multiple output (MIMO), digital beam forming which improves network throughput by spectral efficiency to cover large users. This is achieved by many parallel transmissions using spatially placed antennas instead of a single antenna transmission. Signal directivity increases with more antennas with same the transmit power; therefore, users get a strong signal and less leakage in the other direction.

Figure 1. Typical 5G System Block Diagram



Similarly RADAR, electronic warfare, satellite communication payloads require large numbers of transceivers (transmit and receive signal chain) in their applications.

These high-performance multi-channel receivers require a signal chain with wide bandwidth, high dynamic range, high sample rate, low channel-to-channel skew with deterministic latency.

This reference focuses on the most critical design challenges in receiver synchronization across multiple channels with deterministic latency.

1.1 Key System Specifications

Table 1 lists the key system level specifications for the TIDA-010122 board.

Table 1. Key System Specifications

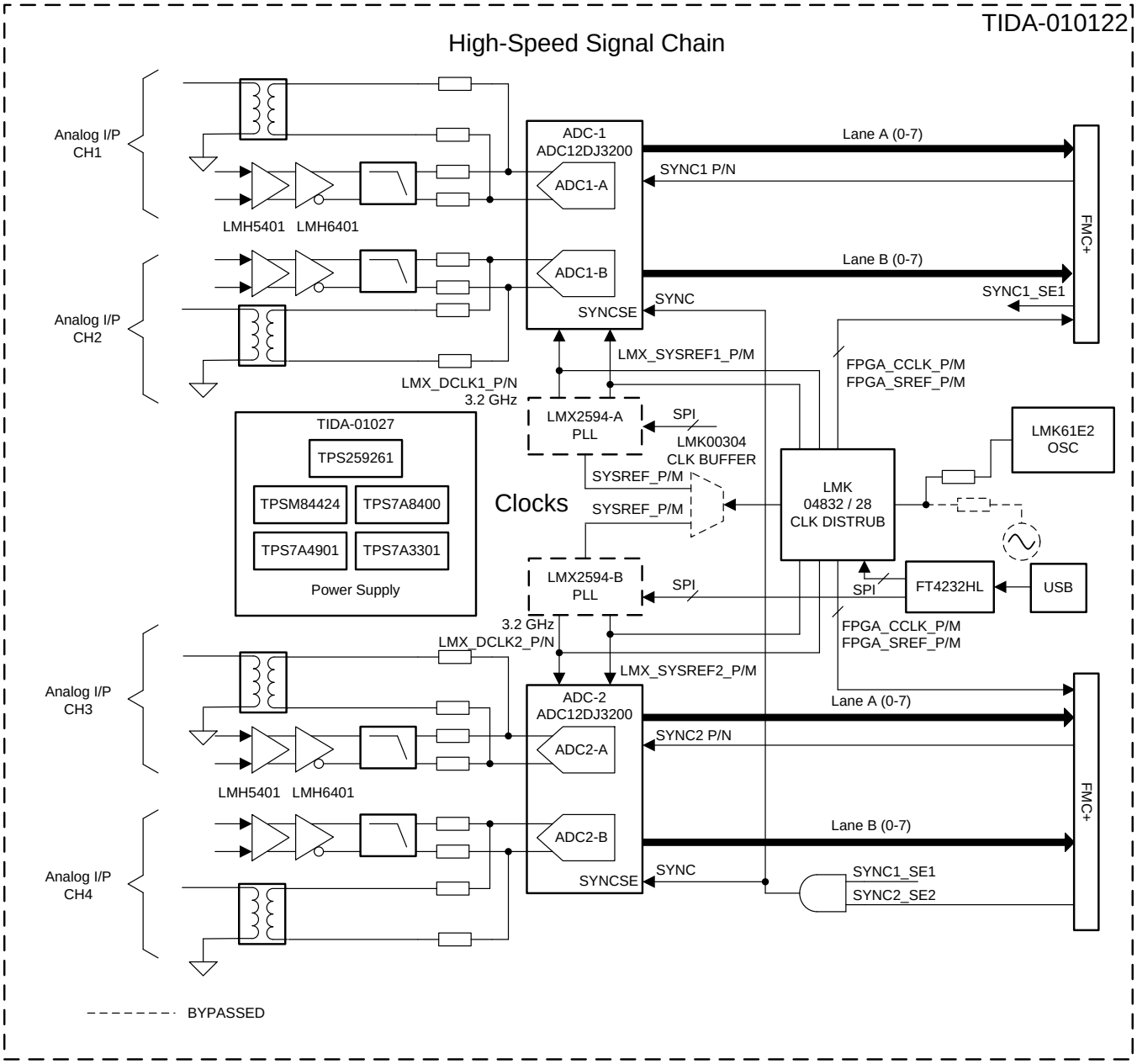
PARAMETER	SPECIFICATIONS			DETAILS
Input channels	4			
Input type	Single ended, differential ended			
Input analog bandwidth(–3 dB)	3.2 GSPS / Channel			
Resolution	12 bit			
Decimation mode	16 × decimation (JMODE15/16), 15 bit - complex data			
System performance (–7 dB FS) F_S = 1480 MHz, F_{NCO} = 1270 MHz and F_{IN} = 1250 MHz	SNR	SFDR	THD	Figure 35
	60.56	70.13	89.48	
Channel-to-channel skew	< 5 ps			
Connector	560 Pin FMC+ interface connector Supports TSW14J57 high-speed capture card			
Power	12-V DC, 4 A			TIDA-01027
Form factor (L × W)	295 mm × 176 mm			

2 System Overview

2.1 Block Diagram

Figure 2 shows the system-level block diagram of the TIDA-010122 design, which was developed using the hardware from the flexible 3.2 GSPS multi-channel AFE reference design for DSOs, RADAR, and 5G wireless test systems (TIDA-01022) along with the power reference design maximizing signal chain ENOB in very high-speed DAQ systems (TIDA-01027).

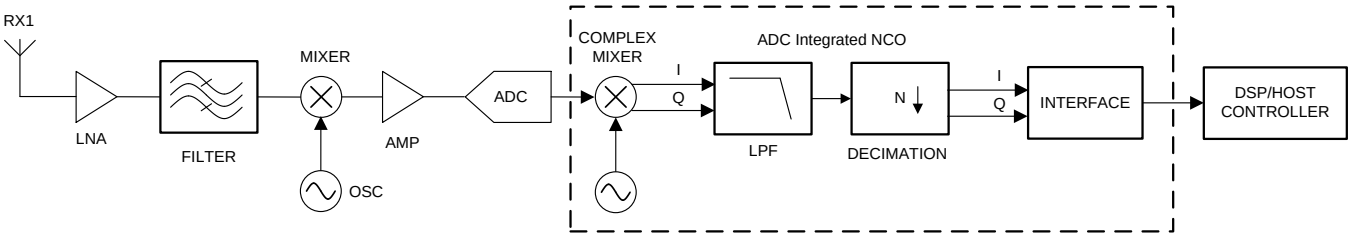
Figure 2. TIDA-010122 System Block Diagram



2.2 Design Considerations

In traditional RF front end architecture, at the receiver the high-frequency radio wave from the antenna are down-converted to intermediate (IF) or baseband frequency using a mixer and local oscillator (LO) and this baseband signal further down converted to lower data rate with optional stages then digitized using baseband or low-speed data converter and transmitter to DSP or FPGA for further processing. This is called traditional IF sampling, Figure 3 shows the block diagram of traditional IF sampling architecture.

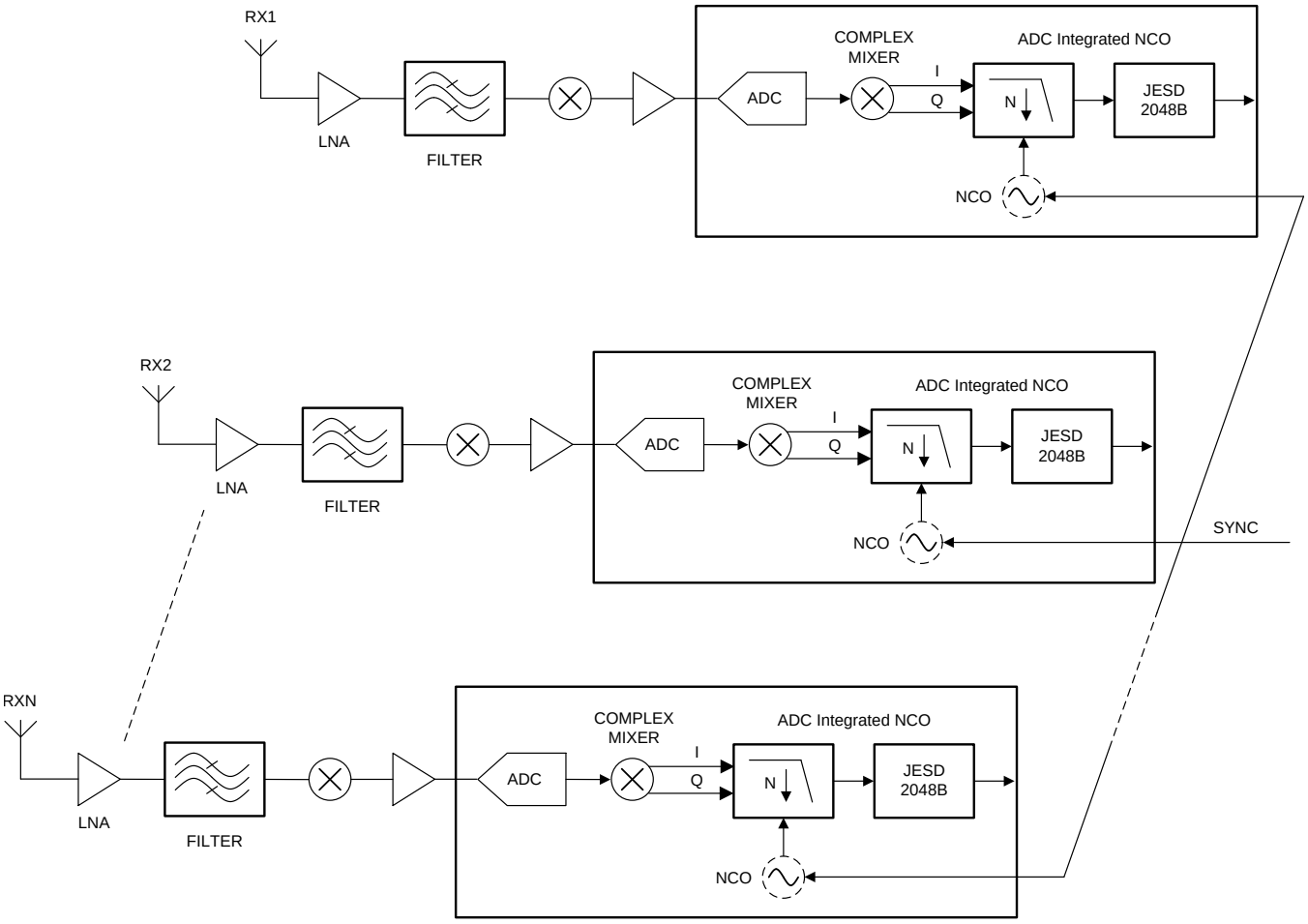
Figure 3. Generic RF Receiver Signal Chain



2.2.1 Design Challenges

The number of channel counts are increasing to improve system performance like receiver bandwidth, sensitivity and channel capacity in wireless networks that use massive MIMO architecture and similar applications such as phase array RADARs get the phase information across multiple receivers to identify targets in cluttered environments with better resolution. Figure 4 shows a typical multi-channel RF receiver signal chain block diagram.

Figure 4. Typical Multi-Channel RF Receiver Signal Chain



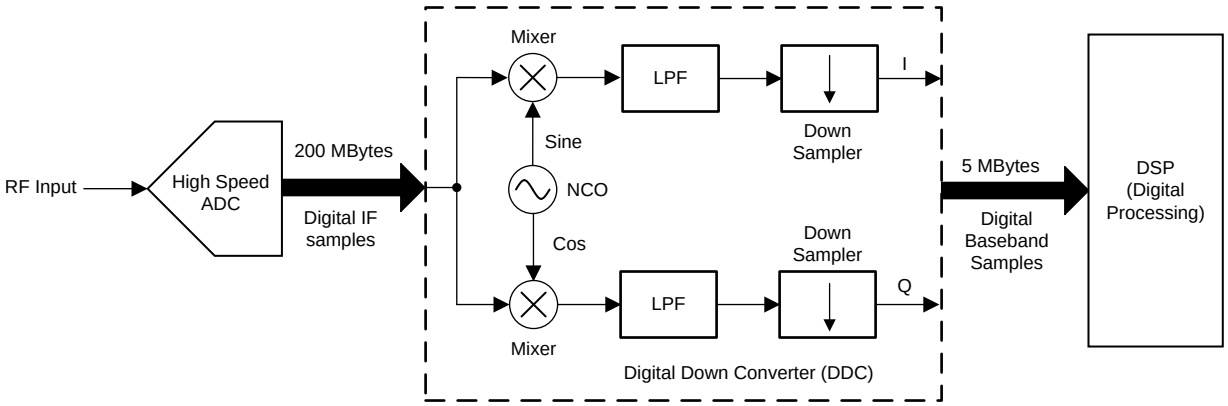
However, in multi-chip synchronization in sampled systems, it is crucial that samples from multiple receivers are aligned exactly with each other. Even a single clock cycle misalignment cannot be tolerated. Synchronization of multiple receivers requires timing calibration, careful routing, and a detailed timing analysis to ensure that the propagation delay across different analog-to-digital converters (ADCs) does not result in channel-to-channel skew that is greater than one clock cycle.

Considering RF signals lying in the frequency range from 300 MHz to 12 GHz supports UHF (300–1000 MHz), L band (1–2 GHz), S band (2–4 GHz), C band (4–8 GHz) and X band (8–12 GHz). In radio systems, receivers typically have high-speed ADC to digitize the band-limited RF or IF signals and these are very high data rates; but in many cases the signal interest is a very small bandwidth; typically in the MHz range and requires a large filter to extract the information.

Digital down conversion (DDC) is a fundamental block in many communication systems which allows the frequency of interest to move down to the spectrum. Therefore, the sample rate, filter requirements and further digital processing complexities are greatly reduced.

Figure 5 shows the overview of DDC in RF systems

Figure 5. DDC Functional Block



Due to applications needs, digital down conversions are done at the RF front end (analog domain) or after digitization in FPGA or DSP processors (digital domain), or a combination of both approaches. These digital features are built into new RF ADCs which further reduces system complexity, software flexibility to choose decimation, NCO frequency, and footprint.

However, overall system synchronization can be achieved with entire signal chains like RF front end, data converter, mixer and NCO which are aligned with the system clock.

This reference design focuses on how to achieve system synchronization in the ADC12DJ3200 JESD204B-based RF ADC and how on chip NCO features allow multi-device synchronization across data converters to achieve deterministic latency.

Furthermore, this reference design addresses critical design challenges to generate precise, low jitter, fast clocking solutions to clock multiple high-speed data converter, mixers, and high-speed FPGA logic devices.

2.3 Circuit Design

This reference design is developed based on the TIDA-01022 hardware platform and its internal circuits satisfy the requirements of JESD204B synchronization standards to achieve deterministic latency.

2.3.1 Multi-Chip Synchronization Requirements - JESD204B Subclass1

The following basic requirements must be met to achieve data convertor synchronization in JESD204B subclass1 based systems:

1. Phase-aligned device clocks for each data converter
2. Meet SYSREF setup *and* hold time requirements relative to the device clock
3. Choose appropriate elastic buffer release point at the receiver to ensure deterministic latency

4. Meet SYNC~ signal timing requirements in time-critical application

2.3.2 Multi-Channel Giga-Sample Clocking

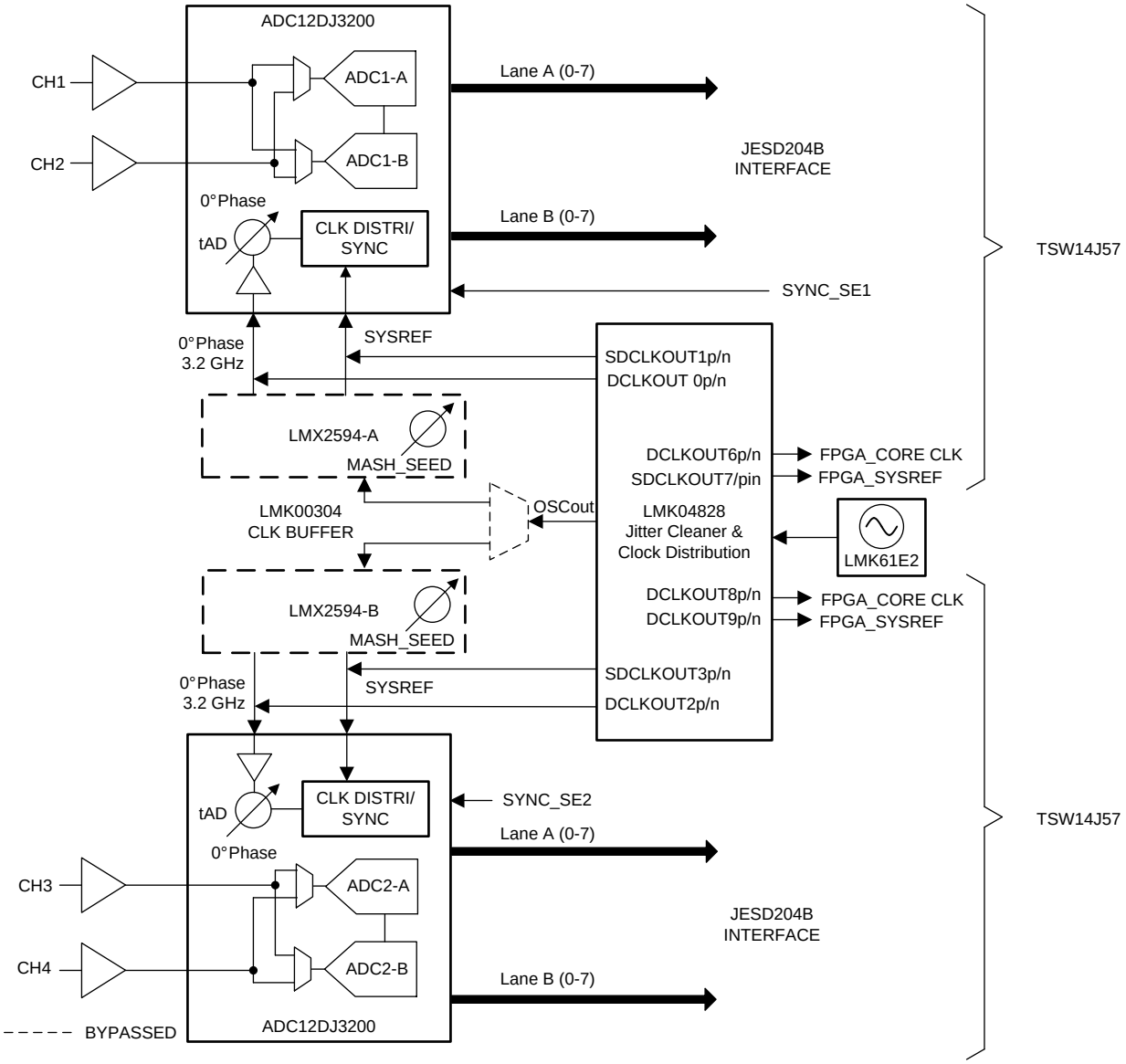
The TIDA-01022 hardware has a flexible clocking platform which helps designers validate system performance with various clocking source options. The default onboard clocking solution uses the LMX2594 clock synthesizer which has excellent phase noise at high frequency. A clock distribution chip called the LMK04828 is used to provide the reference signal to the LMX2594 device, FPGA DCLK, FPGA_CORECLK, and FPGA_SYSREF.

The clocking devices LMK4828, LMX2594, and ADC12DJ3200 are fully compliant with JESD204B subclass 1 requirements.

2.3.2.1 Clock Tree Selection - ADC Clock, SYSREF, and FPGA Clock

Figure 6 shows the clock architecture of the TIDA-010122, the ADC and FPGA clock are generated based on application requirements.

Figure 6. TIDA-010122 Clock Architecture



In this reference design ADC12DJ3200 operated in decimation mode (JMODE15 and JMODE16).

The ADC_SYSREF, FPGA_CORECLK, FPGA_REFCLK and FPGA_SYSREF to be calculated based the ADC device clock (ADC_DEVCLK) requirement and SERDES lanes used for capture.

The system performance like channel to channel skew, SNR, SFDR performance validated with following test condition,.

ADC_DEVCLK = 1480 MHz;

ADC_SYSREF = 18.5 MHz

FPGA_CORECLK = 185 MHz

FPGA_REFCLK = 185 MHz

FPGA_SYSREF = 18.5 MHz

SERDES lane rate = 8

The LMK04828 is used to generate ADC device clock, SYSREF and also provides the required FPGA clocks. Table 2 shows the signal definitions and clock output frequency.

Table 2. LMK04828 Clock Definition for TIDA-010122

Slno	LMK04828 SIGNALS	FREQUENCY OUTPUT	REMARKS
1	OSCout p/n	-	Connected to LMX2594 reference input for generation ADC DEVCLK and SYSREF
2	DCLKOUT0 p/n	1480 MHz	Connected to ADC-1 device clock input
3	SDCLKOUT1 p/n	18.5 MHz	Connected to ADC-1 SYSREF input
4	DCLKOUT2 p/n	1480 MHz	Connected to ADC-2 device clock input
5	SDCLKOUT3 p/n	18.5 MHz	Connected to ADC-2 SYSREF input
6	DCLKOUT4 p/n	185 MHz	FPGA_REF CLK, connected slave to capture FPGA
7	SDCLKOUT5 p/n	-	SYNC signal to LMX2594-B
8	DCLKOUT6 p/n	185 MHz	FPGA_CORE CLK, connected slave to capture FPGA
9	SDCLKOUT7 p/n	18.5 MHz	FPGA_SYSREF, connected slave to capture FPGA
10	DCLKOUT8 p/n	185 MHz	FPGA_CORE CLK, connected master to capture FPGA
11	SDCLKOUT9 p/n	18.5 MHz	FPGA_SYSREF, connected master to capture FPGA
12	DCLKOUT10 p/n	185 MHz	FPGA_REF CLK, connected master to capture FPGA
13	SDCLKOUT11 p/n	-	SYNC signal to LMX2594-A
14	DCLKOUT12 p/n	-	Not used
15	SDCLKOUT13 p/n	-	Not used

Once all the clocks are generated, establish NCO synchronization with the following procedure:

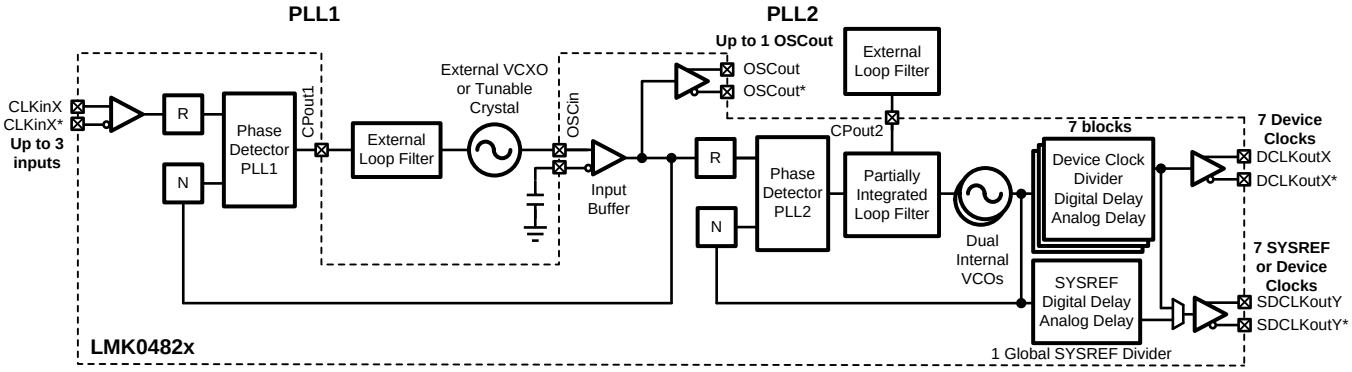
- The TICSPro GUI helps to create the configuration files for the LMK61E2, LMK04828, and LMX2594 devices.
- Download the latest TICSPro GUI software at: http://www.ti.com/tool/TICSPRO-SW

2.3.3 Clock Phase Alignment

The TIDA-01022 hardware has a flexible clocking solution with a number of clocking options to allow users to validate system performance with various clocking configurations. In this reference design, one clocking option is chosen which satisfies design clocking requirements. This clocking solution provides flexibility to adjust clock delay in two places in the clocking path. This delay can be done on the LMK04828 output, the ADC12DJ3200 device, or a combination of these devices.

The LMK04828 device has both analog and digital delay elements in each clock output. Figure 7 shows highlights of the delay elements in the LMK04828 device.

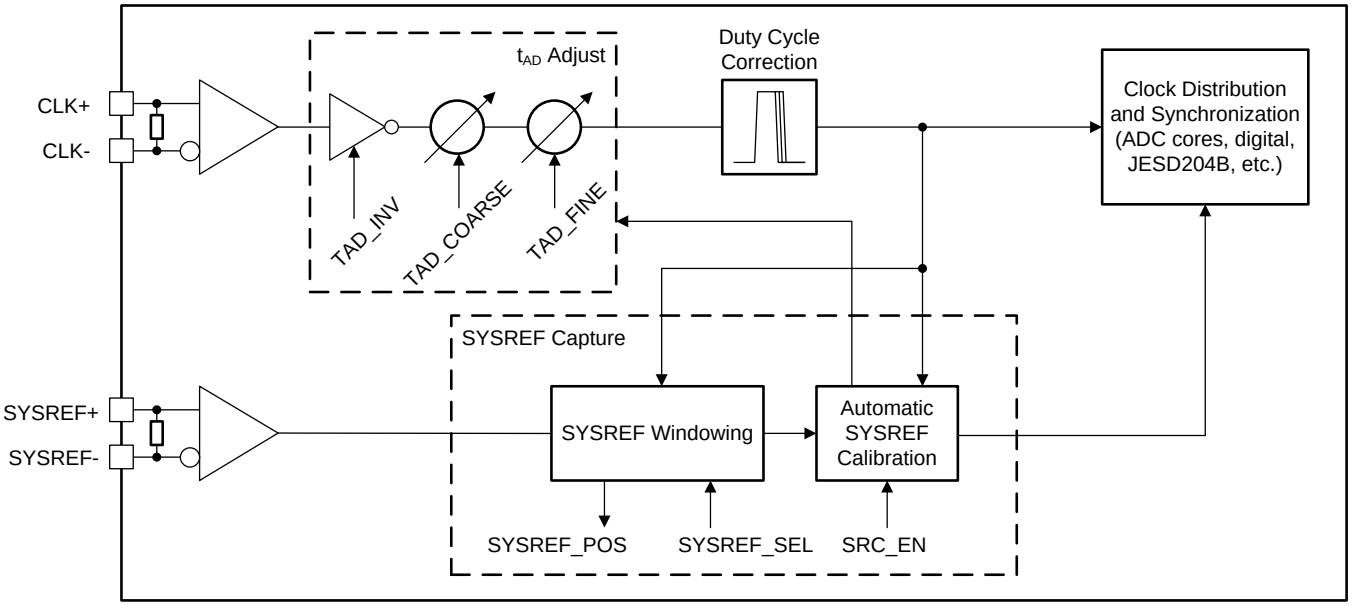
Figure 7. LMK04828 Simplified Block Diagram



The ADC12DJ3200 has t_{AD} adjust features on the device clock path that can be used to shift the sampling instant in 19-fs steps.

Figure 8 shows the internal clock subsystem of the ADC12DJ3200 and highlights t_{AD} components (TAD_INV, TAD_COARSE, and TAD_FINE). These registers allow maximum aperture delay adjustment up to $t_{AD(max)}$ = 293 ps and ultra-low aperture jitter, $t_{AJ(max)}$ = 70 fs, to satisfy the low phase noise requirements.

Figure 8. ADC12DJ3200 Clocking Subsystem



This t_{AD} feature gives the flexibility to adjust t_{AD} registers to align the sampling instants across multiple ADCs with 19-fs resolution.

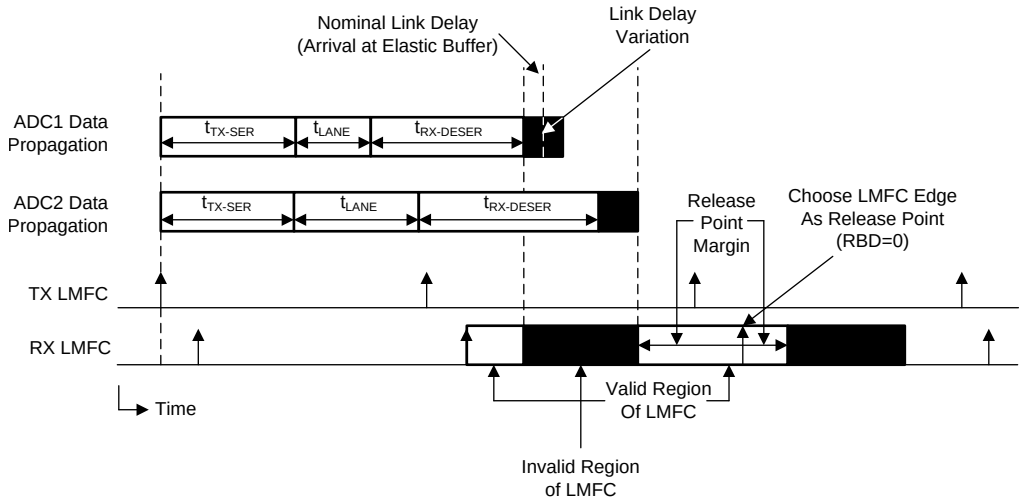
After SYSREF calibration, the calibrated SYSREF values are loaded to the corresponding t_{AD} register:

1. Enable SYSREF calibration and check for SYSREF calibration done bit in 0x2B4 register
2. Load the SYSREF calibrated values of coarse (0x2B6) and fine(0x2B5) register with corresponding t_{AD} registers 0x2B3,0x2B2 after SYREF calibration is done.
3. Disable SYSREF calibration
4. Fine tune t_{AD} register for 0 deg phase delay between ADC1 and ADC2

2.3.4 Choose Proper Elastic Buffer Release Point

Another important requirement is to choose the appropriate elastic buffer release point at the receiver. Each ADC signal chain may have different propagation delay. Figure 9 shows how to define the valid region of LMFC for the elastic buffer release point. Here, two ADCs in the receiver signal chain and the second ADC has a longer routing distance and results in a longer link delay. All the receiver link delays should be same, only then can deterministic latency across ADCs be achieved.

Figure 9. Elastic Buffer for LMFC



Determine the invalid region of LMFC period, then set the release buffer delay (RBD) parameter to shift the release point with number of frame clock from the LMFC edge so it occur within valid LMFC cycle.

2.3.5 SYNC~ Signal Timing Requirement

Digital features like digital up converters (DUCs) in DACs and digital down converters (DDCs) in ADCs greatly reduce system interface speeds for higher sample rates. These DUCs and DDCs uses numerically-controlled oscillators (NCOs) in the systems and these NCOs must be synchronized in all converters to achieve overall system synchronization.

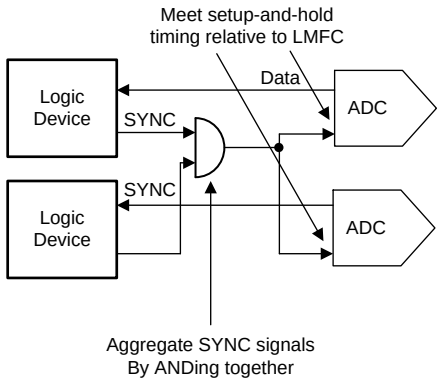
The most common approach is to synchronize the NCOs by using the LMFC rising edge and elastic-buffer release point. In ADCs, the NCOs can be synchronized using the first LMFC edge that occurs after the SYNC signal is de-asserted, which corresponds to the start of the initial lane alignment sequence (ILAS) transmission. In DACs, the typical approach is to synchronize the NCOs when the elastic buffer is released.

There is a timing requirement on the SYNC~ signal to achieve multi-device synchronization across multiple ADCs.

The SYNC~ signal must be de-asserted by all receivers (ADCs) on the same local multi-frame clock (LMFC) edge and received at the transmitter in the same LMFC cycle. This can be done by AND the SYNC signal from all receivers together, then distribute this aggregated signal to each transmitter (ADCs)

Figure 10 shows the SYNC~ signal implementation method for multiple ADCs.

Figure 10. Aggregate SYNC~ Generation for Multiple ADCs

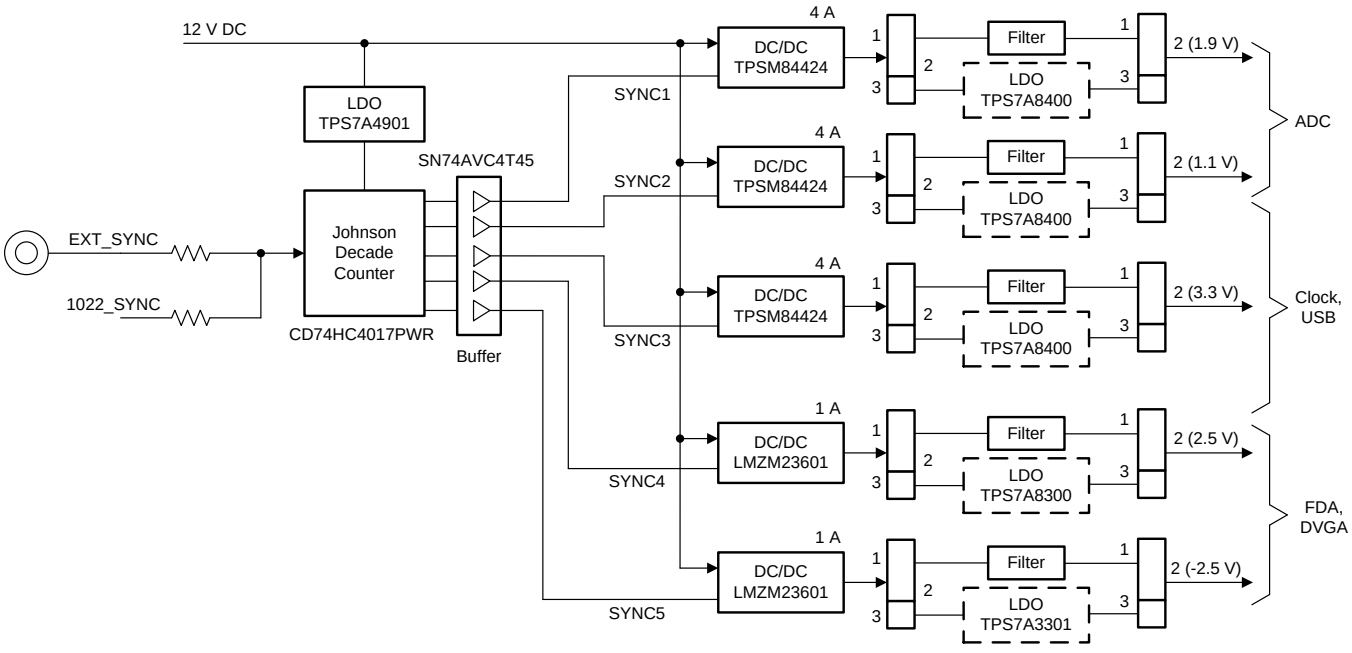


2.3.6 Power

This reference design uses a high-performance, optimized power solution from the TIDA-01027 reference design. This power module satisfies the power requirements of the TIDA-01022 design. The module contains both DC/DC and LDO regulators with an external frequency SYNC feature for synchronization of multiple switching regulators. Also a method of clock phase-shifting enables users to reduce both conducted and radiated EMI.

Figure 11 shows the TIDA-1027 power tree. The module provides 3.3-V, 1.9-V, 1.1-V, 2.5-V, and –2.5-V rails to various analog and digital sections of the TIDA-01022 reference design.

Figure 11. TIDA-01027 Power Tree



For more information, see the Low noise power-supply reference design maximizing performance in 12.8 GSPS data acquisition systems reference design (TIDA-01027).

2.4 Highlighted Products

2.4.1 ADC12DJ3200: 12-bit, Dual 3.2-GSPS or Single 6.4-GSPS RF Sampling ADC

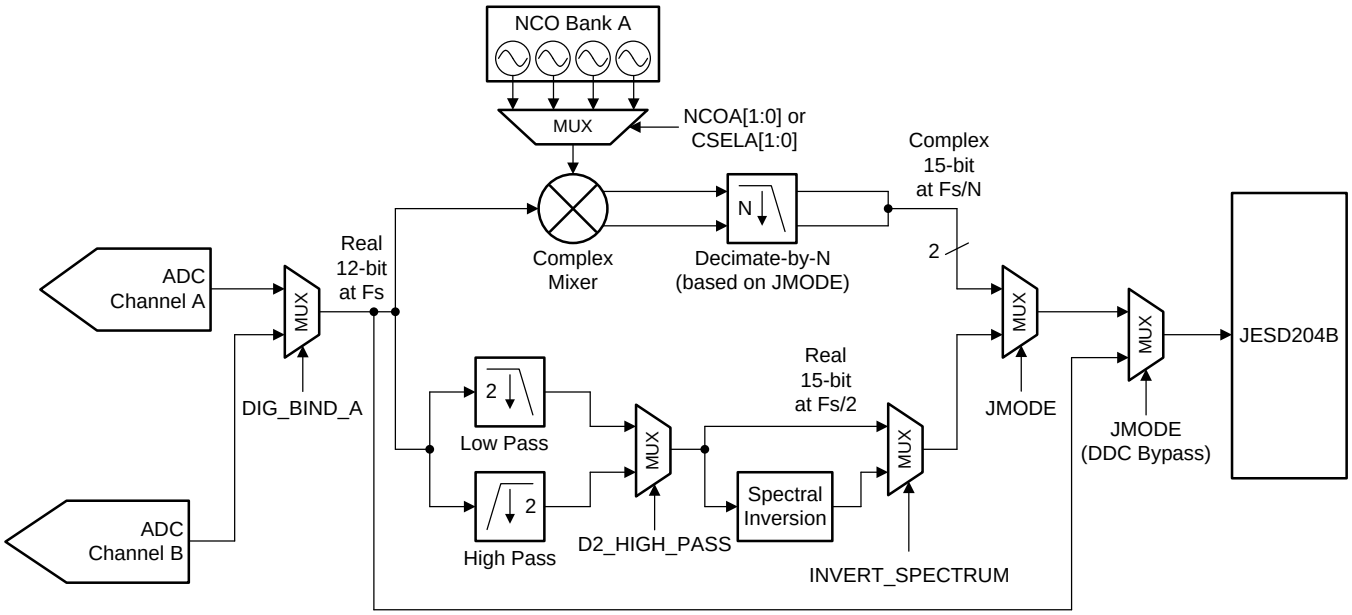
The ADC12DJ3200 device is an RF-sampling giga-sample ADC that can directly sample input frequencies from DC to above 10 GHz. In dual-channel mode, it can sample up to 3200-MSPS and in single channel mode up to 6400-MSPS, full power input bandwidth (–3 dB) of 8.0 GHz, with usable frequencies exceeding the –3-dB point in both dual- and single-channel modes, allows direct RF sampling of the L band, S-band, C-band, and X-band for frequency agile systems.

2.4.1.1 Why Choose the ADC12DJ3200? Key Features

This device offers digital features like digital down conversion (decimation factor 2 ×, 4 ×, 8 ×, and 16 ×), four 32-bit numerical controlled oscillators per DDC and complex mixer. The ADC12DJ3200 on-chip NCO synchronization feature allows NCO synchronization across multiple ADCs using SYSREF or the SYNC~ signal.

Figure 12 shows the DDC block diagram of the ADC12DJ3200 device.

Figure 12. ADC12DJ3200 Internal DDC Block Diagram



Automatic SYSREF calibration, uses the t_{AD} Adjust feature to shift the device clock to maximize the SYSREF setup and hold times or align the sampling instance based on the SYSREF rising edge.

SYSREF position detector and sampling position selection (SYSREF windowing): The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK± rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK±, to maximize setup and hold timing margins.

In addition to these features, this device family offers various sampling rates starting from 1600 MHz to 5200 MHz and 8 to 12 bits of resolution with the same pinout. It allows customers the flexibility to change the data converter speed and resolution based on their applications with the same printed-circuit board (PCB). Also, there is no need for much hardware and software development. Table 3 lists other similar devices which may be considered.

Table 3. ADC12DJ3200 - Similar Devices

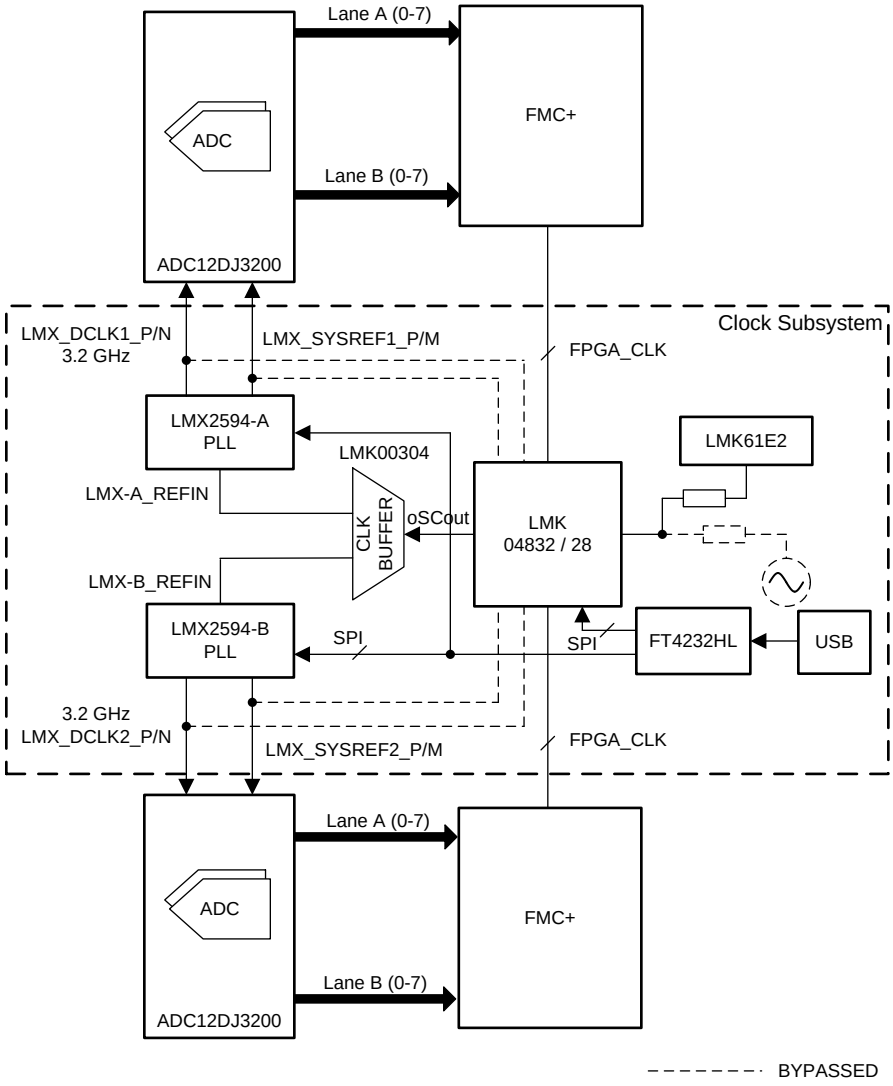
	ADC08DJ3200	ADC12DJ3200	ADC12DJ2700	ADC12J2700	ADC12J1600	ADC12J4000
	Order now	Order now	Order now	Order now	Order now	Order now
	Online datasheet	Online datasheet	Online datasheet	Online datasheet	Online datasheet	Online datasheet
	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet
	Tools & Software	Tools & Software	Tools & Software	Tools & Software	Tools & Software	Tools & Software
Sample rate (Max) (MSPS)	3200	3200	2700	2700	1600	4000
	6400	6400	5400			
Resolution (bits)	8	12	12	12	12	12
Number of input channels	2	2	2	1	1	1
	1	1	1			
Interface	JESD204B	JESD204B	JESD204B	JESD204B	JESD204B	JESD204B
Analog input BW (MHz)	8000	8000	8000	3300	3300	3300
Features	Ultra High Speed	Ultra High Speed	Ultra High Speed	Ultra High Speed	Ultra High Speed	Ultra High Speed
Rating	Catalog	Catalog	Catalog	Catalog	Catalog	Catalog
Input range (Vp-p)	0.8	0.8	0.8	0.725	0.725	0.725
Approx. price (US$)	896.50 | 100u	1919.50 | 100u	1619.50 | 100u	1024.80 | 100u	658.20 | 100u	1949.00 | 100u
Power consumption (Typ) (mW)	2800	3000	2700	1800	1600	2000
Architecture	Folding Interpolating	Folding Interpolating	Folding Interpolating	Folding Interpolating	Folding Interpolating	Folding Interpolating
SNR (dB)	49.1	56.6	56.7	55	55	55
ENOB (Bits)	7.8	9	9	8.8	8.8	8.8
SFDR (dB)	67	67	71	71	70	71
	62					
Operating temperature range (°C)	–40 to 85	–40 to 85	–40 to 85	–40 to 85	–40 to 85	–40 to 85

2.4.2 LMK04828: Ultra-Low Noise JESD204B Compliant Clock Jitter Cleaner

The LMK0482x family is the highest performance clock conditioner with JESD204B support in the industry. The 14 outputs from PLL2 can drive up to seven JESD204B data convertors or other logic devices like FPGA. The device has both analog and digital delay in each clock output path and the analog delay can be adjusted 25-ps fine steps.

Figure 13 shows by combining both LMK04828 and LMX2594; high-performance, low-noise clocking subsystems are created that drive giga-sample speed data converters with JESD204B support.

Figure 13. Giga Sample Clocking Solution With LMX2594 + LMK04828



2.4.3 LMX2594; 15-GHz Wideband PLLatinum™ RF Synthesizer

The LMX2594 device is a high-performance, wideband PLL with integrated VCOs that can generate frequencies from 10 MHz to 15 GHz without using an internal doubler. The high-performance PLL with a figure of merit of –236 dBc/Hz and high-phase detector frequency can attain very low in-band noise and integrated jitter.

The LMK2594 device is an ideal companion part for the ADC12DJxx00 family. The LMK2594 generates a very low noise clock for high-speed data convertor and generates repeating SYSREF which is compliant with the JESD204B standard.

2.4.4 LMK61E2: Ultra-Low Jitter, Fully-Programmable Oscillator

The LMK61E2 device is an ultra-low jitter PLLatinum™ programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly-used reference clocks. The outputs can be configured as LVPECL, LVDS, or HCSL. The device offers ultra-low jitter, as low as 90-fs RMS and the maximum clock output can generate up to 1 GHz with 50 ppm frequency stability. In this reference design, the LMK61E2 is used to provide a reference clock for the LMK04828.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The following hardware components are required to perform the test:

1. 1 × TIDA-01022 hardware
2. 2 × TSW14J57EVM
3. 1 × USB2ANY programmer
4. 1 × Splitter
5. 1 × Variable band pass filter
6. 1 × 6-GHz signal generator
7. 2 × Laptop or desktop PC (Windows 10 OS installed)
8. 1 × 12 V 4 A DC adapter or Lab power supply

3.1.2 TIDA-01022 Hardware Functional Block

Figure 14 shows the TIDA-01022 board with the TIDA-01027 power board. For more information about hardware functional blocks and programming details, see TIDA-01022.

Figure 14. TIDA-01022 Hardware Functional Block

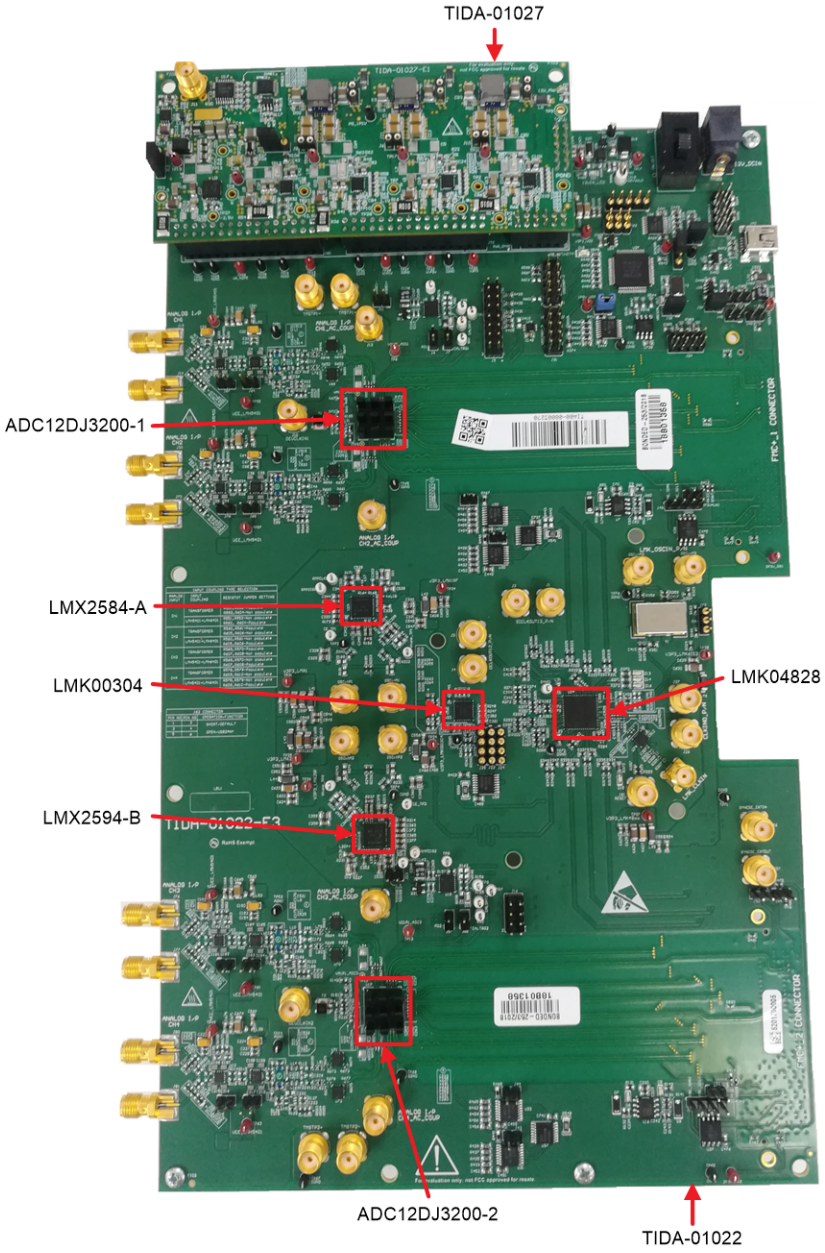


Figure 15 shows the TIDA-01027 board image, in this reference design the TIDA-01027 board is configured as DC/DC free running mode (default mode). The TIDA-01027 output connectors are made compatible with the TIDA-01022 power input headers J58, J59, J60, and J63.

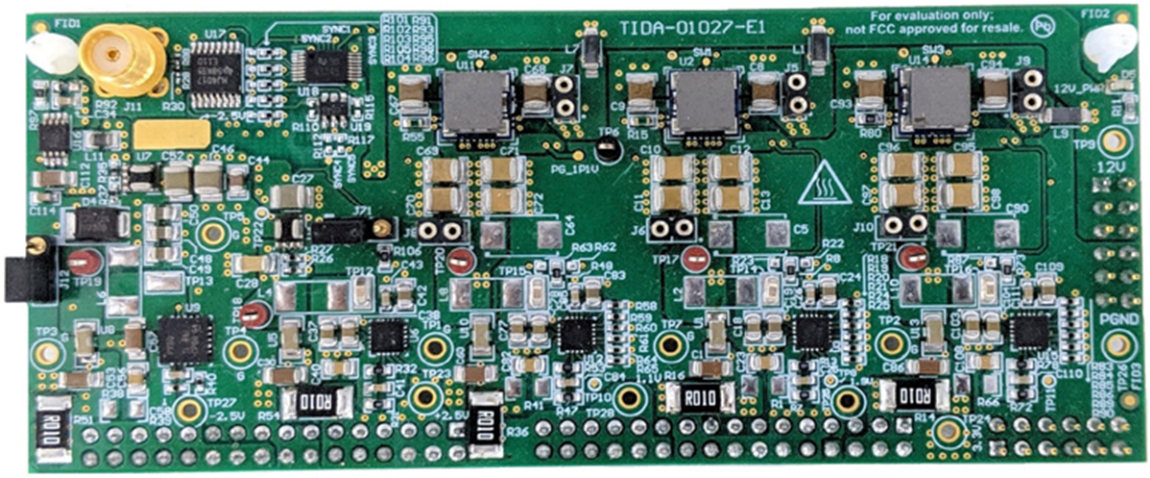
Table 4 shows the input and output specification of the TIDA-01027 power supply module.

Table 4. TIDA-01027 Key Specification

PARAMETER	SPECIFICATION
Input voltage range	5 V to 17 V
Number of outputs	5
Output voltage, maximum output current	1.9 V, 4 A 1.1 V, 4 A 3.3 V, 4 A 2.5 V, 1 A –2.5 V, 800 mA
Efficiency	85%

The board can be connected as Figure 14 shows.

Figure 15. TIDA-01027 Hardware Image



3.1.3 Software

The TIDA-01022 board requires three application software GUIs for validation: HSDC TID GUI, HSDC Pro GUI, and the LMK61xx oscillator programming tool.

1. Use the HSDC TID GUI to configure the data converter (ADC12DJ3200), clocking devices (LMK4828, LMX2594, and LMK61E2), and digital VGA (LMH6401). Use the low-level page to program the device with the respective configuration file. Download the latest HSDC TID GUI software from: http://www.ti.com/lit/zip/tidcfb3
2. Use the HSDC Pro GUI to capture the digitized data with the assistance of a TSW14J57 capture card and provide a spectrum and time-domain plot. Download the latest HSDC Pro GUI software at: http://www.ti.com/tool/dataconverterpro-sw
3. Use the LMK61xx Oscillator Programming Tool to program the LMK61E2 device. Download the latest LMK61xx software at: http://www.ti.com/lit/zip/snac074

3.1.3.1 Getting Started Application GUI

Figure 16, Figure 17, and Figure 18 show screen shots of starting the HSDC TID GUI configuration and the *Programming* tab for the low-level view, respectively.

Figure 16. HSDC TID GUI – Top-Level Navigation View

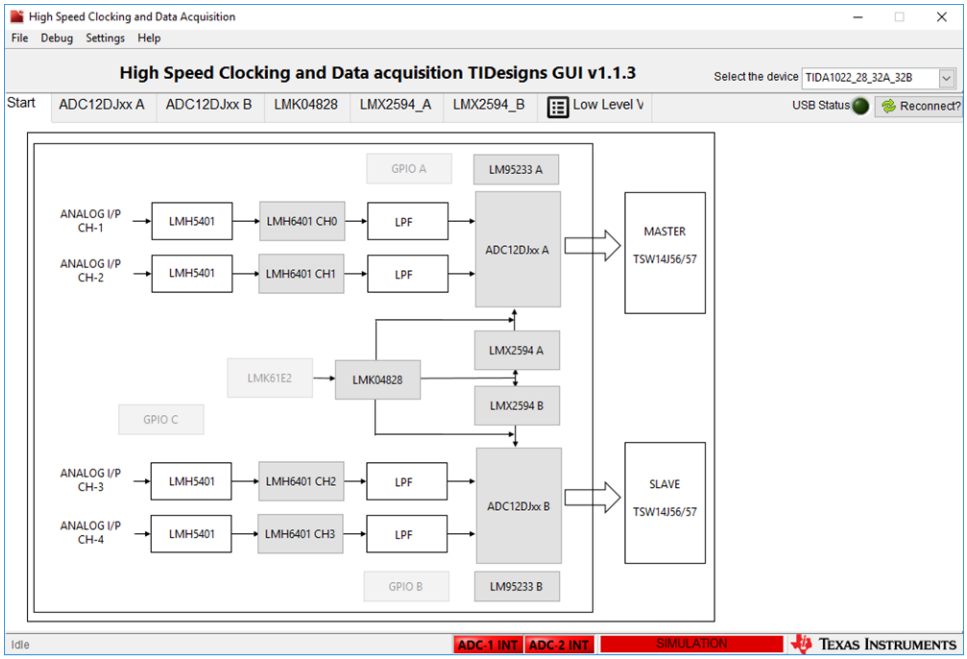


Figure 17. HSDC TID GUI – Low-Level Programming View

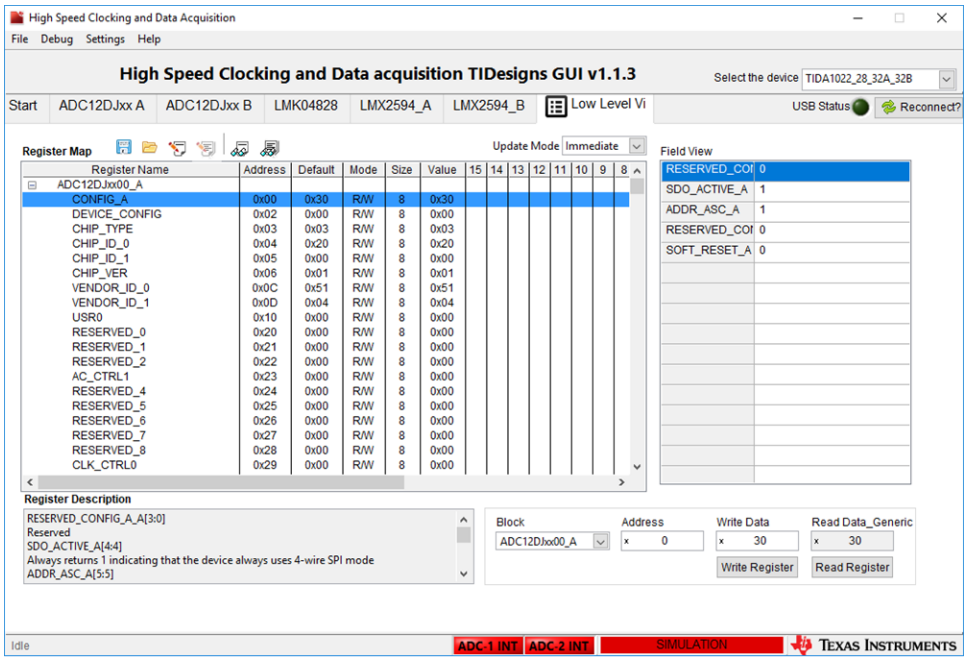


Figure 18. HSDC TID GUI - NCO Programming, Alarm Monitor View

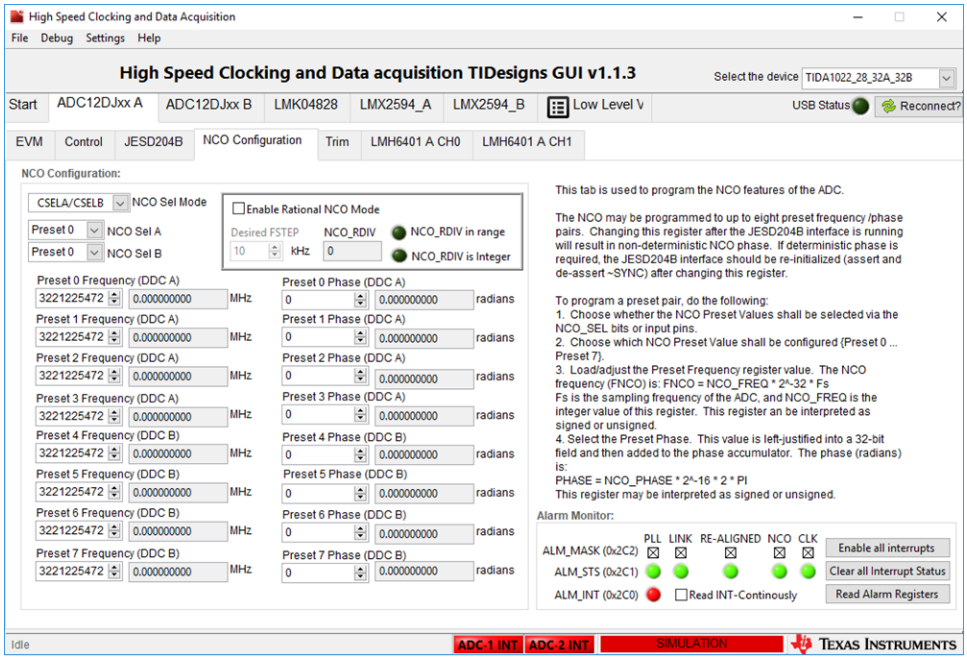
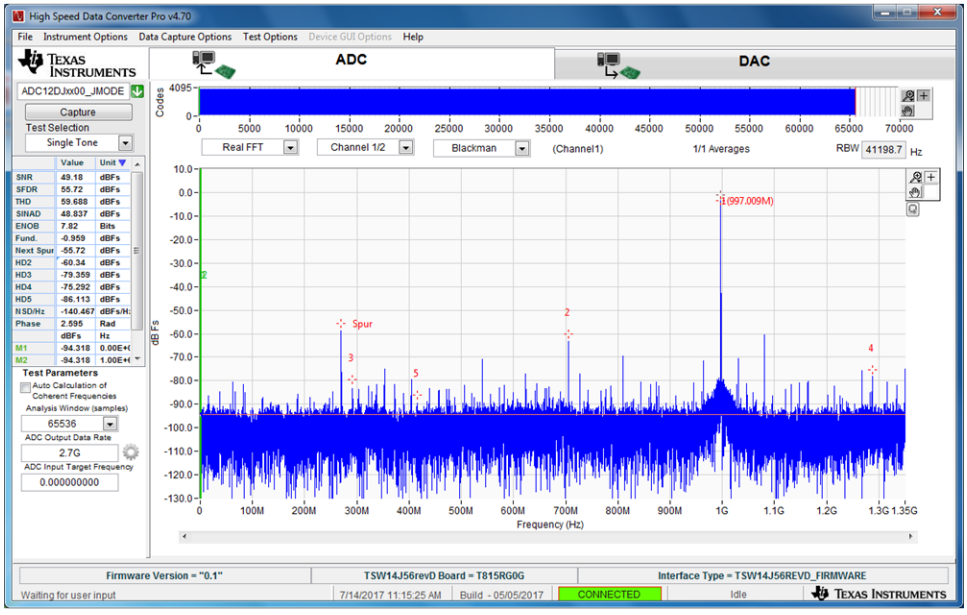


Figure 19 shows the ADC capture screen in HSDC Pro GUI

Figure 19. HSDC Pro ADC Capture GUI (Spectrum)



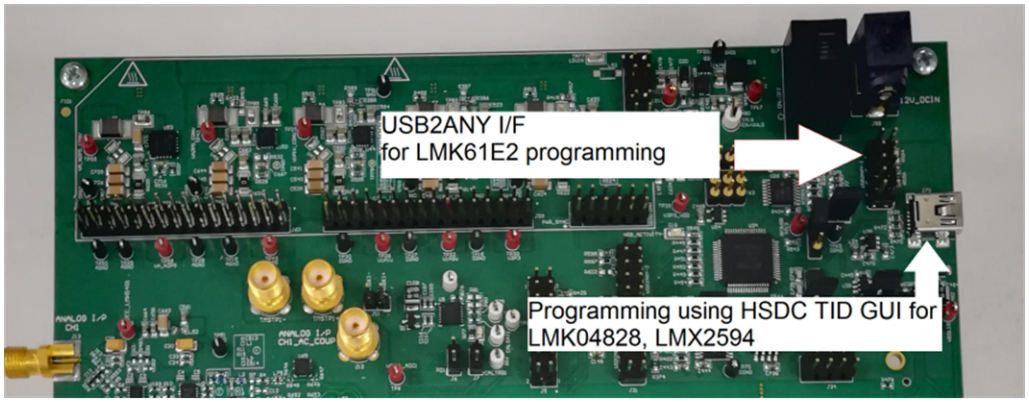
3.1.3.1.1 Hardware Programming

The TIDA-01022 hardware has an onboard FTDI-brand USB controller which is for programming the LMK61E2, LMK4828, and LMX2594 clocking devices and the LMH6401 amplifier using an SPI or I2C interface. The High-Speed Data Converter (HSDC TID) graphical user interface (GUI) supports low-level pages, which can be used to program these devices.

The board also features a USB2ANY programming interface which helps the user to evaluate hardware by using the respective evaluation module (EVM) GUI.

Figure 20 shows the location of programming connector

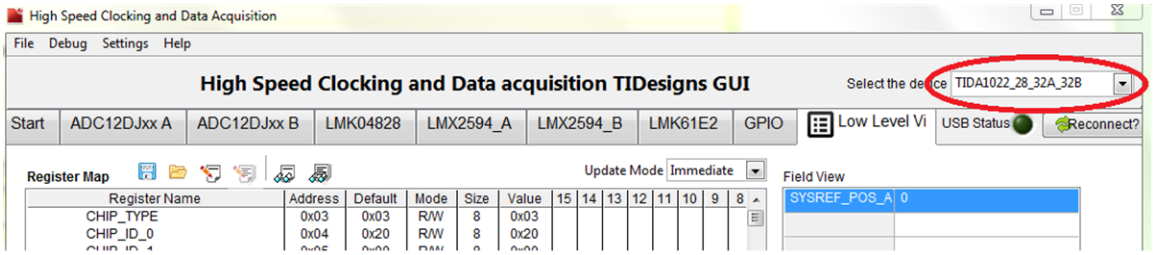
Figure 20. Programming Connector Interface



The programming procedure for the built-in programming interface follows:

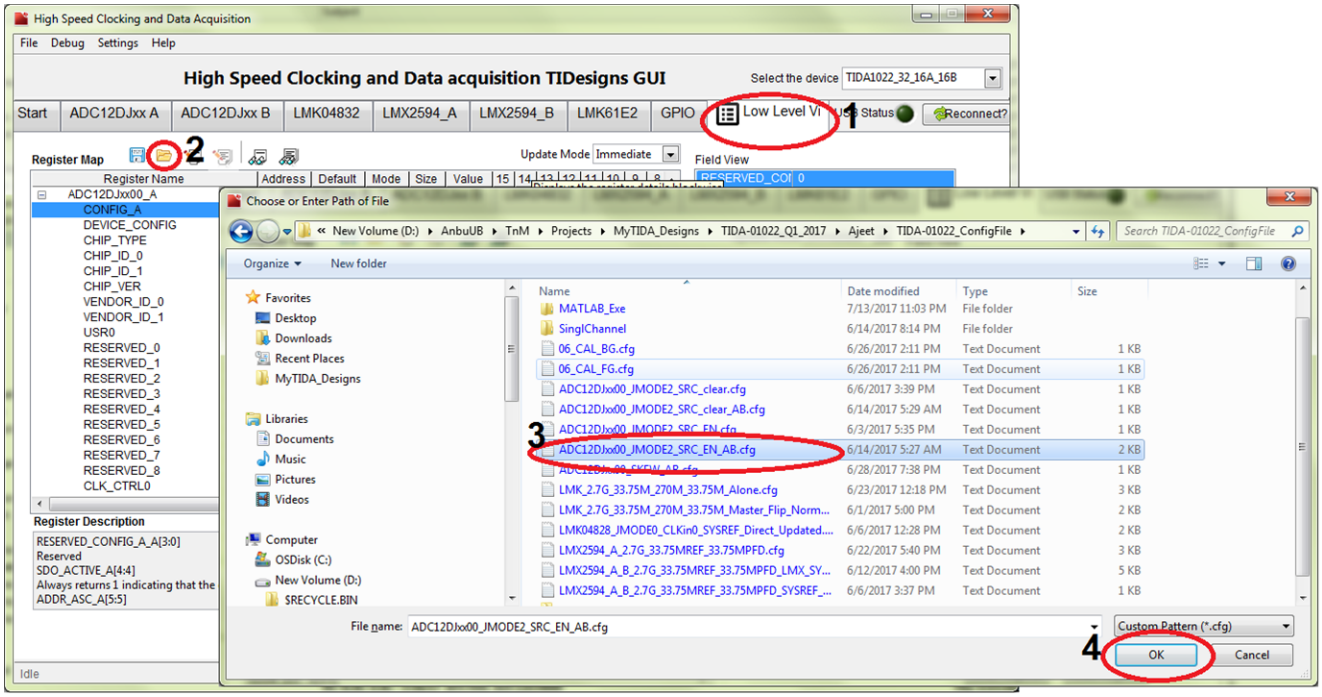
1. Open the HSDC TID GUI and select the “TIDA1022_28_32A_32B” from device selection drop-down menu.

Figure 21. Select a Device in the HSDC TID GUI



2. Navigate to the *Low Level* tab, select the configuration files to be programmed, and click the *OK* button. Follow these steps as numbered and encircled in the screen shot in Figure 22.

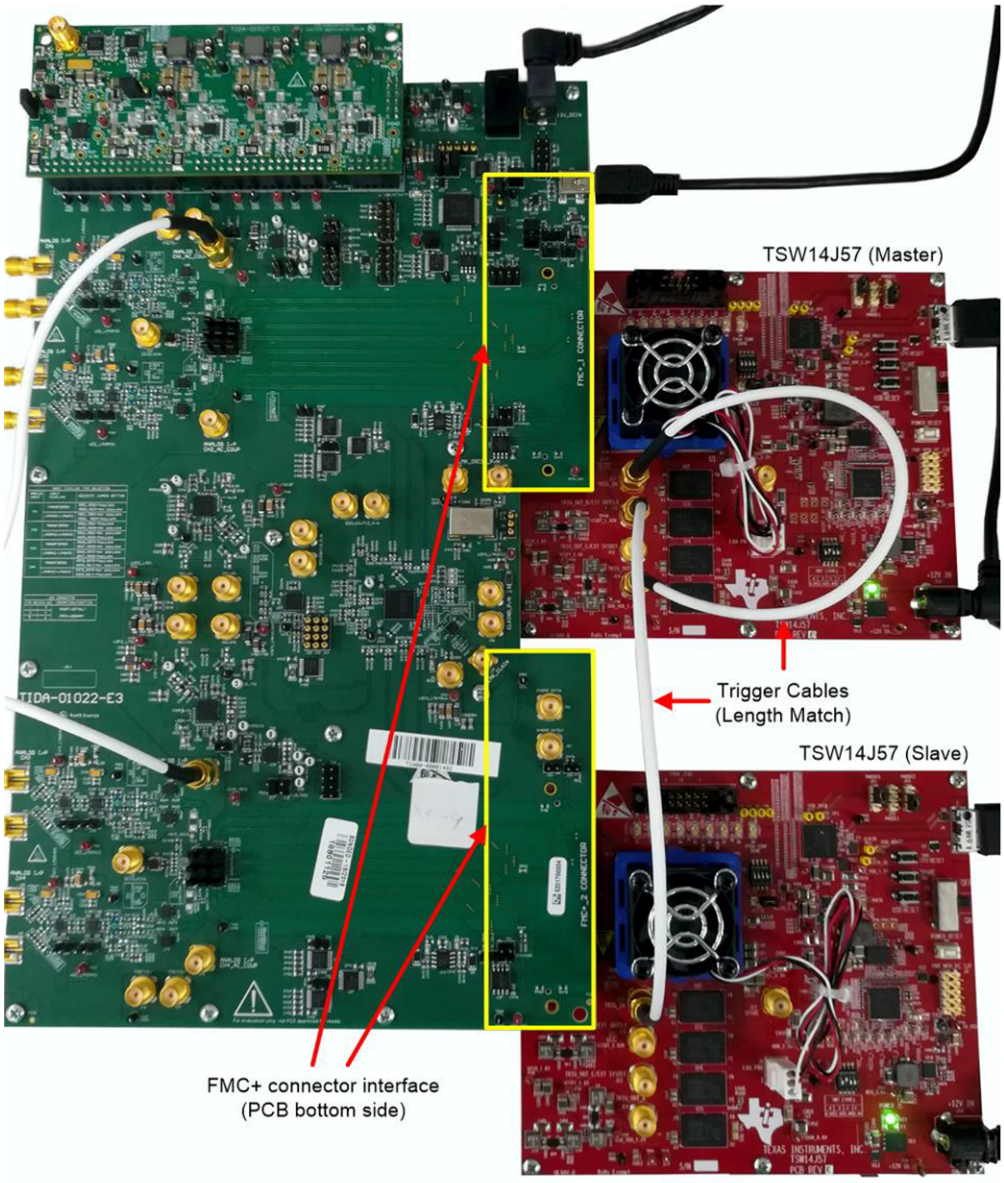
Figure 22. Selecting Configuration Files to be Programmed



3.1.3.2 Host Interface

The TIDA-010122 NCO synchronization can be evaluated using TI's TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card. Populated with an Intel® Arria® 10 device and using the Altera® JESD204B IP solution, the TSW14J57 device can be dynamically configured to support all lane speeds from 1.6 Gbps to 15 Gbps - from 1 to 16 lanes. Together with the accompanying High-Speed Data Converter Pro Graphic User Interface (GUI), it is a complete system that captures and evaluates data samples from the TIDA-01022 reference design. The TIDA-01022 can be directly interfaced with the TSW14J57 device using the FMC+ connector interface. Figure 23 shows the TIDA-01022 interface with the TSW14J57 capture module and trigger cable connection.

Figure 23. TIDA-01022 Interface With TSW14J57 Capture Card



For more information on the TSW14J57 EVM, see the TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card user's guide.

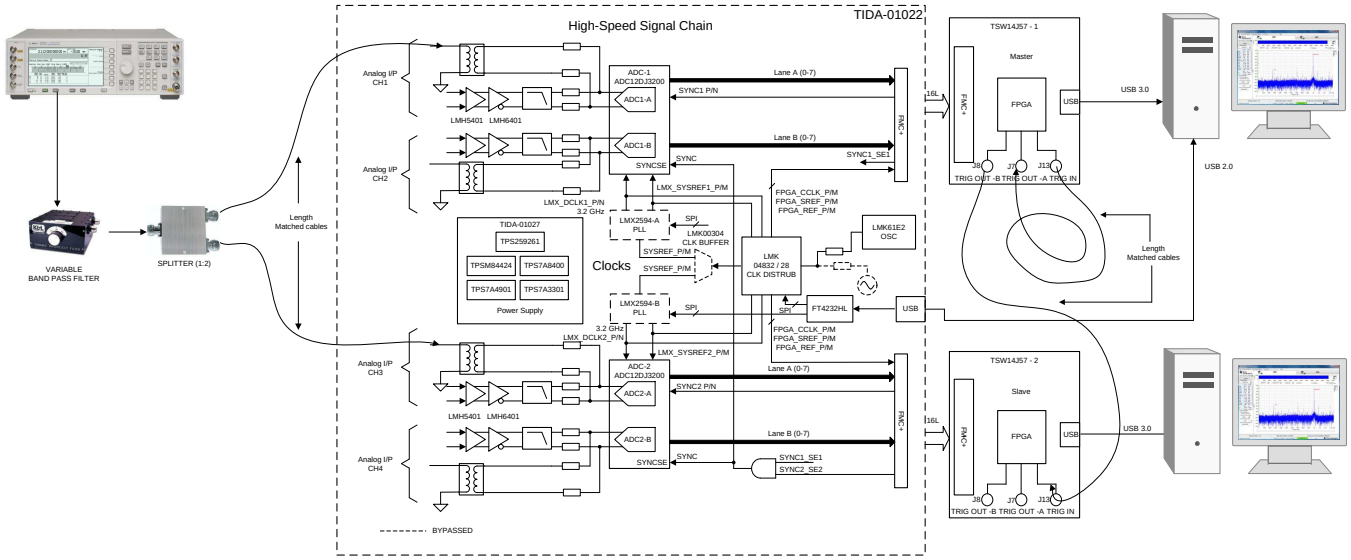
3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Hardware Setup

Figure 24 shows the test setup for NCO synchronization using the TIDA-01022 reference design with transformer input.

Figure 24. Test Setup for 2 × ADC12DJ3200 NCO Synchronization



3.2.1.1.1 SYNC~ Logic Implementation

Aggregated AND logic implemented in the TIDA-01022 hardware is discussed in Section 2.3.5. Figure 25 shows an implementation circuit diagram. Here the SYNC1_SE and SYNC2_SE signal is coming from TSW14J57 capture cards and by combining these signals using AND logic, the output of AND logic is connected to the SYNC signal input of both ADC1 and ADC2. Table 5 shows the resistor jumpers required to implement the SYNC~ signal based synchronization.

Figure 25. TIDA-010122 SYNC~ Implementation Circuit Diagram

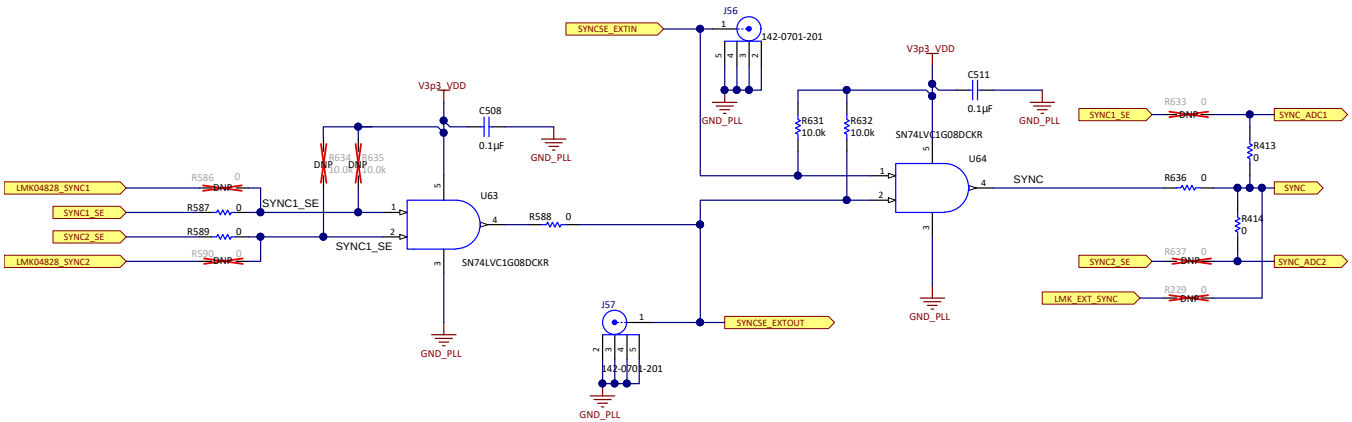
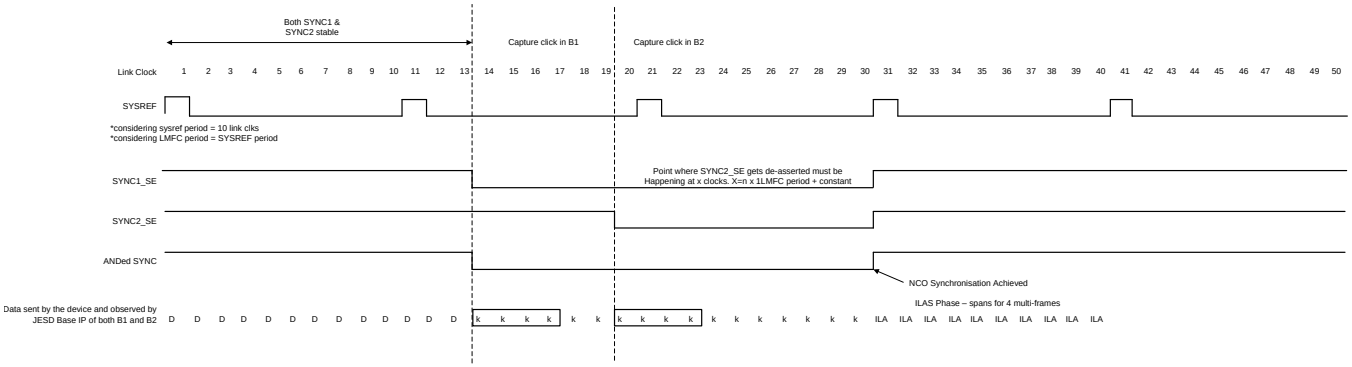


Table 5. SYNC Logic Resistor Jumper Selection

IMPLEMENTATION METHOD	DO NOT POPULATE	POPULATE
SYNC~	R634, R635, R586, R590, R633, R637, R229	R413, R414, R587, R589
SYSREF	R413, R414, R587, R589	R633, R637,

Figure 26 shows the SYNC signal timing diagram of two TSW14J57 capture cards interfaced with two ADC12DJ3200 devices.

Figure 26. SYNC Timing of 2 × ADC12DJ3200 With 2 × TSW14J57

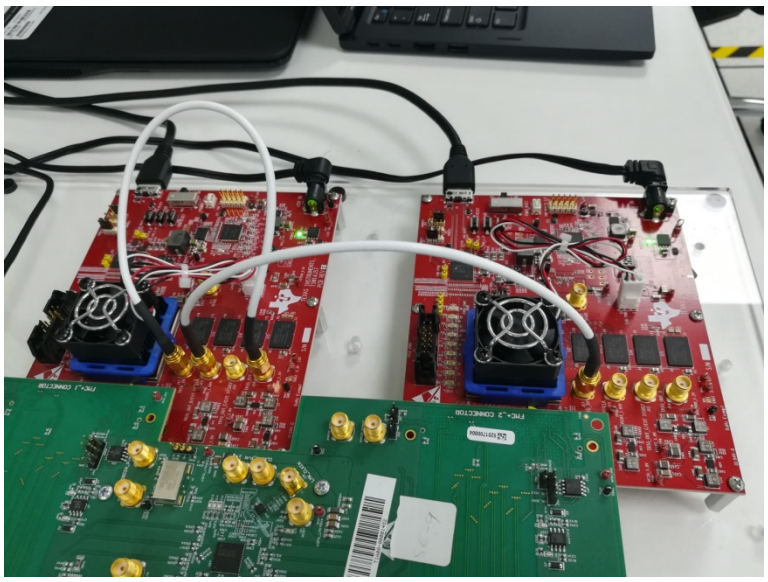


3.2.1.1.2 Master Slave Trigger Capture

The output data from the ADC is captured using the TSW14J57 capture card since the TIDA-01022 has 2 × ADC12DJ3200 devices, 2 × TSW14J57 devices are needed for capture. To enable synchronous capture, these two TSW14J57 devices can be configured as master and slave mode then enable the software trigger in the HSDC Pro GUI software.

- Figure 27 shows the TSW14J57 master slave trigger connection.
- Connect master TSW14J57, J7(TRIG OUT –A) to J13 (TRIG IN) using a high-speed SMA cable for master self-triggering
- Connect the master TSW14J57, J8 (TRIG OUT-B) to J13 (TRIG IN) of the slave TSW14J57 module using a high-speed SMA cable.

Figure 27. Master Slave Trigger Connection



NOTE: Figure 27 illustrates that the length of cable must be length matched.

3.2.2 Test Case

In this reference design, the NCO synchronization is performed with two channels (CH1 and CH3) and the same can be scaled up for high channel counts by using a similar approach.

3.2.2.1 Synchronization Performance in JMODE15

1. Emulate the hardware setup as shown inFigure 24, then provide the input signal to the J12 and J29 SMA connectors of channel 1 and 3 of the TIDA-01022 design through a variable bandpass filter and 2:1 splitter.
2. Connect a high-speed USB3.0 and USB2.0 cable to the capture PC's
3. Provide 12-V, 4-A DC supply to the power connector (J55) of the TIDA-01022 design and a 12-V supply to the TSW14J57 capture card.

Test condition

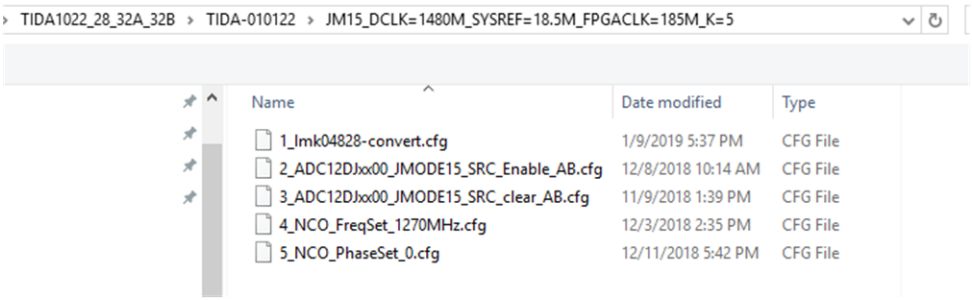
F_S = 1480 MHz
F_{IN} = 1250 MHz
F_{NCO} = 1270 MHz
Mode = JMODE15 (x16 Decimation) - 8 lanes

3.2.2.1.1 Test Procedure

Configure the following using the HSDC TID GUI:

1. Use the J32 connector to program the LMK61E2 device at 18.5 MHz using the USB2ANY programmer associated with the LMK61E2 oscillator programming tool. Set the device address as 0x5A before programming.
2. Load the following configuration file in the LMK04828 using HSDC TID GUI as Figure 28 shows. This generates 1480-MHz DEVCLK and SYSREF 18.5 MHz for both ADC1 and ADC2. This also generates the FPGA reference at 185 MHz, the FPGA core clock at 185 MHz, and the FPGA SYSREF at 18.5 MHz for the FPGA capture card.

Figure 28. Device Configuration File Loading



3. Configure both ADC12DJ3200 JMODE15 (x16 decimation) by loading the configuration file in the *Low Level* page of the HSDC Pro GUI in the following order for both master and slave capture card:
   a. Master capture card:
      i. After powering the TSW14J57 mater capture card, establish the hardware connection.
      ii. Load "ADC12DJxx00_JMODE15_F&K_2_20_sysref.ini" from the *Select ADC* drop-down menu and then update the *ADC Output Data Rate* as 92.5 MHz which is a decimated data rate of 1480 MHz
      iii. Read capture and see the ADC1 spectrum
   b. Slave capture card:

i. Power on the TSW14J57 slave capture card then establish the connection with the hardware

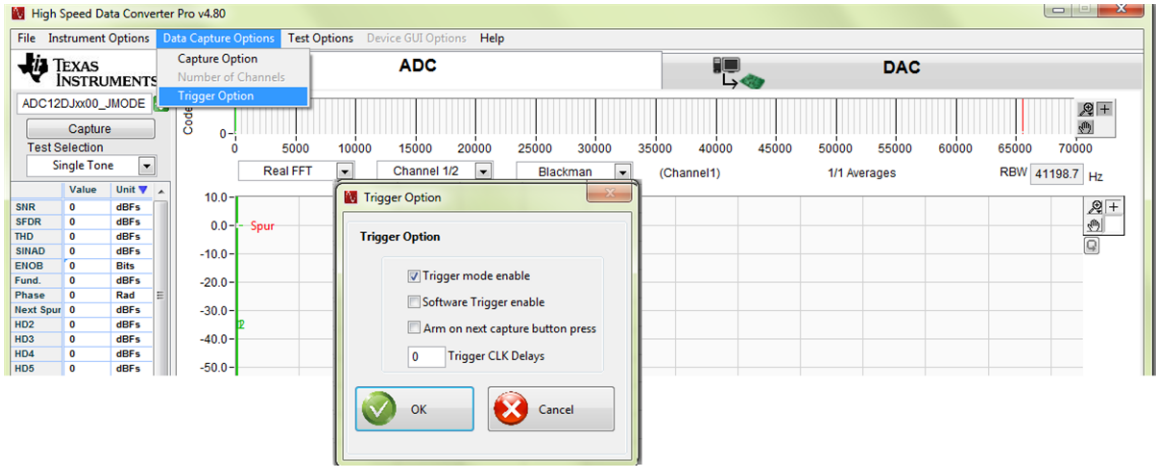
ii. Load “ADC12DJxx00_JMODE15_F&K_2_20_sysref.ini” from the *Select ADC* drop-down menu, then update the *ADC Output Data Rate* as 92.5 MHz which is a decimated data rate of 1480 MHz

iii. Read capture and see the ADC2 spectrum

iv. Load “ADC12DJxx00_JMODE15_F&K_2_20_sysref_skipconfig.ini” from the *Select ADC* drop-down menu

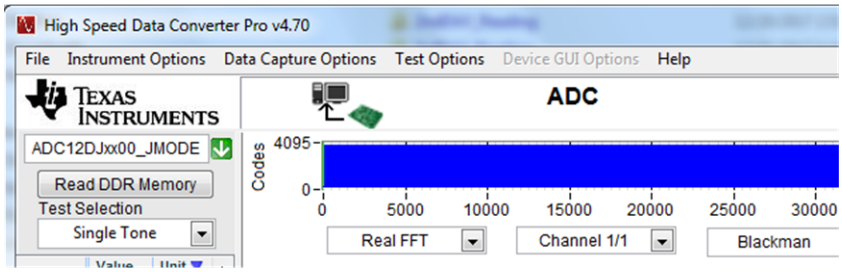
v. Using the *Data Capture Options*, *Trigger Option* selection menu item; select only *Trigger mode enable*:

Figure 29. Trigger Option Selection: Trigger mode enable



vi. After enabling the trigger, the *Capture* button becomes *Read DDR Memory* (see Figure 30):

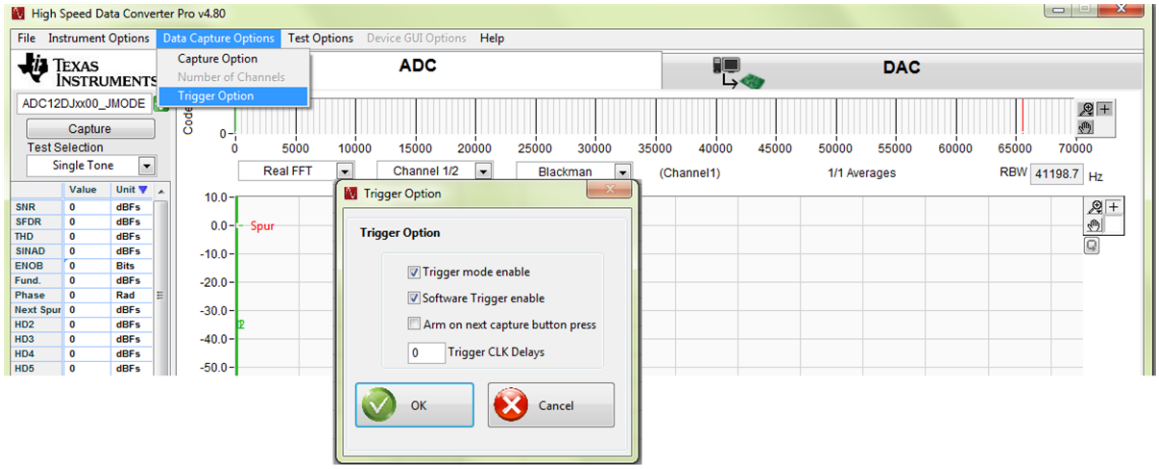
Figure 30. HSDC Pro Slave Capture Read: Read DDR Memory



c. Master capture card:

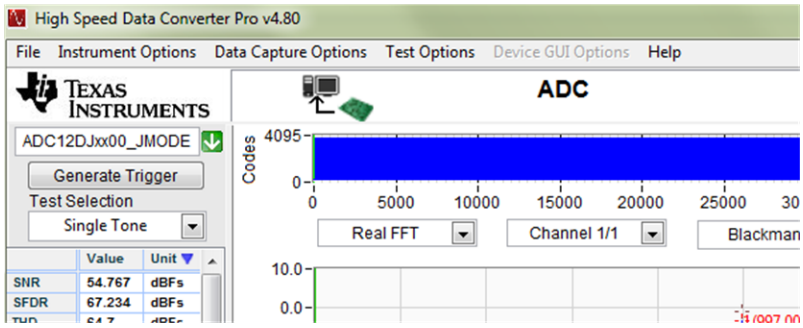
i. Go to the *Data Capture Options* menu, enable both *Trigger mode enable* and *Software Trigger enable* options (see Figure 31).

Figure 31. Trigger Option Selection: 'Trigger mode enable' and 'Software Trigger enable'



ii. After enabling the triggers, the *Capture* button becomes *Generate Trigger* (see Figure 32).

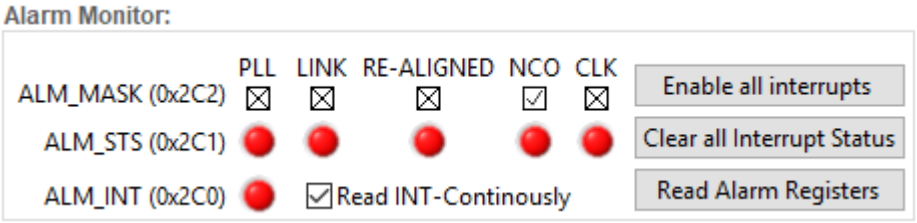
Figure 32. HSDC Pro Slave Capture Read: Generate Trigger



d. NCO Alarm Set:

i. Before doing synchronous capture, configure the NCO alarmregister bit in the alarm register as Figure 33 shows.

Figure 33. Alarm Monitor Register Settings



ii. Set the “Enable NCO interrupt” bit for both ADCs and clear all interrupts using the *Clear all Interrupt Status* button.

iii. Check the “Read INT – continuously” bit for both ADCs.

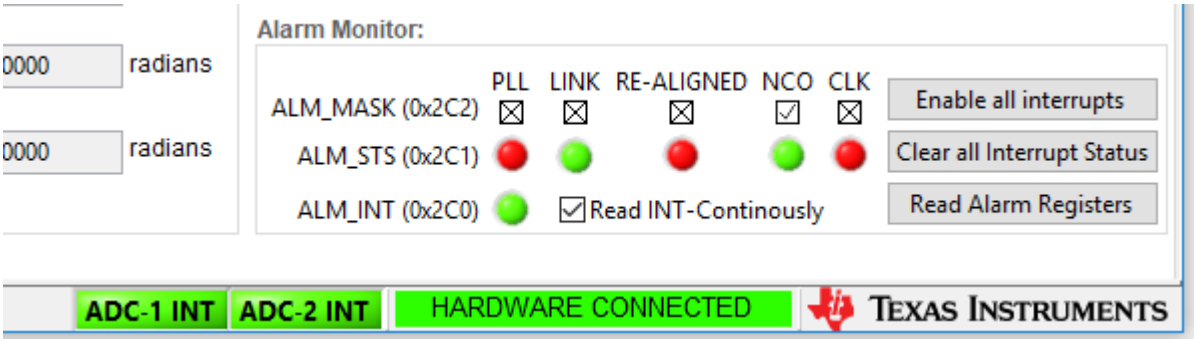
4. **Synchronous Capture with Master Slave mode:**

1. Feed the input signal frequency 1250 MHz, –7 dBFS to channel 1 (J12) and channel 3(J29) from the signal source via splitter.dsds
2. “Read DDR memory” from the slave capture card, make sure the slave is ready for trigger input for capture.
3. Apply “Generate Trigger” from the master capture card, this generates the SYNC pulse to both ADCs.

The rising edge for SYNC~ pulse initiates ILA sequence at the same time for all transmitters with the same LFMC period.

4. After NCO reset, the NCO ALM_STS bit sets and interrupt generates

Figure 34. NCO Alarm Status



5. After NCO synchronization is complete, load "ADC12DJxx00_JMODE15_F&K_2_20_sysref_skipconfig.ini" from the *Select ADC* drop-down menu, then repeat "Read DDR memory on slave" and *Generate Trigger* on the master for another synchronous capture.
6. Export both ADC1 and ADC2 data, then extract the phase and amplitude information from the spectrum using the MATLAB® program and plot the data in the time domain for a channel-to-channel skew measurement. The sample MATLAB code is provided in Appendix A.
7. Adjust the t_{AD} register values to make channel-to-channel skew as CH1 and CH3. See Section 2.3.3 for more details.

3.2.2.2 Synchronization Performance in JMODE16

Test condition

F_S = 3000 MHz
F_{IN} = 54.7 - 2742 MHz
F_{NCO} = 90 - 2700 MHz
Mode = JMODE16 (x16 Decimation) - 16 lanes

3.2.2.2.1 Test Procedure

1. Use the J32 connector to program the LMK61E2 device at 37.5 MHz using the USB2ANY programmer associated with the LMK61E2 oscillator programming tool. Set the device address as 0x5A before programming.
2. Load the configuration file in the LMK04828 from following location

   ".. \TIDA1022_28_32A_32B\TIDA-010122\JM16_DCLK=3000M_SYSREF=37.5M_FPGACLK=187.5M_K=5"

   using HSDC TID GUI. This generates 3000-MHz DEVCLK and SYSREF 37.5 MHz for both ADC1 and ADC2. This also generates the FPGA reference at 187.5 MHz, the FPGA core clock at 187.5 MHz, and the FPGA SYSREF at 37.5 MHz for the FPGA capture card.
3. Configure both ADC12DJ3200 JMODE16 (x16 decimation) by loading the configuration file in the *Low Level* page of HSDC Pro GUI for both the master and slave capture card
4. Perform channel-to-channel measurement across the input signal frequency and select the corresponding NCO frequency for sampling frequency Fs = 3000 MHz.

3.2.3 Performance Test Results

In this reference design, NCO synchronization done with decimation (x16) and the key test parameter like channel-to-channel skew, SNR, SFDR performance is measured with Fs = 1480 MHz, Fin = 1250 MHz input signal frequency in JMODE15.

The channel-to-channel skew performance is measured across the input signal frequency 54.7 MHz–2700 MHz with a different NCO frequency for the maximum sample rate at Fs = 3000 MHz in JMDOE16.

Figure 35 and Figure 36 show the measured spectrum of the TIDA-010122 design at a 1250-MHz input, 1480-MHz sample rate of ADC1 and ADC2 with 1270-MHz NCO frequency.

Figure 35. ADC1 Spectrum - I Data, F_S = 1480 MHz, F_{NCO} = 1270, F_{in} = 1250 MHz

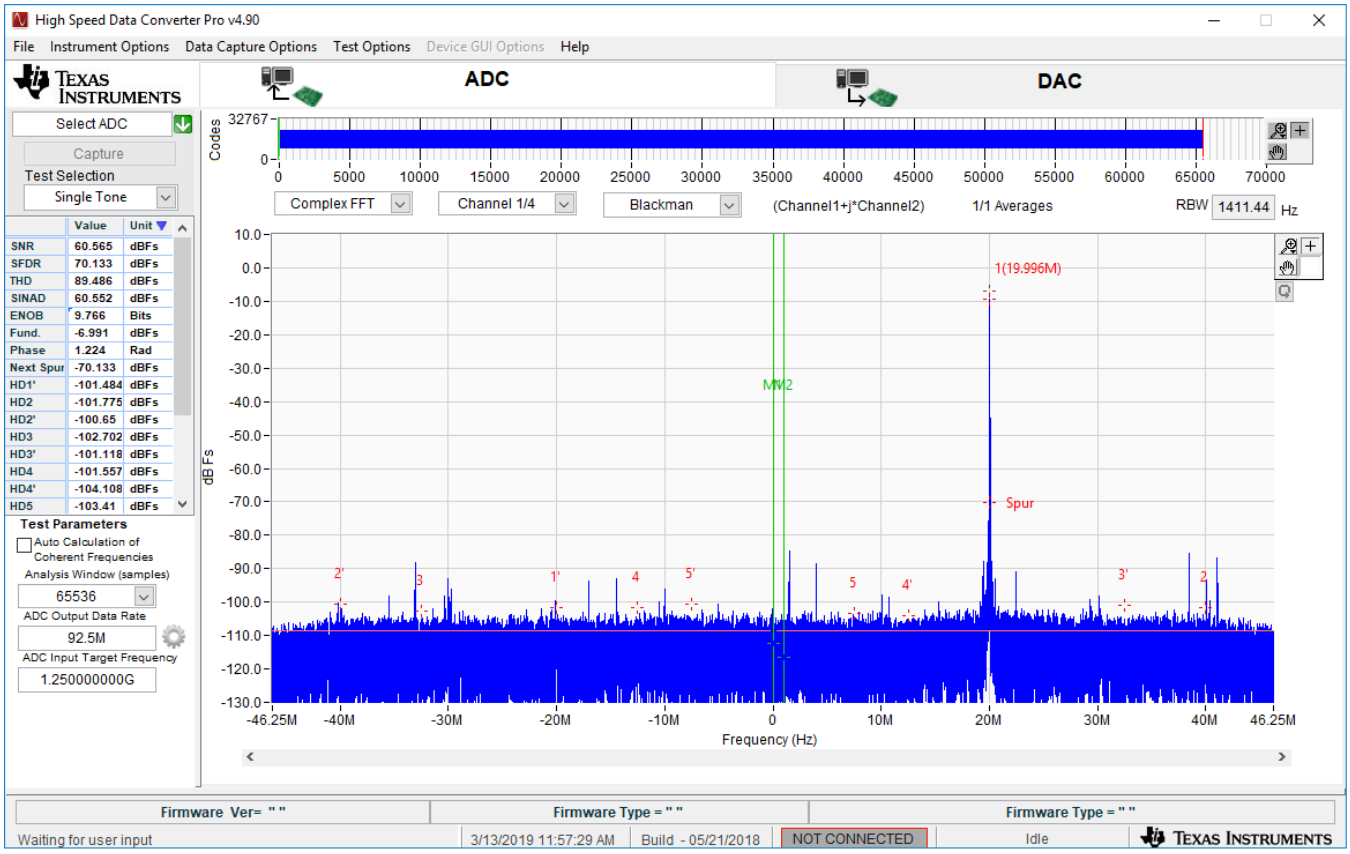


Figure 36. ADC2 Spectrum - Q Data, F_S = 1480 MHz, F_{NCO} = 1270, F_{in} = 1250 MHz

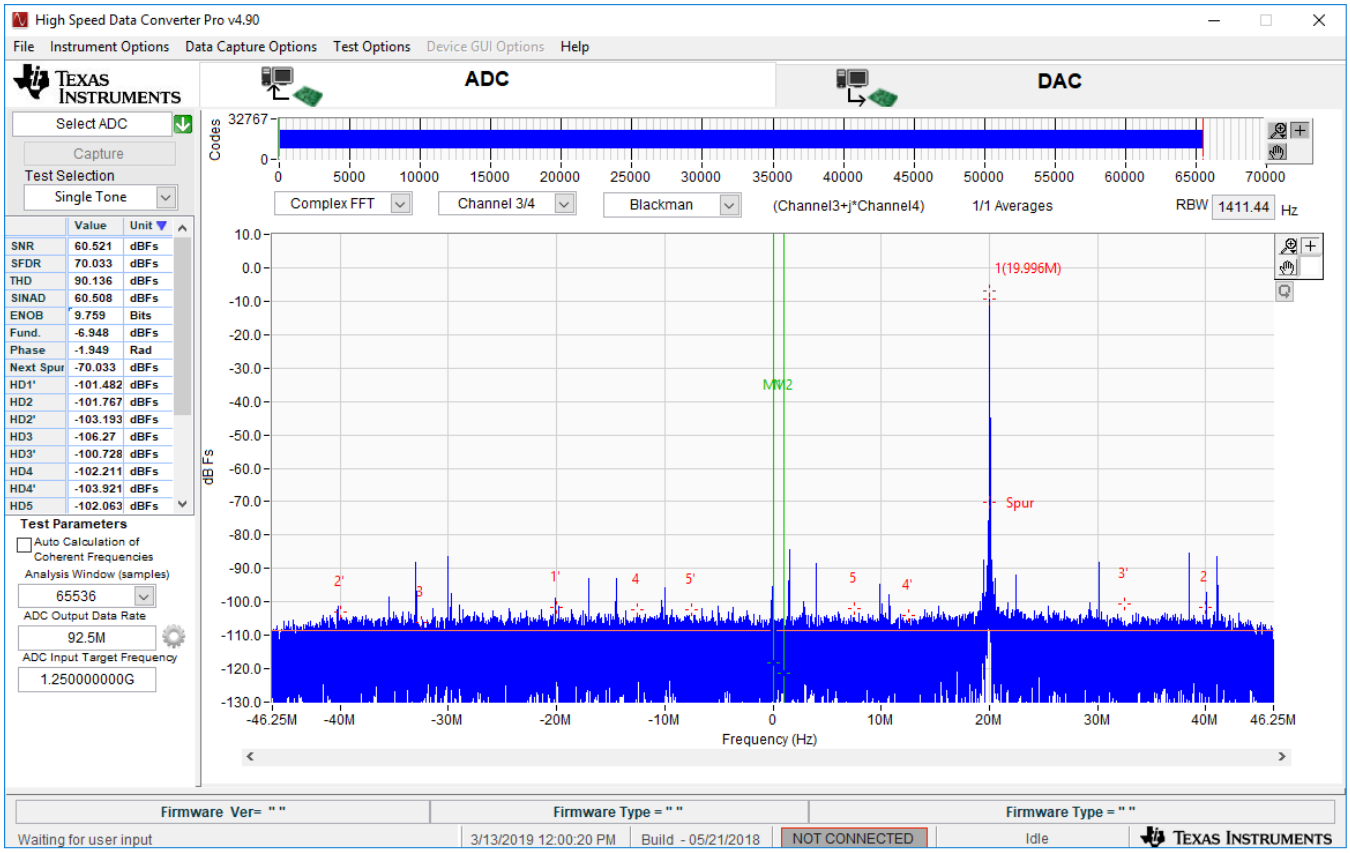


Figure 37 and Figure 38 show the SNR and SFDR performance curve for sampling frequency Fs = 1480 MHz, NCO frequency F_{NCO} = 1250 and input frequency F_{IN} 1200 MHz to 1290 MHz.

Figure 37. SNR Measurement: JMODE15

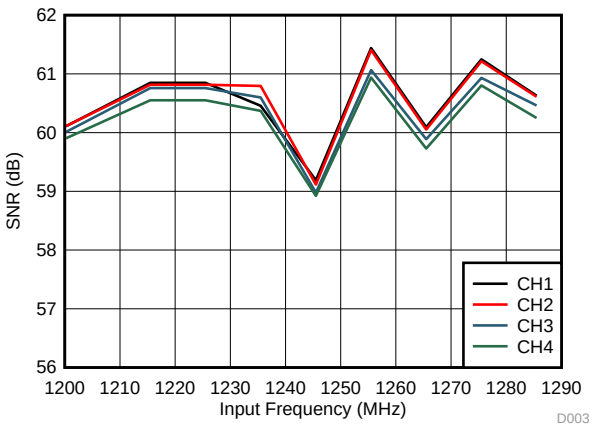


Figure 38. SFDR Measurement: JMODE15

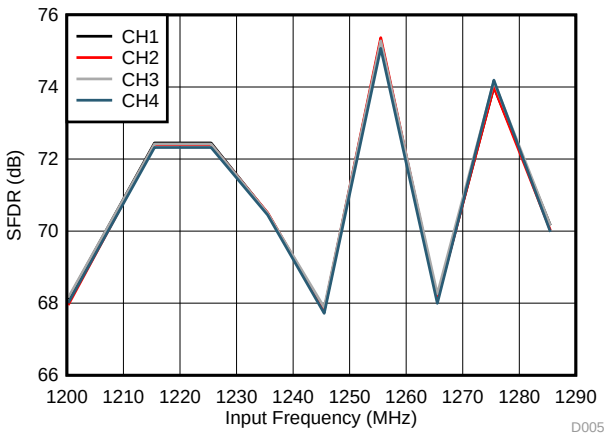


Figure 39 shows the measured time skew between two channels (CH1 and CH3) of the TIDA-010122 design at room temperature with a 1250-MHz input signal and at a sampling frequency of 1480 MHz with decimation x16 and NCO frequency configured as 1270 MHz. Evaluate this skew by calculating the phase difference between signals captured from each ADC. This measurement done with transformer inputs and the measured time skew was less than 1 ps for JMODE15.

Figure 40 shows channel-to-channel skew performance results for a sampling frequency at 3000 MHz with an input frequency from 54.7 MHz to 2742 MHz with a corresponding NCO frequency from 90 MHz to 2700 MHz for JMODE16. The skew variation between channels (CH1 and CH3) are observed at not more than 10 ps.

Figure 39. Channel-to-Channel Skew Measurement: JMODE15

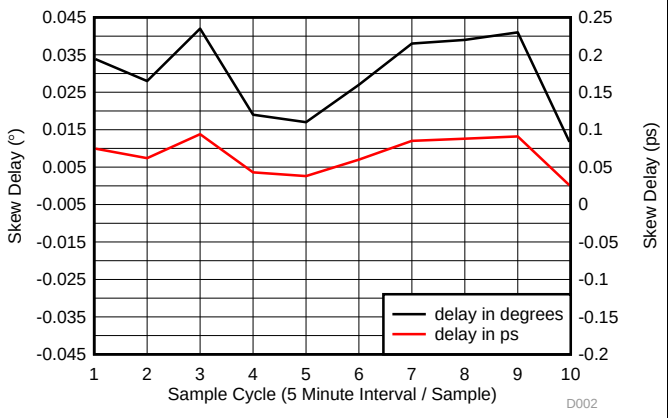
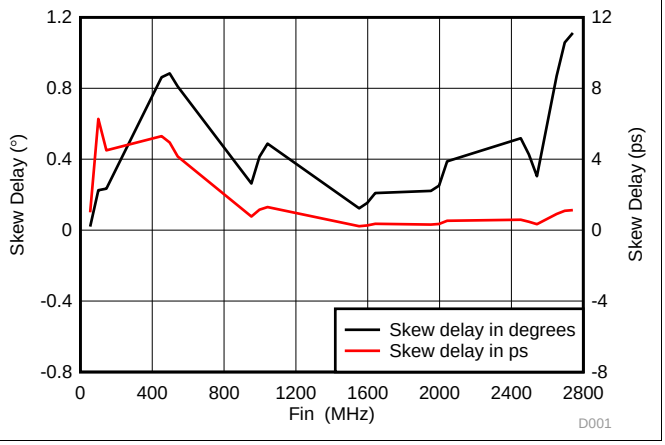


Figure 40. Channel-to-Channel Skew Measurement: JMODE16



NOTE: All the test are carried out at ambient temperature

In summary, the TIDA-010122 reference design demonstrates the ADC12DJ3200 synchronization features that allow multiple similar ADCs to be synchronized and achieves a channel-to-channel skew less than 10 ps with deterministic latency.

This reference design demonstrates the flexibility and features of clock devices such as the LMK04828 and the LMX2594 that help designers to achieve low phase noise, high-frequency clocks for gigahertz sampling applications.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010122.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010122.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010122.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010122.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010122.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010122.

5 Related Documentation

5.1 Related Reference Designs

1. Texas Instruments, Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems
2. Texas Instruments, Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers

5.2 Other Related Documents

1. Texas Instruments, *JESD204B multi-device synchronization: Breaking down the requirements* Analog Applications Journal

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6 About the Author

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6.1 Acknowledgment

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Appendix A Example MATLAB® Program for Analyzing Skew

```
%--------------------------------------------------------%
% Import Data %
%--------------------------------------------------------%
function varargout = SkewCheck_v5(varargin)
close all;

global N;
global samples_all;
global ax;
global num_bits;
global Fs;
global Fin;

global Decimation;
global popupA;
global popupB;


% Declare variables for imported data
data1 = xlsread('read_csv1.csv');
data2 = xlsread('read_csv2.csv');

Fs = 2700e6;
Fin = 997e6;
Fnco = 0;
Decimation = 1;
N = length(data1);
num_bits = 15;

%Removing DC in all the channels
samples_board_1 = data1;
samples_board_1 = samples_board_1 - repmat(mean(samples_board_1),size(samples_board_1,1),1);

samples_board_2 = data2;
samples_board_2 = samples_board_2 - repmat(mean(samples_board_2),size(samples_board_2,1),1);

samples_all = [samples_board_1 samples_board_2];

fig=figure('Units', 'normalized', 'Position',[0.1,0.1,0.5,0.8]);
set(0, 'CurrentFigure', fig);

for i = 1:size(samples_board_1,2)
    waveDataSrc{i} = sprintf('File1_Ch%1d',i);
end

for k = 1:size(samples_board_2,2)
    waveDataSrc{size(samples_board_1,2)+k} = sprintf('File2_Ch%1d',k);
end

popupA = uicontrol('Style', 'popup', 'Units', 'normalized',...
   'String', waveDataSrc,...
   'Position', [0.76,0.935, 0.2, 0.05],...
   'Tag', 'PUA1', 'Callback', @setmap);

popupB = uicontrol('Style', 'popup', 'Units', 'normalized',...
   'String', waveDataSrc,...
   'Position', [0.76,0.905, 0.2, 0.05],...
   'Tag', 'PUB1', 'Callback', @setmap);


ax(1) = axes('DataAspectRatioMode', 'auto', 'PlotBoxAspectRatioMode', 'auto',
'CameraViewAngleMode', 'auto',...
```

```
    'Units', 'normalized', 'Position', [0.06+0,0.06+0.48*1,0.9,0.38]);
ax(2) = axes('DataAspectRatioMode', 'auto', 'PlotBoxAspectRatioMode', 'auto',
'CameraViewAngleMode', 'auto',...
    'Units', 'normalized', 'Position', [0.06+0,0.06+0.48*0,0.9,0.38]);


PlotData(1, 1)

CalcSkewData

end



function PlotData(PUPA, PUPB)
global samples_all;
global ax;
global N;
global num_bits;
global Fs;
global Fin;

global Decimation;

Fsd = Fs/Decimation;


global popupA;
global popupB;

popupAStr = get(popupA, 'String');
popupBStr = get(popupB, 'String');

samples_board_1 = samples_all(:,PUPA);
samples_board_2 = samples_all(:,PUPB);

subplot(ax(1));
% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);

% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

%magitude correction
samples_board_1 = samples_board_1 * (mag_x/mag_y);

plot((0:length(samples_board_1)-1)*(1/Fsd),samples_board_1,...
((0:length(samples_board_2)-1)*(1/Fsd))-(0/(2*Fsd)),samples_board_2);
str_trace1 = sprintf('%s',popupAStr{PUPA});
str_trace2 = sprintf('%s',popupBStr{PUPB});
leg = legend(str_trace1, str_trace2);
set(leg, 'Interpreter', 'none');
title('Time Domain Plot');

% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
```

```
A = 2^(num_bits-1);

% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

subplot(ax(2));
plot((0:N/2)*(Fsd/N), 20*log10(abs(X*2/N/A)), (0:N/2)*(Fsd/N), 20*log10(abs(Y*2/N/A)));
title('FFT Plot of ADC 1');

fprintf('\nIndex_x:%d; Index_y:%d\n',index_x, index_y);

% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_x));

% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff = mod(phase_diff, 2*pi);
%phase_diff_deg = mod(phase_diff / pi * 180, 360);
boardstring = '';
if phase_diff > pi
    boardstring = 'Brd1 Lags Brd2';
    phase_diff = 2*pi-phase_diff;
else
    boardstring = 'Brd2 Lags Brd1';
    phase_diff = phase_diff;
end

phase_diff_deg = phase_diff / pi * 180;


skew_ps = phase_diff_deg / (360*Fin) / 1e-12;

abc_title1 = sprintf('%s by %3.3f deg or %3.3f ps', boardstring, phase_diff_deg, skew_ps);
subplot(ax(1));
title(abc_title1);

abc_title2 = sprintf('Fin = %3.3f MHz', Fin*1e-6);
subplot(ax(2));
title(abc_title2);
end


function skewdata=CalcSkewData()
global samples_all;
global N;
global num_bits;
global Fs;
global Fin;

global Decimation;

Fsd = Fs/Decimation;

for row = 1:size(samples_all,2)
    for col = 1:size(samples_all,2)
        samples_board_1 = samples_all(:,row);
        samples_board_2 = samples_all(:,col);

        % Get FFT of for each board.
        window = blackman(N);
        X=fftshift(fft(window.*samples_board_2));
        Y=fftshift(fft(window.*samples_board_1));
        X = X(N/2:end);
        Y = Y(N/2:end);
```

```
            A = 2^(num_bits-1);

            % Find the bin with the largest amplitude. This is the sine wave.
            [mag_x index_x] = max(abs(X));
            [mag_y index_y] = max(abs(Y));

            %magitude correction
            samples_board_1 = samples_board_1 * (mag_x/mag_y);

            % Get FFT of for each board.
            window = blackman(N);
            X=fftshift(fft(window.*samples_board_2));
            Y=fftshift(fft(window.*samples_board_1));
            X = X(N/2:end);
            Y = Y(N/2:end);
            A = 2^(num_bits-1);

            % Find the bin with the largest amplitude. This is the sine wave.
            [mag_x index_x] = max(abs(X));
            [mag_y index_y] = max(abs(Y));

            % Get the phase of each signal at the appropriate bin.
            phase_x = angle(X(index_x));
            phase_y = angle(Y(index_x));

            % Calculate the phase difference and time skew.
            phase_diff = phase_y - phase_x;

            phase_diff_deg = phase_diff / pi * 180;

            skew_ps = phase_diff_deg / (360*Fin) / 1e-12;

            abc_title = sprintf('%3.3f°/%3.3fps', phase_diff_deg, skew_ps);
            skewdata{row,col}=abc_title;
        end
    end

    f = figure;
    t = uitable(f,'Data',skewdata, 'Units', 'Normalized', 'Position',[0, 0, 1, 1],
    'ColumnWidth',{150});

    end

    function setmap(source,callbackdata)
    global popupA;
    global popupB;

    PlotData(get(popupA, 'Value'), get(popupB, 'Value'));
    end
```

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