Design Guide: TIDA-080005

Full high-resolution DLP® sub-system reference design for high-speed desktop 3D printing

TEXAS INSTRUMENTS

Description

This high resolution, high speed 3D printing Reference Design enables faster development of professional 3D printing applications using DLP ®Pico™ technology. This design uses a stereolithography (SLA) technique, where a photo-resin is exposed to successive 2-dimensional patterns to create a 3-dimensional object one layer at a time. This design uses the DLP Pico 0.47 1080p DMD (DLP4710) with the new display and light controller DLPC3479. The DLP4710 DMD offers an excellent balance between resolution, size, and cost, targeting small form-factor desktop 3D printers and enabling a wide variety of 3D printing use cases across consumer, professional, and industrial applications. It includes electronics and optics along with software to generate pattern sets for the 3D printing process. The design also includes the DLPA3005 PMIC and LED driver.

Resources

TIDA-080005	Design Folder
DLP4710(DMD)	Product Folder
DLPC3479	Product Folder
DLPA3005	Product Folder

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Features

- 1920 x 1080 resolution with flexible and precise light contol
- Compact PCB Layout supporting 1080p (DLP4710) optical engine and includes HDMI and USB connectivity
- Used in DLP4710EVM-LC layout
- 19-V Input and LED current drive up to 16 A (blue/green) and 12 A (red)
- PC software GUI to send any type of pattern to the light engine

Applications

- Personal electronics
  - Desktop 3D Printers
- Industrial:
  - Custom Parts manufacturing

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1 System Description

Stereolithography is an additive manufacturing method that employs a photo-curable resin. Exposing the photo-resin to successive two-dimensional object cross sections creates the three-dimensional object a single layer at a time. The resin, composed of monomers, cross-links when exposed to light of a sufficient energy level. The cross-linking of the monomers generates a polymer chain, creating a solid material where the resin was exposed. Stereolithography was traditionally achieved by outlining the object layer with a laser. DLP technology allows an entire layer to be exposed simultaneously by dynamically masking a broad light source. Due to layer-based printing, this technique is fundamentally much faster compared to alternate technologies.

Figure 1 shows a typical block diagram of a 3D printing system that uses the stereolithography technique.
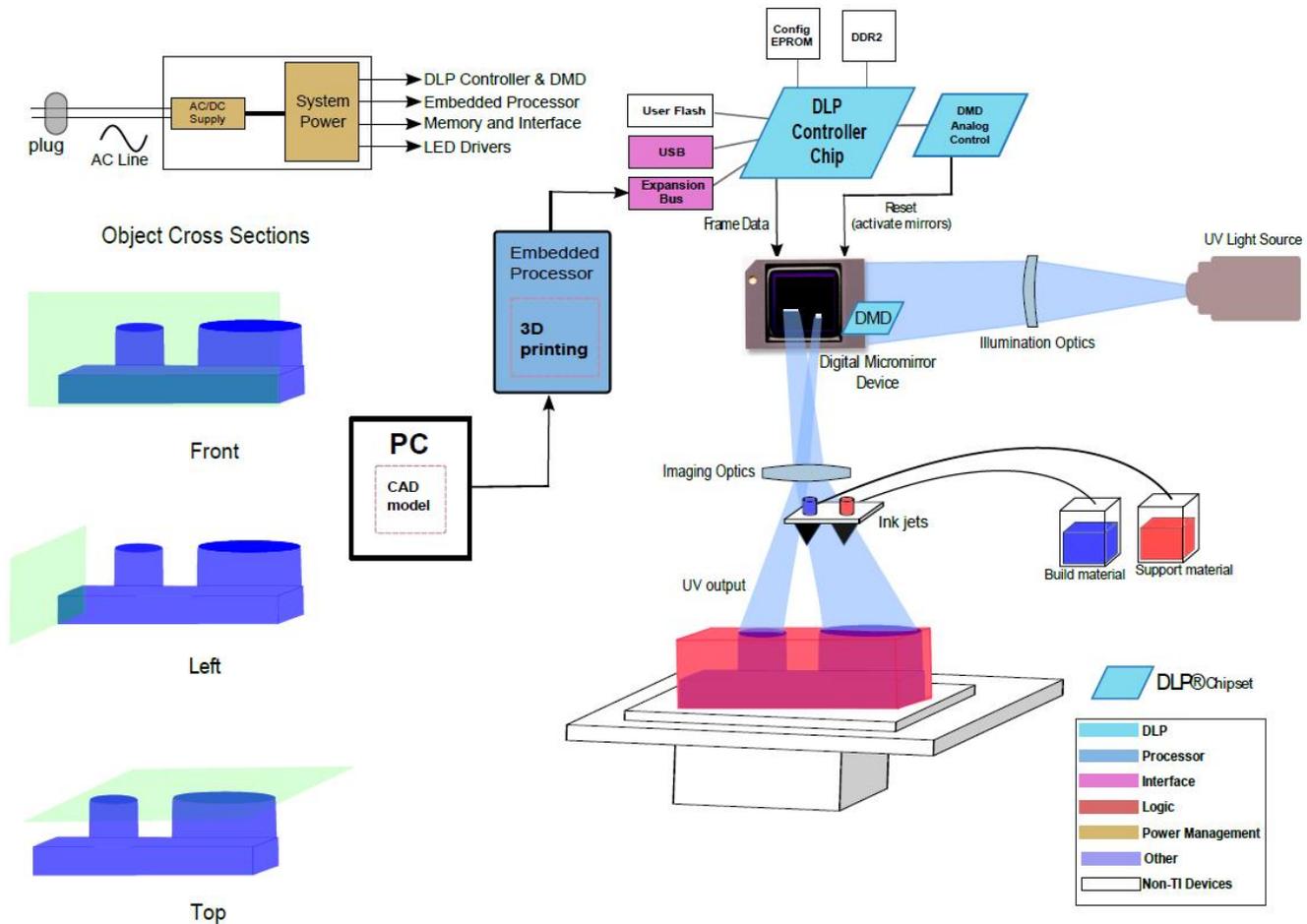

Figure 1. 3D printing system block diagram

Typical 3D printer requirements are shown in Table 1.

Table 1. Typical 3D Printer System Requirements

| Feature	Requirements
Pattern Speed	1 Hz to 100 Hz
X-Y Resolution	50 µm to 100 µm
Build Area	225 mm x 120 mm
Pattern	Binary or 8 bit grayscale patterns using external pattern mode

1.1 Applications for 3D Printing

DLP technology offers high-precision and high-speed printing in stereolithography compared to alternate technologies such as FDM (fused deposition molding) or laser-based stereolithography. The table below lists the key features of DLP technology and their corresponding benefits in 3D printing applications.

Table 2. DLP Features and Design Benefits for 3D Printing

DLP Feature	Design Benefit
Layer-by-layer printing: Micromirror array exposes an entire layer in one shot	Faster build speed than **point-by-point** technologies and constant build time independent of layer complexity.
Easily programmable high-resolution patterns	Enables sub-50 µm resolutions on the image plane and easily adjusts layer thickness
Extended wavelength support	Compatible with a wide range of polymers and resins
Reliable MEMS technology	No expensive parts (e.g. ink jets) to replace - translates to lower cost of ownership

2 System Overview

2.1 Block Diagram
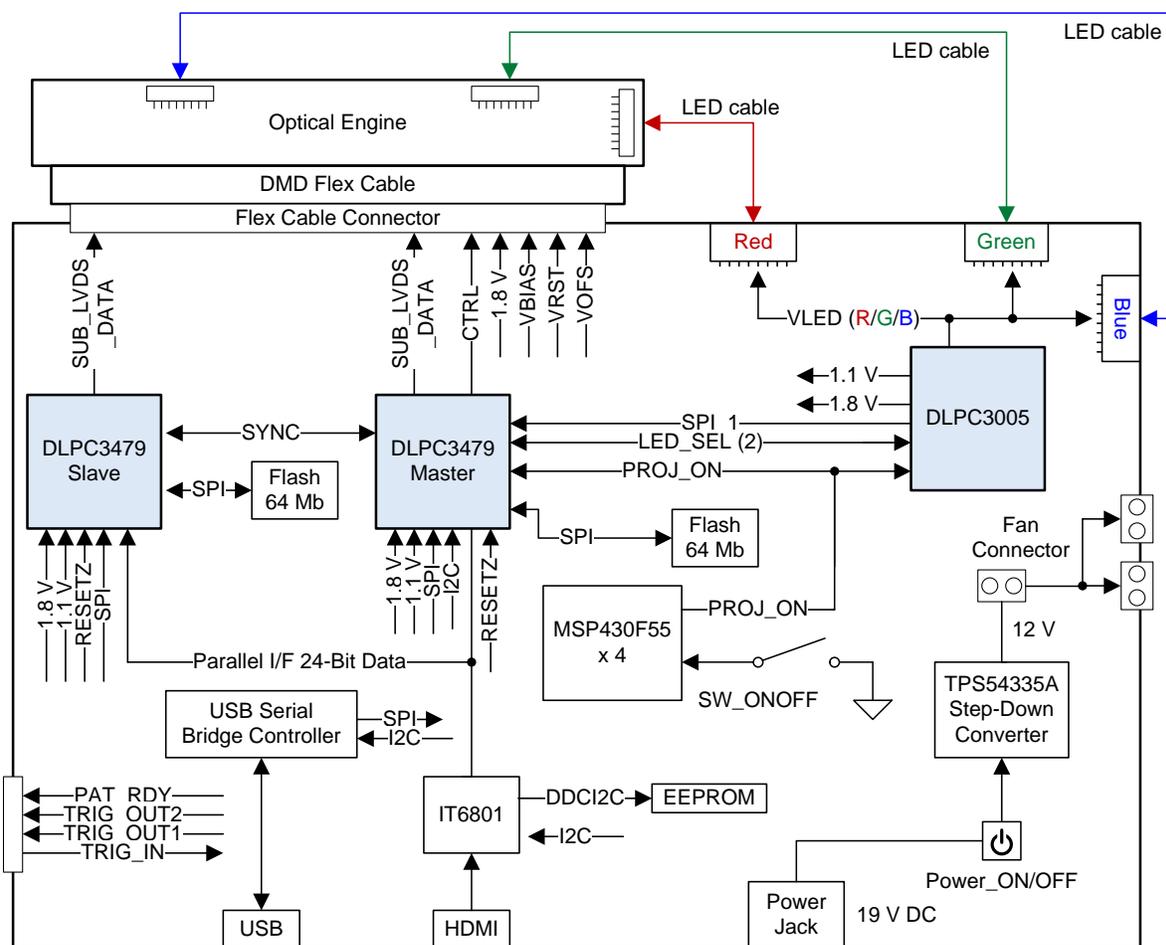
Figure 2. TIDA-080005 Block Diagram

Full high-resolution DLP® sub-system reference design for high-speed desktop 3D printing
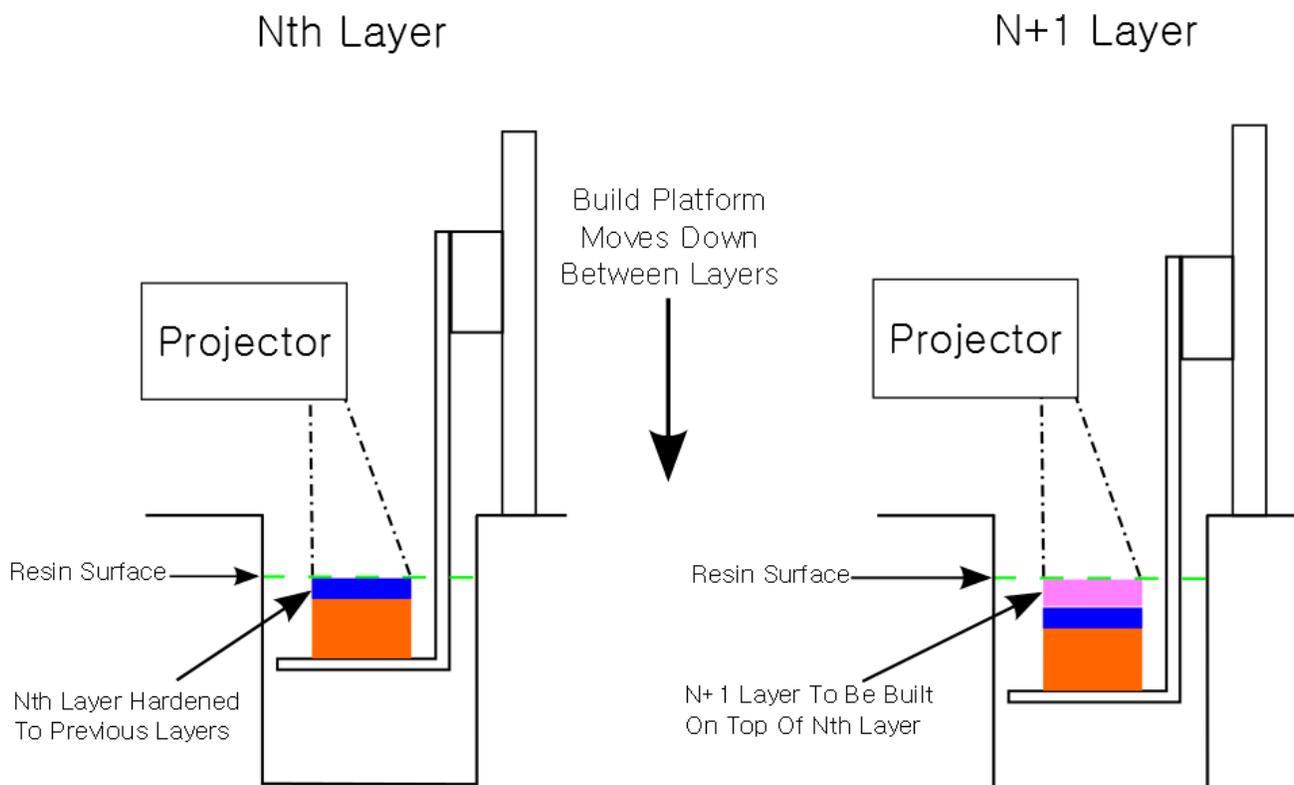
2.2 Design Considerations

See the following documents for DLP system design considerations:

- *TI DLP® Pico™ System Design: Optical Module Specifications*
- *TI DLP® System Design: Brightness Requirements and Tradeoffs*
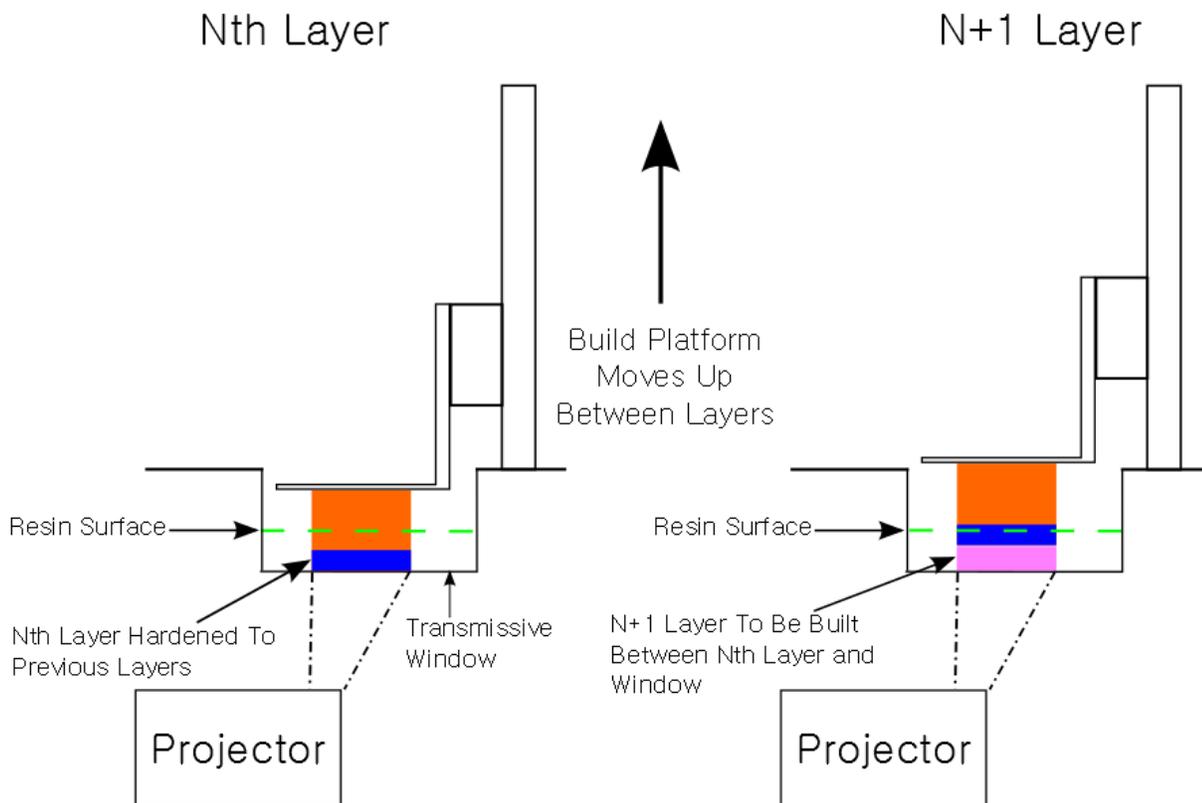
2.2.1 3D Printer Build Orientation

The 3D printer can be designed using two methods – Top-down or bottom-up build orientations.

Figure 3. Top-Down 3D Printing Method

Bottom-Up Build Orientation

Figure 4. Bottom-Up 3D Printing Method

The top-down build method has its layer thickness defined by the distance from the build platform - or partially-built object - and the upper surface of the resin. This means the time for the resin's surface layer to return to level after each build platform movement must be considered.

The bottom-up build method is more popular as it solves two key issues; resin settling time, and layer thickness control. The bottom-up build orientation requires the projected layer images to be transmitted through a material into the resin vat from below. The build platform starts flush against the transmissive window and steps upward with each layer. The build platform's orientation to the window means the resin's surface does not impact the build, and the layer thickness is clearly defined between the platform and the window.

The bottom-up build requires a smaller volume of resin in the vat at a time but requires the user to constantly refill the vat as resin is used. The challenge of overcoming stiction also exists between the hardened layers and the transmissive window. E s. If the solidified resin does not separate cleanly and easily from the transmissive window, delicate features may be destroyed during the build process. Ensure that the resin adheres strongly to the build platform material because the weight of the object is suspended from the platform during the build. The bottom-up build method is illustrated in Figure 4.

2.2.2 Object Layer Images

Object layer images can be made by hand using a drawing utility or created by slicing STL file models. STL files are the standard default input file for 3D printers, and are readily available in multiple online libraries. STL files can be sliced using the Freesteel slicer utility found under following link. The output image file format recommended is BMP. The output images from the slicer have to have a 16:9 aspect ratio, but need to be resized to the DLP4710 resolution of 1920 × 1080. Object features should be colored white and the background should be black. Any white pixels in the object layer images will be printed in the resin.
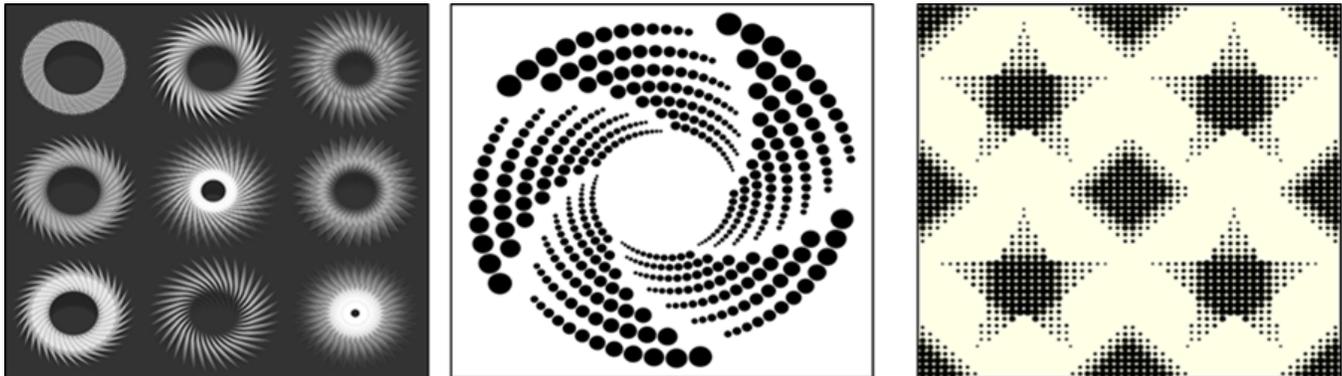

Figure 5. Example Layer Images

2.3 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.47-in 1080p DLP chipset. For a list of these documents, see Section 6

3   Hardware, Software, Testing Requirements, and Test Results

3.1   Required Hardware and Software

3.1.1   Hardware

Assuming default condition as shipped:

1. Power up the DLP4710 Light Control EVM by applying an external DC power supply
    (19 V DC, 4.74 A) to PWR_IN connector (J28).
    External Power Supply Requirements:

    *   Nom Output Voltage: 19 VDC

    *   Max Output Current: 4.74 A

    *   Efficiency Level: V
    NOTE: TI recommends using an external power supply that complies with applicable regional safety
    standards such as UL, CSA, VDE, CCC, PSE, etc.

2. Move PS_ON/OFF slide switch (SW28) to the ON position.
    +3.3V (D43) and INTZ (D57) LED indicates when 19 V power is applied.

3. Push ON/OFF switch (SW21) to turn on the DLP4710 Light Control EVM.
    +3.3V (D43), SYS_ON-OFF (D36), M_IRQ (D33) and S_IRQ (D34) LED indicates that the DLP4710
    Light Control EVM is turned on.

4. After the DLP4710 Light Control EVM is turned on, a DLP Light Control splash image will be projected.

5. The focus and zoom of the image can be adjusted on the optical module (Figure 6).
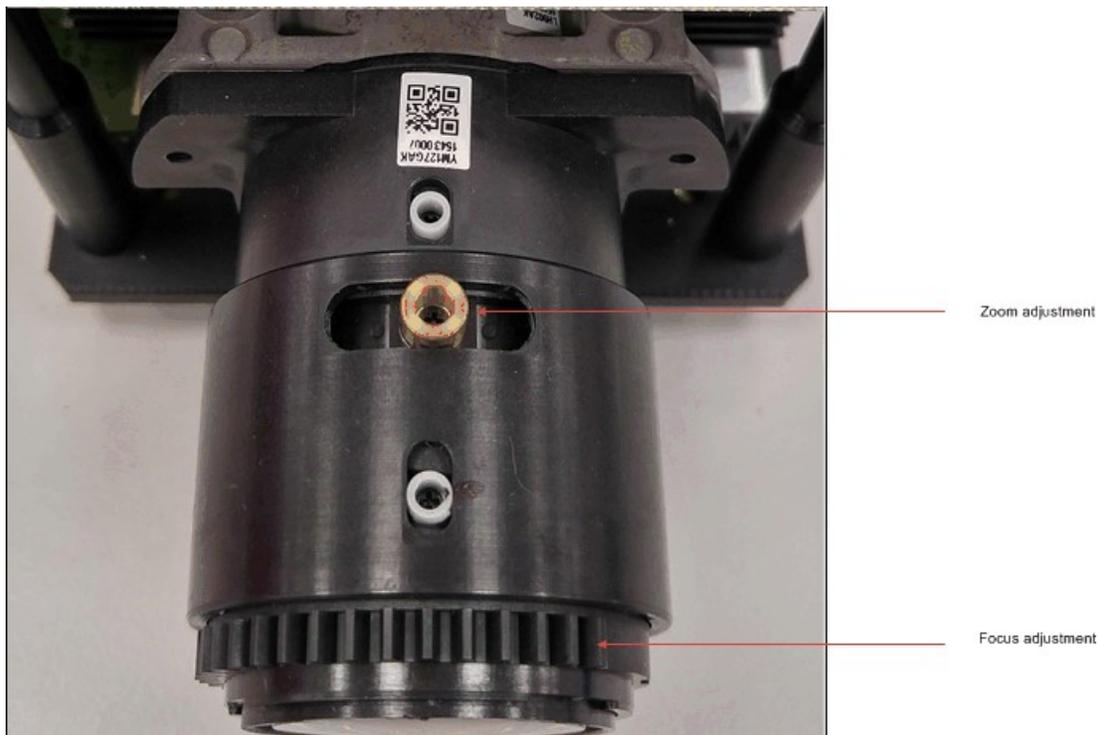
Figure 6. Optical Module With Focus and Zoom Adjustment

6. Connect USB to the DLP4710 Light Control EVM and open the DLP4710 Display and Light Control Graphical User Interface (GUI) on your computer. If needed, connect an HDMI source to the EVM and communicate to the EVM over the GUI software.

7. Via the GUI the EVM can be set to Video Display Mode or Light Control Modes. Refer to the GUI user's guide for further description. Note: Install Jumper J7 on the DLP4710 Light Control EVM to set the needed Trigger IN/OUT voltage on the EVM.

8. When turning off the projector, push ON/OFF switch (SW21) and then move slide switch (SW28) to the OFF position prior to removing the power cable.

CAUTION

To avoid potential damage to the DMD, be sure to turn off the projector using the sequence listed in Section 3.1.1 before disconnecting the power.

There are eleven LED indicators on the DLP4710 Light Control EVM (Table 3):

Table 3. DLP4710 Light Control EVM LEDs

Location	Name	Description
D33	M_IRQ	LED OFF during DLPC3479_Master boots LED ON when DLPC3479_Master boot-up process is completed and ready to receive commands
D34	S_IRQ	LED OFF during DLPC3479_Slave boots LED ON when DLPC3479_Slave boot-up process is completed and ready to receive commands
D36	SYS_ON-OFF	LED ON when projector is in normal operation
D43	+3.3V	LED ON when 19 V Power is applied and +3.3 V is working normally
D44	WPC_01	Reserved
D45	WPC_02	Reserved
D46	WPC_03	Reserved
D56	RESETZ	LED ON when DLPC3479 is in RESET
D57	INTZ	LED ON when DMD is in PARK mode
D66	STAT_LED1	LED blinking when PC is communicating to flash over SPI
D67	STAT_LED0	LED blinking when PC is communicating to DLPC3479 over I2C

3.1.1.1 Connectors, Headers, and Switch Description

Table 4. DLP4710 Light Control EVM Installed Connectors

Connector	Name	Description
J7	PWER_SEL	Header for voltage level selection for Trigger-IN/OUT
J8	M_3DR	Connector for selecting 3DR signal usage (Display or Light Control) for DLPC3479 Master
J9	S_3DR	Connector for selecting 3DR signal usage (Display or Light Control) for DLPC3479 Slave
J11	I2C	Connector for the I2C interface (DeVaSys USB-I2C/IO board)
J18	HDMI	Connector for HDMI input
J21	SPI	External SPI Programming interface connector
J22	DMD CNNT	Connector for DMD Flex Cable
J23	Spy-Bi-Wire	MSP430 Spy-Bi-Wire Programming interface connector
J24	WPC	Reserved
J26	Color Sensor	Reserved
J28	PWR_IN	Connector for 19 V DC power
J32	Fan1	Connector for 12 V Fan
J33	Fan2	Connector for 12 V Fan

Table 4. DLP4710 Light Control EVM Installed Connectors (continued)

Connector	Name	Description
J34	MSP_JTAG	MSP430 JTAG Programming interface connector
J35	SPI_SEL	Header to select Master/Slave SPI flash for external SPI Programming interface
J36	TSTPT	Header for remaining DLPC3479 test points (not used)
J40	RED	Connector for RED LED cable
J41	GREEN	Connector for GREEN LED cable
J42	BLUE	Connector for BLUE LED cable
J43	Fan3	Connector for 12 V Fan
J45	TEMP	Reserved
J47	Mini_USB	Connector for Cypress USB controller
J48	TRIG	Connector for Trigger-in and Triger-out for Light Control Application
SW21	ON/OFF	Projector ON/OFF Switch
SW28	PS_ON/OFF	Power Supply ON/OFF Switch

3.1.1.2 DLP4710 Light Control Trigger

Table 5. DLP4710 Light Control Trigger [1]

DLPC3479 PIN	J48 PIN CONNECTOR		I/O	FUNCTION
	NO.	DESC		
3DR	5	TRIGGER_IN	Input	For light control applications: Reserved for external trigger signal (Input). Applicable to internal pattern streaming mode only. The 3DR pin on the DLPC3479 can be used as a 3D left or right reference indicator or as trigger input signal for light control application. A jumper on J8 and J9 has to be set to determine the use case for this pin. For display application: Connect pin 1 and pin 2 of J8 (DLPC3479 Master) and pin 1 and pin 2 of J9 (DLPC3479 Slave) For light control application: Connect pin 2 and pin 3 of J8 (DLPC3479 Master) and pin 2 and pin 3 of J9 (DLPC3479 Slave).
TSTPT_4	7	TRIGGER_OUT1	Output	TRIG_OUT_1 signal.
GPIO_06	3	PATTERN_RDY	Output	Pattern ready signal. Applicable to internal pattern streaming mode only.
GPIO_07	4	TRIGGER_OUT2	Output	TRIG_OUT_2_signal.

[1] Install Jumper J7 to set Trigger IN/OUT voltage on the EVM (Jumper is not included by default). For 3.3-V signal level: Connect pin 2 and p 3 of J7. For 1.8-V signal level : Connect pin 1 and pin 2 of J7.

3.1.2 Software

The software required for this reference design is available for download on the DLP4710EVM-LC tool folder.

3.2 *Testing and Results*

For 3D printer, typically a mono-chrome sequence is used unlike an RGB sequence for a display application. DLPC3479 controller is designed with these requirements in consideration. The timing diagram of a typical sequence for 3D printing applications is shown in Figure 7.
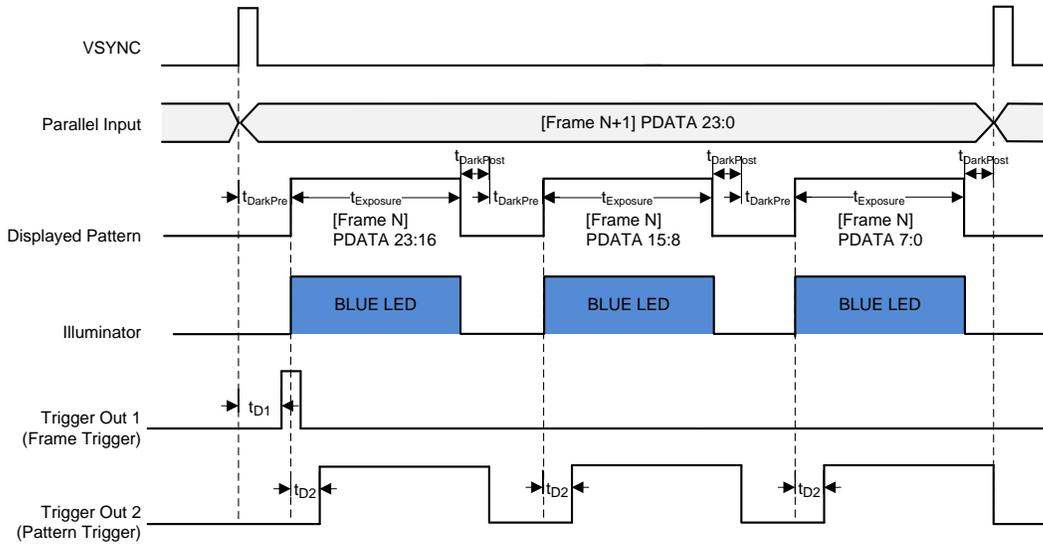

Figure 7. External Pattern Streaming Timing Sequence (24-bit Monochrome)

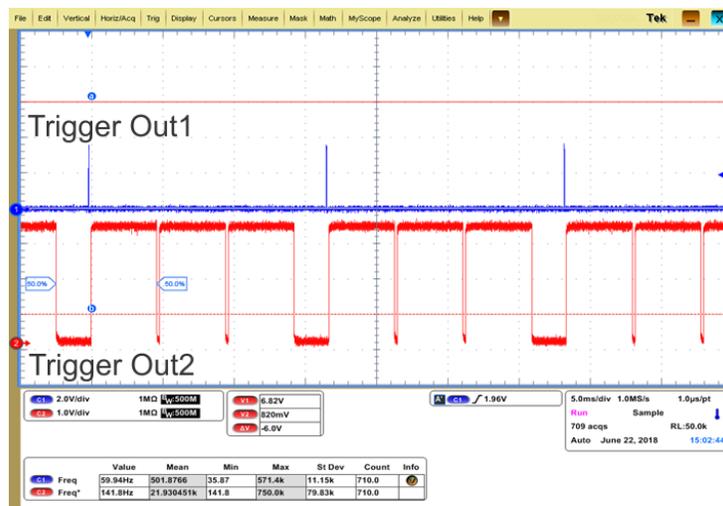This sequence has been verified on the DLP4710 light control EVM. The Trigger Out1 configuration is shown in Figure 8.

Figure 8. Scope plots of Trigger Out1 and Trigger Out2 (24-bit Monochrome)

Different types of mono-chrome and RGB images are tested on the light engine for good image quality as shown in Figure 9.
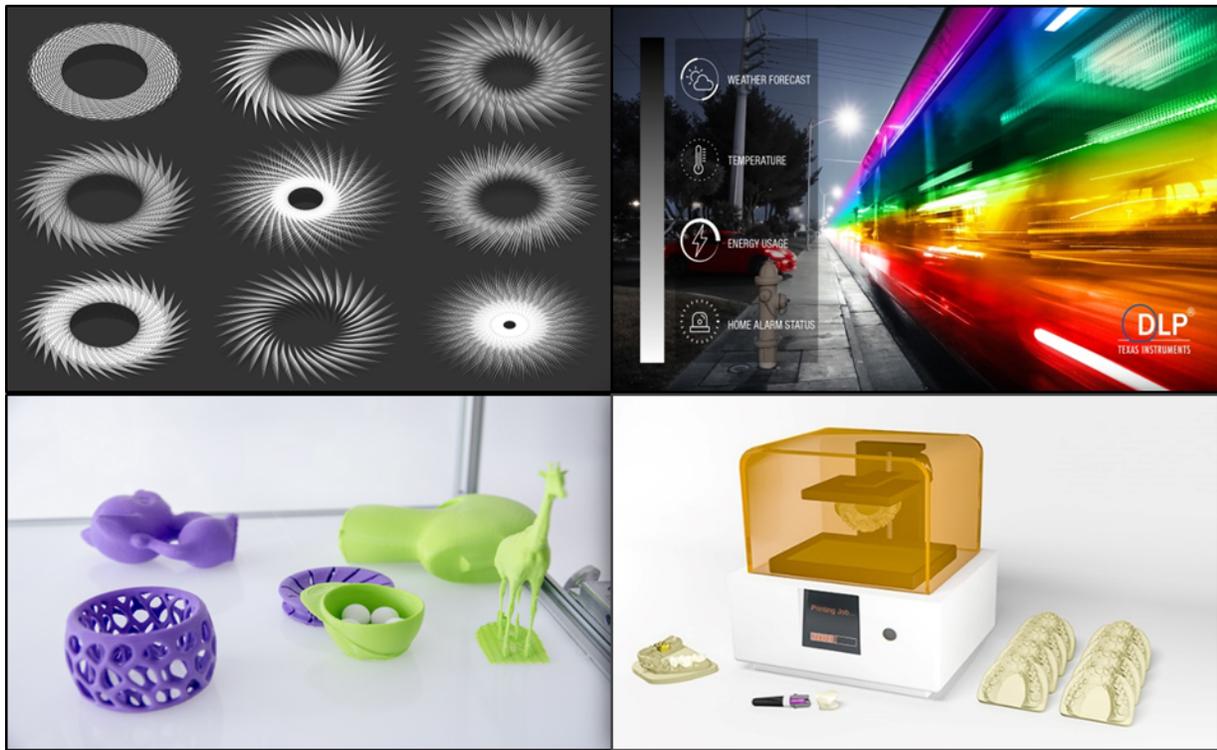
Figure 9. Monochrome and RGB Image Testing

Another key advantage that the light controller EVM provides is the ability for the users to enter *standby mode*, after printing one layer, during the build platform movement.This mode turns-off the illumination to minimize the exposure of resin to light source during the build platform movement and put the DMD in 50/50 duty cycle mode (which is strongly recommended). The stand-by mode sequence was verified on DLP 4710 EVM. The time delay between the execution of I2C command and turning off of illumination was measured to be approximately 455 µs as shown in Figure 10

To exist the stand-by-mode, the controller reconfigures the pattern timing and turns on the illumination source afterwards. This has been verified on the DLP4710 Light Control EVM. The time delay between the execution of the I2C command and the Illumination turning ON is shown in Figure 11
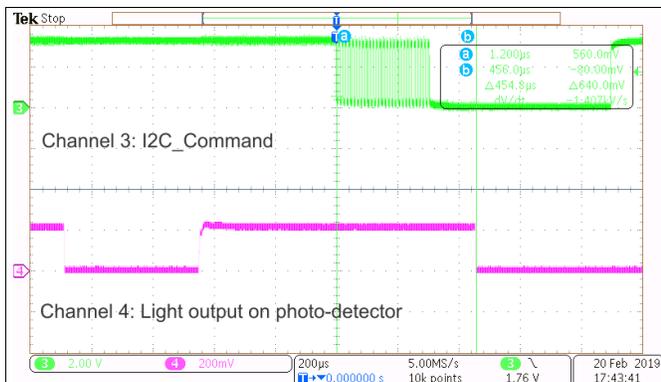

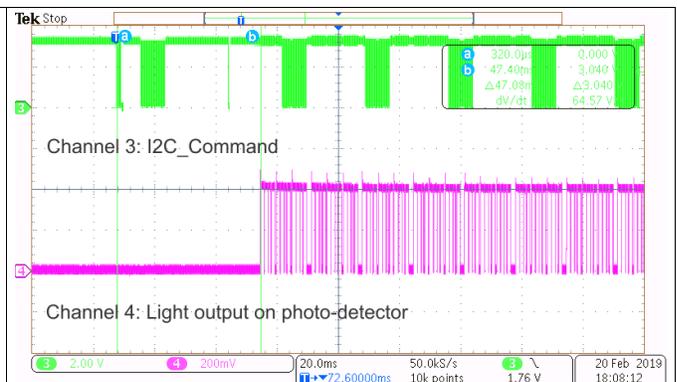**Figure 10. Delay between I2C command and Illumination turining off**

Figure 11. Delay between I2C command and Illumination turining on

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4 Design Files

4.1 *Schematics*

To download the schematics, see the design files at TIDA-080005.

4.2 *Bill of Materials*

To download the bill of materials (BOM), see the design files at TIDA-080005.

4.3 *PCB Layout Recommendations*

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the DLPC3479, DLP4710, and DLPA3005 data sheets.

4.3.1 DLPC3479 Layout Guidelines

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. Each DLPC3479 contains 2 internal PLLs which have dedicated analog supplies (V_{DD_PLLM}, V_{SS_PLLM}, V_{DD_PLLD}, V_{SS_PLLD}). Isolate the V_{DD_PLLx} power and V_{SS_PLLx} ground pins using (as a minimum) a simple passive filter consisting of two series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. Place all four components as close to the ASIC as possible. It is especially important to keep the leads of the high-frequency capacitors as short as possible. It is best to connect both capacitors across V_{DD_PLLM} and V_{SS_PLLM}/V_{DD_PLLD} and V_{SS_PLLD} respectfully on the ASIC side of the Ferrites.

Choose ferrite beads with these characteristics:

*   DC resistance less than 0.40 Ω
*   Impedance at 10 MHz equal to or greater than 180 Ω
*   Impedance at 100 MHz equal to or greater than 600 Ω

Correct PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated as if they were analog signals. Therefore, V_{DD_PLLM} and V_{DD_PLLD} must be a single trace from each DLPC3479 to both capacitors and then through the series ferrites to the power source. Ensure that the power and ground traces are as short as possible, parallel to each other, and as close as possible to each other.
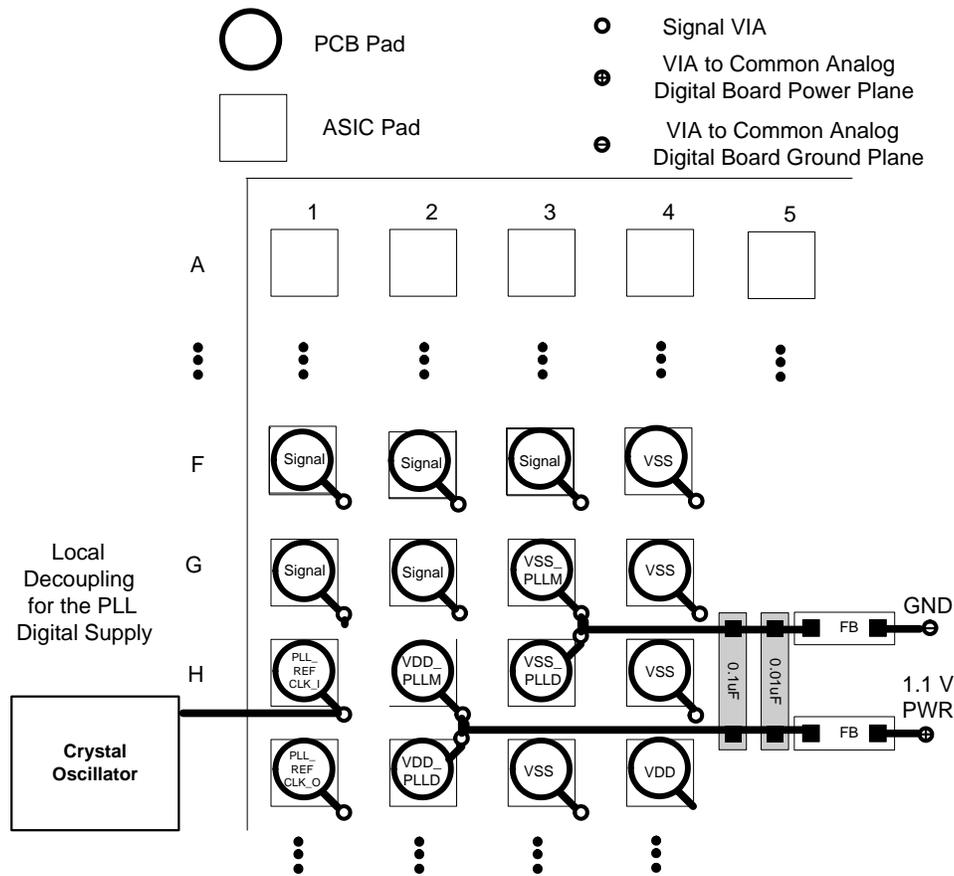
Figure 12. PLL Filter Layout

4.3.2 DLPC3479 Reference Clock

The DLPC3479 requires an external reference clock to supply its internal PLL. A crystal oscillator can supply this reference. For flexibility, the DLPC3479 accepts either of two reference clock frequencies, but both must have a maximum frequency variation of ±200 ppm (including aging, temperature, and trim component variation).

The two DLPC3479 devices require a single dedicated oscillator where the oscillator output drives both DLPC3479 devices. The oscillator must drive the PLL_REFCLK_I pin on each DLPC3479. Leave the PLL_REFCLK_O pins unconnected.

The external oscillator must be able to drive at least a 15-pF load. Routing length from the oscillator to each DLPC3479 should be closely matched.

4.3.3 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, tie unused ASIC input pins through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with an internal pullup or pulldown resistors, it is unnecessary to add external pullup or pulldown resistance unless specifically recommended. The internal pullup and pulldown resistors are weak. Do not expect them to drive the external line. The DLPC3479 implements very few internal resistors and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullup or pulldown resistance, use the value 8 kΩ (maximum).

Never tie unused output-only directly to power or ground. Leave them open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they must be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

4.3.4 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 6. Max Pin-to-Pin PCB Interconnect Recommendations[1][2]

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See [3]	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See [3]	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See [3]	inch (mm)
DMD_LS_WDATA	6.5 165.1	See [3]	inch (mm)
DMD_LS_RDATA	6.5 165.1	See [3]	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See [3]	inch (mm)

[1] Maximum signal routing length includes escape routing.

[2] Multi-board DMD routing length is more restricted due to the impact of the connector.

[3] Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

Table 7. High Speed PCB Signal Routing Matching Requirements[(1)][(2)][(3)][(4)]

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH**[(5)]	**UNIT**
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	inch (mm)
	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC3479 or the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single ended.
(5) Mismatch variance for a signal group is always with respect to reference signal.

4.3.5   Number of Layer Changes

•   Single-ended signals: Minimize the number of layer changes.

•   Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.

4.3.6   Stubs

•   Avoid stubs.

4.3.7   Terminations

•   No external termination resistors are required on DMD_HS differential signals.

•   The DMD_LS_CLK and DMD_LS_WDATA signal paths should include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.

•   The DMD_LS_RDATA signal path requires a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.

•   DMD_DEN_ARSTZ does not require a series resistor.

4.3.8   Routing Vias

•   Minimize the number of vias on DMD_HS signals and do not exceed two.

•   Locate any and all vias on DMD_HS signals as close to the ASIC as possible.

•   TMinimize the number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals and do not exceed

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two.

- Locate any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals as close to the ASIC as possible.

4.3.9 DLPA3005 Layout Guidelines

For switching power supplies, the layout is an important step in the design, especially when it concerns high peak currents and high switching frequencies. If the layout is not carefully designed, the regulator may show stability issues and/or EMI problems. Therefore, it is recommended to use wide and short traces for high-current paths and for their return power ground paths. For the DMD HV regulator, place the input capacitor, output capacitor, and the inductor as close as possible to the IC. In order to minimize ground noise coupling between different buck converters it is advised to separate their grounds and connect them together at a central point under the part. For the DMD HV regulator, the recommended value for the capacitors is 1 µF for VRST and VOFS, 470 nF for VBIAS. The inductor value is 10 µH.

The high currents of the buck converters concentrate around pins VIN, SWITCH and PGND (Figure 13). The voltage at the pins VIN, PGND and FB are DC voltages while the pin SWITCH has a switching voltage between VIN and PGND. In case the FET between pin 52 and pin 53 is closed, the red line indicates the current flow while the blue line indicates the current flow when the FET between pin 53 and pin 54 is closed.

These paths carry the highest currents and must be kept as short as possible.

For the LDO DMD, it is recommended to use a 1 µF, 16 V capacitor on the input and a 10 µF, 6.3 V capacitor on the output of the LDO assuming a battery voltage of 12 V.

For LDO bucks, it is recommended to use a 1 µF, 16 V capacitor on the input and a 1 µF, 6.3 V capacitor on the output of the LDO.
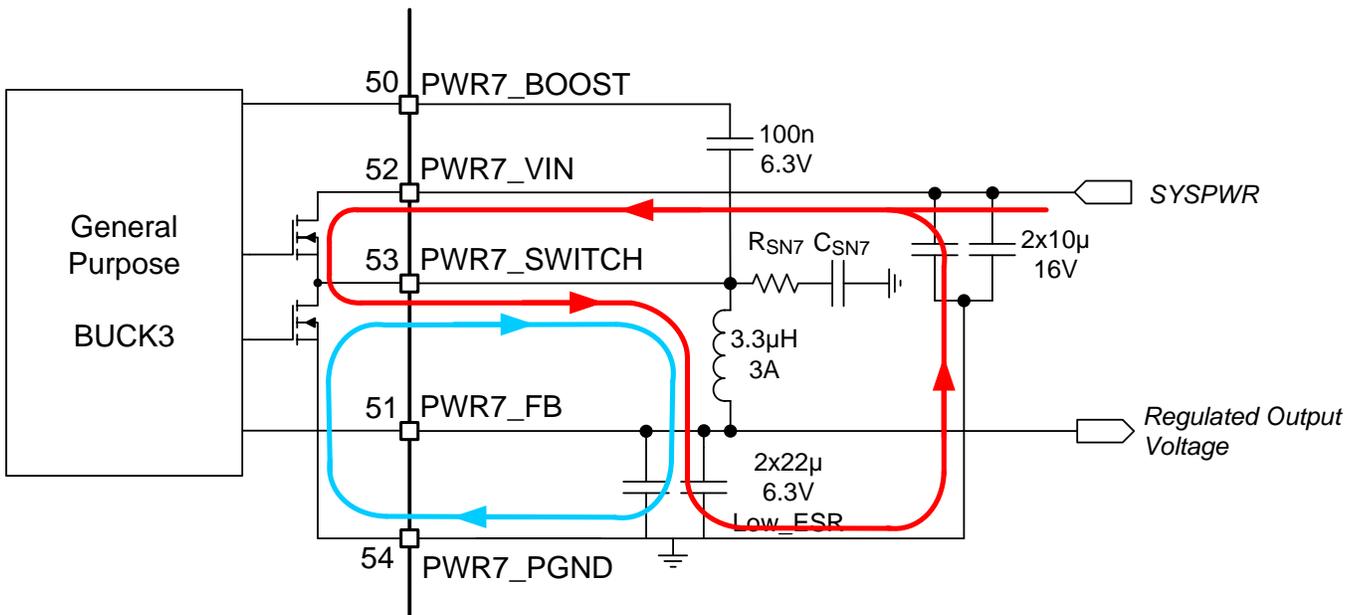
Figure 13. High AC Current Paths in a Buck Converter

The trace to the VIN pin carries high AC currents. Therefore ensure the trace is low resistive to prevent voltage drop across the trace. Place the decoupling capacitors as close to the VIN pin as possible.

The SWITCH pin is connected alternatingly to the VIN or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of VIN, and containing high frequencies. This high frequencies can lead to EMI problems if not properly designed. To reduce EMI problems, place a snubber network (R_{SN7} and C_{SN7}) at the SWITCH pin to prevent and/or suppress unwanted high-frequency ringing at the moment of switching.

The PGND pin sinks high current and is typically connected to a star ground point such that it does not interfere with other ground connections.

The FB pin is the sense connection for the regulated output voltage which is a DC voltage. No current flows through this pin. The voltage on the FB pin is compared with the internal reference voltage in order to control the loop. The FB connection should be made at the load such that I×R drop is not affecting the sensed voltage.

4.3.9.1   SPI Connections

The SPI interface consists of several digital lines and the SPI supply. If routing of the interface lines is not done properly, communication errors can occur. Prevent SPI lines from picking up noise and possibly interfering with sources by keeping them away from the interface.

Preven noise accumulation by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. Connect the SPI interface with a separate ground to the DGND of the DLPA3005 (Figure 14). This conenction design prevents ground noise between SPI ground references of DLPA3005 and the controller, due to the high current in the system.
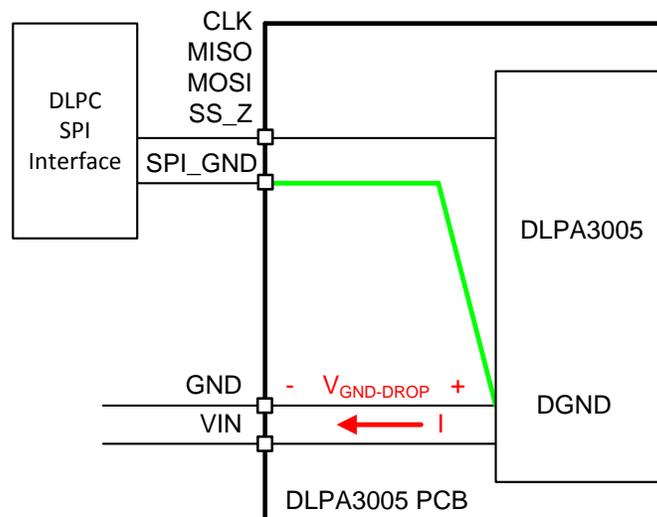
Figure 14. SPI Connections

Ensure that interfering sources are kept away from the interface lines as much as possible. It is especially important to route high current lines such as the neighboring PWR_7 pin correctly. If the PWR_7 pin is routed too close SPI_CLK pin for instance, it could lead to false clock pulses and thus communication errors.

4.3.9.2 R_{LIM} Routing

R_{LIM} senses the LED current. To accurately measure the LED current, connect the RLIM_K_1 and RLIM_K_2 lines close to the top-side of measurement resistor R_{LIM}. Connect RLIM_BOT_K_1 and RLIM_BOT_K_2 close to the bottom-side of R_{LIM}.

Because the switched LED current flows through R_{LIM} a low-ohmic ground connection for R_{LIM} is strongly advised.

4.3.9.3   LED Connection

The large currents that flow through the wiring from the external RGB switches to the LEDs switches require special attention to the LED connection. Two perspectives apply when wiring the LED-to-RGB switches.

• The resistance of the wiring, R_{series}
• The inductance of the wiring, L_{series}

The location of the parasitic series impedances are depicted in Figure 15.
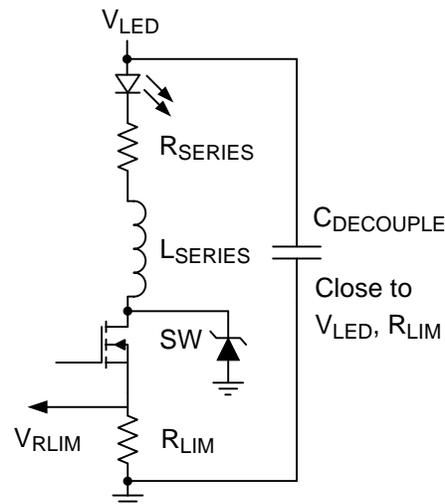
Figure 15. Parasitic Inductance (L$_{Series}$) and Resistance (R$_{series}$) in Series with LED

Currents up to 16 A can flow through the wires connecting the LEDs to the RGB switches. Noticeable dissipation can occur easily. Every 10 mΩ of series resistances implies results in a 16-A average LED current and a parasitic power dissipation of 2.5 W. This disipation may cause PCB heating, but more importantly, overall system efficiency is deteriorated.

Additionally, the resistance of the wiring can impact the control dynamics of the LED current. Be sure to consider routing resistance as a component of the LED current control loop. V$_{LED}$ controls the LED current . Equation 1 describes how for a small change in V$_{LED}$ (ΔV$_{LED}$) the resulting LED current variation (ΔI$_{LED}$) depends on the total differential resistance in that path.

$$\Delta I_{LED} = \frac{\Delta V_{LED}}{r_{LED} + R_{series} + R_{on\_SW\_Q3,Q4,Q5} + R_{LIM}}$$

where

- r$_{LED}$ is the differential resistance of the LED
- R$_{on\_SW\_Q3,Q4,Q5}$ the on resistance of the strobe decoder switch
- L$_{series}$ is ignored because realistic values are usually sufficiently low to cause any noticeable impact on the dynamics   (1)

All the comprising differential resistances are in the range of 12.5 mΩ to several 100's mΩ. Without paying special attention, a series resistance of 100 mΩ can easily be obtained. It is advised to maintain the series resistance sufficiently low (for example <10 mΩ).

The series inductance is important when considering the switched nature of the LED current. While cycling through R,G and B LEDs, the current through these branches turns-on and turns-off in short time duration. Specifically turning off is fast. A current of 16 A goes to 0 A in a matter of 50 ns. This drop implies a voltage spike of about 1 V for every 5 nH of parasitic inductance.

Minimize the series inductance of the LED wiring by:

- Short wires
- Thick wires and/or multiple parallel wires
- Small enclosed area of the forward and return current path

If the inductance cannot be made sufficiently low, use a Zener diode to clamp the drain voltage of the RGB switch so that it does not surpass the absolute maximum rating. Choose a clamping voltage value between the maximum expected V$_{LED}$ and the absolute maximum rating. Allow sufficient margin of the clamping voltage relative to the mentioned minimum and maximum voltage.

4.3.10 DMD Flex Cable Interface Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board-to-board connector to a flex cable. The flex cable provides the interface of data and Ctrl signals between the DLPC3479 controller and the DLP4710 DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer Figure 16.
- Place a minimum of two 220-nF decoupling capacitor close to VBIAS. Capacitor C3 and C10 in Figure 16.
- Place a minimum of two 220-nF decoupling capacitor close to VRST. Capacitor C1 and C9 in Figure 16.
- Place a minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C2 and C8 in Figure 16.
- Place a minimum of four 220-nF decoupling capacitor close to VDDI and VDD. Capacitor C4, C5, C6 and C7 in Figure 16.
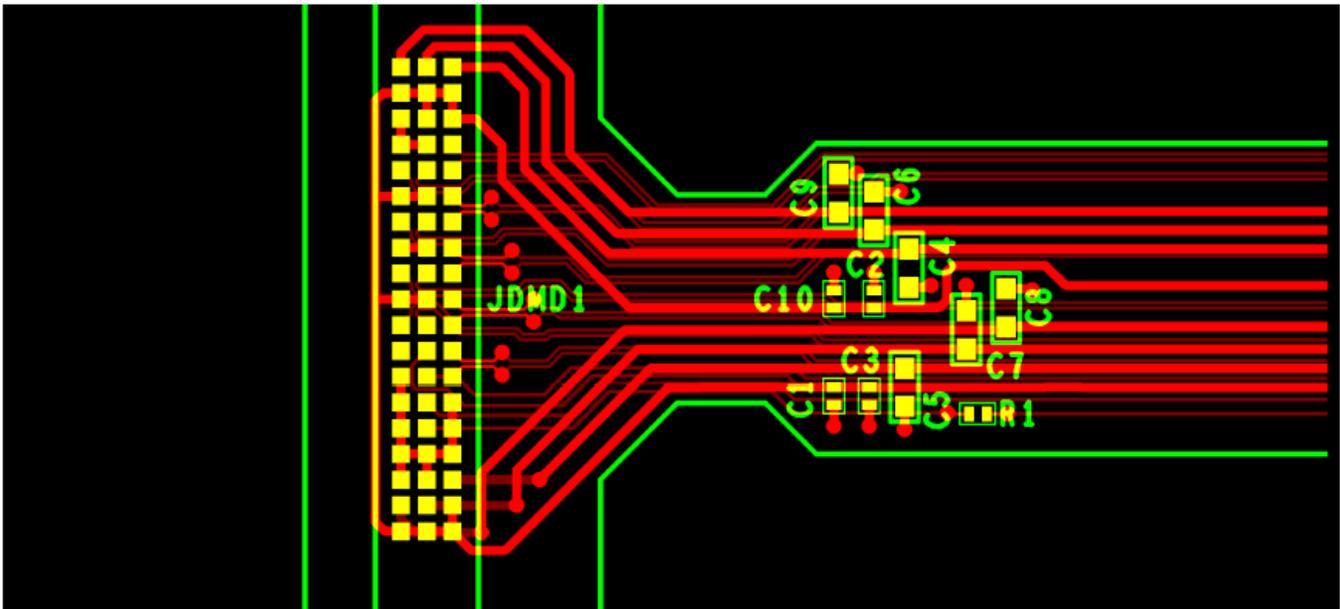
Figure 16. Power Supply Connections

4.4 Layout Prints

To download the layer plots, see the design files at TIDA-080005.

4.5 Cadence Project

To download the Cadence project files, see the design files at TIDA-080005..

4.6 Gerber Files

To download the Gerber files, see the design files at TIDA-080005..

4.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-080005..

5 Software Files

To download the software files, see the design files at TIDA-080005..

6 Related Documentation

1. Texas Instruments, *DLP4710 Light Control EVM User's Guide*
2. Texas Instruments, *DLPC3479 Display and Light Controller Data Sheet*
3. Texas Instruments, *DLP4710 (0.47 1080p DMD) Data Sheet*
4. Texas Instruments, *DLPA3005 PMIC and LED Driver IC Data Sheet*

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