Design Guide: TIDA-010057
Ultrasound Smart Probe Power Supply Reference Design

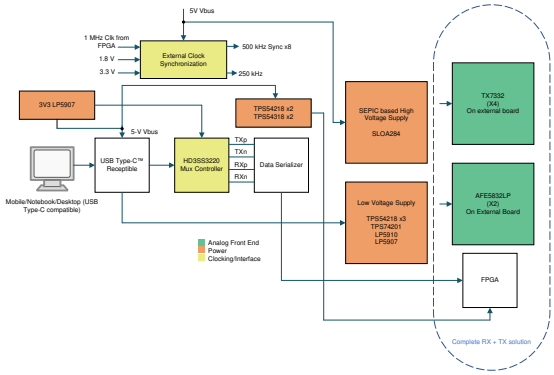
Description

Significant technological advancements and a high degree of integration in medical imaging, especially hand-held ultrasound smart probes, are pushing engineers to come up with highly efficient, noise-immune power systems in a small size. This reference design documents end-to-end power and data acquisition, for our high-performance 128-channel transmitter and 64-channel receiver design *(Highly Integrated Signal Chain Solutions TX7332 and AFE5832LP for Smart Ultrasound Probes)*. The power tree includes a single-stage transformer-less high-voltage generation (± 80 V and height <5mm) for transmit and the point-of-load low-voltage for the AFEs & FPGA from a 5 V USB Type-C™. This reference design enables low-noise (< 10mV ripple), efficient rails and better thermal performance (< 10°C temperature rise) achieving system efficiency – 80%, receive data SNR > 55dB and ultra-compact size (90mm by 45mm by 20mm). All power rails can be synchronized to an external clock using our integrated buffer-divider CDCE949. This design also supports 1-S battery input with a normal ultrasound operation of up to 2 hours.

Resources

TIDA-010057	Design Folder
HD3SS3220, TPS54218, LM3488, TPS61178	Product Folder
CDCE949, TPS7A39, TPS74201, LMZM23601	Product Folder
INA231 , LP5910, LP5907, LMV112	Product Folder

Ask our TI E2E™ support experts

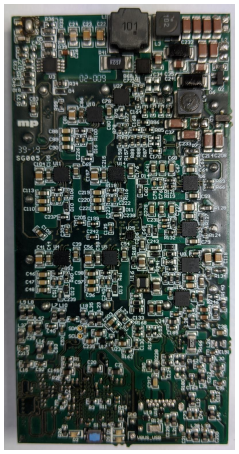


Features

- Transformer less dual rail high-voltage (±80 V @ 25 mA) generation from 5 V i USB Type-C™ in single stage implementation to meet component height requirement of < 5 mm
- Low ripple, low voltage supply for the front end and FPGA from a 5-V USB Type-C™ input
- Compact board size (less than 90mm by 45 mm by 20mm)
- End-to-end system efficiency – 80% running at full load
- Receive data SNR > 55 dB (Noise floor below –90 dB)
- EN/DISABLE supplies for power optimization and all rails can be synchronized to external clock
- Accurate real time power consumption measurement using high performance instrumentation amplifier INA231
- High-speed data acquisition over USB Type-C™ up to 4.2 Gbps

Applications

- Ultrasound Smart Probe

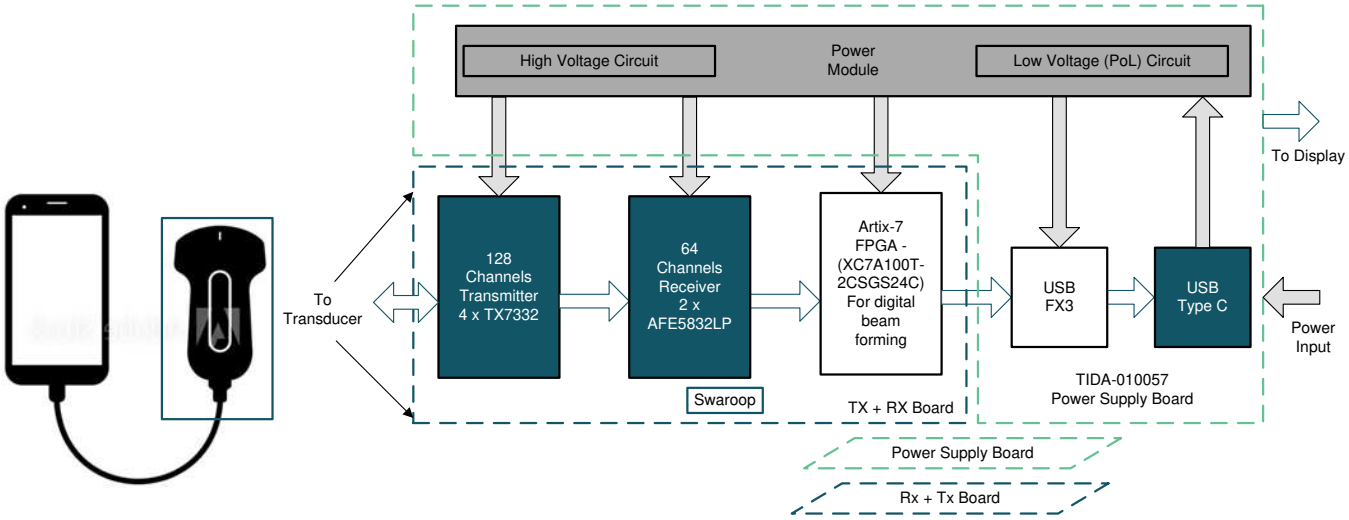


1 System Description

Ultrasound imaging is a widely used technique for diagnostic purpose. In addition to high-performance cart-based ultrasound systems, it is now possible to use a handheld device (smart probe) to accomplish high-quality ultrasound imaging. These smart probes leverage the power and resources of a mobile/tablet to process and display ultrasound images. A typical use case for these systems is to bring modern medical imaging technology to remote places, making the diagnostics faster and much more efficient. This small equipment is typically powered by battery (1S/2S), or from USB source. The data can be transferred over USB or Wi-Fi®.

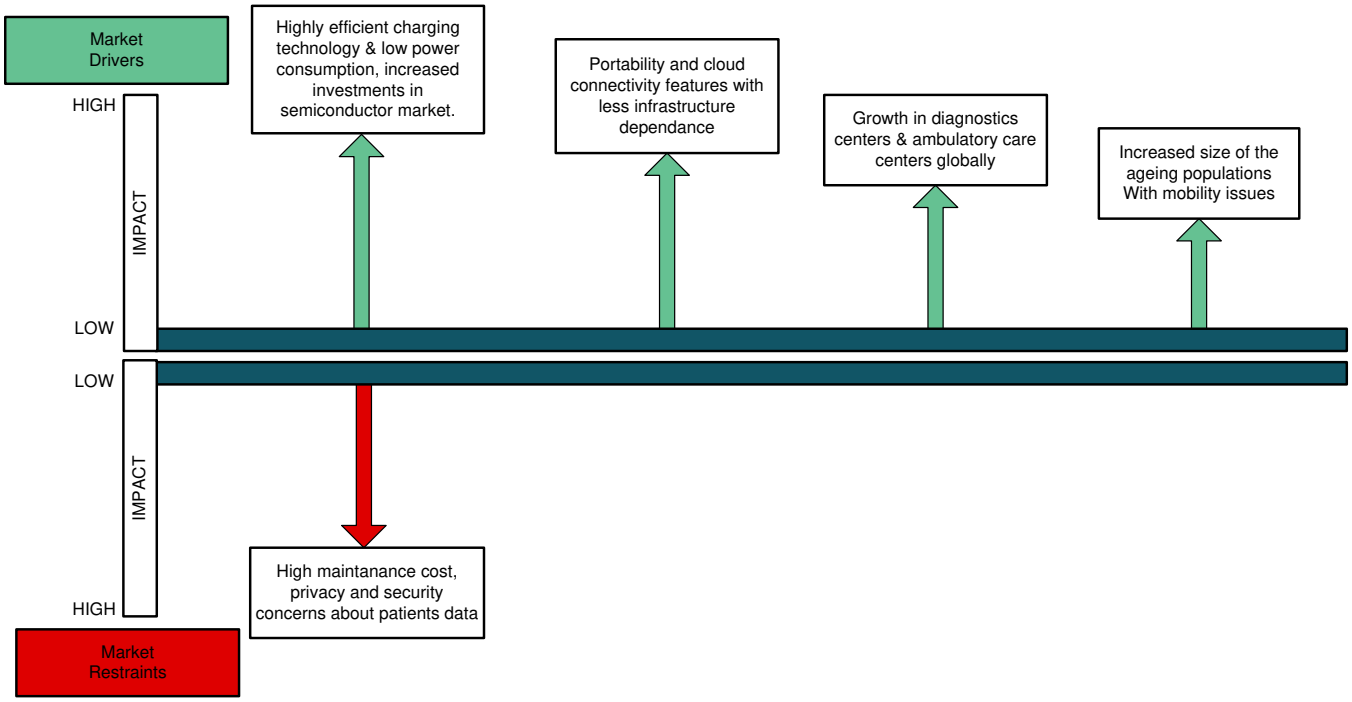
Figure 1 (left) shows a generic picture of such smart probe ultrasound scanner depicting a probe connected to a mobile device. Figure 1 (right) shows the block diagram of the smart probe, which includes transmit (TX) and receive (RX) analog front end (AFEs) for transmitting and receiving ultrasonic pulses and a FPGA to perform beam-forming. The whole setup is powered through the power supply board, consisting of DC-DC converters to generate point of load voltages, HV circuit for powering the transmit chip TX7332 (used in the design) and USB controller for data and power management.

Figure 1. Generic Smart Probe (left), System Block Diagram of Smart Probe Ultrasound Scanner (right)



One use case for these systems is to bring modern medical imaging technology to remote villages in developing countries for the first time. Smart ultrasound probes, or ultra-portable ultrasound systems, are the perfect fit for this task due to their cost-effectiveness. The day is fast approaching when most doctors will carry a smart probe unit in their pockets, similar to their stethoscope, by which they can not only hear, but also see inside the body—potentially leading to a market of a few million units worldwide within the next decade, complementing standard ultrasound systems. Figure 2 shows the factors that are the leading reasons for boom in Smart Probe market

Figure 2. Market Drivers and Restraints for Ultrasound Smart Probe



1.1 Key System Specifications

The Table 1 shows the complete system specifications of the power design of Smart Probe. The table is divided into two sections describing specifications of HV Circuit and LV Circuit.

Table 1. Key System Specifications

Parameter	Specifications	Details
System Input Voltage (V_{IN})	4.25V - 5.5V (USB Type-C)	Design supports 1S Battery input (3.3V-4.2V)
External Clock Synchronization	1MHz, 500 kHz & 250 kHz	Onboard buffer/divider is used to provide the sync clock from 1MHz source
High Voltage Circuit Specifications	Architecture: Single Ended Primary Inductance Converter (SEPIC)	
Positive Output Voltage (V_{OUT+})	Up to 80V	Symmetric positive and negative output. Can be set by external feedback resistors
Negative Output Voltage (V_{OUT-})	Up to -80V	
Output Current (I_{OUT})	up to 30mA per rail	
Total High Voltage Power (P_{HV})	2.4W + 2.4W	
Load Regulation	<2%	Load applied symmetrically on positive and negative rail
Voltage Accuracy	<1%	Voltage Accuracy: voltage difference between positive and negative rail across the load

Table 1. Key System Specifications (continued)

Parameter	Specifications	Details
Output Voltage Ripple	0.1% of the output voltage	
Switching frequency	250 kHz	
Transmit Low Voltage Supply (±5V) Specifications		
Switcher Output Voltage (positive)	5.7V	This Boost output can be fed as input to HV Supply or -5V supply to enable 1S operation.
LDO Output Voltage	5V	
Output Current	150 mA	Maximum LDO output current
Output Voltage Ripple	10 mV (V_{OUT} : 5.7V I_{OUT} : 1A)	
Switcher Output Voltage (negative)	-5.3V	Inverting Buck Topology
LDO Output Voltage	-5V	
Output Current	150 mA	
Output Voltage Ripple	10 mV (V_{OUT} : -5.3V I_{OUT} : 1A)	
Receive Low Voltage Supply Specifications		
AFE5832 Supply Rails with Low Noise LDOs	1.2V (300 mA maximum), 1.8V (1.5A maximum), 3.3V (250 mA maximum)	LP5910, TPS74201, LP5907 LDOs are used for respective rails followed after TPS54218 DC-DC Buck
Switcher Output Voltage	1.4 V, 2.0 V, 3.5 V	Low Dropout to maximize system efficiency
DC-DC Output Voltage Ripple (1.4 V)	8 mV	
LP5910 (1.2 V) PSRR (Output Ripple) at 500 kHz	-40 dB (80 µV)	
DC-DC Output Voltage Ripple (2.0 V)	8 mV	
TPS74201 (1.8 V) PSRR (Output Ripple) at 500 kHz	-50 dB (25.2 µV)	
DC-DC Output Voltage Ripple (3.5 V)	13 mV	
LP5910 (3.3 V) PSRR (Output Ripple) at 500 kHz	-40 dB (130 µV)	
FPGA & FX3 Supply Specifications		
Switcher Output Voltage	1 V (2 A maximum), 1.2 V (2 A maximum), 1.8 V(2 A maximum), 2.5 V (2 A maximum)	The inductance values are optimized for higher efficiency and load currents of 1A, 400 mA, 1A and 500 mA respectively
Maximum Output Voltage Ripple	15 mV	
System Power Measurement	Total Power; FPGA Power and TX Power	System current, voltage and power measurement of various subsystems using INA231

2 System Overview

There is a growing interest in a hand-held ultrasound system in order to help maximize the effectiveness of point-of-care support and diagnosis for patients . Traditionally, ultrasound systems are of a cart based type, which integrates a higher number of channels to achieve higher performance and superior image quality.

Ultrasound analog front ends and transmitter chips have achieved over 80% reductions in power and size. These advancements allow for higher channel integration and the lowest power possible, which is a must requirement for hand held portable probes since they are typically battery operated (1S/2S). Higher receiver and transmitter channel count in the system gives a better image resolution. Figure 3 show the image quality difference between a 16-CH, 32-CH and a 64-CH system. Because of the power and area limitation in portable ultrasound systems, most of systems in the market are able to integrate 16 or 32 channel receivers and transmitters. The high voltage MUX is used to excite 128 transducer elements; see Figure 4. Some of the limitations for the existing solution are a lower image quality because of only a 16 channel receiver and a lower frame rate because of higher imaging time due to limited number of channels. This reference design proposes a solution which contains a complete power solution for TI's high performance 128-Ch Tx/64-Ch Rx ultrasound smart probe solution (TX7332+AFE5832LP).

Figure 3. Image Resolution and Quality Across Channel Integration

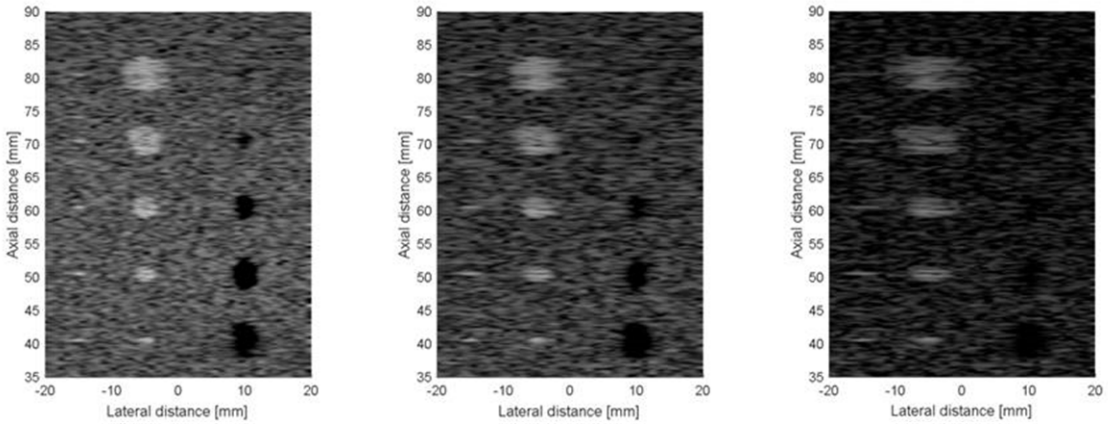
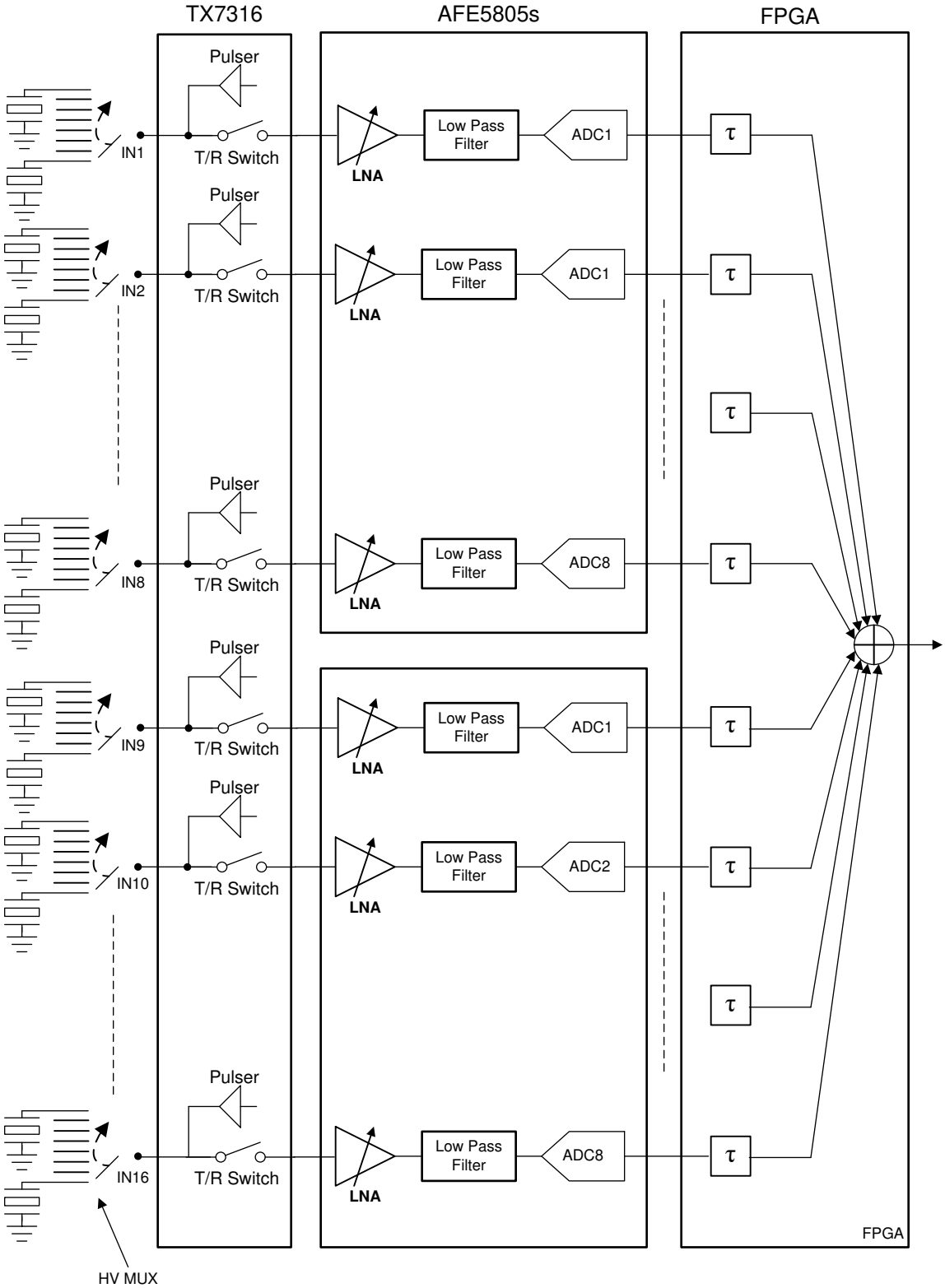


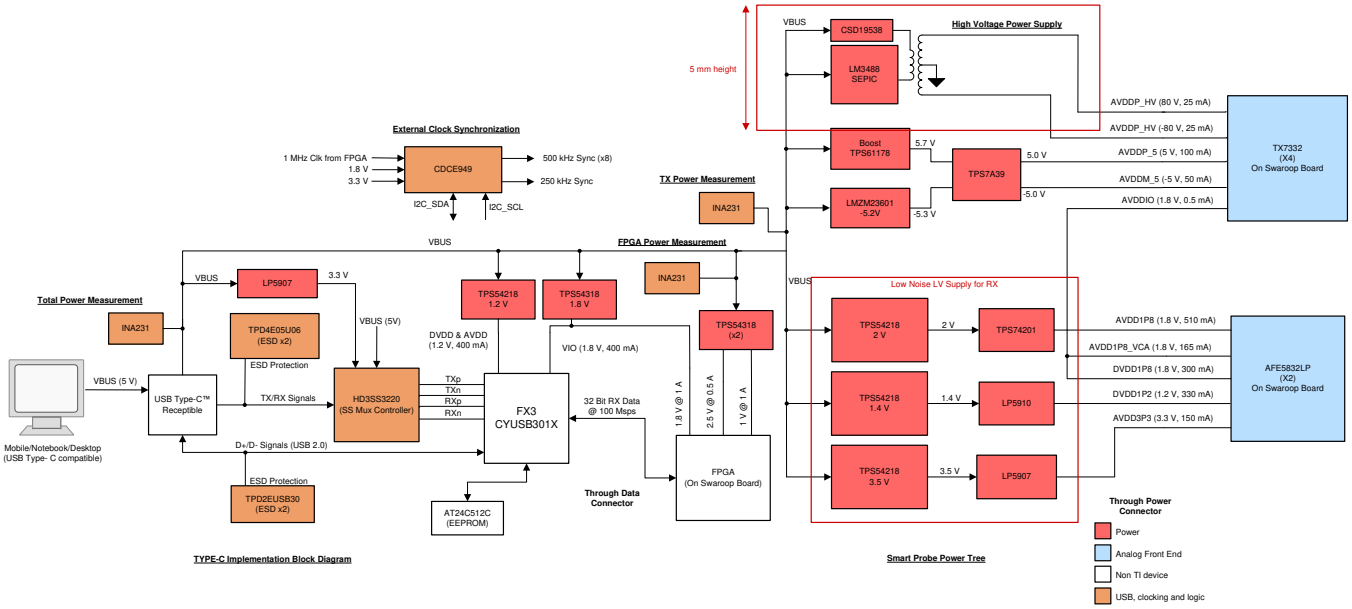
Figure 4. 16 Channel System



To achieve the target area, all the power supplies and USB Type-C interface are kept on another PCB which is vertically stacked to Rx + Tx board through connector. The other advantage of having power supplies and USB Type-C interface on separate PCB is that it increases isolation of switching noise from power supply and USB Type-C to sensitive receiver and transmitter devices. This power supply board generates a total of 11 different supplies (Including ±80 V) from USB Type-C 5 V with a capability of delivering maximum 15W peak power. It is usual practice to have a CDC or LMK to generate clock for the system. This approach leads to a higher power consumption and extra space on the board. In the proposed solution, to reduce power and board space, the FPGA itself is used to provide clock to all the chips. The power supply board requires 10 LVDS signals including clock and sync. Each LVDS buffer in the FPGA consumes ~39mW/ch which for all 10 LVDS buffers the total power is 390mW. In ultrasound systems the transmitter is active only for 1% of imaging duration. For rest of the duration, the receiver device receives the echo to form the full image. On the same concept, the transmitter device (TX7332) also kept active only for 1% duration which in order to reduce the clock power further, the LVDS signals going to TX7332 is programmed in tri-state mode for 99% duration. The LVDS buffer power in Tri-state mode is 11 mW/ch making the total power consumption of the clocking scheme 213mW. This is an improvement from a conventional clocking scheme power which is greater than 500mW.

2.1 Block Diagram

Figure 5. System Level Block Diagram of TIDA-010057



This design implements a full power tree solution that includes a single-stage transformer-less HV generation for transmit and the point-of-load LV for the AFEs and FPGA from a 5-V USB Type-C input. The entire implementation is divided into two sections, the high voltage power supply (SLOA284) and a low voltage supply. The system takes its input from a mobile phone, notebook, or desktop from a 5V USB Type-C. This 5V input is then used by different power management solutions used to power both the FPGA and the AFE5832LP and TX7332. In order to monitor the power consumption of various sub-systems in the design. For the low voltage supplies for both AFE5832LP and TX7332, each DC/DC converter is followed by an LDO to remove noise with a higher PSRR. Since the ultrasound smart probe is a noise sensitive design, the high PSRR is a key specification for an increase in image quality. The FPGA, USB controller, and clocking supply are powered by highly efffieint and low power solutions using the TPS54218 and the LP907. The FX3 device on the power supply board is programmed with USB Bulk Data Source Sink test to evaluate the speed of the data transfer The measured data speed is 4.2 Gbps which aligns with the expected value from the FX3 datasheet. Finally, there are INA231's to monitor the current of each power stage to ensure a higher performing operation.

2.2 Design Considerations

The power design for a hand-held ultrasound equipment is complex and has a lot of system level challenges associated with it. All these challenges comes primarily due to the small size of the complete solution. Achieving high efficiency in low power rails with fixed synchronize frequency operation is the key care about since losses in the form of heat will increase the temperature of the board. Typically there is no cooling mechanisms employed in the end equipment due to its compact portable nature. Following are the key design considerations in the smart probe power solution.

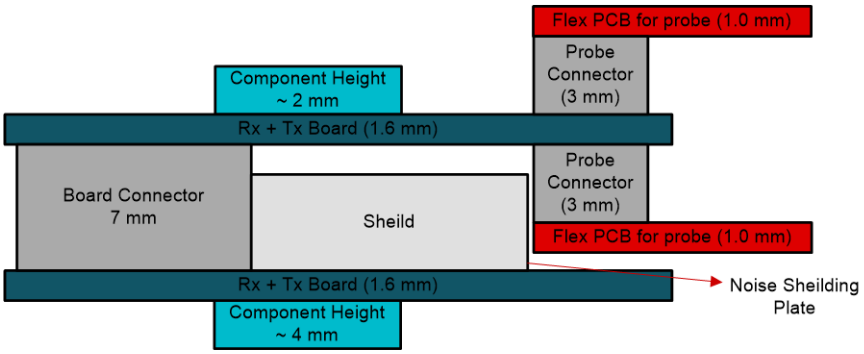
2.2.1 Small Compact Size

The size of the complete solution is kept in a hand-held form factor. The solution includes:

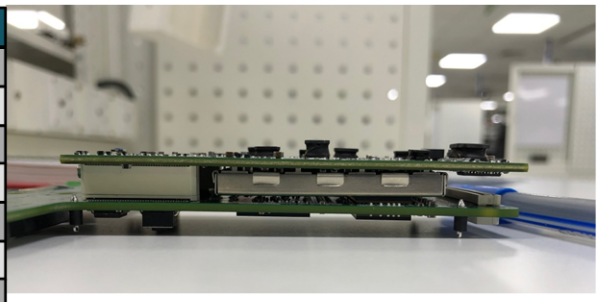
- The transmit circuit with transducers. The design employs 128-Ch transmit using TX7332, industry's first 32-Ch ultrasound transmitter
- 64-Ch receive using AFE5832LP
- High-performance FPGA for beam-forming
- High-voltage circuit for transmit power
- 9 independent low-voltage rails to deliver point of load power and USB and data capture section to power and transfer received data to the PC or tablet.

All of these sections are placed on a two-board assembly with TX, RX, and FPGA on one and the remainder is on the Power Board discussed in this design. Figure 6 shows the height distribution of complete system. The total height of the solution is <20 mm. Figure 6 also shows the corresponding real image of the implemented solution.

Figure 6. Total Height of the complete solution



Component	Height
Component height on bottom	4 mm
Power supply board	1.6 mm
Board to board connector	7 mm
Rx + Tx Board	1.6 mm
Probe connector	3 mm
Flex PCB for probe transducer	1 mm
Total board height	18.2 mm



2.2.2 Transformer less Solution

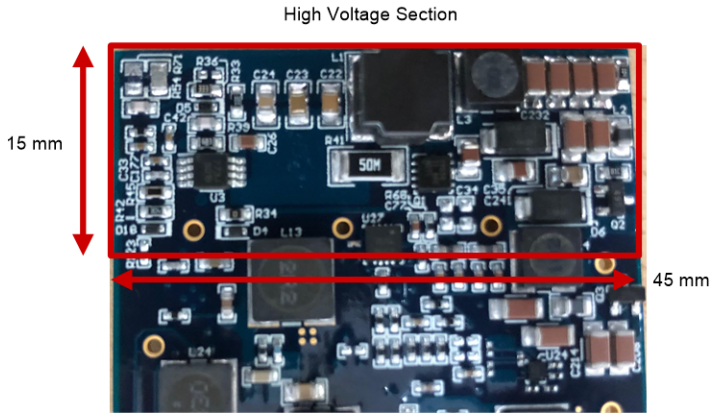
The design implements a transformer less power management solution to meet component height requirement of less than 5mm.Dual Rail HV (±80 V at 25 mA) generation from 5-V USB with single stage implementation and Point of Load (also supports 3.6-V battery input). Below are the key constraints in the design for power supply in smart probe ultrasound scanners:

- Efficiency > 80%
- Thermal performance (temperature rise <15 °C above ambient)

- SNR > 55dB (Noise floor below -90dB)
- HV Rail accuracy (between +ve and –ve HV lines) 1%
- Load regulation accuracy within 2%

Figure 7 shows the board image of the portion of high voltage circuit implemented in the design. The corresponding section is highlighted in red.

Figure 7. High-voltage Section Implemented in 45mm x 15mm x 4.3mm (complete circuit routed and placed on top layer)



2.3 Highlighted Products

2.3.1 TPD4E05U06 4-Channel Ultra-Low-Capacitance IEC ESD Protection Diode

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

2.3.2 TPD2EUSB30 2-Channel ESD Solution for SuperSpeed USB 3.0 Interface

The TPD2EUSB30 is a 2 channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode arrays. The TPDxEUSB30/A devices are rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Contact). These devices also offer 5 A (8/20 µs) peak pulse current ratings per IEC 61000-4-5 (Surge) specification.

2.3.3 2.3.3 HD3SS3220 10Gbps USB 3.1 USB Type-C™ 2:1 MUX With DRP Controller

The HD3SS3220 is a USB SuperSpeed (SS) 2:1 MUX with DRP port controller. The device provides Channel Configuration (CC) logic and 5V VCONN sourcing for ecosystems implementing USB Type-C. The HD3SS3220 can be configured as a Downstream Facing Port (DFP), Upstream Facing Port (UFP) or a Dual Role Port (DRP) making it ideal for any application.

2.3.4 TPS54218 2.95V to 6V Input, 2A Synchronous Step-Down SWIFT™ Converter

TheTPS54218 device is a full-featured, 6-V, 2-A, synchronous, step-down current-mode converter with two integrated MOSFETs. The TPS54218 device enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the device footprint with a small, 3 mm x 3 mm, thermally enhanced, QFN package.

2.3.5 TPS54318 2.95V to 6V Input, 3A Synchronous Step-Down SWIFT™ Converter

TheTPS54318 device is a full-featured, 6-V, 3-A, synchronous, step-down current-mode converter with two integrated MOSFETs. The TPS54318 device enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the device footprint with a small, 3 mm x 3 mm, thermally enhanced, QFN package.

2.3.6 CSD19538Q3A 100V, N ch NexFET MOSFET™, single SON3x3, 49mOhm

The CSD19538Q3A is a 100-V, 49-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize conduction losses and reduce board footprint in PoE applications.

2.3.7 LM3488 2.97V to 40V Wide Vin Low-Side N-Channel Controller for Switching Regulators

The LM3488 is a versatile low-side N-FET high-performance controller for switching regulators. This device is suitable for use in topologies requiring low-side FET, such as boost, flyback, or SEPIC. Moreover, the LM3488 can be operated at extremely high switching frequency to reduce the overall solution size. The switching frequency of LM3488 can be adjusted to any value from 100 kHz to 1 MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor. The LM3488 can also operate a 100% duty cycle.

2.3.8 TPS61178 20-V Fully Integrated Sync Boost with Load Disconnect

The TPS61178x family is a 20-V synchronous Boost converter with the gate driver built-in for load disconnect. The TPS61178x integrates two low on-resistance power FETs: A 16-mΩ switching FET and a 16-mΩ rectifier FET. The TPS61178x uses the fixed frequency peak current mode control with the slope compensation integrated. At the light load, the TPS61178 enters into the auto PFM mode while TPS611781 is in the forced PWM mode.

2.3.9 LMZM23601 36-V, 1-A Step-Down DC-DC Power Module in 3.8-mm × 3-mm Package

The LMZM23601 integrated-inductor power module is specifically designed for space-constrained industrial applications. It is available in two fixed output voltage options of 5-V and 3.3-V, and an adjustable (ADJ) output voltage option supporting a 1.2-V to 15-V range. The LMZM23601 has an input voltage range of 4-V to 36-V and can deliver up to 1000-mA of output current. This power module is extremely easy to use, requiring only 2 external components for a 5-V or 3.3-V output design. All aspects of the LMZM23601 are optimized for performance driven and low EMI industrial applications with space-constrained needs. An open-drain, Power-Good output provides a true indication of the system status and negates the requirement for an additional supervisory component, saving cost and board space. Seamless transition between PWM and PFM modes along with a no-load supply current of only 28 µA ensures high efficiency and superior transient response for the entire load-current range. For easy output current scaling the LMZM23601 is pin-to-pin compatible with the 500-mA output current capable LMZM23600.

2.3.10 TPS7A39 Dual, 150mA, Wide-Vin, Positive and Negative Low-Dropout (LDO) Voltage Regulator

The TPS7A39 device is a dual, monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150 mA of current. The regulated outputs can be independently and externally adjusted to symmetrical or asymmetrical voltages, making this device an ideal dual, bipolar power supply for signal conditioning.

2.3.11 TPS74201 Single-output 1.5-A LDO regulator, adjustable (0.8V to 3.3V), any or no cap, programmable soft start

The TPS742 series of low-dropout (LDO) linear regulators provide an easy-to-use, robust power-management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

2.3.12 LP5910 300-mA low-noise low-IQ low-dropout (LDO) linear regulator

The LP5910 is a low-noise LDO that can supply up to 300 mA of output current. Designed to meet the requirements of RF and analog circuits, this device provides low noise, high PSRR, low quiescent current, and superior line transient and load transient response. Using new innovative design techniques the LP5910 offers class-leading noise performance without a noise bypass capacitor and with the option for remote output capacitor placement.

2.3.13 LP5907 250-mA ultra-low-noise low-IQ low-dropout (LDO) linear

The LP5907 is a low-noise LDO that can supply up to 250 mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

2.3.14 INA231 28V, 16-bit, i2c output current/voltage/power monitor w/alert in wcsp

The INA231 is a current-shunt and power monitor with a 1.8-V compliant I2C interface that features 16 programmable addresses. The INA231 monitors both shunt voltage drops and bus supply voltage, providing increased protection by asserting the ALERT pin if the values are outside the programmed range. Programmable calibration value, conversion time, and averaging, combined with an internal multiplier, enable direct readouts of current in amperes and power in watts, thus reducing host processing.

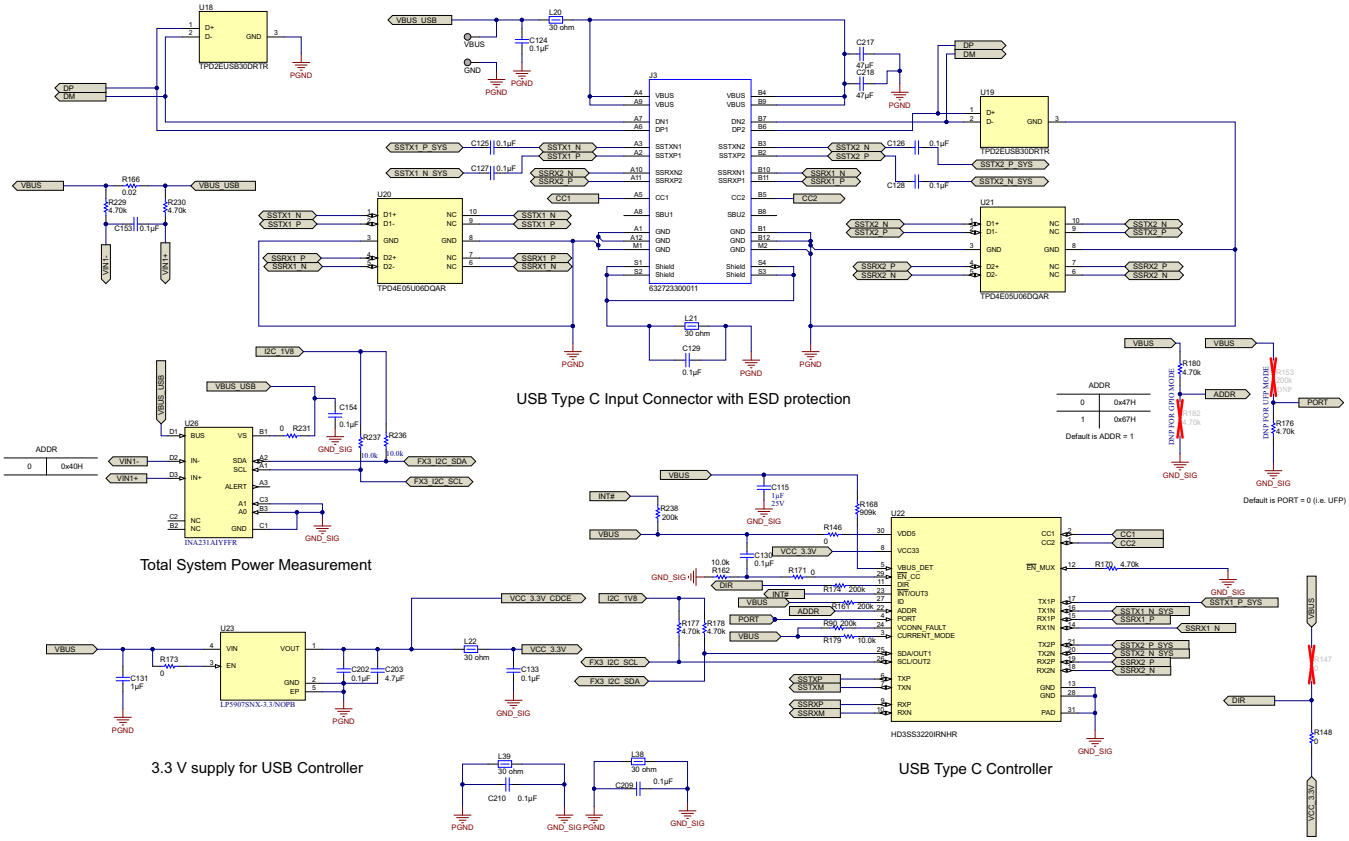
2.4 System Design Theory

This section describe the detailed implementation of each section of the power supply data communication implementation.

2.4.1 Input Section

The input section consists of USB Type-C connector for input voltage of 5V which is controlled by TIs HD3SS3220 port controller which is a USB SuperSpeed (SS) 2:1 mux with DRP port controller. The device provides Channel Configuration (CC) logic and 5V VCONN sourcing for ecosystems implementing USB Type-C. The input section is also provided by input power measurement setup which uses INA231 to continuously measure the current, USB bus voltage and real-time power consumption of the system.Figure 8shows the schematic of the implementation discussed previously.

Figure 8. Input Section of TIDA-010057



2.4.2 Designing of SEPIC based High Voltage Supply

2.4.2.1 Basic Operation Principle of SEPIC Converter

In a single ended primary inductance converter (SEPIC) design, the output voltage can be higher or lower than the input voltage. The SEPIC converter shown in Figure 9 uses two inductors: L1 and L2. The two inductors can be wound on the same core, or uncoupled since the same voltages are applied to them throughout the switching cycle.

Figure 9. SEPIC Converter Topology

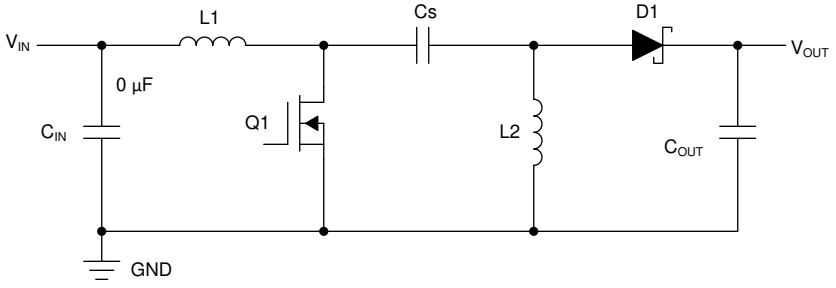
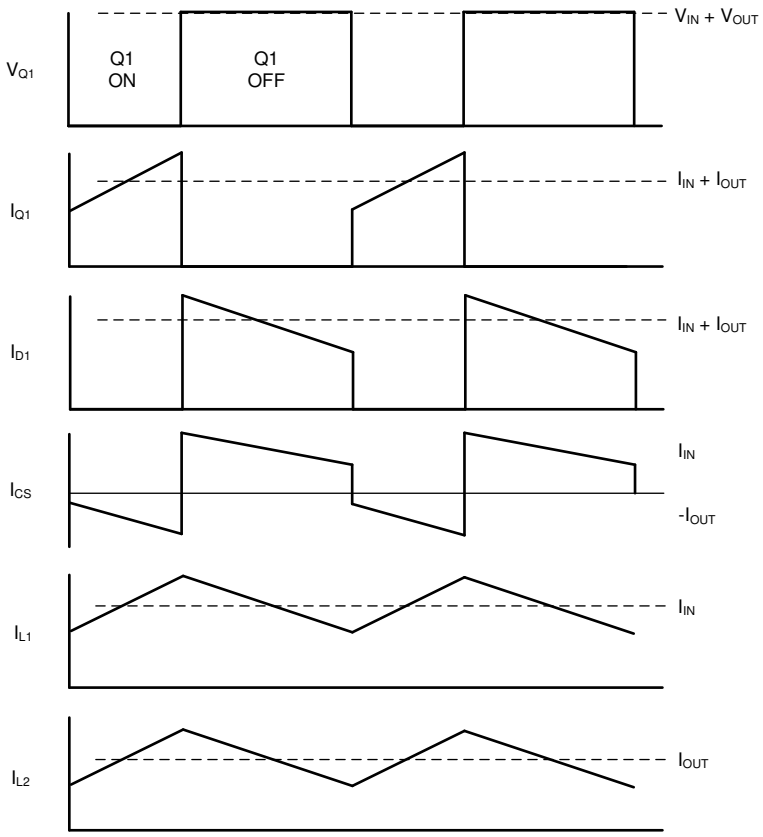


Figure 10. SEPIC Converter Switching Waveforms

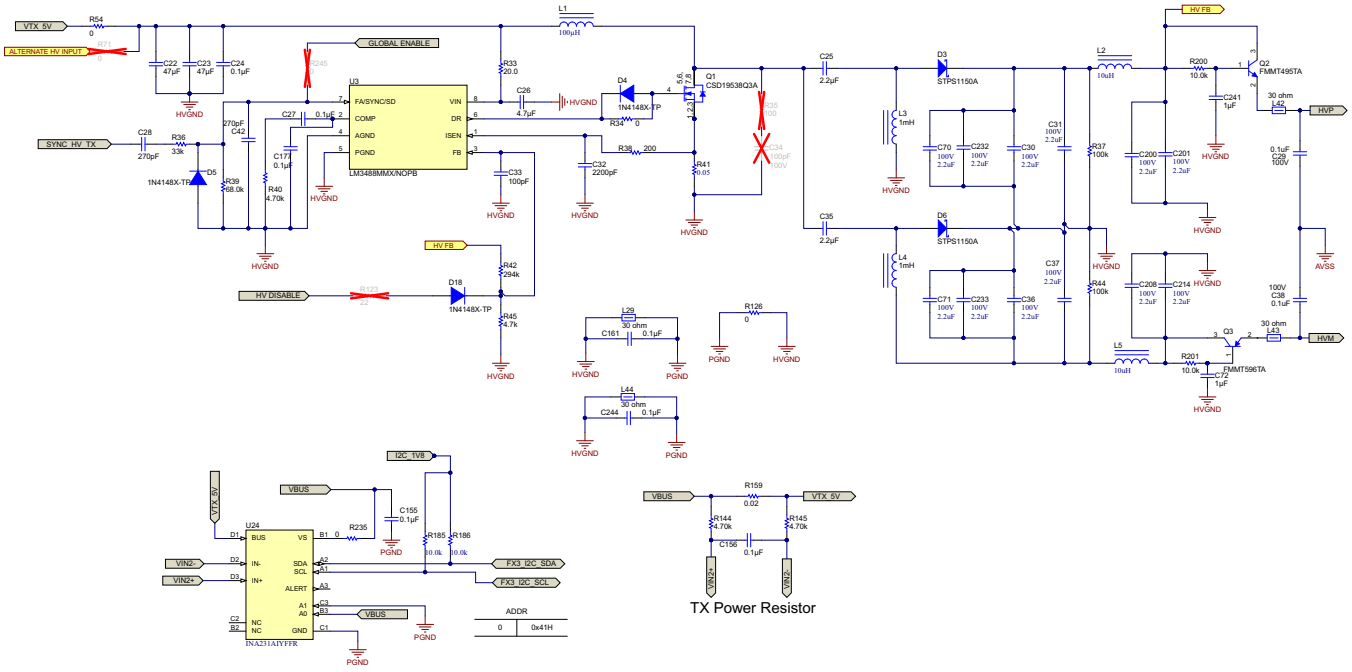


To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when Q1 is off and not switching. During steady-state CCM, pulse-width modulation (PWM) operation, and neglecting ripple voltage, capacitor Cs is charged to the input voltage, Vin. When Q1 is off, the voltage across L2 must be Vout. Since Cin is charged to Vin, the voltage across Q1 when Q1 is off is Vin + Vout, so the voltage across L1 is Vout. When Q1 is on, capacitor C, charged to Vin, is connected in parallel with L2, so the voltage across L2 is –Vin. The currents flowing through various circuit components are shown in Figure 6. When Q1 is on, energy is being stored in L1 from the input and in L2 from Cs. When Q1 turns off, L1's current continues to flow through Cs and D1, and into Cout and the load. Both Cout and Cs get recharged so that they can provide the load current and charge L2, respectively, when Q1 turns back on.

2.4.2.2 Design of Dual SEPIC Supply using uncoupled inductors

This section describes the implementation of the dual HV supply using uncoupled inductors. The specifications of the dual supply is described in Table 1.The sections below provide a step by step method to design the supply. This system can be thought of as two parallel output stages coupled through cap C25 & C35 with the primary side as shown in Figure 11. To create a high voltage dual supply, the output stage of the SEPIC had to be designed differently. As shown in Figure 11, the output capacitors are charged to the positive rail of 80 V for the top stage. Similarly, the output capacitors of the bottom stage are charged to a negative supply of -80 V. This is due to the inclusion of the HVGND shown below between R37 and R44. Using the HVGND. a dual supply SEPIC was achieved. Following the output of both rails, a Pi and Power Filter were used to attenuate the ripple of the high-voltage supply.

Figure 11. SEPIC Converter Schematic



2.4.2.3 Duty Cycle

For a SEPIC converter operating in a continuous conduction mode (CCM), the duty cycle is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D} \quad (1)$$

For the high voltage design used in this reference design, LM34888 can reach a duty cycle of 100%. Using Equation 1, the calculated duty cycle was 94.15%.

Vd is the forward voltage drop of the diode D1. The maximum duty cycle is:

$$D_{max} = \frac{V_{OUT} + V_D}{V_{IN(min)} + V_{OUT} + V_D} \quad (2)$$

2.4.2.4 Inductor Selection

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_L = I_{IN} \times 40\% = I_{OUT} \times \frac{V_{OUT}}{V_{IN(min)}} \times 40\% \quad (3)$$

The inductor values can be calculated by:

$$L1 > \frac{V_{IN(min)}^{\ 2} \times D}{R \times f_{sw} \times P_{out}} = 70.1\,\mu H \quad (4)$$

$$L2 > \frac{(1-D) \times V_{OUT}^{\ 2}}{R \times f_{sw} \times P_{out}} = 1020.8\,\mu H \quad (5)$$

The inductor value chosen for L1 was 100uH and 1000uH for L2 for easier component selection and availability.

The fsw is the switching frequency and Dmax is the duty cycle at the minimum Vin. The peak current in the inductor, to ensure the inductor does not saturate, is given by:

$$I_{L1(peak)} = I_{OUT} \times \frac{V_{OUT} + V_D}{V_{IN(min)}} \times \left(1 + \frac{40\%}{2}\right) \quad (6)$$

$$I_{L2(peak)} = I_{OUT} \times \left(1 + \frac{40\%}{2}\right) \quad (7)$$

2.4.2.5 Power MOSFET Selection

The parameters governing the selection of the MOSFET are the minimum threshold voltage Vth(min), the onresistance RDS(ON), gate-drain charge QGD, and the maximum drain to source voltage, VDS(max). Logic level or sublogic-level threshold MOSFETs should be used based on the gate drive voltage. The peak switch voltage is equal to Vin + Vout. The peak switch current is given by:

$$I_{Q1(peak)} = I_{L1(peak)} + I_{L2(peak)} \quad (8)$$

The RMS current through the switch is given by:

$$I_{Q1(rms)} = I_{OUT} \sqrt{\frac{\left(V_{OUT} + V_{IN(min)} + V_D\right) \times \left(V_{OUT} + V_D\right)}{V_{IN(min)}^2}} \quad (9)$$

The MOSFET power dissipation PQ1 is approximately:

$$P_{Q1} = I_{Q1(rms)}^2 \times R_{DS(ON)} \times \left(V_{OUT} + V_{IN(min)}\right) \times I_{Q1(peak)} \times \frac{Q_{GD} \times f_{SW}}{I_G} \quad (10)$$

PQ1, the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of Equation 10) and switching loss as shown in the second term. IG is the gate drive current. The RDS(ON) value should be selected at maximum operating junction temperature and is typically given in the MOSFET data sheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget. The MOSFET chosen was the CSD19538Q3A, with VDS MAX of100 V and a RDS, ON of 58 mΩ.

2.4.2.6 Output Diode Selection

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current IQ1(peak). The minimum peak reverse voltage the diode must withstand is:

$$V_{RD1} = V_{IN(max)} + V_{OUT(max)} = 85\ V \quad (11)$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended in order to minimize the efficiency loss.

2.4.2.7 Coupling Capacitor Selection

The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by:

$$I_{Cs(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN(min)}}} \quad (12)$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic capacitors work well for through-hole applications where the size is not limited and they can accommodate the required RMS current rating. The peak-to-peak ripple voltage on Cs (assuming no ESR):

$$\Delta V_{Cs} = \frac{I_{OUT} \times D_{max}}{C_s \times f_{sw}} = 0.042\ V \tag{13}$$

A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on Cs. Hence, the peak voltage is typically close to the input voltage.

2.4.2.8 Output Capacitor Selection

In a SEPIC converter, when the power switch Q1 is turned on, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor sees large ripple currents. Thus the selected output capacitor must be capable of handling the maximum RMS current. The RMS current in the output capacitor is: (14

The ESR, ESL, and the bulk capacitance of the output capacitor directly control the output ripple. Assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance. Hence,

$$E_{SR} \le \frac{V_{ripple} \times 0.5}{I_{L1(peak)} \times I_{L2(peak)}} \le 42\ m\Omega \tag{14}$$

$$C_{OUT} \ge \frac{I_{OUT} \times D}{V_{ripple} \times 0.5 \times f_{sw}} \ge 2.355\ \mu F \tag{15}$$

The output cap must meet the RMS current, ESR and capacitance requirements. In surface mount applications, tantalum, polymer electrolytic, and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

2.4.2.9 Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$I_{Cin(rms)} = \frac{\Delta I_L}{\sqrt{12}} = 0.18\ A \tag{16}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 μF or higher value, good quality capacitor would prevent impedance interactions with the input supply.

2.4.2.10 Programming the Output Voltage

The output voltage can be programmed using a resistor divider between the output and the feedback pins. he resistors are selected such that the voltage at the feedback pin is 1.26V. RF1 and RF2 can be selected using the equation,

A 100-pF capacitor may be connected between the feedback and ground pins to reduce noise.

Below are the calculations for the compensation:

$$f_{RHPZ} = \frac{\left(\left(1 - D_{max}\right)2 \times V_{OUT}\right)}{2\pi \times f_c \times 0.5 \times I_{OUT}} = 1.31\,kHz \tag{17}$$

$$f_R = \frac{1}{2\pi \times D_{max} \times \sqrt{L2 \times C_s}} = 3.35\ kHz \tag{18}$$

$$f_C = \frac{f_R}{6} = 219\ Hz \tag{19}$$

$$RC = \frac{\left(2\pi \times f_c \times C_{OUT} \times {V_{OUT}}^2 \left(1 + D_{max}\right)\right)}{\left(G_{CS} \times G_{MA} \times V_{REF} \times V_{IN(min)}\right) \times D_{max}} = 1.9\ k\Omega \tag{20}$$

$$CC1 = \frac{4}{2\pi \times f_c \times RC} = 1.5\ \mu F \quad (21)$$

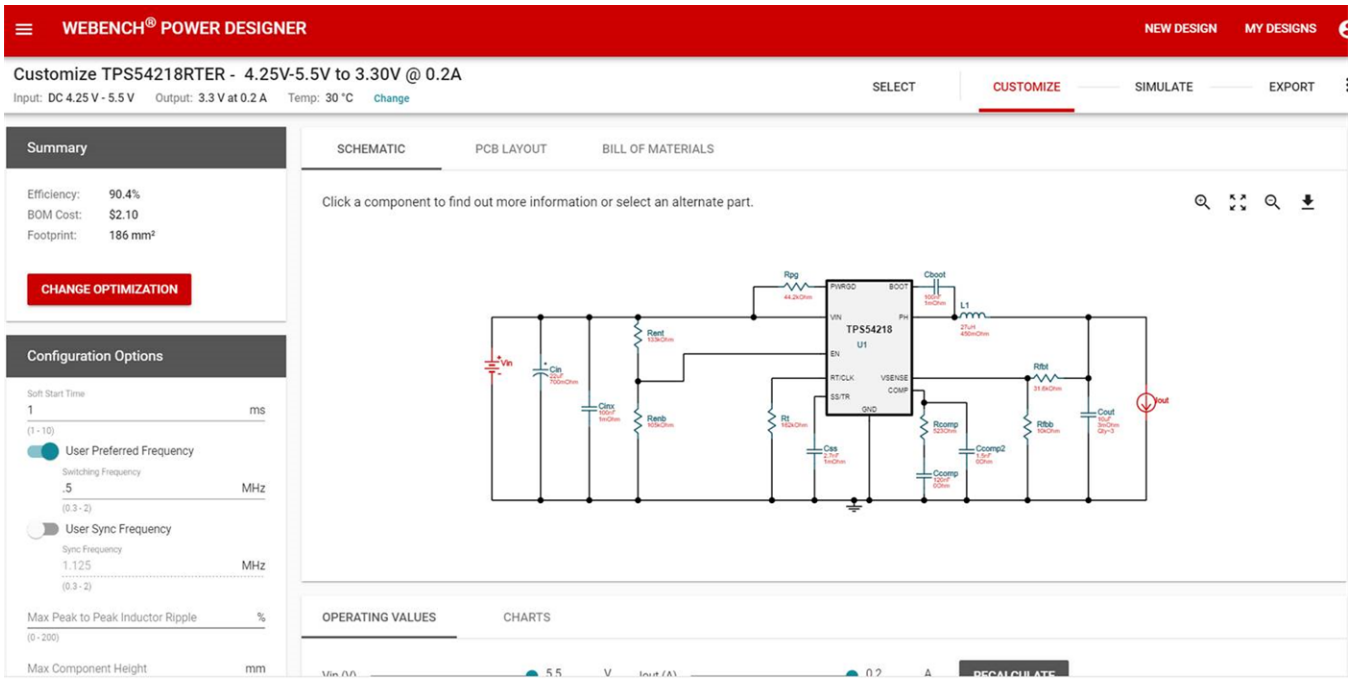
$$CC2 = \frac{\left(C_{OUT} \times ESR\right)}{RC} = 47.4\ \mu F \quad (22)$$

2.4.3 Designing the Low Voltage Power Supply

The different sub-systems such as transmit section, receive section, FPGA & data section in the design uses different power rails. Each with its own constraints such as analog supply, digital supply, low noise etc. The primary point of load is generated by using a switching buck converter followed by a LDO (for noise sensitive rails). Figure 11 shows the block level representation of the various low voltage rails and the architecture.

2.4.4 Designing the TPS54218 through Webench Power Designer

Figure 12. Webench Design Using the TPS54218



The Figure 12 shows a Webench design used to evaluate the TPS54218 with an output voltage of 3.3 V at 200mA. Webench Power Designer tool allows the user to simulate real time data for the product selected (efficiency, transient response, startup, etc.) and a capability to export Altium files to complete a board design.

For the ultrasound power supply design, the TPS54218 was selected to power the low voltage for the FPGA and the AFE5832LP. Since the size of the total solution was a concern, a module was considered. Comparing the difference between a power module and a dc/dc converter (internal inductor vs external inductor), the total system efficiency was evaluated. The DC/DC converter solution (TPS54218) allowed for more flexibility by increasing the inductor value, which led to an increase in efficiency (see Figure 14 in Power Measurement section).

When comparing how different inductor values effect the efficiency of a buck converter, the TPS54218 was evaluated with two different inductor values. In Figure 13, the TPS54218 efficiency was tested for two different inductor values (2.2uH vs 33uH) using a load generator. For light load conditions, the 33uH inductor had a much higher efficiency when compared to the 2.2uH solution. This is due to the AC conduction losses of the inductor which decrease the efficiency of the solution. Moving forward for the the low voltage power supply design, a 33uH inductor was chosen to improve the efficiency.

Figure 13. TPS54218 Efficiency (2.2uH vs 33uH)

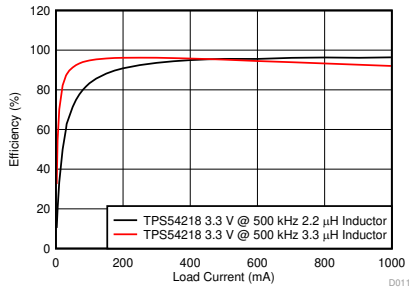


Figure 14. TPS54218 2V Supply Output Voltage Ripple

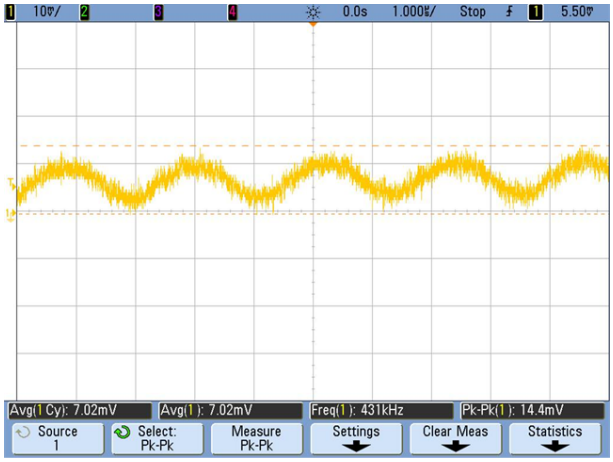


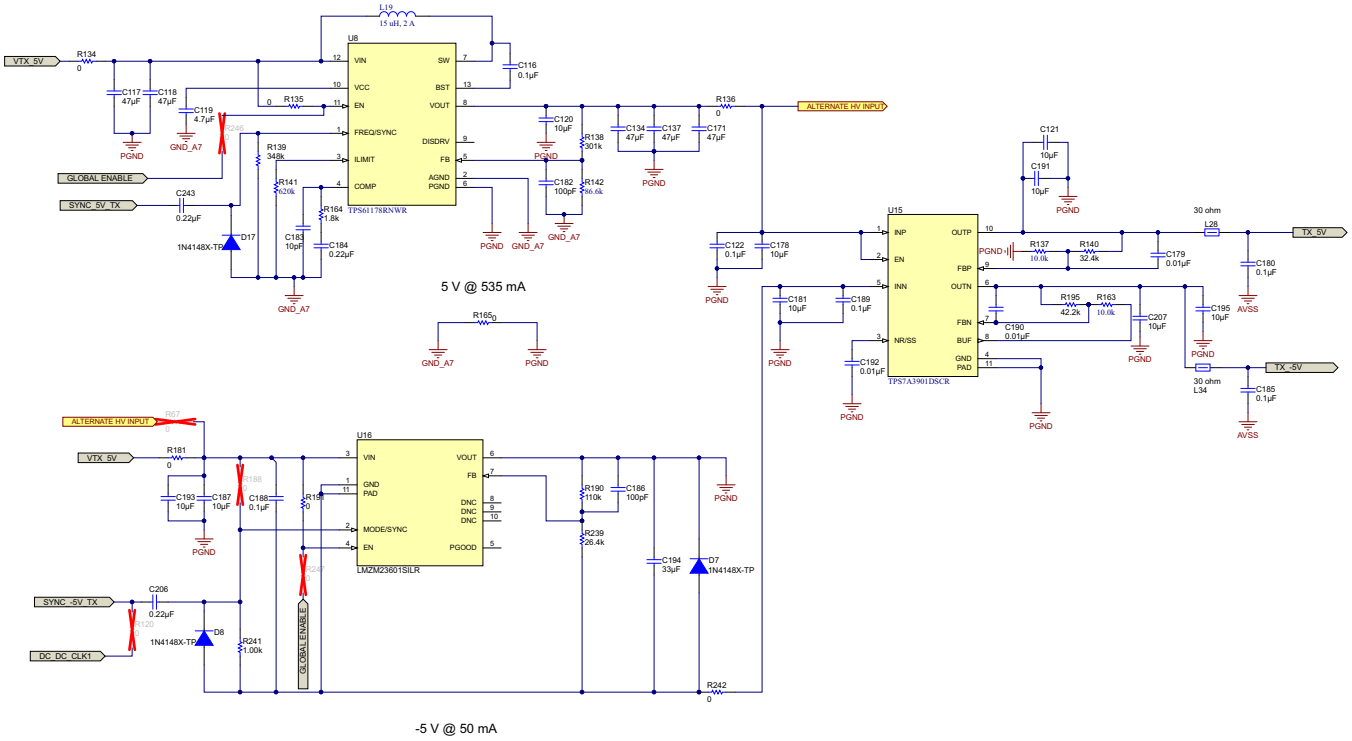
Figure 14 shows the 2 V supply output voltage ripple of the TPS54218. The measured Pk-Pk ripple was measured at 14.4mV. The remaining low voltage power supplies all had an output voltage ripple of less than 10m V.

2.4.5 ± 5V Transmit Supply Generation

Figure 15 shows the schematic of the implementation of transmit ±5 V rail. The boost device TPS61178 boosts the USB voltage(4.25 V-5.5 V) to 5.7 V and LMZM23601 device which is set up in inverting buck mode generates -5.3 V. Both the positive and the negative outputs are fed to dual low noise TPS7A39 LDO to generate ±5 V @ maximum 150 mA per rail.

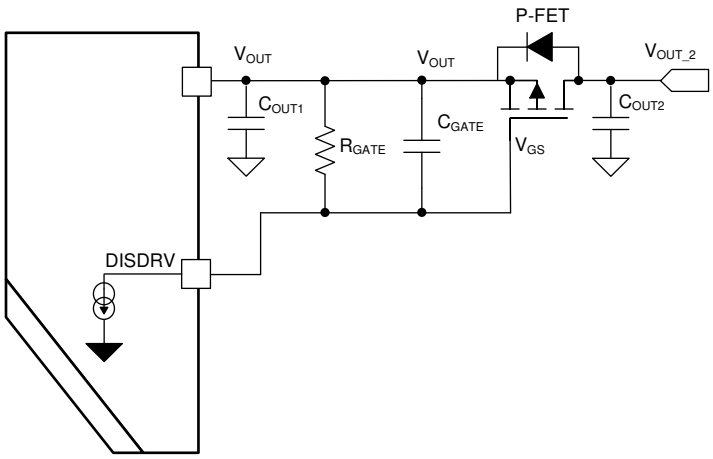
The device TPS61178 is also useful in the situation where high voltage requirement is high in the system say 100 V, or the system is power using 3.6 V (1S battery) source. This stage can be used as an intermediate input to the high-voltage circuit. This can be enabled by setting the required output voltage using the resistor divider (R138 and R142). Then removing R54 to disable existing USB input to HV circuit and placing R71, 0 ohm resistor as the input.

Figure 15. Schematic of the ±5V Transmit Circuit



The device TPS61178 also has a feature of true load disconnect (not implemented in the existing design). Placing an external P-FET between the output and the point of load, the device has a pin called DISDRV which can be used to turn off the FET in case of any short conditions. This feature is particularly useful when using an intermediate boost stage to power the high voltage circuit. The input to the high voltage circuit can be completely cut-off in case of any output short happens resulting in protection of the circuitry. The user can implement the same in their design providing a more robust system.Figure 16 shows the implementation of the load disconnect in TPS61178. For detailed information on the FET selection and other aspects, please refer to the Application and Implementation section of the device datasheet.

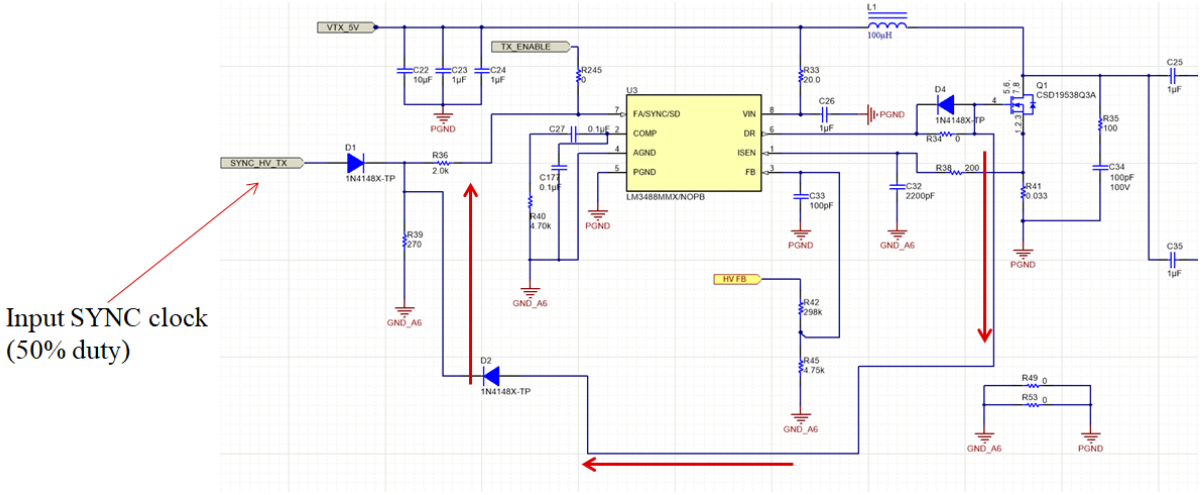
Figure 16. The Load Disconnect FET Connected in TPS61178



2.4.6 System Clock Synchronization

The schematic shown in Figure 11 can be synchronized to an external clock signal only if the duty cycle of the latter is larger than the duty cycle of the controller itself (larger than 93%). This design can be synchronized to an external clock with 50% Duty cycle by implementing the solution shown in Figure 17. The various point of load supplies can be synchronized to external clock which is available on the power connector discussed in section Power and data output connector. The signal from clock source pin DC_DC_CLK_1 is further is divided and distributed to respective supplies supplies and their switching frequencies. Figure 17 shows schematic of the implementation. The source clock is first buffered through LMV112SD and then one output is fed to -5.3V rail at 1 MHz (SYNC -5V_TX) and another one is given as an input to 9Ch-integrated clock buffer and divider device CDCE949. The 8 outputs are 500kHz for the seven TPS54218 buck devices and one TPS61178 for 5V rail, the 9th output is 250kHz for the HV circuit. The configuration of the device CDCE949 can be stored in the integrated EEPROM CDCEL9XXPROGEVM or over I2C. If CDCEL9XXPROGEVM is used, the configuration file can be found in the design files.

Figure 17. Schematic of External Clock Synchronization Implementation



The high voltage circuit can be synchronized to an external clock with 50% duty cycle. The controller LM3488 imposes a limit on the duty cycle clock pulse width to be larger than the duty cycle of the supply which is very high in the current implementation. The schematic shown in Figure 17 depicts the implementation. Two diodes forming an OR-ing system are introduced. One diode is placed from the gate drive pin to the sync pin. The other one comes from the input clock signal. The resistor R36 and R39 are series SYNC resistor and discharge resistor, respectively. If DR_pin is more positive than SYNC_HV_TX, then D1 will be reverse-biased and the SYNC-PIN will be driven high from D2. If DR_pin is less positive than SYNC_HV_TX, then D2 will be reverse-biased and SYNC_PIN will be driven High from D1. Test results are shown in Figure 18 and Figure 19 at the case of no load and full load.

Figure 18. Synchronization at No Load With 50% Duty Cycle Clock

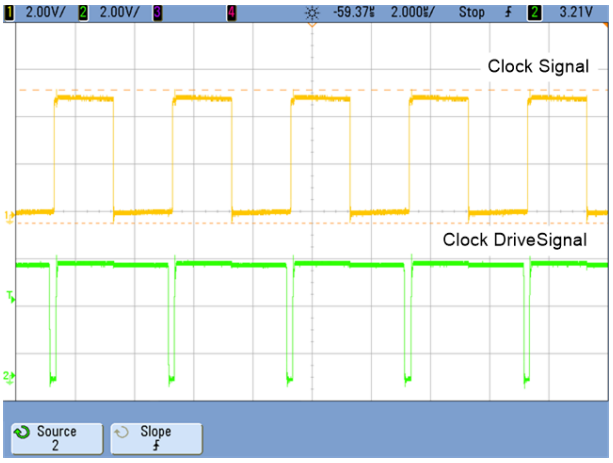
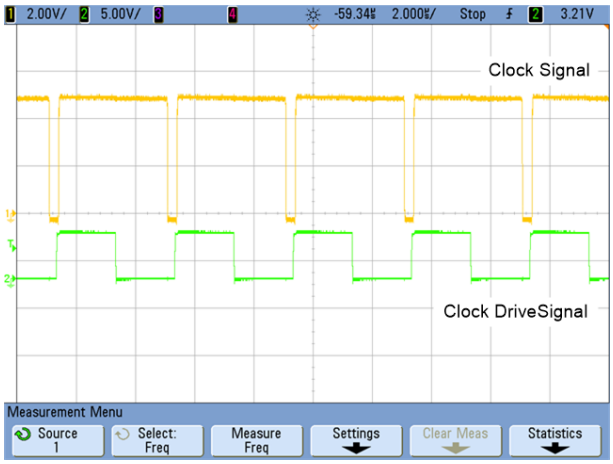


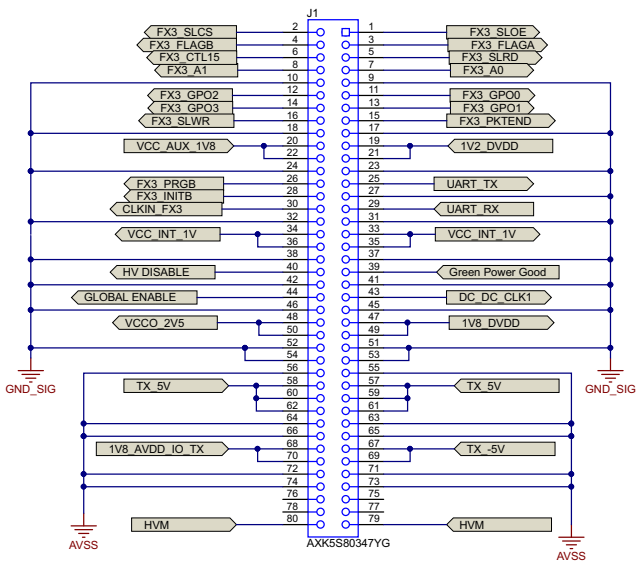
Figure 19. Synchronization at Full Load With 50% Duty Cycle Clock



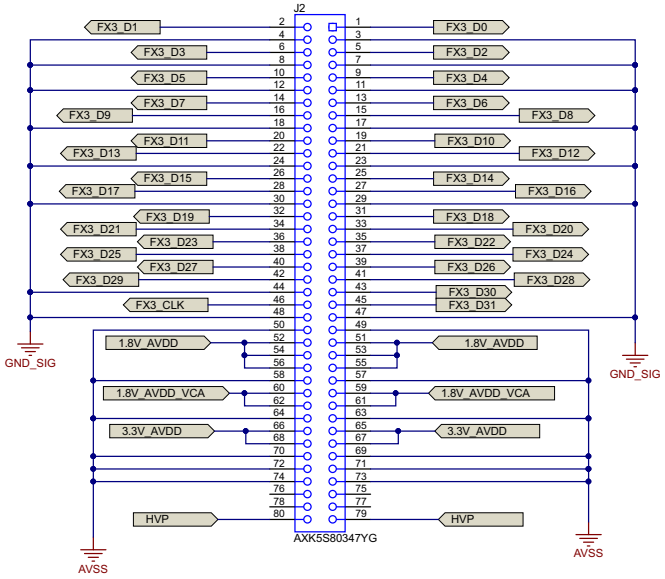
2.4.7 Power and data output connector

Figure 20 shows the schematic of the data and power connector placed on the board. 2 set of connectors are placed on the board to connect to the TX+RX AFE Board. Multiple signals are also coming from the FPGA to communicate with the FX3 device. A clock signal named DC_DC_CLK 1 of 1MHz frequency is coming from the FPGA to be the source clock for the power supply clock synchronization. 32 bit data line are also coming from the FPGA to the data serializer device FX3. Different Power rails are distributed among the connectors for ease of layout and keeping the routing length short. The High voltage rails are put separately on two connector ensuring equal lengths and separation. They are routed along the edge of the board too to keep it away from sensitive circuitry. The connector used is Panasonic's AXK5S80347YG.

Figure 20. Schematic of the connector between TIDA-010057 and TX+RX AFE board



Input Power Connector



Input Data Connector

2.4.8 System Current and Power Monitoring

The TIDA-010057 reference design provides a provision for users to monitor system current, bus-voltage, and power consumption. TI's INA231 28V, 16-bit, I^{2}C output current/voltage/power monitor is used to monitor various sections of the design. The Fig. 1 shows the circuit schematic in which the INA231 ICs are indicated in red boxes. Three INAs are implemented in the schematic. One INA measures the total current and power consumed in the system. The other two INAs will monitor the current and powers of Transmitter (Tx) and FPGA units respectively.

Figure 21. Block Diagram of the Power Poard Highlighting the Power Measurements Block

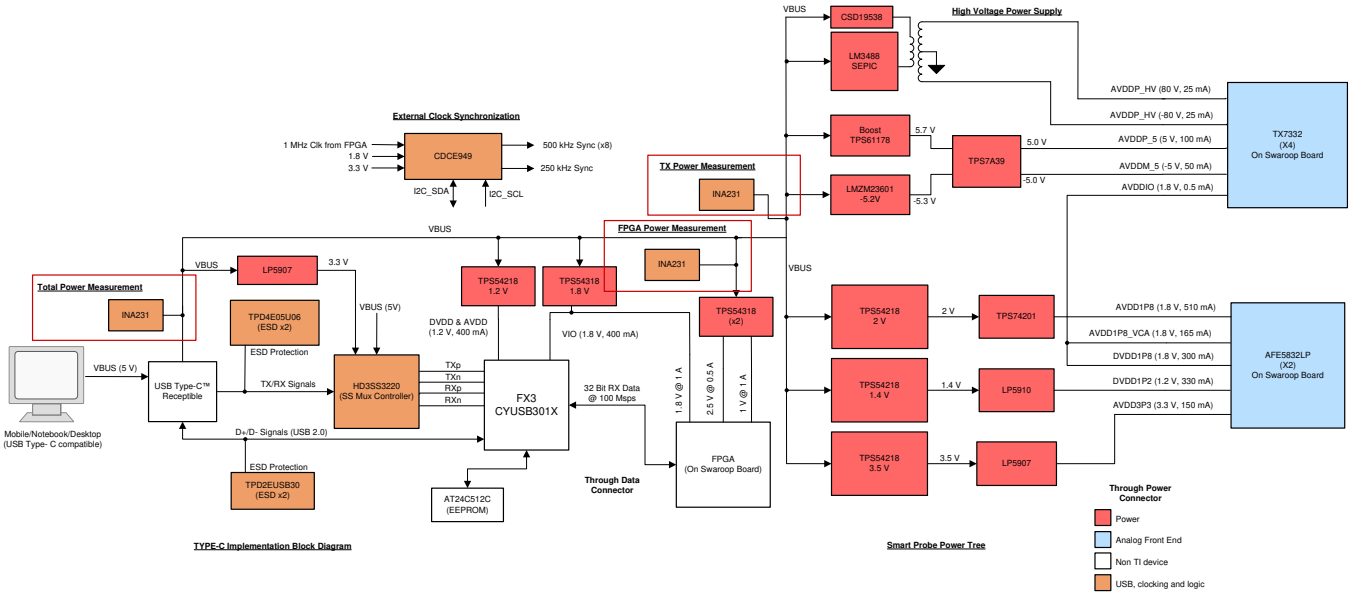
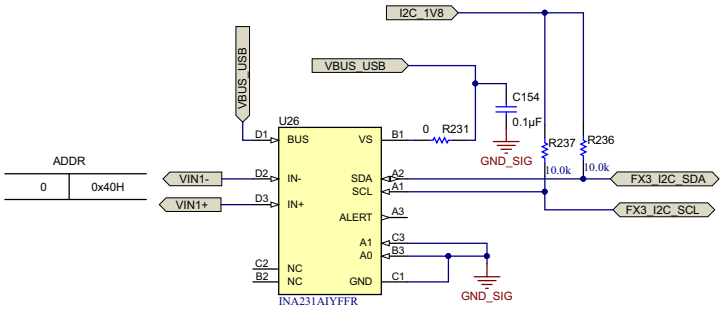


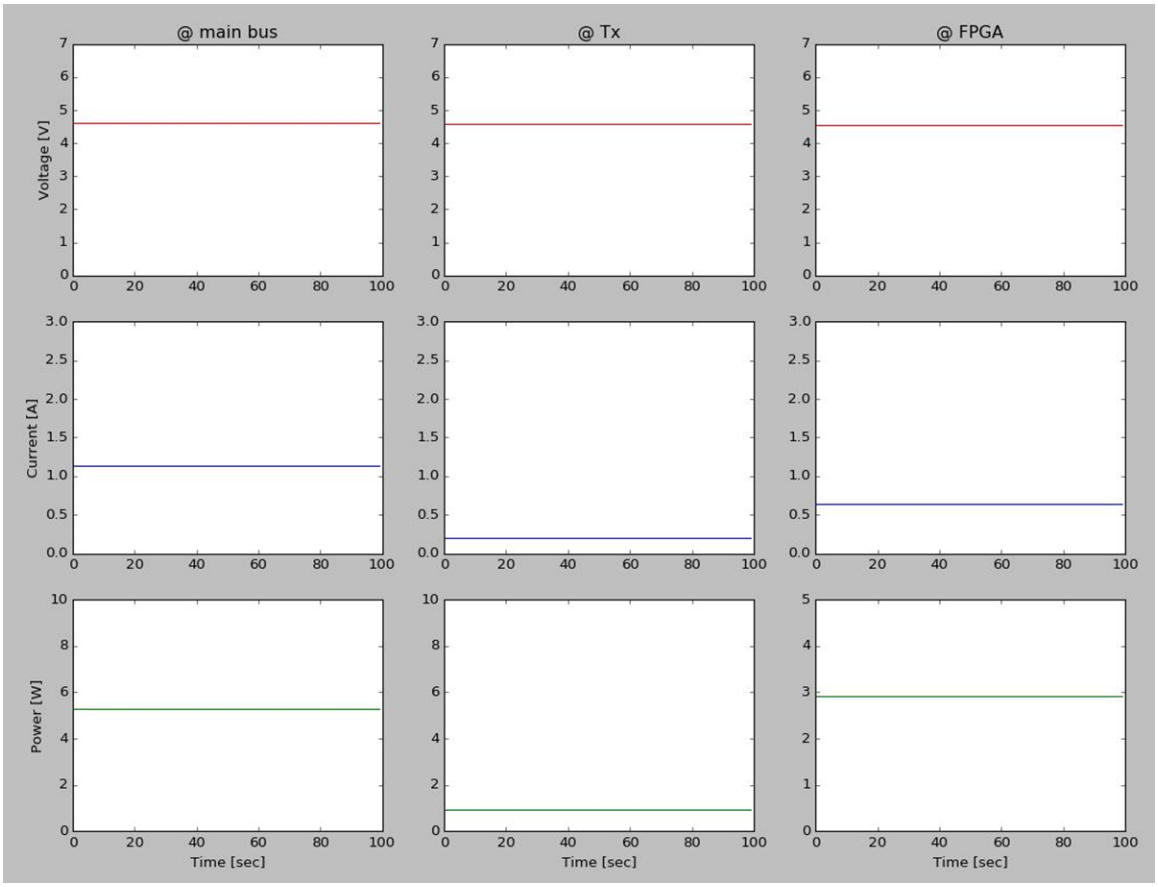
Figure 22. Schematic of the Power Measurement Section Implemented Using INA231



Total System Power Measurement

The communication is done through the I^{2}C interface. FX3 module (FX3 CYUSB8301x) in the power board is configured as the master and the INAs are configured as slaves. The measured voltage, current and power values can be dynamically plotted against time as shown in Figure 23. The described figure is generated using python by capturing the data sent by FX3. The same data is available in the latest version on AFEs FX3 code **Slavefifosync.img**.

Figure 23. Sample Plot of Measured Values Against Time



3 Hardware, Software, Testing Requirements, and Test Results

3.1 Testing and Results

The following section shows the test results of this reference design. During the measurement, the power source can be electronic power supply.

3.1.1 Test Setup

Figure 24 shows the front and back images of the TIDA-010057 board. The EMI shield placed between the AFE and TIDA-010057 board will provide EMI reduction. The 2 connectors dock into the TX + RX board and the USB Type-C connector connects it to the PC or tablet. The TIDA-10057 reference design has been evaluated and characterized by using two boards. The first board is a passive connector board which docks on to the power board. The adapter board has connectors placed around it to connect to load when needed. Figure 25 and Figure 26 shows the top and bottom of the adapter board. Various signals are also taken out to pins as well to connect to MCU for I^2C communication, providing clock for synchronization and so on.

Figure 24. Front (left) and back (right) images of the TIDA-010057 board

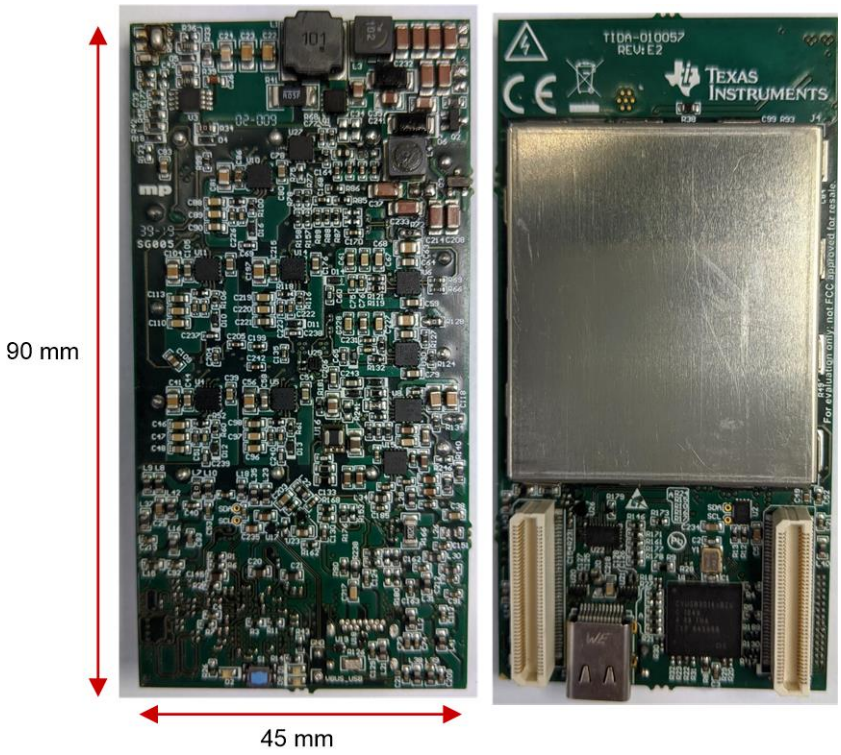


Figure 25. Passive Adapter Board – Front Load Connector Side

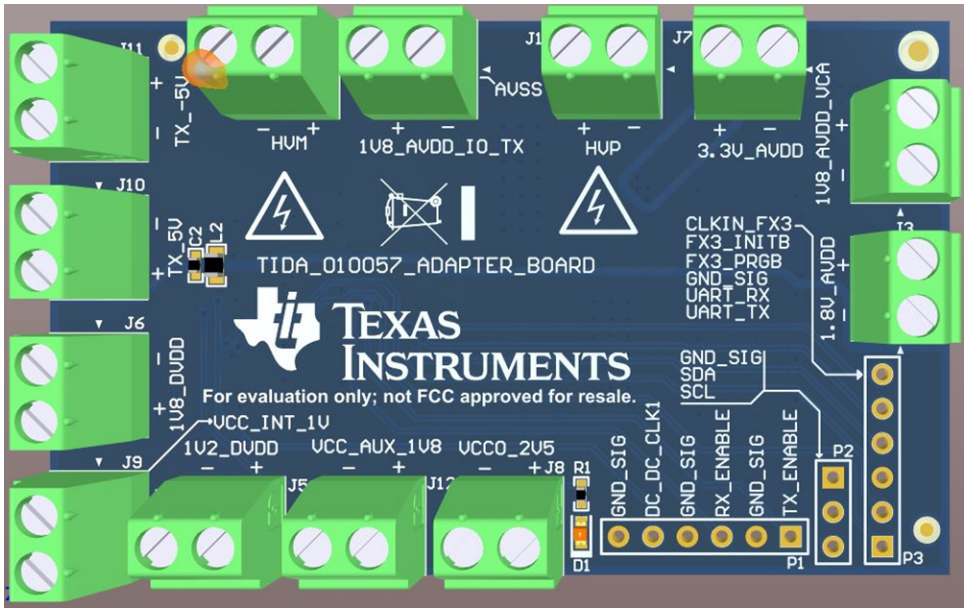
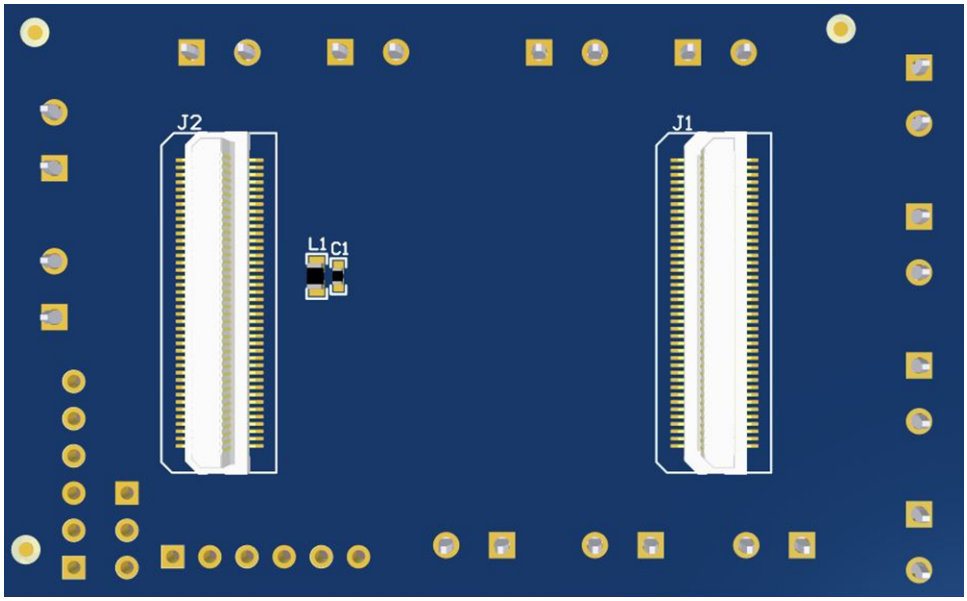


Figure 26. Passive Adapter Board – Back Docking Connector Side



The second board used for evaluation is TX+RX AFE board as discussed in *Highly Integrated Signal chain Solutions TX7332 and AFE5832LP for Smart Ultrasound Proves application note*. The complete system is powered through a Type-C connector with computer on the other side with required softwares installed. For software information and other detailed implementation, please visit the webpage of the devices TX7332 and AFE5832 and go to request access now.

3.1.2 Test Results

3.1.2.1 High Voltage Power Supply

Figure 29 and Figure 28 shows the output ripple of the high voltage circuit of both negative and positive rail at full load, respectively. The ripple is measured at the output capacitor before the π filter, the peak to peak ripple is close to 25 mV. Figure 27 and Figure 28 show the ripple measured after the Power Filter, which is significantly attenuated.

Figure 27. Efficiency Curve of SEPIC HV Power Supply

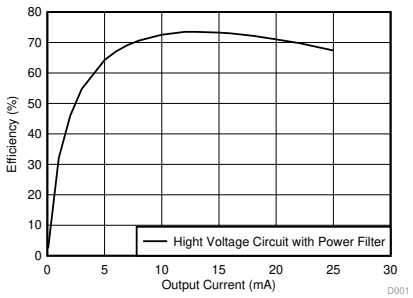
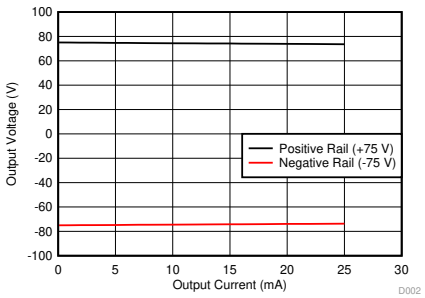


Figure 28. Load Symmetry of SEPIC Showing Accuracy of Less Than 1% and Load Regulation Less Than 2%



3.1.2.2 Output Ripple Measurement

Figure 29 and Figure 31 show the output ripple of the high voltage circuit of both negative and positive rail at full load, respectively. The ripple is measured at the output capacitor before the π filter, the peak to peak ripple is close to 25 mV. Figure 30 and Figure 32 shows the ripple measured after the Power Filter, which is significantly attenuated.

Figure 29. Output Ripple of Negative Rail Before Power Filter

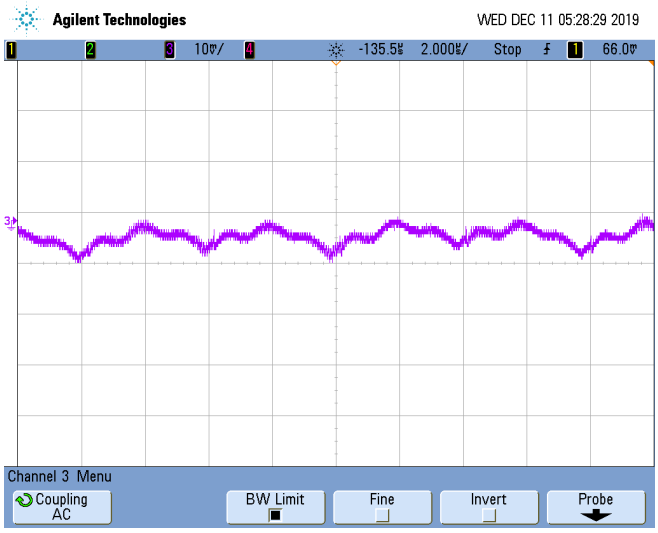


Figure 30. Output Ripple of Negative Rail After Power Filter

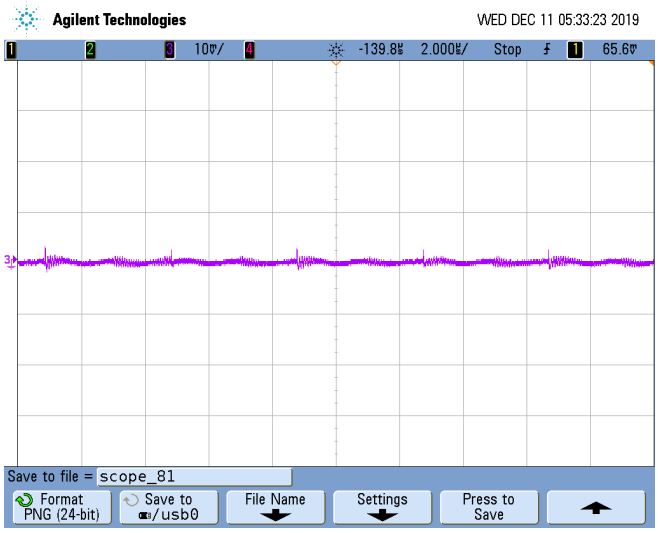


Figure 31. Output Ripple of Positive Rail Before Power Filter

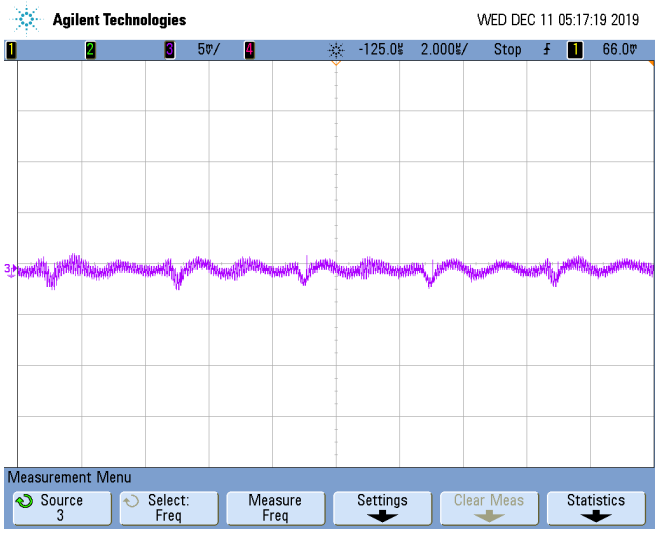
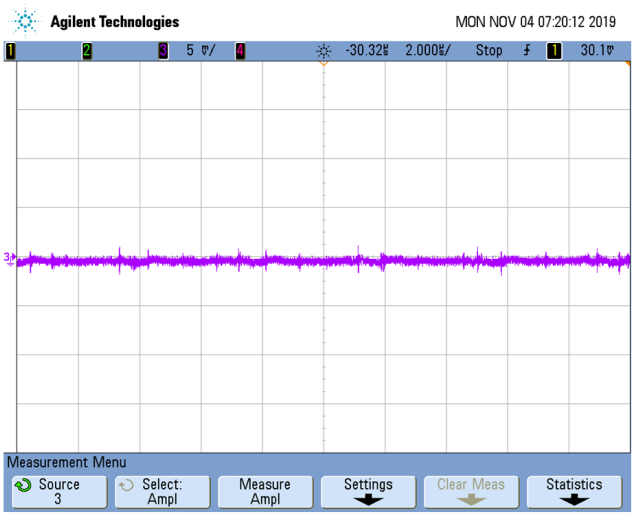


Figure 32. Output Ripple of Positive Rail After Power Filter



3.1.2.3 Load Transient Test

Figure 33 shows the load transient response of the power supply. The load of 25 mA per rail is applied onto both positive and negative rail with a duty cycle 20% at pulse repetition frequency of 5 kHz, as shown in purple waveform. A drop of less than 50 mV is observed on both the rails. Moreover, the load transient response test is repeated in case the load of the power supply is 1 A per rail with a duty cycle of 1%, at pulse repetition frequency of 5 kHz. The result in Figure 34, shows a drop of less than 1 V per rail.

Figure 33. Load Transient Response of Positive and Negative Output Rail With Symmetrical Loads (25 mA)

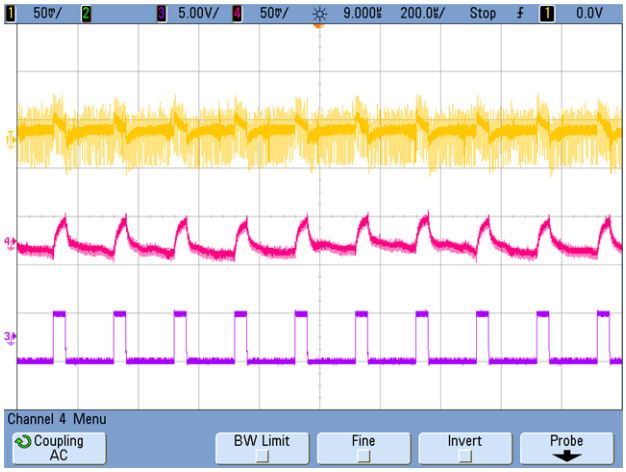
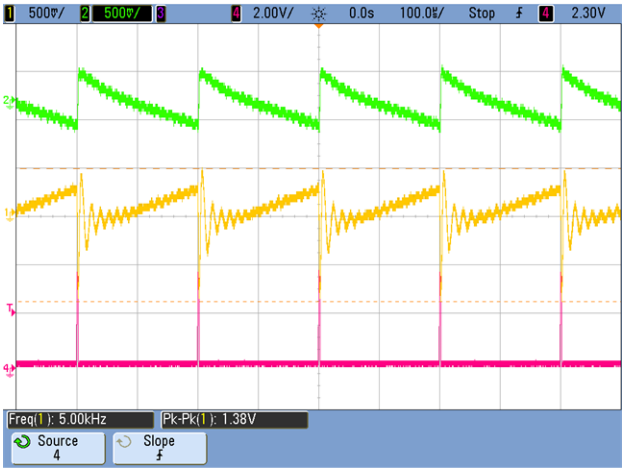


Figure 34. Load Transient Response of Positive and Negative Output Rail With Symmetrical Loads (1A)



3.1.2.4 Noise Measurement

Figure 35 and Figure 36 show the FFT of the received data collected from TX + RX setup consisting of TX7332 as transmit device and AFE5832LP as receive device. Figure 35 shows the noise with ideal bench supply and Figure 36 shows the noise with High Voltage supply generated by this design. The SNR in case of bench power supply and SEPIC based supply are 55.297 dB & 55.264 dB, respectively. This demonstrates that the noise performance of this design is comparable with the bench power supply.

Figure 35. FFT of the Received Data Using Bench Power Supply, Showing SNR of 55.297 dB

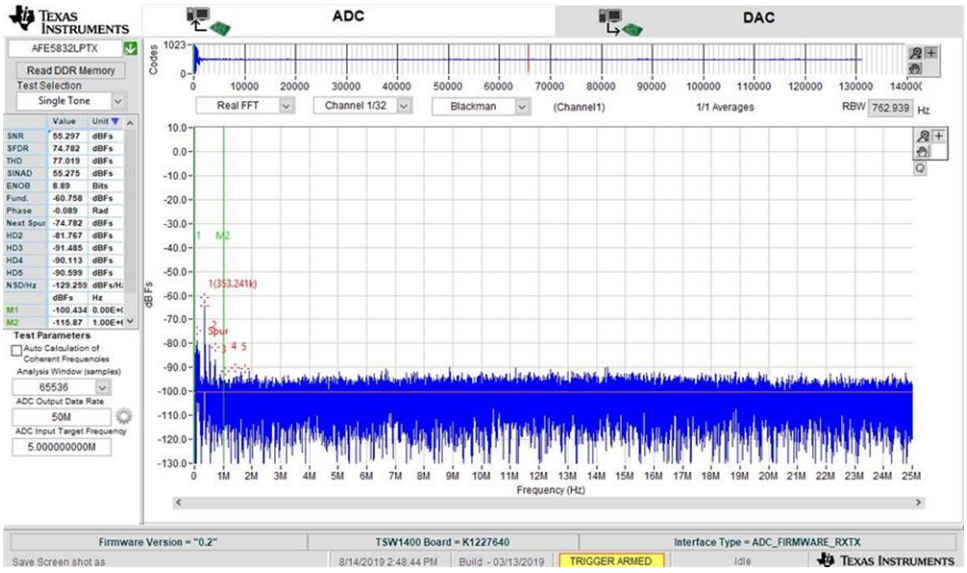
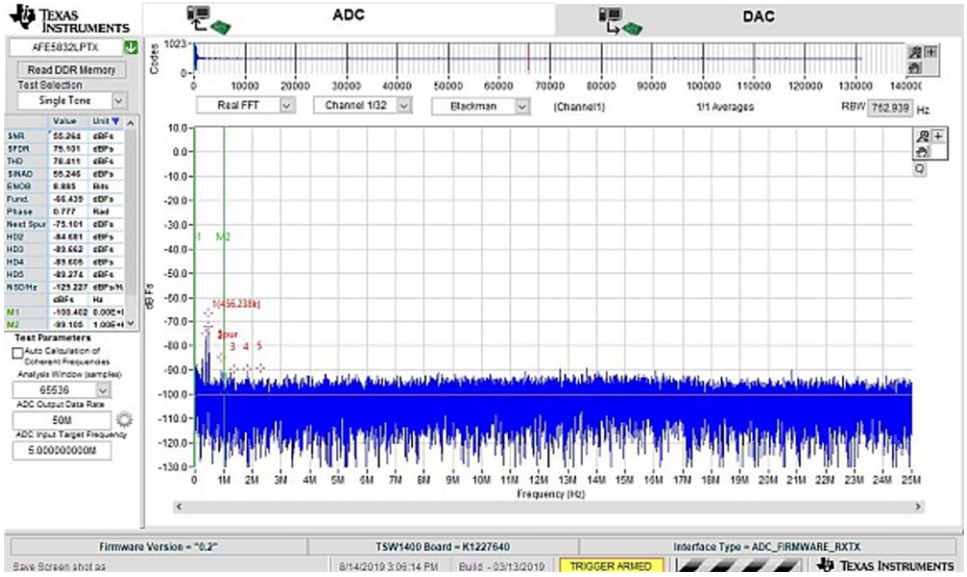


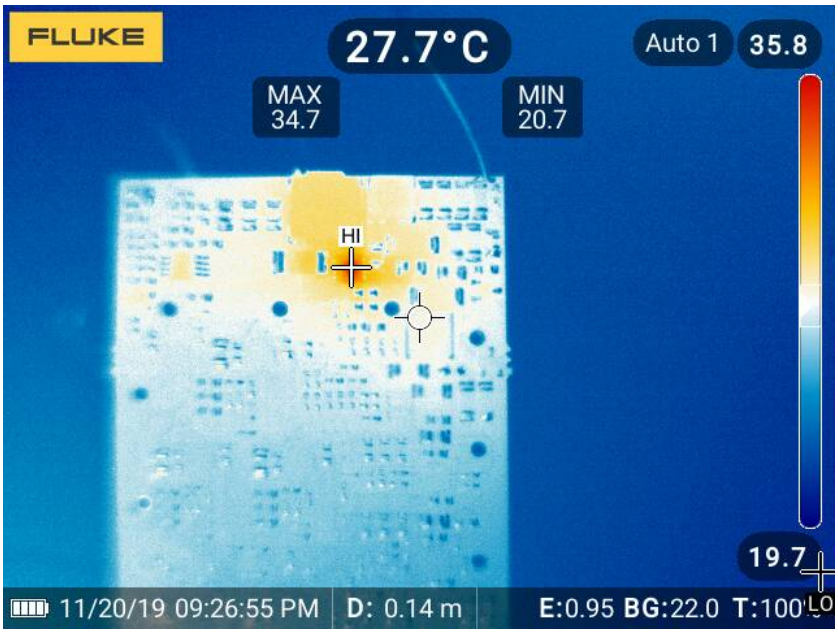
Figure 36. 11 FFT of the Received Data Using SEPIC Power Supply, Showing SNR of 55.264 dB



3.1.2.5 Thermal Performance

Figure 37 shows a thermal image of the high voltage circuit, with symmetrical load of 25 mA on each rail with 20 % duty cycle at 5 kHz shown in Figure 33. The maximum temperature is 34.7°C, reached after 30 minutes of powering on at ambient temperature of 20°C.

Figure 37. Thermal Performance of High Voltage Section



3.1.2.6 Low Voltage Power Supply

3.1.2.6.1 Thermal Performance

Figure 38 is a block diagram representation of the low voltage thermal performance testing. The testing used a load generator and a power resistor for each rail in order to test the thermal performance of the board at each load currents worst case.

Figure 38. LV Test Setup Block Diagram

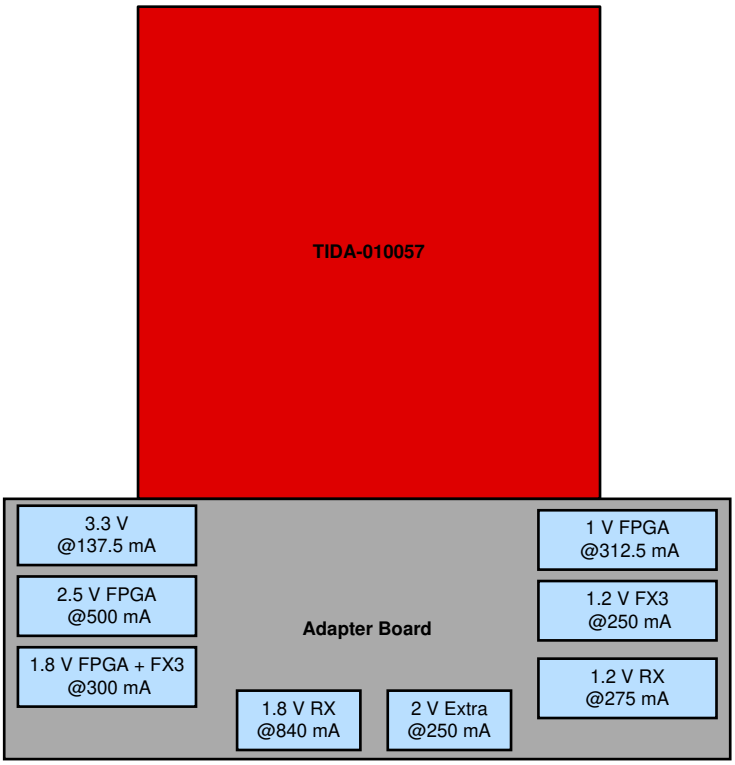


Table 2 shows all of the low voltage power supplies rails with each of their total currents. These values were tested in for their thermal performance in Figure 39 and Figure 40.

Table 2. Low Voltage Power Supply Rail with Their Current Total

RAIL	TOTAL CURRENT (mA)
3.3 V Rail	137.5
2.5 V FPGA	500
1.8 V FPGA+FX3	300
1.8 V RX	840
1.2 V RX	275
1.2 V FX3	250
1 V FPGA	312.5
2 V Extra	250
TPS54218 (3.3 V)	1000

Figure 39 shows a thermal image of the bottom of the low voltage circuit board with all the rails shown in Table 2 at the full load condition. The maximum temperature is 29.9°C with an ambient temperature of 28.4°C. Figure 40 shows a thermal image of the top of the low voltage circuit board with all the rails at the full load condition. The maximum temperature is 32.1°C, with an ambient temperature of 30.1°C

Figure 39. Thermal Performance of Low Voltage Supply (Bottom)

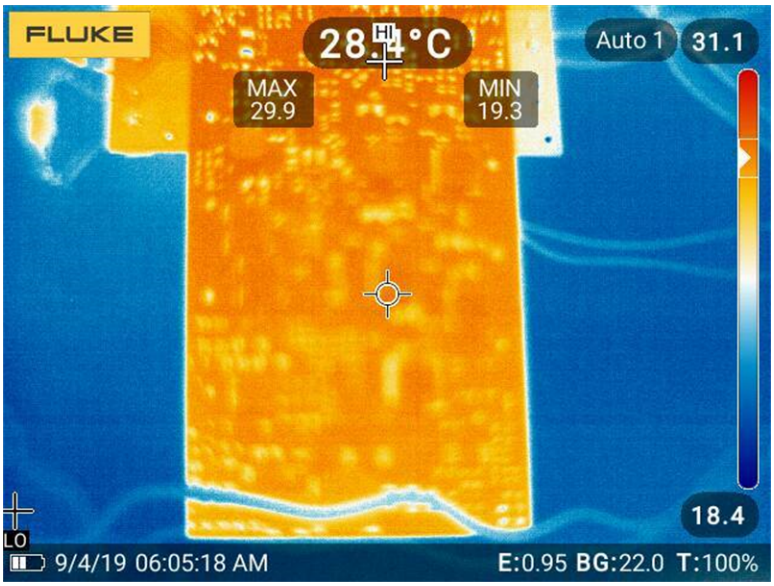


Figure 40. Thermal Performance of Low Voltage Supply (Top)

3.1.2.6.2 FX3 Supply

Figure 41. 1.2 FX3 Supply Efficiency

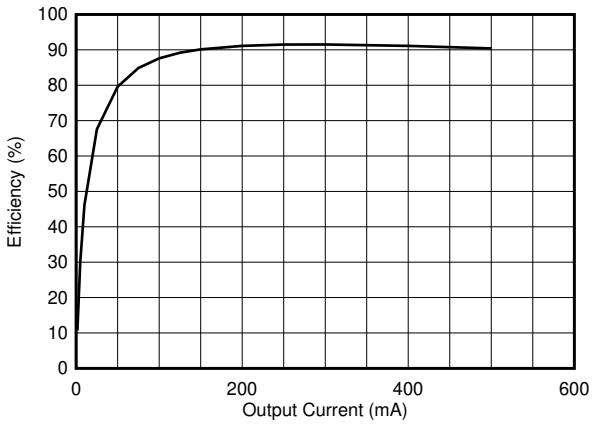


Figure 42. 1.8 FX3 + FPGA Efficiency

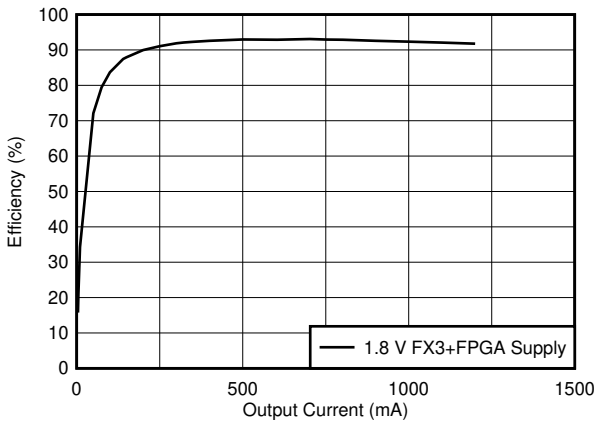


Figure 43. 2.5V FPGA Supply Efficiency

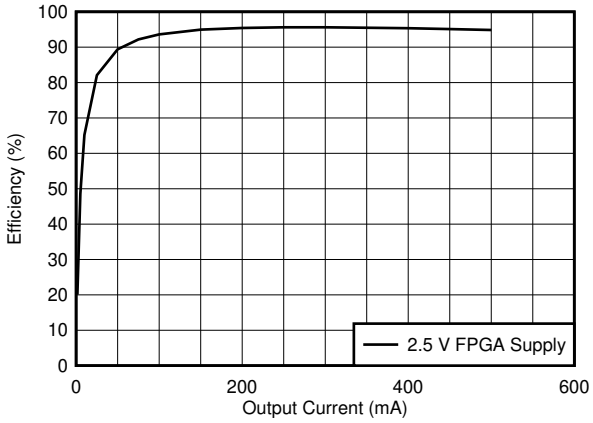


Figure 44. 1V FPGA Supply Efficiency

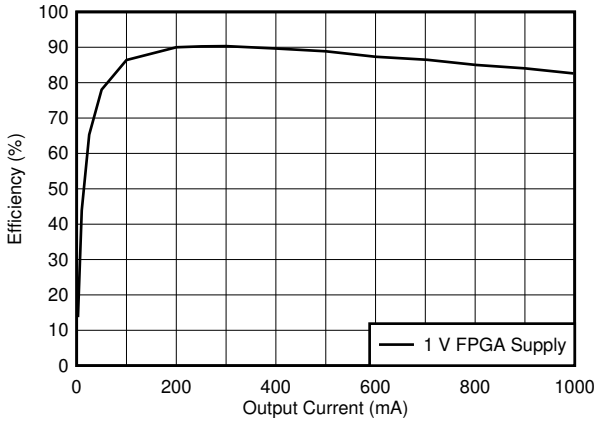


Figure 45. 3.3V RX Supply with LDO Efficiency

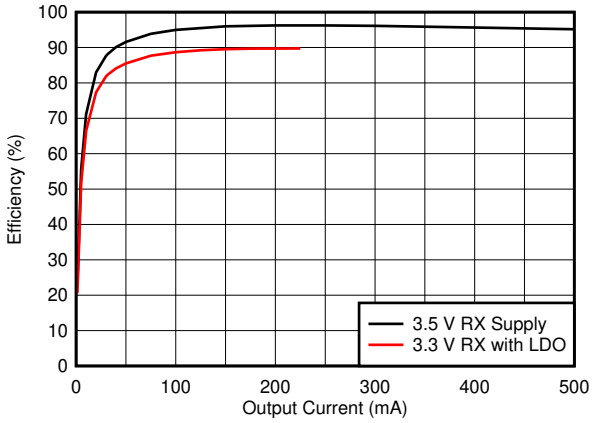


Figure 46. 1.8V Rx with LDO Efficiency

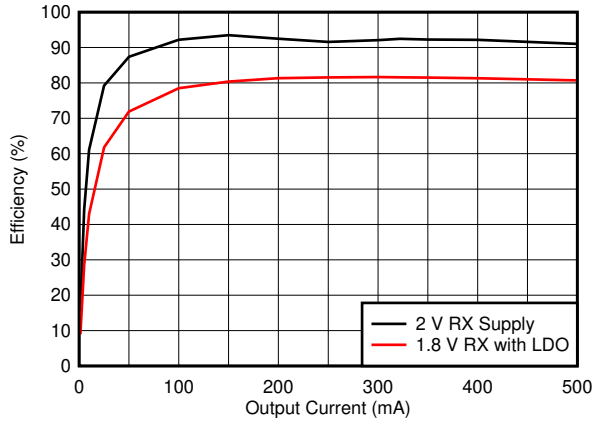


Figure 47. 1.2V Rx with LDO Efficiency

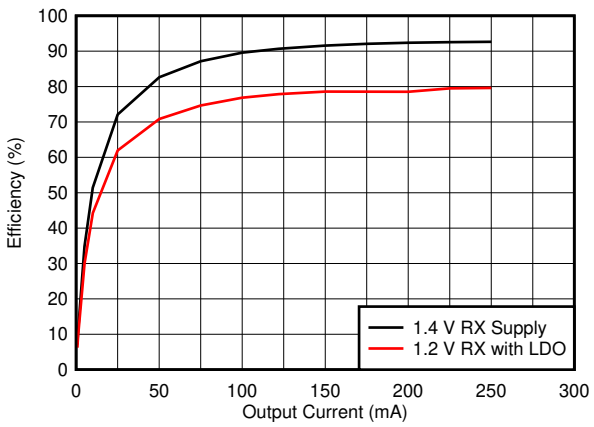


Figure 48. 5V Rx Supply with LDO Efficiency

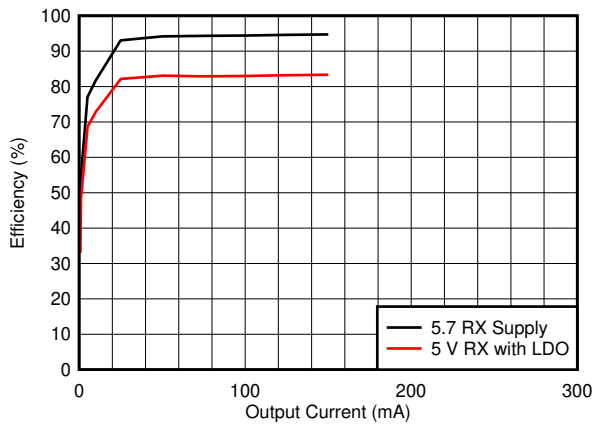
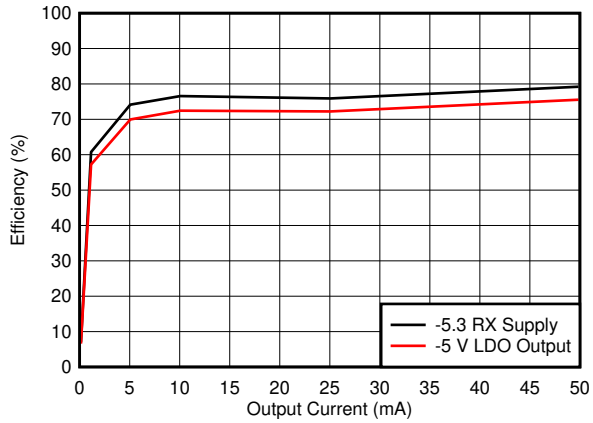


Figure 49. -5V Rx Supply with LDO Efficiency



4 Layout Guidelines

The complete design is made on a 12-Layer board with high speed signals routed on two-signal layers compatible USB recommendation. The impedance is kept 90 for those layers. Figure 50 shows the stack up of the board. The board has 5 ground layers, 2 power layers and 2 signal layers.

Figure 50. Layer stack up of TIDA-010057

	Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
	Top Overlay	Overlay							
	Top Solder	Solder Mask/Coverlay	Surface Material	1	Solder Resist	3.5			0
1	Top Layer	Signal	Copper	2.598				Top	
	Dielectric1	Dielectric	Core	4.164	FR-4 High_Tg	4.2			
2	GND1	Signal	Copper	0.709				Not Allowed	
	Dielectric 2	Dielectric	None	4.488	FR-4 High_Tg	4.2			
3	Signal Layer 1	Signal	Copper	0.709				Not Allowed	
	Dielectric 3	Dielectric	None	5.733	FR-4 High_Tg	4.2			
4	GND2	Signal	Copper	0.709				Not Allowed	
	Dielectric 4	Dielectric	None	4.488	FR-4 High_Tg	4.2			
5	POWER1	Signal	Copper	0.709				Not Allowed	
	Dielectric 5	Dielectric	None	4.13	FR-4 High_Tg	4.2			
6	POWER2	Signal	Copper	0.709				Not Allowed	
	Dielectric 6	Dielectric	None	4.488	FR-4 High_Tg	4.2			
7	GND4	Signal	Copper	0.709				Not Allowed	
	Dielectric 7	Dielectric	None	4.13	FR-4 High_Tg	4.2			
8	POWER3	Signal	Copper	0.709				Not Allowed	
	Dielectric 8	Dielectric	None	4.488	FR-4 High_Tg	4.2			
9	GND6	Signal	Copper	0.709				Not Allowed	
	Dielectric 9	Dielectric	None	5.733	FR-4 High_Tg	4.2			
1...	Signal Layer 2	Signal	Copper	0.719				Not Allowed	
	Dielectric 10	Dielectric	None	4.488	FR-4 High_Tg	4.2			
1...	GND7	Signal	Copper	0.709				Not Allowed	
	Dielectric 12	Dielectric	None	4.164	FR-4 High_Tg	4.2			
1...	Bottom Layer	Signal	Copper	2.598				Bottom	
	Bottom Solder	Solder Mask/Coverlay	Surface Material	1	Solder Resist	3.5			0
	Bottom Overlay	Overlay							

Total Thickness: 64.79mil

4.1 High-Voltage Supply Layout

Layout in SEPIC is very critical. While designing, the most important rule is to reduce the noise in the high current switching loop, which is shown in Figure 51. The current flows from the input supply to the primary inductor and through the MOSFET. To minimize induced EMF due to switching currents, it is desirable to keep parasitic inductance of this loop as low as possible. Components (primary inductors, input electrolytic capacitors, and FET) must be placed as close as possible to each other. In this layout, a single ground plane was used, and all the signals return onto this low impedance plane, as shown in Figure 52. In case the HV circuit is placed in proximity to the transducer, shielding might be necessary to minimize effects of radiated interference from HV section.

Figure 51. Hot Loop in SEPIC Configuration

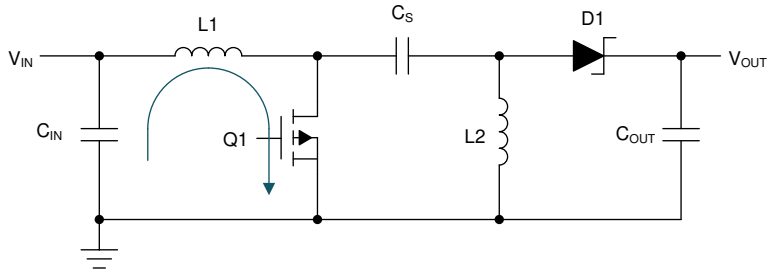
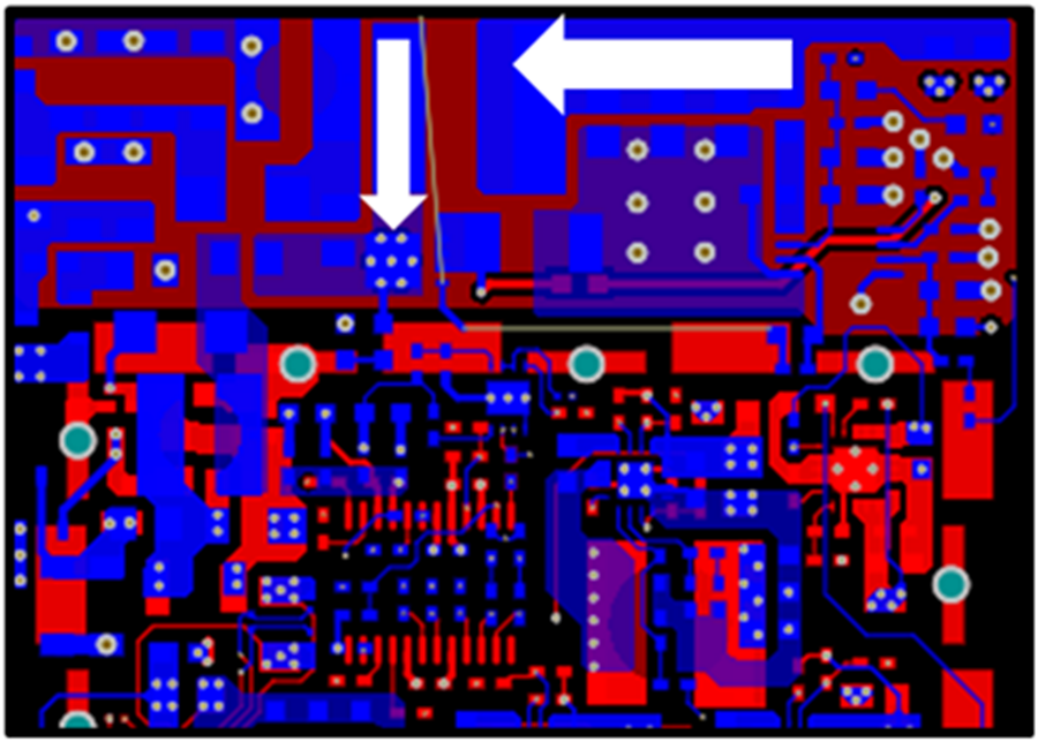


Figure 52. Layout Section of HV



4.2 USB Section Layout Guidelines

The USB data section comprises of HD3SS3220 Mux controller and FX3 data serializer. Figure 53 shows the routing and placement of the various high speed sections. The device HD3SS3220 has high speed differential signals SSTX and SSRX. The length mismatch should be minimal between these two pair. The design keeps < 3mil length mismatch between these two pair. Figure 53 also shows various other sections of the circuit such as low voltage circuit with the EMI shield placed with all the clocking and LV inductor placed inside. This side faces the TX+RX AFE board hence in order to reduce the EMI noise coupling, a shield is placed between the two. The top most part is a plane comprising the ground of the high voltage circuit. There is no component placed in this region to keep space for the transducer connector and transducer and also to keep a shielding layer from the bottom side.

Figure 53. Placement and Layout of the Different Sections of the Design, High Speed Data Section, LV and HV Section (top layer)

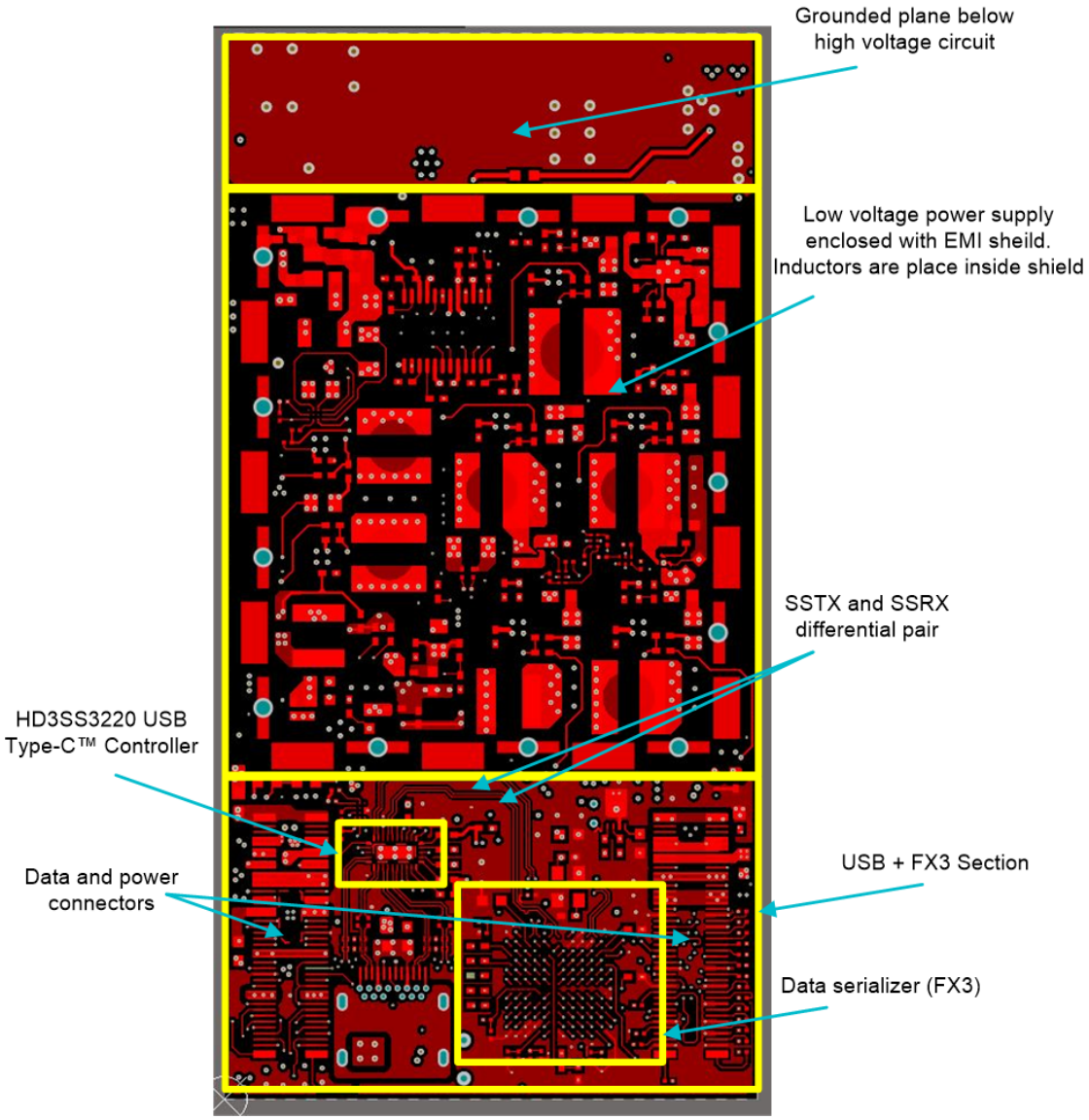


Figure 54 shows the corresponding bottom side of the board highlighting various sections of the board. On this side, at the top, complete high voltage circuit is placed and its layout is discussed separately in Section 4.2.

Figure 54. Placement and Layout of the Different Sections of the Design, High-speed Data Section, LV and HV Section (bottom layer)

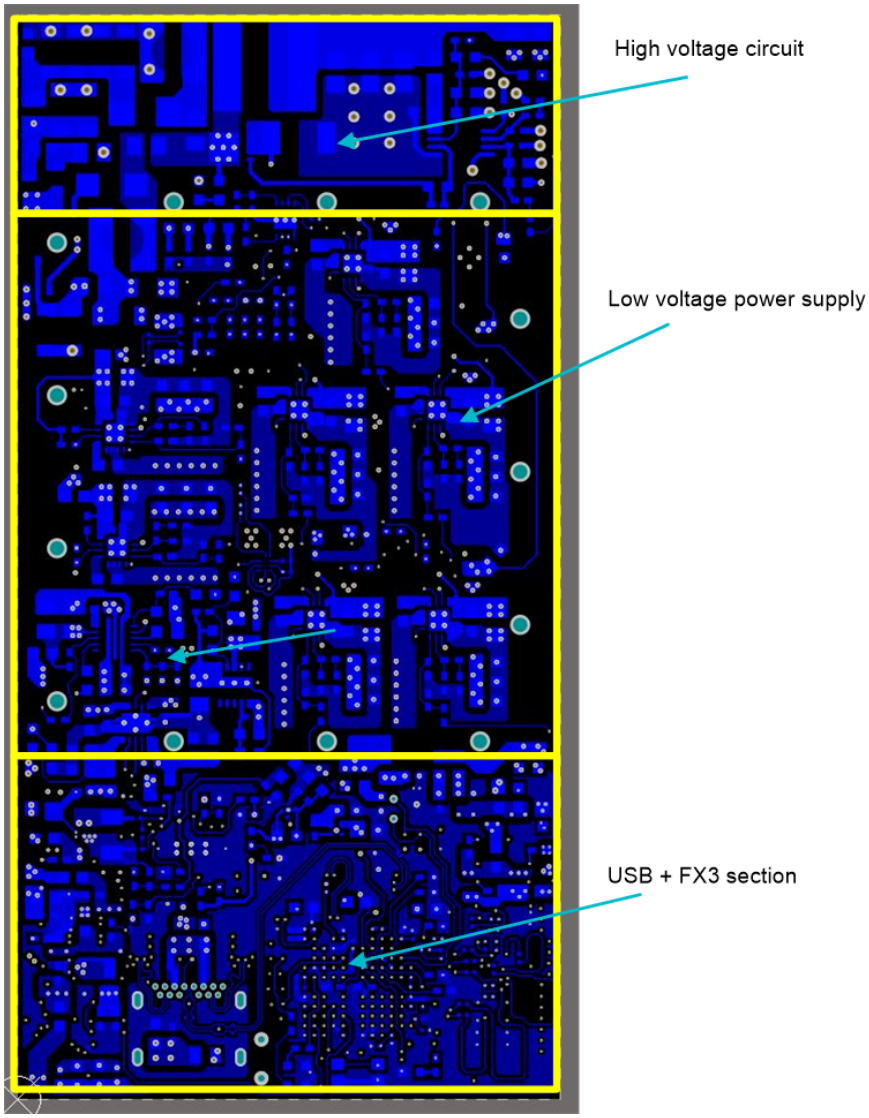
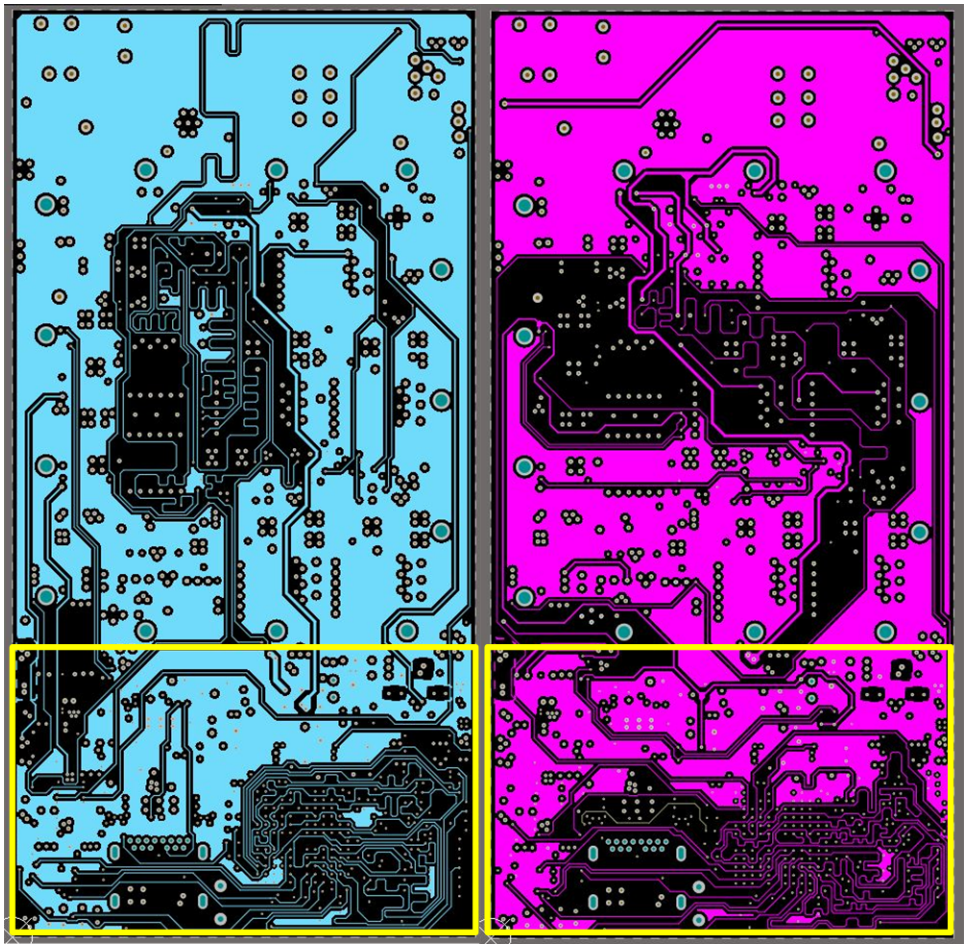


Figure 55 shows the placement and layout of the high-speed 32-bit data signals routed on signal layers. The maximum length of the routed signals is kept 1500 mil with length mismatch of < 100mil. The impedance of the layer is 90 ohm.

Figure 55. Placement and Layout of the High-Speed 32-Bit Data Signals Routed on Signal Layers (highlighted yellow area shows routing)



5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-010057.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010057.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010057.

5.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010057.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010057.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010057.

6 Software Files

To download the software files, see the design files at TIDA-010057.

7 Related Documentation

- *Seven Design Challenges for Ultrasound Smart Probes*
- Texas Instruments, Highly Integrated Signal Chain Solutions TX7332 and AFE5832LP for Smart Ultrasound Probes Application Report
- Texas Instruments, Designing Bipola rHigh Voltage SEPIC Supply for Ultrasound Smart Probe Application Report

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