TI Designs: TIDA-010018
Isolated power and data interface for low-power applications reference design

Description

This reference design provides power and data isolation for low and ultra-low power applications. Generating isolated and non-isolated power rails with a high efficiency and containing a power efficient isolated data interface for three forward- plus one reverse-direction channels. Targeted applications are isolated loop powered 4- to 20-mA transmitters. This design can be adapted to other applications requiring highly-efficient power conversion and isolated data transmission while being powered from sources with a limited current capability. The design demonstrates the performance of switching regulators, low dropout regulators (LDOs) and a digital isolator. All of these devices feature an ultra-low current consumption in the lower μA range. Support of ultra-high power efficiency configuration as well as low output ripple performance.

Resources

TIDA-010018	Design Folder
ISO7041	Product Folder
TPS60402	Product Folder
TPS62125	Product Folder
TPS62745	Product Folder
TPS727	Product Folder

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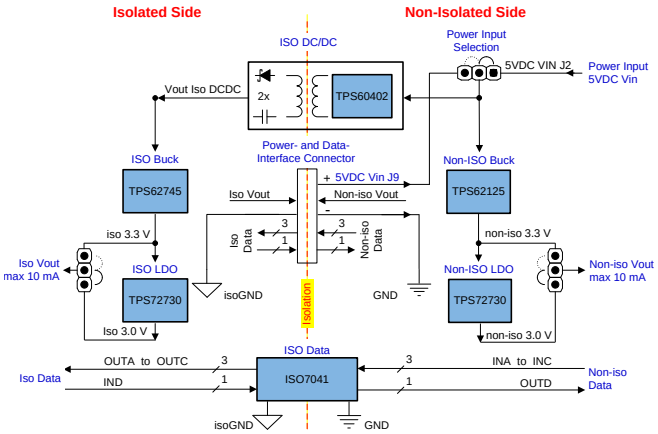
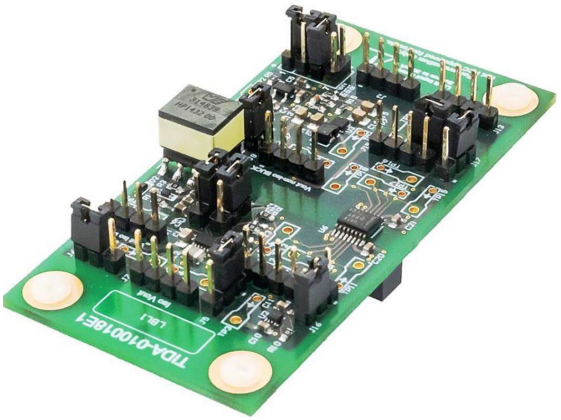
Features

- Power Input: 5 VDC; source needs to be current limited to < 30 mA
- Ultra-low power, isolated data interface
  - 5, 16, 130 μA per channel at 10, 100, 1000 kbps
  - 3 forward-channels, 1 reverse-channel
- Isolated 10-mA DC/DC Converter
  - Efficiency up to 86.5%
  - Functional isolation
- 3.3-V, 10-mA buck converter on non-isolated side
  - Efficiency up to 93%, VOUT ripple < 15 mVpp
- 3.3-V, 10-mA buck converter on isolated side
  - Efficiency up to 92%, VOUT ripple < 20 mVpp
- 3.0-V, 10-mA LDOs
  - I_Q = 16 μA @ Iout = 1 mA
  - PSRR > 36 dB at ≤ 200 kHz

Applications

- Temperature transmitter
- Flow transmitter
- Pressure transmitter





1 System Description

The main purpose of the reference design is to support the design of isolated transmitters. The need for isolation is based on the fact, that the transmitter in a 4-to 20-mA system can be located hundreds or even thousands of meters far from the receiver and from the power source of the system (for example, 4-to 20-mA analog input module of a PLC). The transmitters sensor element (for example, thermocouple) is often directly connected to grounded metallic objects, while the receiver and the transmitters loop input is referred to the ground of the receiver. Unwanted ground loops can be unintentionally established as a consequence of the possible large distance between transmitter and receiver. Keeping the transmitters sensor front end electrically isolated breaks these ground loops and their undesired influence on the accuracy of the measured and transmitted signal. The isolated DC/DC block of the reference design isolates the sensor front end of the transmitter by providing an isolated supply voltage and isolated ground. The isolated data block provides an isolated communication path for the sensor front end of the transmitter in a similar way.

Figure 1. TIDA-010018 in Isolated Two-Wire Loop Powered 4- to 20-mA System

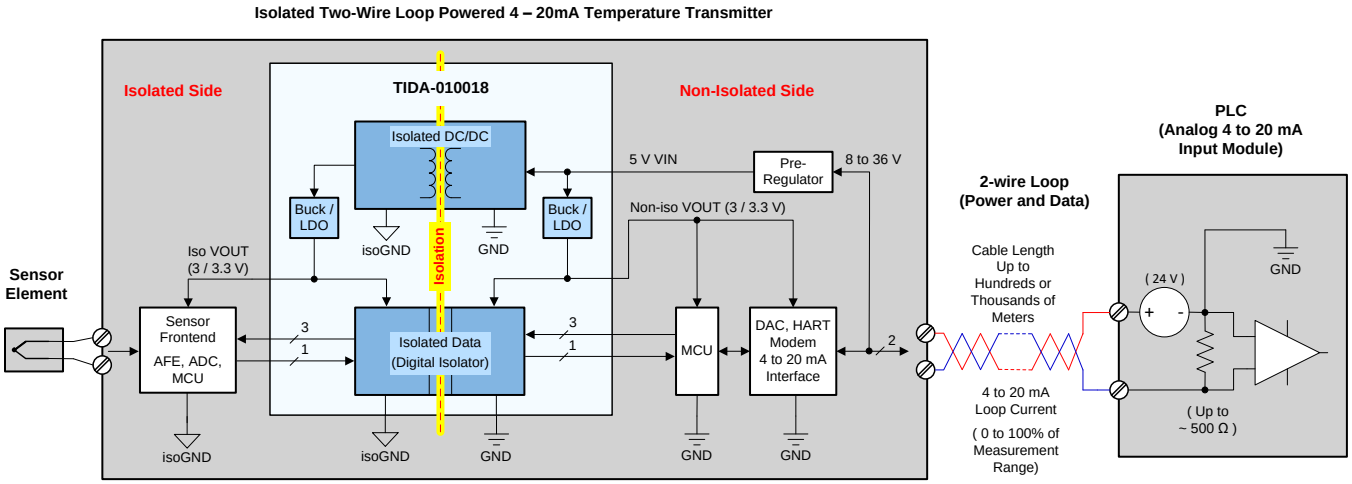


Figure 1 shows an exemplary use of this reference design in an isolated two-wire loop powered 4- to 20-mA transmitter. The reference design uses an intermediate 5-V rail, generated from the 8 V to 36 V, 4- to 20-mA loop, as its input power source. The 5-V input of the reference design is usually provided by a pre-regulator (LDO, low power buck or shunt regulator). The reference design generates the aforementioned isolated power rail (*Iso VOUT*: 3 V or 3.3 V) for powering the isolated side of the transmitters (sensor element, AFE, ADC, optional MCU and the isolated side of the digital isolator). Likewise, the power rail (*Non-iso VOUT*: 3 V or 3.3 V) for powering the non-isolated side transmitter-electronics (MCU, DAC, optional HART modem, 4- to 20-mA interface and the non-isolated side of the digital isolators) is generated by the design too. Under normal operating conditions, the total current consumption of the electronic transmitter must be less than the actual loop current. A loop current from 3.8 mA to 20.5 mA is defined by the *NAMUR recommendation: NE 043* as the available current range for the measurement signal. Loop currents less than 3.6 mA and larger than 21 mA can be assigned to indicate failures. The majority of loop-powered 4–20 mA transmitters have their internal electronics designed to consume less current than 3.6 mA – even at loop currents within the 3.8-mA to 20.5-mA measurement range. This limited supply current budget requires either a highly efficient power solution, or ultra-low power components in the previously-mentioned circuit blocks, or a combination of both. The reference design demonstrates the use of ultra-low I_Q buck converters for achieving such a high-power efficiency. The analog electronics of the transmitter often require a low-noise, low-ripple supply voltage. The buck converters of the reference design can be supplemented by ultra-low I_Q LDOs, acting as low-noise post regulators and attenuating the output ripple of the buck converters.

1.1 Key System Specifications

CAUTION

This reference design is made available for parameter performance evaluation only and is not intended for isolation voltage testing.

To prevent damage to the reference design, any voltage applied as a supply or digital I/O must be maintained within the recommended operating range as given in the data sheet of the devices used.

WARNING

To minimize the risk of fire, the user's power source shall not exceed the maximum ratings of 5.25 VDC, 30 mA. Refer to the user guide.

Use only the top-side header J2 OR the bottom-side Power- and Data-Interface Connector (receptacle J9) as the power input for the reference design.

Use the Power Input Selection header (J18) and related jumper SH-J18 to select either J2 or J9 as the sole power input of the reference design.

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Power Input (Header J2 or Receptacle J9)		
Operating supply voltage	5 V (4.4 V to 5.25 V)	Section 2.5.1
Power input selection	Use header J18 and related jumper SH-J18 to select either J2 or J9 as sole power input	
ISO DC/DC (*Vin ISO DCDC* = 5 V)		
Maximum total Iout (Sum of all currents drawn from *Vout Iso DCDC*)	10 mA	Section 3.2.2.1
Typical efficiency, *Vout Iso DCDC* at specific Iout of ISO DC/DC	at 100 µA : 42%, 5.9 V at 100 µA	
	at 1 mA 81%, 5.7 V	
	at 4 to 5 mA : 86.5 % peak, 5.6 V	
	at 10 mA : 85%, 5.4 V	
NON-ISO BUCK (*Vin non-iso BUCK* = 5 V, *Vout non-iso BUCK* = 3.3 V)		
Maximum total Iout (Sum of all currents drawn from *Vout non-iso Buck*)	10 mA	Section 3.2.2.3
Typical efficiency at specific Iout non-iso BUCK	at 100 µA: 71%	
	at 1 mA: 90%	
	at 10 mA: 93%	

Table 1. Key System Specifications (continued)

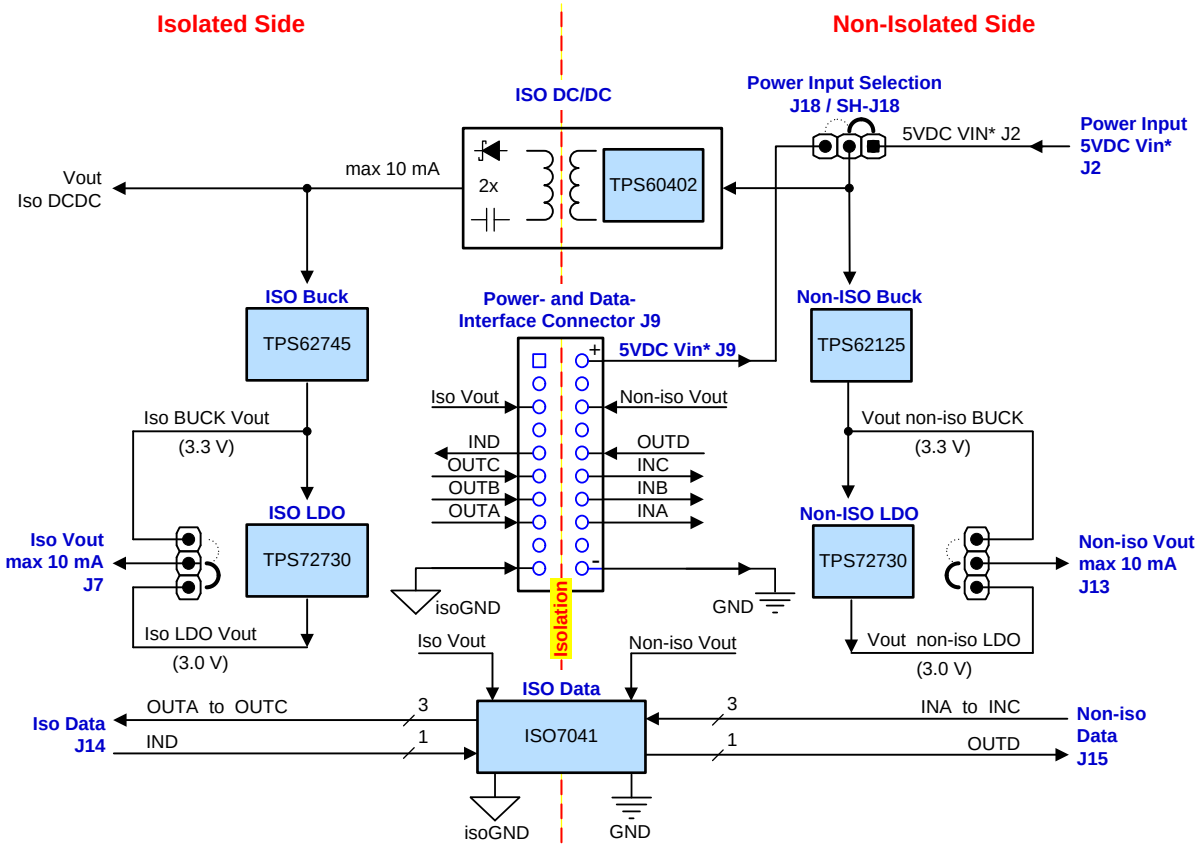
PARAMETER	SPECIFICATIONS	DETAILS
ISO BUCK (*Vin Iso BUCK* = 5 V, *Iso BUCK Vout* = 3.3 V)		
Maximum Iout (Sum of all currents drawn from *Iso BUCK Vout*)	10 mA	Section 3.2.2.2
Typical efficiency at specific Iso BUCK Iout	at 100 µA: 92% at 3.3 Vout	
	at 1 mA: 93% at 3.3 Vout	
	at 10 mA: 93% at 3.3 Vout	
LDOs (*LDO Vin* = 3.3 V, *LDO Vout* = 3.0 V, ISO and NON-ISO LDO)		
Maximum Iout (Sum of all currents drawn from any of the outputs of the LDO)	10 mA	Section 3.2.2.4
Typical efficiency, quiescent current, Vout at specific LDO Iout	at 100 µA: 82%, 10.6 µA, 3.0024 V	
	at 1 mA: 89.6%, 15.5 µA, 3.0023 V	
	at 10 mA: 90.4%, 52.8 µA, 2.9995 V	
ISOLATION		
Isolation	Functional isolation, depends on transformer, digital isolator and board construction	See the data sheet of transformer T1 and of digital isolator

2 System Overview

2.1 Block Diagram

Figure 2 shows the functional block diagram of the design.

Figure 2. TIDA-010018: Functional Block Diagram



2.2 Design Considerations

The design is divided into an isolated side and into a non-isolated side.

CAUTION

This reference design is made available for parameter performance evaluation only and is not intended for isolation voltage testing.

To prevent damage to the reference design, any voltage applied as a supply or digital I/O must be maintained within the recommended operating range as given in the data sheet of the devices used.

All circuit blocks of the design are branded by the prefix “ISO” or “Non-ISO”, depending to which side of the design they belong. Therefore, the ISO LDO is not a very special isolated LDO, but is simply the LDO which is located on the isolated side of the reference design.

The design can be evaluated in a standalone test setup, using the headers on the top side of the PCB. Header J2 acts in this configuration as the power input of the reference design to which the user's power source must be connected.

WARNING

To minimize the risk of fire, the user's power source shall not exceed the maximum ratings of 5.25 VDC, 30 mA. Refer to the user guide.

Power Input Selection header (J18) must be configured by jumper SH-J18 in a way, that header J2 is selected as the sole power input of the reference design when the reference design is configured for a standalone test setup.

Refer to user guide Section 3.

The header J7 and J13 serve as the power outputs of the reference design and are rated for a maximum 10-mA of output current on the isolated and non-isolated output voltage rails. On each of the circuit sides, the reference design allows the user to select either the 3-V output of the LDO or the 3.3-V output of the Buck used. The direct usage of the output of the buck ensures a design with highest power efficiency, but is characterized by a larger output voltage ripple. Using the LDO as a post regulator provides a low-noise output rail, but generates additional losses in the circuitry.

Headers J14 and J15 represent the connection to the data pins of the digital isolator used in the ISO Data block. Three channels (A to C) are available for data transmission from the non-isolated side to the isolated side, one channel (D) is available for data transmission from the isolated side to the non-isolated side. This channel setup enables the usage of communication protocols as SPI, I2C, and UART.

The ISO DC/DC block is a highly efficient isolated DC/DC converter designed to use the *5VDC Vin* to generate the *Vout Iso DCDC*-rail (available on J1) with the highest possible 86.5% efficiency at an output current of 4 to 5 mA. The voltage on the *Vout Iso DCDC*-rail shows some dependencies on its output current, board temperature, and the accuracy of the *5VDC Vin* input voltage. Final voltage regulation of the *Iso Vout* (on J7) is provided by the ISO BUCK which can optionally be extended by the ISO LDO as a post regulator.

Alternatively, this reference design can also be evaluated as a plug-on board in conjunction with a specifically-designed hardware which represents the typical circuitry (for example, as Figure 1 shows: sensor front end, MCU, pre-regulator, output interface, …) of the targeted end application. When evaluating the board in such a manner, the Power- and Data-Interface Connector J9 serves as the alternative power input of the TIDA-010018 reference design. The aforementioned specifically designed hardware acts under this alternative test setup as power source.

WARNING

To minimize the risk of fire, the user's power source shall not exceed the maximum ratings of 5.25 VDC, 30 mA. Refer to the user guide.

The Power Input Selection header (J18) must be configured by jumper SH-J18 in a way, that the Power- and Data-Interface Connector J9 is selected as the sole power input of the reference design when the reference design is evaluated as a plug-on board in conjunction with a specifically designed hardware. The specifically designed hardware represents the typical circuitry of the targeted end application and shall not exceed the maximum power source ratings of 5.25 VDC, 30 mA.

Refer to user guide Section 3.

J9 is a receptacle and is mounted on the bottom side of the PCB, enabling that the TIDA-010018 reference design can be used as plug-on board on such a specifically designed hardware as mentioned afore. J9 contains in addition all the *Iso* and *Non-Iso Data* and *Vout* rails which are also available on the top side of the board as headers J7 and J13 to J15, to finally support its usage as plug-on board.

2.3 Design Considerations

2.4 Highlighted Products

This reference design features the following devices:

ISO7041: Ultra-low power, four-channel digital isolator

TPS60402: 60-mA charge pump voltage inverter with fixed 50-kHz operation

TPS62125: 3 V–17 V, 300-mA Buck converter with adjustable enable threshold and hysteresis

TPS62745: Dual-cell ultra-low I_Q step down converter for low-power wireless applications

TPS727: 250-mA, ultra-low I_Q, fast transient response, RF low-dropout linear regulator

2.4.1 ISO7041

The ISO7041 device is an ultra-low power, multichannel digital isolator that can be used to isolate CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. Innovative edge based architecture combined with an ON-OFF keying modulation scheme allows these isolators to consume very-low power while meeting 3000-V_{RMS} isolation rating per UL1577. The per channel dynamic current consumption of the device is under 120 μA/Mbps and the per channel static current consumption is 4.2 μA at 3.3 V, allowing for use of the ISO7041 in both power and thermal constrained system designs.

The device can operate as low as 2.25 V, as high as 3.6 V, and is fully functional with different supply voltages on each side of isolation barrier. The four channel isolator comes in a 16-QSOP package with three forward-direction channels and one reverse-direction channel in a 16-QSOP package. The device has default output high and low options. If the input power or signal is lost, default output is *high* for the ISO7041 device without the suffix F and *low* for the ISO7041F device with the F suffix.

Figure 3. Simplified Application Schematic

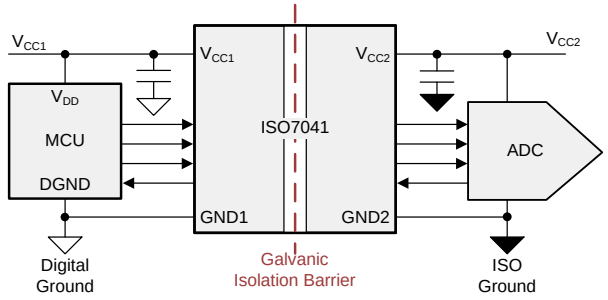


Figure 4. Power Consumption vs Data Rate at 3.3 V

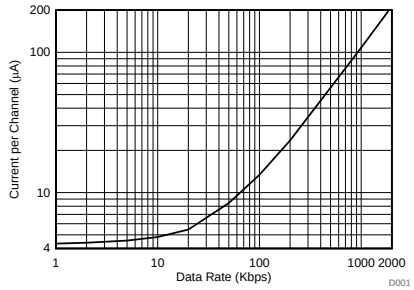
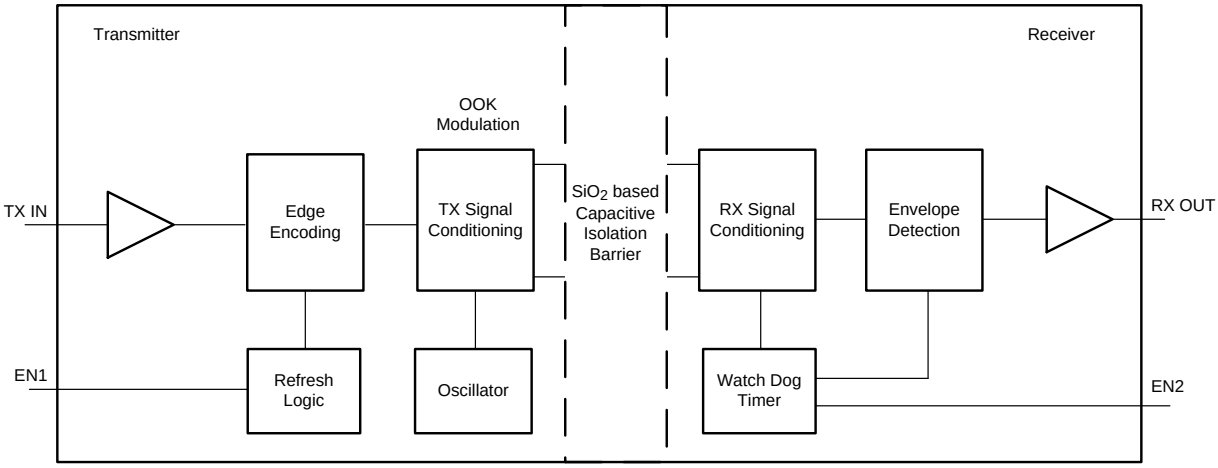


Figure 5. Conceptual Block Diagram of a Digital Capacitive Isolator



Features

- Ultra-low power consumption
  - 4.2 µA per Channel quiescent current (3.3 V)
  - 15 µA per Channel at 100 kbps (3.3 V)
  - 116 µA per Channel at 1 Mbps (3.3 V)
- Robust isolation barrier
  - >100-Year projected lifetime
  - 3000 V_{RMS} Isolation rating
  - ±100 kV/µs Typical CMTI
- Wide Inge: 2.25 V to 3.6 V
- Wide temperature range: –55°C to +125°C
- Small 16-QSOP package (16-DBQ)
- Signaling rate: Up to 2 Mbps
- Default output *high* (ISO7041) and *low* (ISO7041F) options
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity

  - Very low emissions
- Safety-related certifications (planned):
  - UL 1577 Component recognition program
  - DIN V VDE V 0884-11
  - CQC, TUV and CSA certifications
  - IECEx (IEC 60079-0 & IEC 60079-11) and ATEX (EN 60079-11)

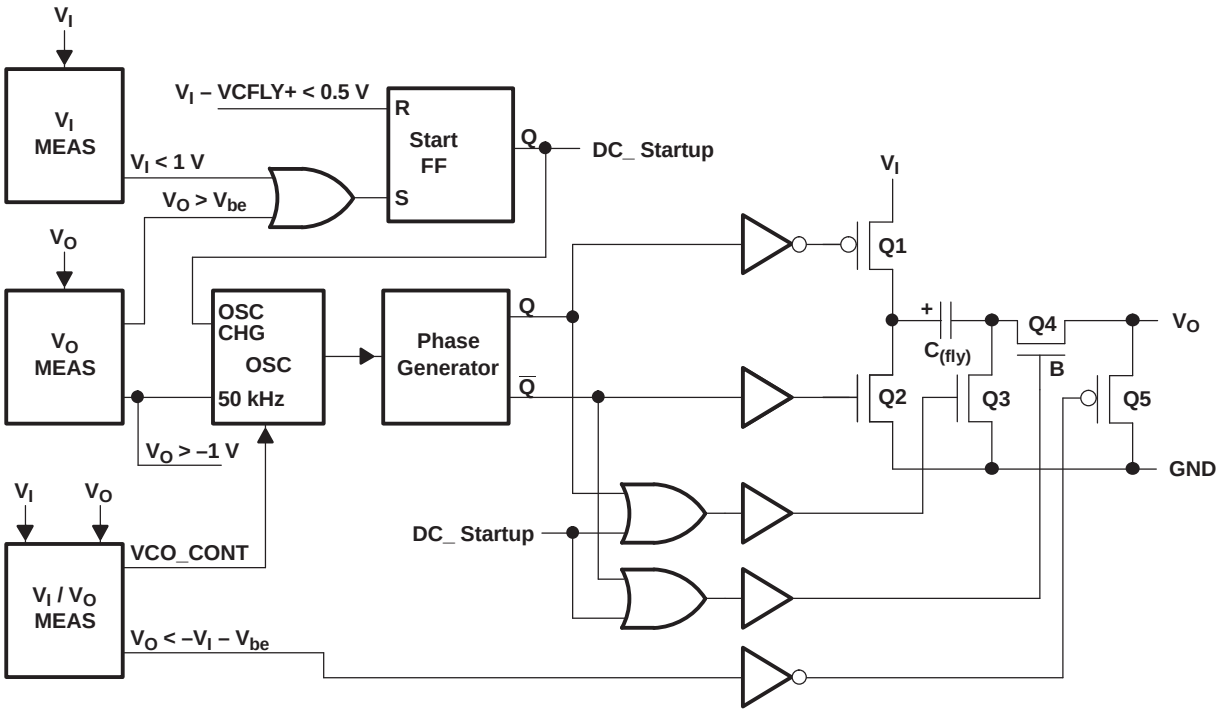
2.4.2 TPS60402

The TPS6040x family of devices generates an unregulated negative output voltage from an input voltage ranging from 1.6 V to 5.25 V. The devices are typically supplied by a pre-regulated supply rail of 5 V or 3.3 V. Due to its wide input voltage range, two or three NiCd, NiMH, or alkaline battery cells, as well as one Li-Ion cell can also power them.

Only three external 1-µF capacitors are required to build a complete DC-DC charge pump inverter. Assembled in a 5-pin SOT-23 package, the complete converter can be built on a 50-mm^2 board area. Additional board area and component count reduction is achieved by replacing the Schottky diode that is typically needed for start-up into load by integrated circuitry.

The TPS6040x can deliver a maximum output current of 60 mA with a typical conversion efficiency of greater than 90% over a wide output current range. Three device options with 20-kHz, 50-kHz, and 250-kHz fixed-frequency operation are available.

Figure 6. Functional Block Diagram



Features

- Inverts input supply voltage
- Up to 60-mA output current
- Only three small 1-µF ceramic capacitors needed
- Input voltage range from 1.6 V to 5.5 V
- PowerSave-mode for improved efficiency at low-output currents (TPS60400)
- Device quiescent current typical 65 µA
- Integrated active Schottky-diode for start-up into load

- Small 5-pin SOT-23 package
- Evaluation module available TPS60400EVM-178

2.4.3 TPS62125

The TPS62125 device is a high-efficiency synchronous step-down converter optimized for low and ultra-low power applications providing up to 300-mA output current. The wide input voltage range of 3 V to 17 V supports 4-cell alkaline and 1- to 4-cell Li-Ion batteries in series configuration as well as 9-V to 15-V powered applications. The device includes a precise low-power enable comparator which can be used as an input supply voltage supervisor (SVS) to address system specific power-up and power-down requirements. The enable comparator consumes only 6-µA quiescent current and features an accurate threshold of 1.2 V typical as well as an adjustable hysteresis. With this feature, the converter can generate a power supply rail by extracting energy from a storage capacitor fed from high impedance sources such as solar panels or current loops. With its DCS-Control scheme the converter provides power-save mode operation to maintain highest efficiency over the entire load current range. At light loads the converter operates in pulse frequency modulation (PFM) mode and transitions seamlessly and automatically in pulse width modulation (PWM) mode at higher load currents. The DCS-Control™ scheme is optimized for low-output ripple voltage in PFM mode in order to reduce output noise to a minimum and features excellent AC load regulation. An open-drain power good output indicates once the output voltage is in regulation.

Figure 7. Typical Application Schematic

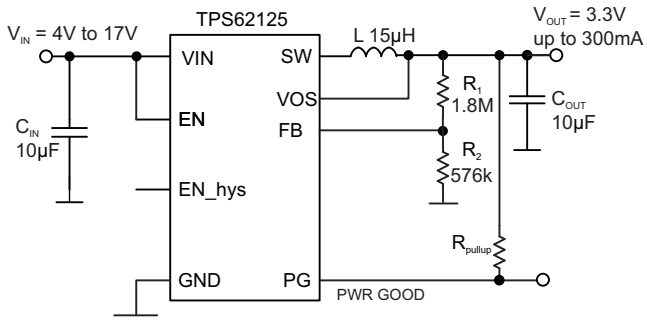


Figure 8. Efficiency vs. Output current, VOUT = 3.3 V

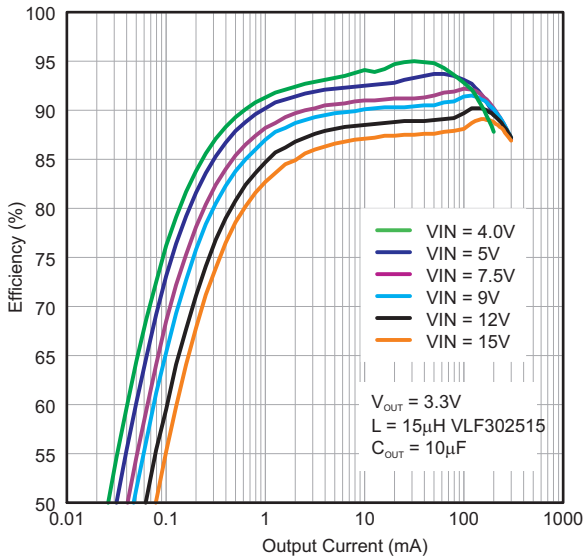
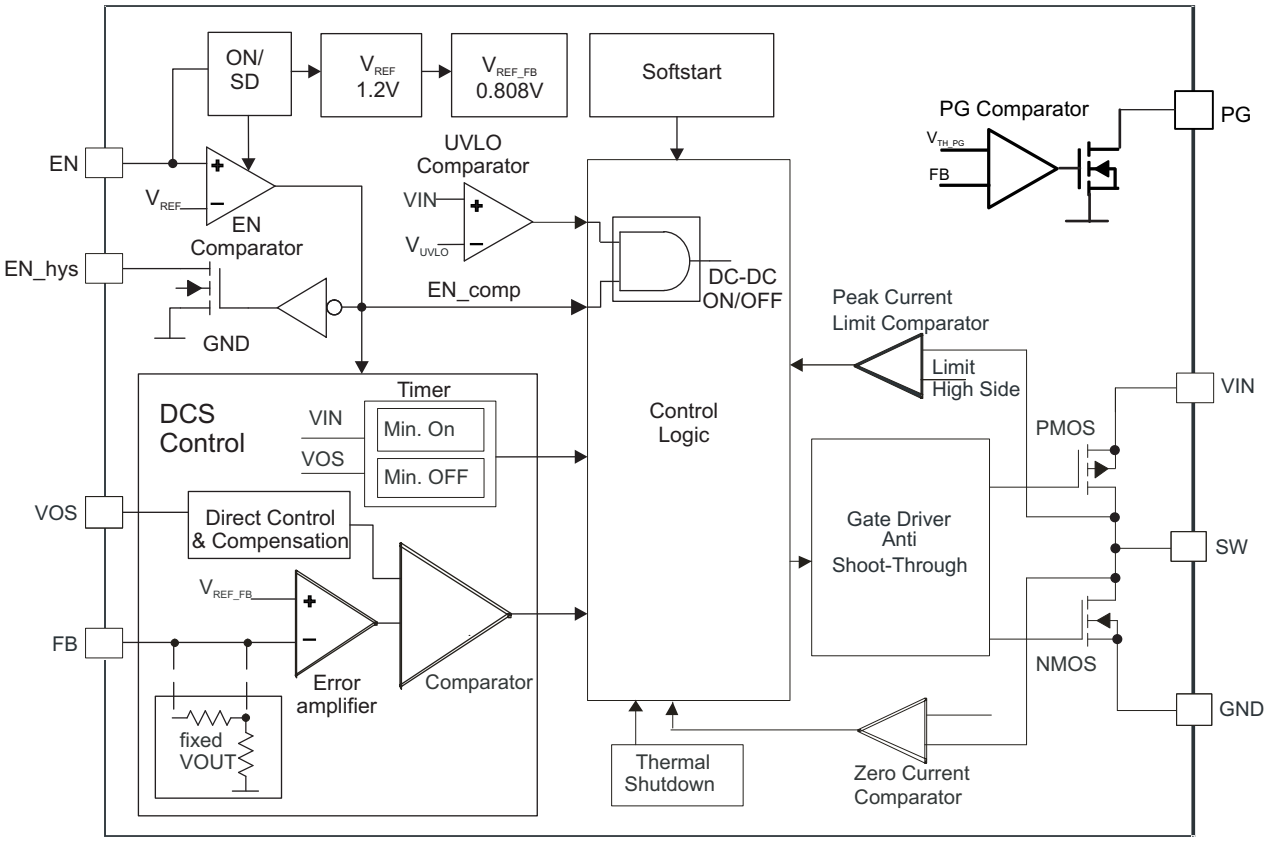


Figure 9. Functional Block Diagram



Features

- Wide input voltage range 3 V to 17 V
- Input supply voltage supervisor (SVS) with adjustable threshold and hysteresis consuming typical 6-µA quiescent current
- Wide output voltage range 1.2 V to 10 V
- Typical 13-µA quiescent current
- 350-nA Typical shutdown current
- Seamless power save mode transition
- DCS-Control™ scheme
- Low output ripple voltage
- Up to 1-MHz switching frequency
- Highest efficiency over wide V_{IN} and V_{OUT} range
- Pin-to-pin compatible with TPS62160 and TPS62170
- 100% Duty cycle mode
- Power Good open drain output
- Output discharge function
- Small 2-mm × 2-mm 8-pin WSON package

2.4.4 TPS62745

The TPS62745 device is a high-efficiency ultra-low power synchronous step down converter optimized for low power wireless applications. It provides a regulated output voltage consuming only 400-nA quiescent current. The device operates from two rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-SO2, Li-MnO2 or four to six cell alkaline batteries. The input voltage range up to 10 V allows also operation from a USB port and thin-film solar modules. The output voltage is set with four VSEL pins between 1.8 V and 3.3 V for the TPS62745 or 1.3 V and 2.8 V for the TPS627451. TPS62745 features low output ripple voltage and low noise with a small output capacitor. An internal input voltage switch controlled by pin EN_VIN_SW connects the supply voltage to pin VIN_SW. The switch is intended to be used for an external voltage divider, scaling down the input voltage for an external ADC. The switch is automatically opened when the supply voltage is below the undervoltage lockout threshold. The TPS62745 device is available in a small, 12-pin, 3 mm × 2 mm WSON package.

Figure 10. Typical Application Schematic

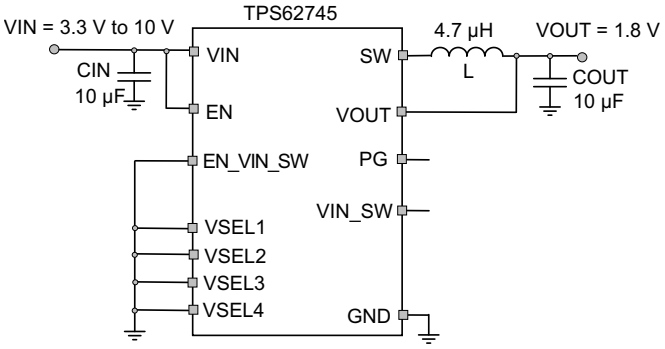


Figure 11. Efficiency vs. Output current, V_{OUT} = 3.3 V

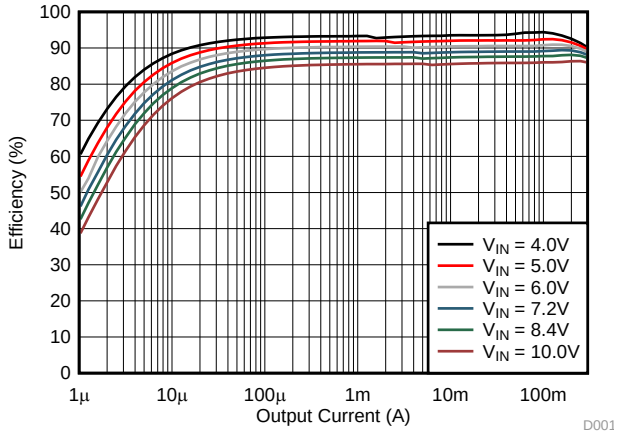
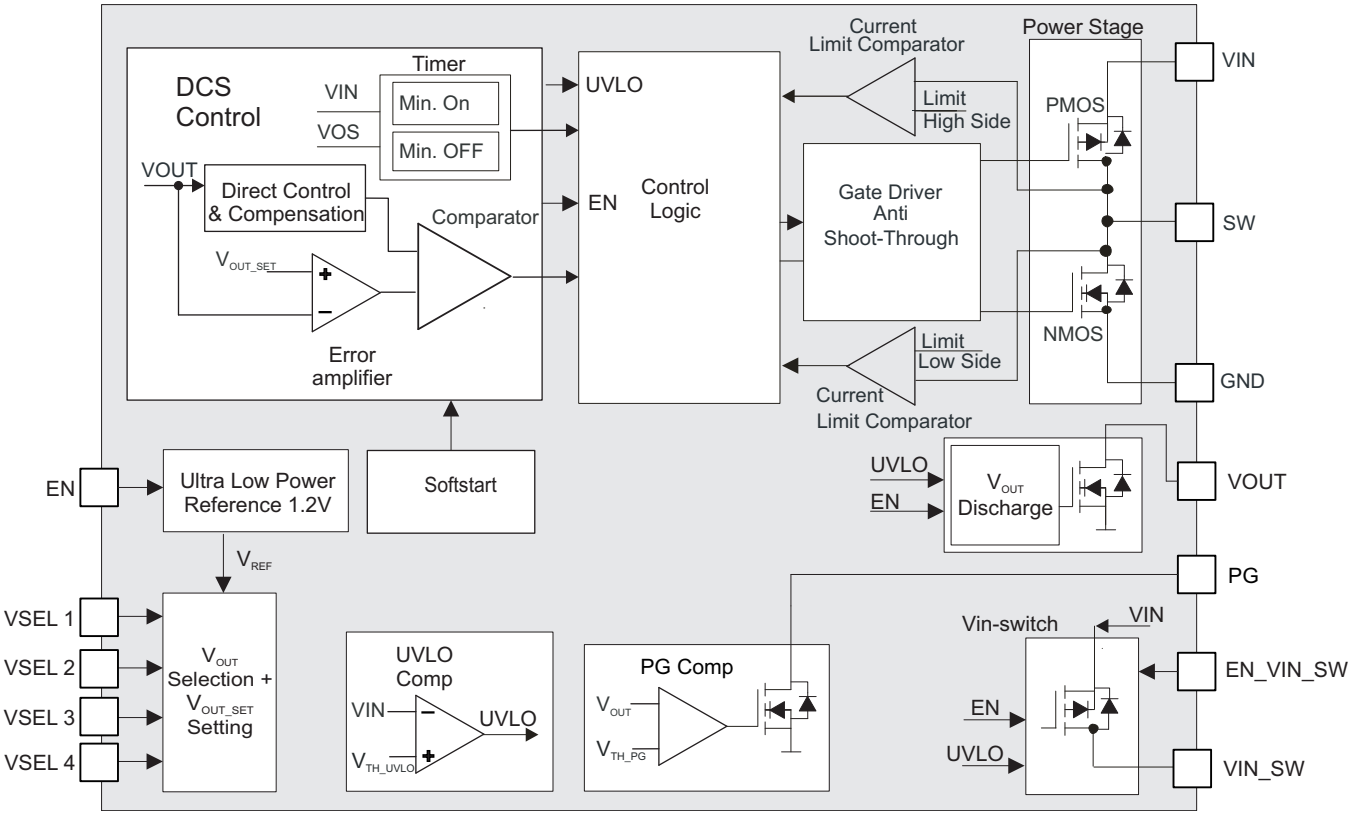


Figure 12. Functional Block Diagram



Features

- Input voltage range VIN from 3.3 V to 10 V
- Typical 400-nA quiescent current
- Up to 90% efficiency with load currents > 15 µA
- Up to 300-mA output current
- Low output ripple voltage
- RF-friendly DCS-Control™
- 16 selectable output voltages from:
  - 1.8 V to 3.3 V (TPS62745)
  - 1.3 V to 2.8 V (TPS627451)
- Integrated input voltage switch
- *Integrated Discharge Function* at VOUT
- *Open Drain Power Good* output
- Operates with a tiny 3.3-µH or 4.7-µH inductor
- Small 3 mm × 2 mm WSON package

2.4.5 TPS727

The TPS727 family of low-dropout (LDO) linear regulators are ultra-low quiescent current LDOs with excellent line and ultra-fast load transient performance and are designed for power-sensitive applications. The LDO output voltage level is preset by the use of innovative factory EEPROM programming. A precision band-gap and error amplifier provides overall 2% accuracy over load, line, and temperature extremes. The TPS727 family is available in 1.5-mm × 1.5-mm SON and wafer chip-scale (WCSP) packages that make the devices ideal for handheld applications. This family of devices is fully specified over a temperature range of T_J = –40°C to +125°C.

Figure 13. Typical Application Circuit

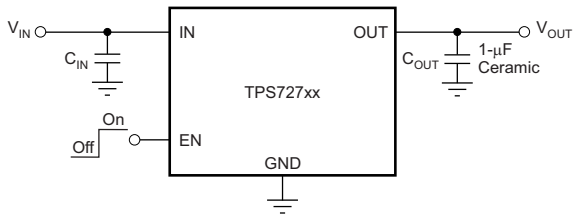


Figure 14. PSRR vs Frequency (VIN – VOUT = 0.3 V, TPS72718)

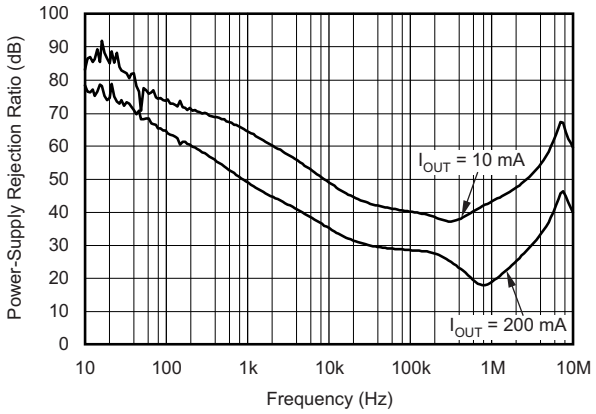
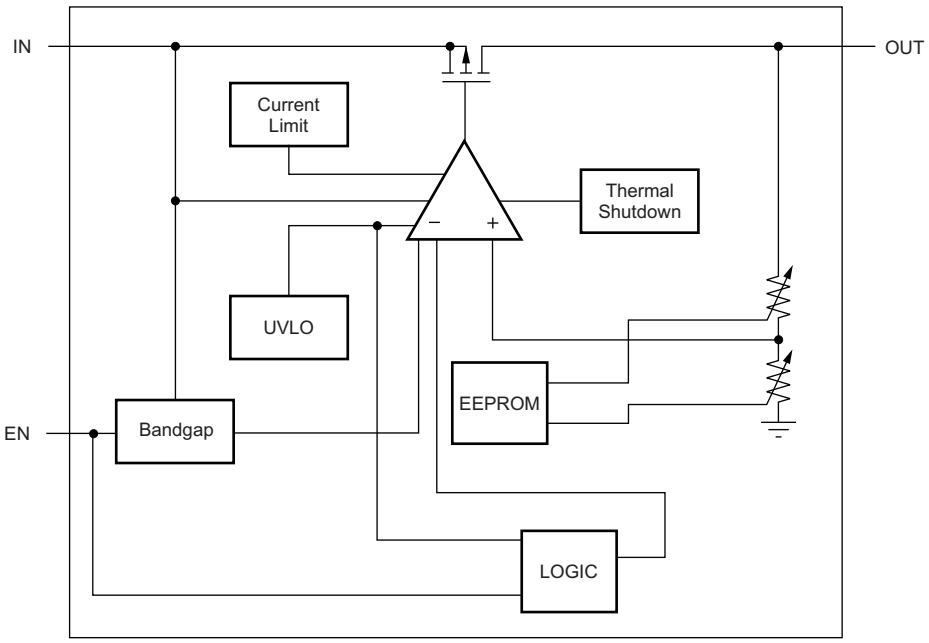


Figure 15. Functional Block Diagram



Features

- Very low dropout:
  - 65 mV Typical at 100 mA
  - 130 mV Typical at 200 mA
  - 163 mV Typical at 250 mA
- 2% Accuracy over load, line, temperature
- Ultra-low I_Q: 7.9 µA
- Excellent load transient performance:±50 mV for 200 mA loading and unloading transient
- Available in fixed-output voltages from 0.9 V to 5 V using innovative factory EEPROM programming
- High PSRR: 70 dB at 1 kHz
- Stable with a 1.0-µF ceramic capacitor
- Thermal shutdown and overcurrent protection
- Available in 4-Ball, 0.4-mm pitch wafer-level chip scale and 1.5-mm × 1.5-mm SON packages

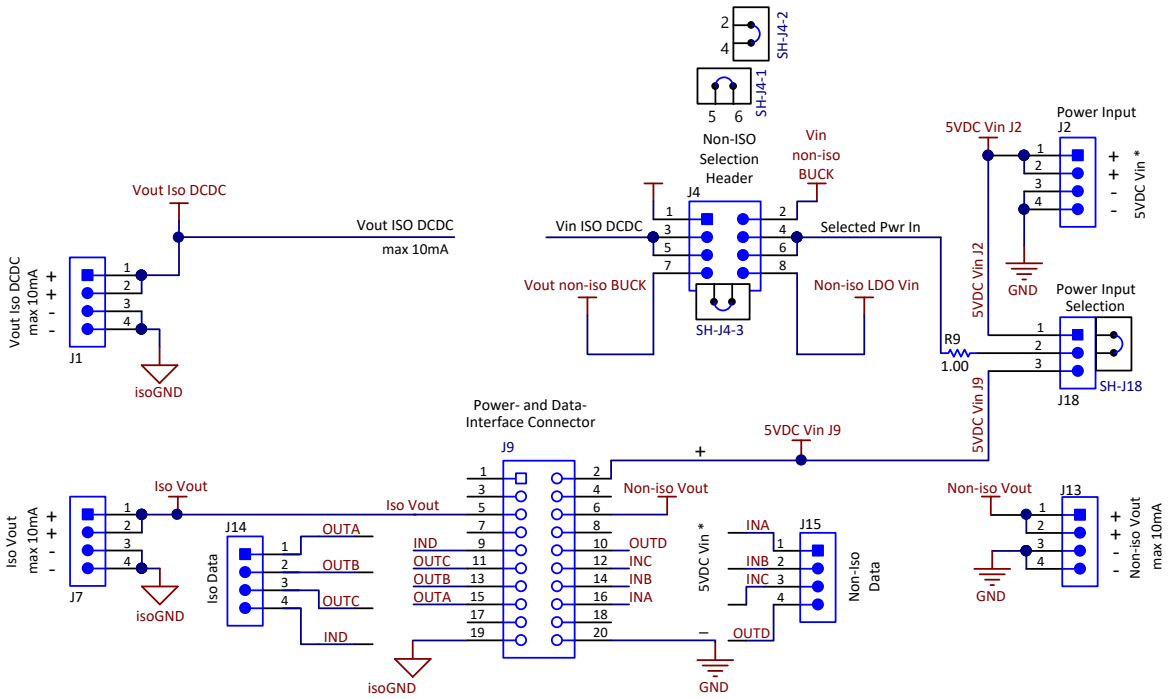
2.5 System Design Theory

The following subsections provide details about the specific circuit block used in this reference design.

2.5.1 Power- and Data-Inputs and –Outputs

Figure 16 shows the specific implementation of the Power- and Data-Inputs and –Outputs in the TIDA-010018 design. The reference design is either powered by using header J2 or receptacle J9 as power input. The selection of the desired power input is done by the Power Input Selection header J18 and the respective jumper SH-J18.

Figure 16. TIDA-010018: Implementation of Power- and Data-Inputs and -Outputs



Shorting pins 1 and 2 of J18 by SH-J18 selects the *5VDC Vin J2* applied on the power input header J2 when the reference design is evaluated in a standalone test setup. Shorting pins 2 and 3 of J18 by the jumper SH-J18 selects the *5VDC Vin J9* applied on the Power- and Data- Interface Connector receptacle J9 when the reference design is evaluated as a plug-on board in conjunction with a specifically-designed hardware. The selected power input is decoupled by resistor R9 from the input bypass capacitors of the connected ISO DC/DC, LDO, or BUCK converter. R9 helps to reduce a possible ringing and input voltage overshoot during power-up. Ringing and input voltage overshoot can be caused by the high-quality, multi-layer ceramic input bypass capacitors of the ISO DC/DC, LDO, or BUCK converter in conjunction with the inductance of the wires used to make the connection to a power source. J4 is the central Non-ISO Selection Header which distributes the *Selected Pwr In* to the ISO DC/DC input and the NON-ISO BUCK. The jumper SH-J4-1 shorts the pins 5 and 6 of J4, the jumper SH-J4-2 shorts pins 2 and 4 of J4 for the purpose of this distribution. The NON-ISO LDO serves as post regulator for the NON-ISO BUCK. The jumper SH-J4-3 shorts pins 7 and 8 of J4 and connects the input *Non-iso LDO Vin* of the NON-ISO LDO with the output of the NON-ISO BUCK, *Vout non-iso BUCK*.

J13 is the header for the *Non-iso Vout*, the regulated 3.3-V output provided by the NON-ISO BUCK or 3-V output provided by the NON-ISO LDO. The specific selection for the 3.3 V from the NON-ISO BUCK is done by using a jumper wire to connect pin 2 of J12 with pin 2 of J8. Alternatively, pin 2 of J12 must be shorted to pin 1 of J12 to select the 3.0 V from the NON-ISO LDO. See Section 2.5.3, NON-ISO BUCK and Section 2.5.4, NON-ISO LDO for details. The *Non-iso Vout* is used to power the non-isolated side of the ISO DATA circuit block (see Section 2.5.7, ISO DATA).

The isolated side of the reference design is powered by the output of the ISO DC/DC (*Vout Iso DCDC* available on header J1). The total current consumption from the output of the ISO DC/DC must be limited to 10 mA. The ISO DC/DC feeds the input *Vin Iso BUCK* of the ISO BUCK via jumper SH-J6 when populated on header J6 (see Section 2.5.5, ISO BUCK). The ISO BUCK provides the 3.3–V *Iso BUCK Vout* which powers the input *Iso LDO Vin* of the ISO LDO when the jumper SH-J19 is populated on the respective header, J19. It is either the 3.3 V from the ISO BUCK or the 3 V from the ISO LDO which is available as *Iso Vout* on the header J7. The *Iso Vout* is used to power the isolated side of the ISO DATA circuit block (see Section 2.5.7, ISO DATA). The selection of where the *Iso Vout* is coming from is done by the jumper setting on header J5. SH-J5 shorting pins 1 and 2 of J5 selects the 3.3 V of the ISO BUCK. Shorting pins 2 and 3 selects the 3.0 V from the ISO LDO instead. The headers J14 and J15 are the digital inputs for the *Iso Data* and for the *Non-Iso Data*.

The majority of the aforementioned headers are targeted for the evaluation of the reference design in a standalone test setup. However, the Power – and Data-Interface Connector J9 is targeted to evaluate the reference design as a plug-on board in conjunction with a specifically-designed hardware. J 9 provides for that purpose, not only the *5VDC Vin J9* for powering the reference design, but feeds the specifically-designed hardware with the *Non-iso Vout* and *Iso Vout* generated by the reference design. Together with the ISO DATA circuit, J9 provides the 4-wire data isolation for the specifically-designed hardware in this test case.

2.5.2 ISO DC/DC

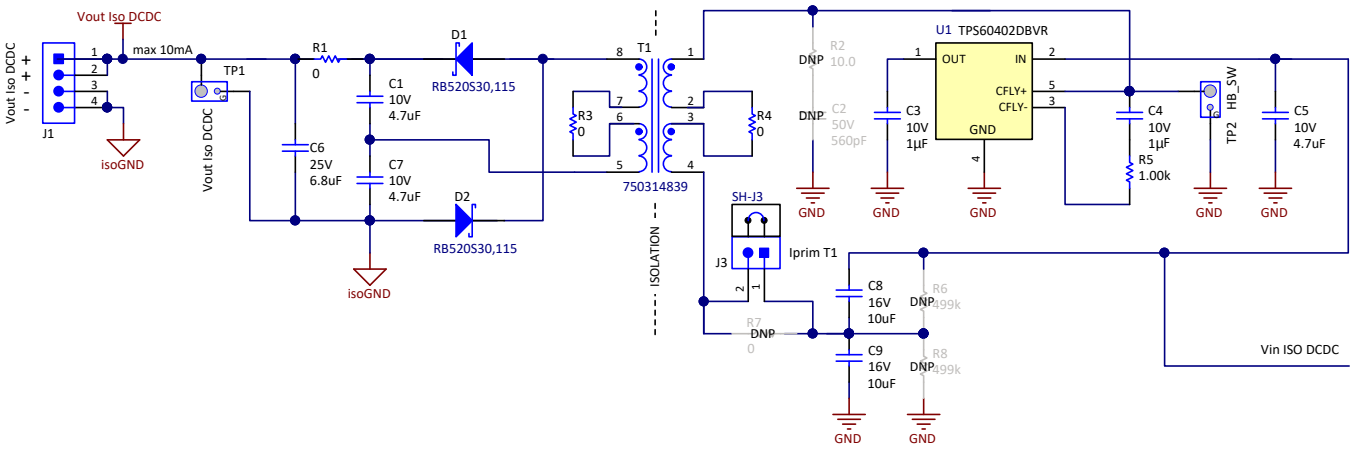
The ISO DC/DC is the main power circuit block of this reference design. Its purpose and performance requirements are directly related to the basic power-related performance requirements of this reference design: providing power-isolation for low- and ultra-low-power applications. The generation of an isolated power rail for medium and high power levels is a general design task for which a wide variety of components, supporting tools, and literature is available.

Design challenges rise-up in case that isolated power rail needs to be generated for low- and ultra-low-power levels below a ten- to twenty-mW power level. This holds especially true when the targeted application requires high-power conversion efficiency or when the input current budget for this power conversion is limited to (ultra-)low levels as has been outlined in Section 1.

The basic solution for this design challenge is provided in the TIDA-00349 tool folder. The complete design theory and the details of their implementation is found in the Uniquely efficient isolated DC/DC converter for ultra-low power and low-power applications reference design manual.

Figure 17 shows the implementation of the ISO DC/DC in the TIDA-010018 design. The input of the ISO DC/DC and *Vin ISO DCDC*, is connected to pins 3 and 5 of the Non-ISO Selection Header J4. The ISO DC/DC is equipped with two dedicated testpoints and one dedicated header, enabling probing of dedicated signals.

Figure 17. TIDA-010018: Implementation of the ISO DC/DC



J1: *Vout Iso DCDC* – accurate measurement of the output voltage of the ISO DC/DC and connecting a load (SMU or resistor decade). Influence of measurement cable voltage drop is eliminated by a four-wire connection, supported by the four-pin header J1.

J3: *Iprim T1* – measurement of the primary winding current of the transformer T1

TP1: *Vout Iso DCDC* – measurement of the output voltage ripple of the ISO DC/DC

TP2: *HB_SW* – probing of the switch node of the ISO DC/DC half bridge power stage

The 2 pins of header J3 are shorted by jumper SH-J3 in the default configuration. Replacing jumper SH-J3 with a self-made jumper wire adapter and positioning a current probe on this jumper wire adapter enables measurement of the primary winding current of the transformer – see Figure 18 and Section 3.2.2.6, Waveforms of ISO DC/DC.

Figure 18. Current Probe with Self-made Adapter Wire for Primary Winding Current Measurement

Figure 19. Probe With Long Ground Lead and Alligator Clip vs Probe With Ground Spring

The reference design contains test points (TP) for all the different circuit blocks to simplify the evaluation of the board. To modify the probe, remove the probe tip cover. In addition, the ground lead and alligator clip must be replaced by a ground spring as Figure 19 shows. The modified probes fit directly into the test points (TP). The small ground spring significantly reduces the noise, which can couple otherwise into the long ground lead of a standard probe configuration.

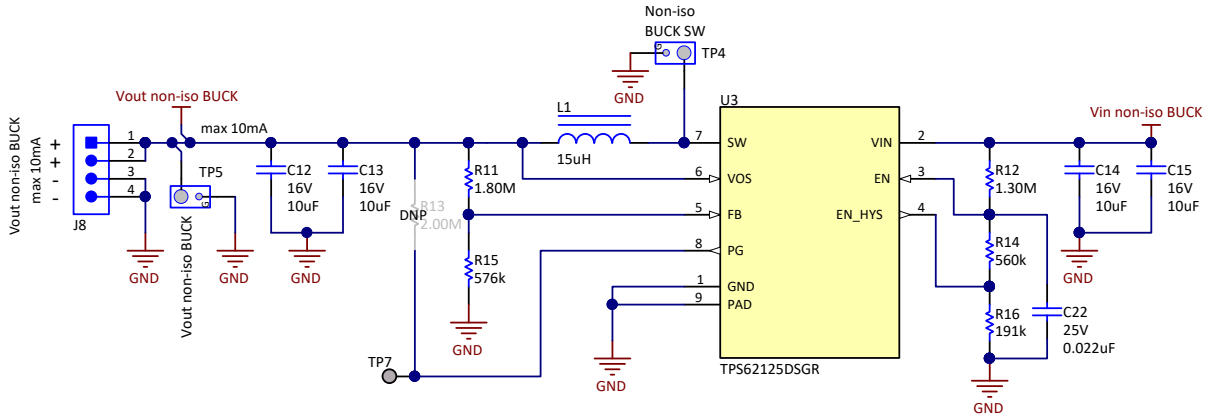
2.5.3 NON-ISO BUCK

Figure 20 shows the implementation of the NON-ISO BUCK in the TIDA-010018 design. The input of the NON-ISO BUCK, *Vin non-iso BUCK*, is connected to pin 2 of the Non-ISO Selection Header J4. The output, *Vout non-iso BUCK*, is connected to pin 7 of J4.

The TPS62125 was selected as buck converter for the following:

- Synchronous rectification for increased efficiency and reduced number of external components
- Power Save Mode for high-power conversion efficiency for the desired ultra-low output currents
- DCS-Control for a small and predictable output voltage ripple in power-save mode
- Precision enable and programmable hysteresis for user-programmable UVLO

Figure 20. TIDA-010018: Implementation of the NON-ISO BUCK



C14 and C15 act as input bypass capacitors. Resistors R12, R14, and R16 are selected to provide the user-programmable UVLO and hysteresis. Following the “Enable Threshold and Hysteresis Setting” section of the *TPS62125 3-V to 17-V, 300-mA Step-Down Converter With Adjustable Enable Threshold and Hysteresis* data sheet, the voltage for the start-up of the TPS62125 device is 3.985 V and 3.14 V for the stop level, respectively. The additional capacitor Cxx which is connected in parallel to the series connection of R14 and R16 provides an additional delay during which the input voltage of the TPS6125 device can rise to an even higher voltage level. The higher voltage increases the stored energy in C14 and C15 which provides a smooth start-up of the NON-ISO BUCK. This is especially important if there is a decreased input current limit.

Resistors R11 and R15 form the output voltage divider and set *Vout non-iso BUCK* at 3.3 V. The inductor L1 form together with the output capacitors C12 and C13 the LC output filter of the NON-ISO BUCK. Their selections follow the recommendations given in the “Output Filter Design” section of the TPS62125 data sheet. The use of C12 and C13 with a total 20-µF capacitance helps for a smooth startup of the NON-ISO LDO.

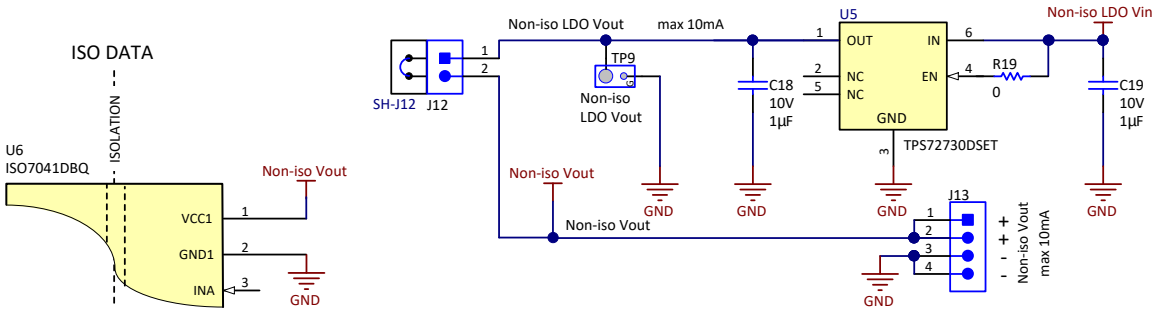
The NON-ISO BUCK is equipped with two dedicated testpoints and one dedicated header, enabling probing of dedicated signals:

- J8: *Vout non-iso BUCK* – accurate measurement of the output voltage of the NON-ISO BUCK and connecting a load (SMU or resistor decade). Influence of measurement cable voltage drop is eliminated by a four-wire connection, supported by the four-pin header J8.
- TP4: *Non-iso BUCK SW* - probing of the switch node of the NON-ISO BUCK power stage.
- TP5: *Vout non-iso BUCK* – measurement of the output voltage ripple of the NON-ISO BUCK.

2.5.4 NON-ISO LDO

Figure 21 shows the specific implementation of the NON-ISO LDO in the TIDA-010018 design. The input of the NON-ISO LDO, *Non-iso LDO Vin,* is connected to pin 8 of the Non-ISO Selection Header J4. The output of the NON-ISO LDO, *Non-iso LDO Vout*, is connected to pin 1 of the header J12.

Figure 21. TIDA-010018: Implementation of the NON-ISO LDO



The main purpose of NON-ISO LDO circuit block is to remove the remaining output ripple voltage of the NON-ISO BUCK. The LDO is a 3.0-V version of the TPS727 LDO-family. The TPS727 devices consume extremely low quiescent current while simultaneously delivering excellent PSRR with very little headroom (VIN – VOUT differential voltage), and very good transient response. These features are combined with low noise without a noise-reduction pin.

The output voltages of the NON-ISO BUCK and the NON-ISO LDO have been selected in a way, that the input voltage of the LDO is 300 mV higher than its regulated output voltage. This 300-mV headroom is desired to compensate for the output voltage tolerances of the NON-ISO BUCKs and NON-ISO LDOs, and to enable the desired high PSRR and low I_Q of the LDO. The TPS727 does not require an output voltage divider and provides improved output voltage accuracy.

C19 is the input bypass capacitor, C18 acts as output capacitor of the LDO. The TPS727 device has an internal soft start, ramping up the output voltage of the device with a typical slope of 0.07 V/µs which is independent of the output capacitor. Remember that such a fixed output voltage ramp-up slope requires a dedicated current to be delivered by the LDO and by the upstream buck converter. The *TPS727 250-mA, ultra-low I_Q, fast transient response, RF low-dropout linear regulator* data sheet gives a current demand of 70 mA as an example for a 1-µF output capacitor during its soft start. The current demand scales linearly with the total output capacitance of the LDO (the output capacitor of the LDO plus bypass capacitors of the connected downstream load). The current consumption of the connected downstream load must be added to this current demand. More details are found in the *Soft Start* section of the *TPS727* data sheet.

As previously mentioned, the increased current during start-up is mainly provided by the input capacitor of the LDO and the output- and input- capacitors of the upstream buck converter. This leads to dropping voltages of those capacitors, because this reference design requires being powered by a power source which shall not exceed the maximum ratings of 5.25 VDC, 30 mA. The dropping input voltages of the NON-ISO BUCK and of the NON-ISO LDO might cause the UVLO-OFF level of those devices to be reached and that those devices need multiple attempts to start.

The NON-ISO LDO is equipped with a dedicated testpoint and two dedicated headers, enabling probing of dedicated signals:

- J12 – pin1: *Non-iso LDO Vout* – accurate measurement of the output voltage of the NON-ISO LDO and connecting a load (SMU or resistor decade) when jumper SH-J12 is not populated.
- SH-J12 – shorts pins 1 and 2 of J12 when jumper is populated – powers the non-isolated side of the ISO DATA block of the reference design
- J13: *Non-iso Vout* – Supply voltage of non-isolated side of the ISO DATA block of the reference design.
- TP9: *Non-iso LDO Vout* - probing of the output voltage of the NON-ISO LDO.

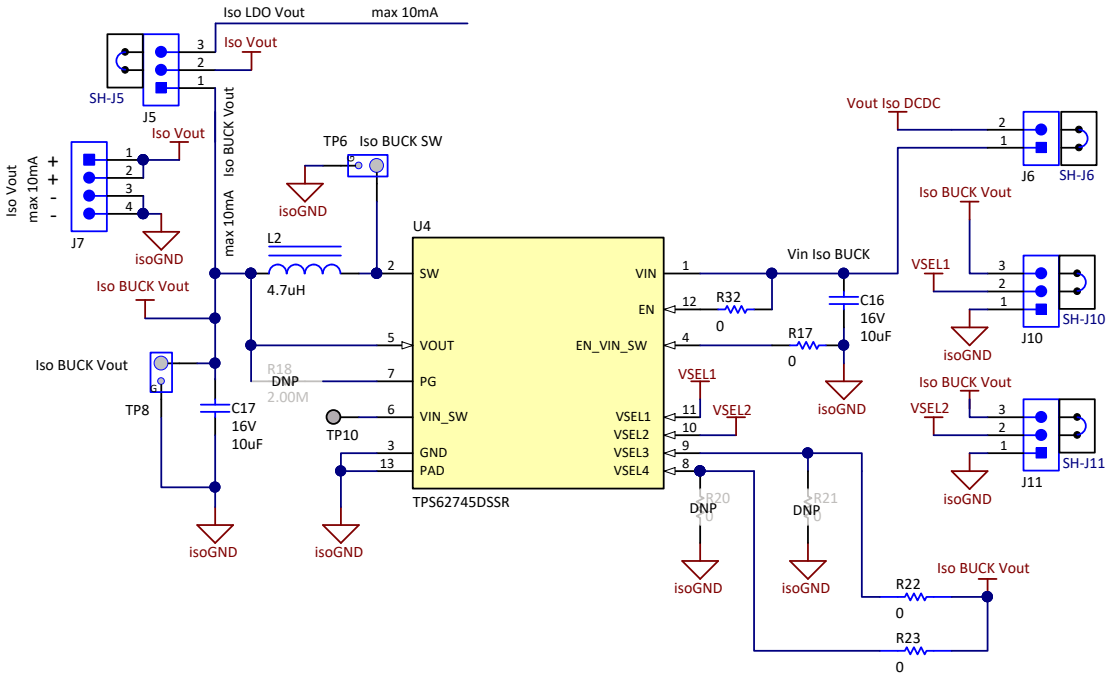
2.5.5 ISO BUCK

Figure 22 shows the implementation of the ISO BUCK in the TIDA-010018 design. The input of the ISO BUCK, *Vin Iso BUCK*, is connected to pin 1 of header J6.

The TPS62745 was selected as buck converter due to the following:

- 3.3- to 10-V input voltage range for tolerating rising output voltage of ISO DC/DC under no-load and light load conditions, see Figure 27
- Synchronous rectification for increased efficiency and reduced number of external components
- Ultra-low 400-nA quiescent current and power save mode for high-power conversion efficiency for the desired ultra-low output currents. This helps to compensate the losses of the ISO DC/DC - especially at ultra-low output currents.
- DCS-Control for a small and predictable output voltage ripple in power-save mode
- Selectable fixed output voltages for increased output voltage accuracy and reduced number of external components

Figure 22. TIDA-010018: Implementation of the ISO BUCK



C16 acts as input bypass capacitor. Resistors R22, R23 and the headers J10 and J11 together with the default setting of the jumpers SH-J10 and SH-J11 set the output voltage of the ISO BUCK, *Iso BUCK Vout* to a fixed voltage of 3.3 V. More details about the output voltage setting over the full 1.8-V to 3.3-V range are in the “Output Voltage Setting for TPS62745” table in the TPS62745 dual-cell ultra-low I_Q step-down converter for low-power wireless applications data sheet. The inductor L2 and the output capacitor C17 form the LC output filter of the ISO BUCK. Their selections follow the recommendations given in the “Output Filter Design” section of the TPS62745 data sheet.

Because the VIN-switch TPS62745 is not used in this reference design, R17 is utilized to tie the EN_VIN_SW-pin of the TPS62745 to isoGND.

The ISO BUCK is equipped with two dedicated testpoints and one dedicated header, enabling probing of dedicated signals:

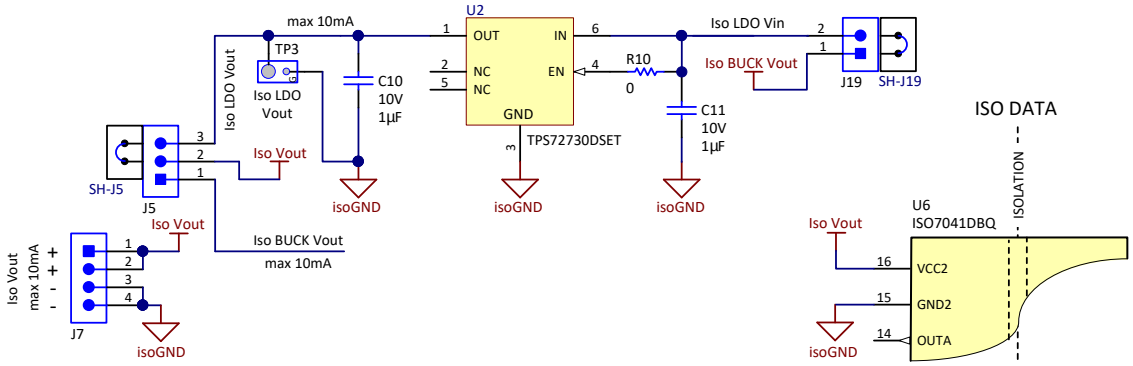
- J5 – pin 1: *Iso BUCK Vout* – accurate measurement of the output voltage of the ISO BUCK and connecting a load (SMU or resistor decade) when jumper SH-J5 is not populated.
- TP6: *Iso BUCK SW* - probing of the switch node of the ISO BUCK power stage.
- TP8: *Iso BUCK Vout* – measurement of the output voltage ripple of the NON-ISO BUCK.

2.5.6 ISO LDO

Figure 23 shows the specific implementation of the ISO LDO in the TIDA-010018 design. The input of the ISO LDO, *Iso LDO Vin*, is connected to pin 2 of header J19.

The main purpose of the ISO LDO circuit block is to remove the remaining output ripple voltage of the ISO BUCK. The explanations as given in the NON-ISO LDO-section Section 2.5.4regarding the features and operation of the LDO in conjunction with its upstream buck converter and with the load of the LDO are valid for the ISO LDO too.

Figure 23. TIDA-010018: Implementation of the ISO LDO



C11 is the input bypass capacitor, C10 acts as output capacitor of the ISO LDO. The ISO LDO is equipped with a dedicated testpoint and one dedicated header, enabling probing of dedicated signals:

- J5 – pin 3: *Iso LDO Vout* – accurate measurement of the output voltage of the ISO LDO and connecting a load (SMU or resistor decade) when jumper SH-J5 is not populated.
- TP3: *Iso LDO Vout* - probing of the output voltage of the ISO LDO

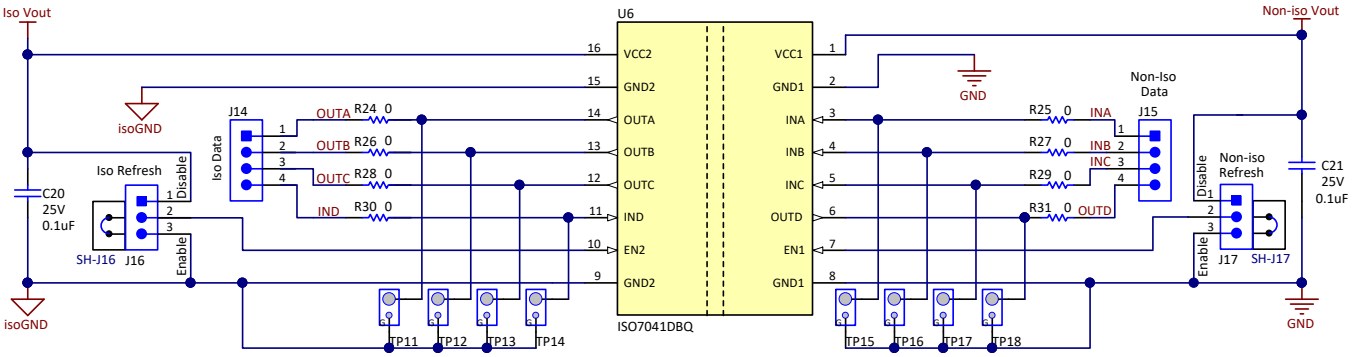
2.5.7 ISO DATA

Figure 24 shows the implementation of the Isolated Data Interface in the TIDA-010018 design.

The ultra-low power, multi-channel digital isolator ISO7041 is selected to isolate the digital I/Os on the isolated side (*Iso Data* on J14) from the ones on the non-isolated side (*Non-iso Data* on J15). The per channel dynamic current consumption of the device is under 120 µA/Mbps and the per channel static current consumption is 4.2 µA at 3.3 V, allowing for use of the ISO7041 in power constrained system designs such as in this reference design.

The ISO7041 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high-frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. The ENx pins of side A and side B must be tied low to enable refresh or high to disable refresh. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching.

Figure 24. TIDA-010018: Implementation of the ISO DATA



This reference design features one transmit channel and three receive channels on the isolated side and three transmit- and one receive-channel on the non-isolated side.

The VCC1 supply voltage pin 1 on the non-isolated side of the ISO7041 device is powered from *Non-iso Vout* and is connected to pin 2 of J12 and to pins 1 and 2 of J13.

Similarly, the VCC2 supply voltage pin 16 on the isolated side is powered from *Iso Vout* and is connected to pin 2 of J5 and to pins 1 and 2 of J7.

Headers J16 and J17 together with their respective jumpers SH-J16 and SH-J17 serve the purpose of enabling (jumpers shorting pins 2 and 3) or disabling (jumpers shorting pins 1 and 2) the refresh feature of the ISO7041.

The ISO DATA block is equipped with two headers, and eight testpoints for connecting and probing of the 4 I/Os on the isolated and on the non-isolated side of this reference design. All the I/Os as well as the *Iso Vout* and the *Non-iso Vout* are additionally available on the Interface Connector J9 on the bottom side of the PCB:

- J14 and J9: *OUTA, OUTB, OUTC, IND* – connecting the four I/Os on the isolated side
- J15 and J9: *INA, INB, INC, OUTD* - connecting the four I/Os on the non-isolated side
- TP11 to TP14: *OUTA, OUTB, OUTC, IND* - probing of the four I/Os on the isolated side
- TP15 to TP18: *INA, INB, INC, OUTD* - probing of the four I/Os on the non-isolated side

3 Hardware, Software, Testing Requirements, and Test Results

CAUTION

This reference design is made available for parameter performance evaluation only and is not intended for isolation voltage testing.

To prevent damage to the reference design, any voltage applied as a supply or digital I/O must be maintained within the recommended operating range as given in the data sheet of the devices used.

WARNING

To minimize the risk of fire, the power source used must not exceed the maximum ratings of 5.25 VDC, 30 mA. Refer to the user guide.

Use only the top-side header J2 *or* **the bottom-side** *Power- and Data-Interface Connector* **(receptacle J9) as the power input for the reference design.**

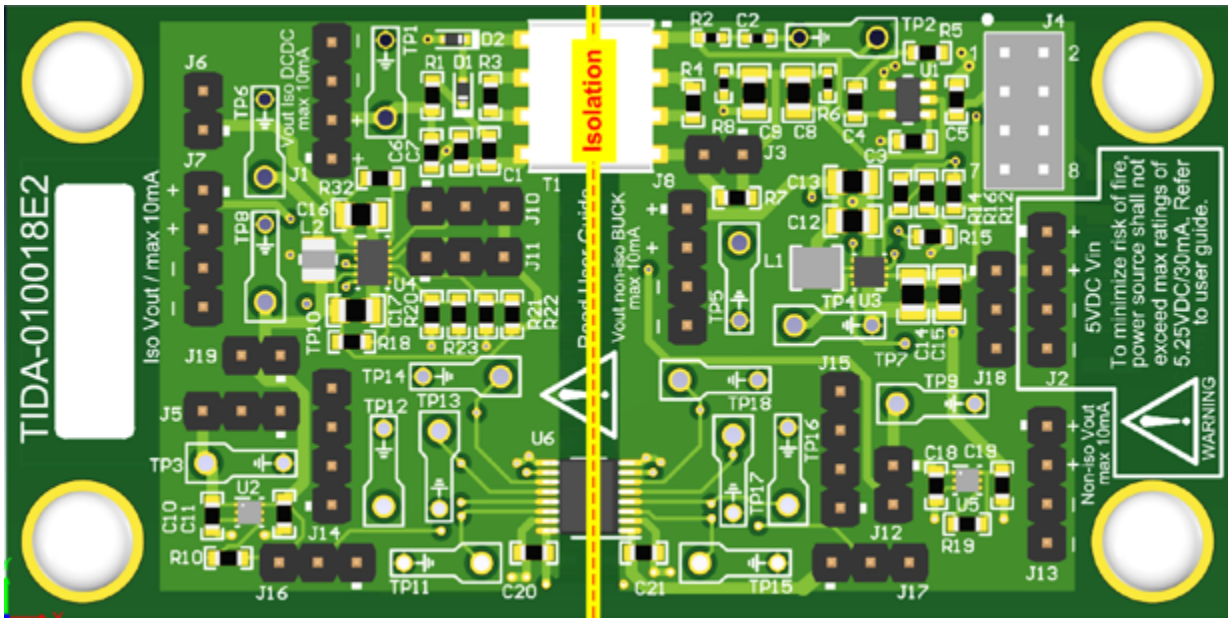
Use the *Power Input Selection* **header (J18) and related jumper SH-J18 to select either J2 or J9 as the sole power input of the reference design.**

3.1 Required Hardware and Software

3.1.1 Hardware

Figure 25 is the top view of the reference design board. All of the integrated circuits (TPS60402, TPS62125, TPS62745, TPS727, and ISO7041) are located on the top side of PCB. The left side of the board is the isolated side and the right side is the non-isolated side of this reference design.

Figure 25. TIDA-010018: Top View



3.1.1.1 Used Headers and Receptacles

Table 2 shows the functions of the different headers and receptacles.

Table 2. Header and Receptacle Functions

HEADERS ON TOP SIDE	DESCRIPTION
J1	*Vout Iso DCDC*: Output of ISO DC/DC
J2	*5VDC Vin*: sole power input for board evaluation in a standalone test setup, see Section 3 and Section 2.2
J3	Measurement of the T1 primary winding current of the transformer
J4	Non-ISO Selection Header: selects connections of *Vin ISO DCDC*, *Vin non-iso BUCK*, *Vout non-iso BUCK*, *Non-iso LDO Vin* and *Selected Pwr In*
J5	*Iso Vout* selection: selects either *Iso LDO Vout* or *Iso BUCK Vout* as the *Iso Vout* on J7 on the board
J6	Connects *Vin Iso BUCK* to *Vout Iso DCDC*
J7	*Iso Vout*: *Iso Vout* output selected by J5, powers isolated side of ISO DATA
J8	*Vout non-iso BUCK*: Output of NON-ISO BUCK
J10, J11	*Iso BUCK Vout* voltage setting: seeSection 2.5.5
J12	J12 sets NON-ISO LDO to provide *Non-iso Vout* on J13
J13	*Non-iso Vout*: *Non-iso Vout* output, connected by J12 to NON-ISO LDO, powers non-isolated side of ISO DATA
J14	*Iso Data:* Data interface connector on isolated side of the ISO7041 device
J15	*Non-iso Data*: Data interface connector on non-isolated side of the ISO7041 device
J16, J17	Refresh enable for ISO7041: Enabled when related jumpers SH-J16 and SH-J17 short pins 2 and 3, disabled when shorting pins 1 and 2. Identical jumper settings on J16 and J17 needed, see datasheet of ISO7041

Table 2. Header and Receptacle Functions (continued)

HEADERS ON TOP SIDE	DESCRIPTION
J18	*5VDC Vin* power source selection: selects either J2 or J9 as the boards sole power input for IsoDCDC and Non-isoBuck, see Section 3, Section 2.2 Jumper SH-J18 shorts pins 1 and 2 of J18: J2 is sole power input Jumper SH-J18 shorts pins 2 and 3 of J18: J9 is sole power input
J19	Connects *Iso LDO Vin* to *Iso BUCK Vout*
RECEPTACLE ON BOTTOM SIDE	**DESCRIPTION**
J9	Power- and Data-Interface Connector : data interface and sole power input for board evaluation as a plug-on board in conjunction with a specifically designed hardware, see Section 3 and Section 2.2

3.1.1.2 Jumper Setting

Figure 26 shows the default jumper settings of the TIDA-010018 board for a standalone test setup. Details are provided in Table 3.

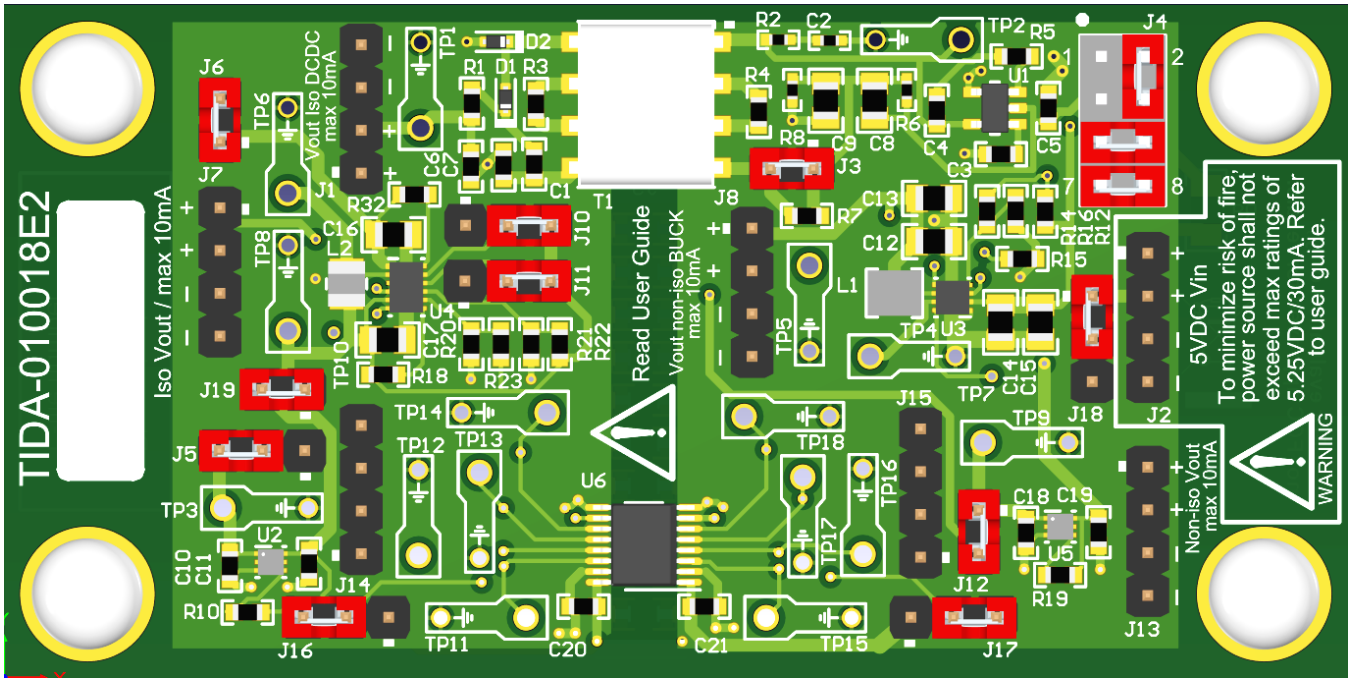
Header J2 is configured by jumper SH-J18 on header J18 to act as the sole power input of the reference design. The respective Buck is followed by the respective LDO as a post regulator for both sides (isolated and non-isolated) of the design.

The isolated and non-isolated side of the ISO DATA block is powered by the 3-V outputs of the respective LDOs. The refresh logic is enabled on both sides of the digital isolator U6.

Table 3. TIDA-010018: Default Jumper Settings - Standalone Test Setup

HEADER		CONNECTED BY	HEADER		COMMENT
	PIN #			PIN #	
J3	1	SH-J3	J3	2	Replace SH-J3 with self-made adapter wire to measure the primary winding current of transformer T1 - *Iprim T1* - with a current probe
J4	2	SH-J4-2	J4	4	Connects *Vin non-iso BUCK* to *Selected Pwr In*
	5	SH-J4-1		6	Connects *Vin ISO DCDC* to *Selected Pwr In*
	7	SH-J4-3		8	Connects *Non-iso LDO Vin* to *Vout non-iso BUCK*
J5	2	SH-J5	J5	3	Connects *Iso Vout* to *Iso LDO Vout*
J6	1	SH-J6	J6	2	Connects *Vin Iso BUCK* to *Vout Iso DCDC*
J10, J11	2	SH-J10, SH-J11	J10, J11	3	Connects *VSEL1* and *VSEL2* to *Iso BUCK Vout* -resulting in 3.3 V for *Iso BUCK Vout*
J12	1	SH-J12	J12	2	Connects *Non-iso Vout* to *Non-iso LDO Vout*
J16, J17	2	SH-J16, SH-J17	J16, J17	3	Enables Refresh for the *Digital Isolator* U6
J18	1	SH-J18	J18	2	*Power Input Selection* - selects header J2 as sole *Power Input (5VDC Vin)*
J19	1	SH-J19	J19	2	Connects *Iso LDO Vin* to *Iso BUCK Vout*

Figure 26. TIDA-010018: Default Jumper Settings - Standalone Test Setup



3.1.2 Software

There is no software related to this reference design.

3.2 Testing and Results

3.2.1 Test Setup

To test the efficiency of every single circuit block and their combination, the first channel of a dual-channel SMU (Keysight B2912A) was used to power the board. A input voltage up to 5.25 V, limited to 30 mA, was applied on pin 1 of the Power Input header J2, referenced to pin 3(*GND*) of J2. Pin 2 and 4 of J2 have been used as sense terminals for the input of the voltmeter of the SMU which features a high-input impedance.

Table 4 shows the Basic connection of Power Input Header J2 and Basic Jumper Setting of Power Input Selection Header J18.

The output current and output voltage of the circuit blocks under test were controlled and measured by SMU.

Pin 1 and 2 of header J18 are shorted to select J2 as sole power input.

For every test setting in Table 4, the 1-Ω resistor, R9, is included in the circuit. Test results have been retroactively adjusted by removing the losses caused by R9.

Table 4. Basic Connection of Power Input Header J2 and Basic Jumper Setting of Power Input Selection Header J18

POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
SMU-Ch1-Force-High (red)	Test leads banana plug to 0.64-mm square pin socket	J2	1				
SMU-Ch1-Sense-High (red)			2				
SMU-Ch1-Force-Low (black)			3				
SMU-Ch1-Sense-Low (black)			4				
		J18	1	Jumper	J18	2	

3.2.2 Test Results

3.2.2.1 ISO DC/DC

The output of ISO DC/DC is loaded on header J1 with a current ranging from 10 μA to 10 mA.

Table 5 shows the connection and jumper setting for the efficiency test of the ISO DC/DC.

Table 5. Connection and Jumper Setting for the Efficiency Test of the ISO DC/DC

POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
SMU-Ch2-Force-High (red)	Test leads banana plug to 0.64-mm square pin socket	J1	1		J1	1	Connect Reverse Protection Diode - Cathode
SMU-Ch2-Sense-High (red))			2				
SMU-Ch2-Force-Low (black)			3		J1	3	Connect Reverse Protection Diode – Anode
SMU-Ch2-Sense-Low (black)			4				
		J4	5	Jumper	J4	6	
		J3	1	Jumper	J3	2	

Figure 27 through Figure 29 show the resulting graphs of those measurements.

Figure 27. ISO DC/DC Efficiency and VOUT vs IOUT, VIN as Parameter

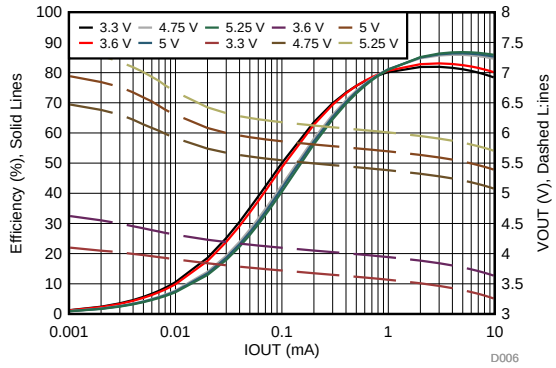


Figure 28. ISO DC/DC Efficiency and IIN vs IOUT, VIN as Parameter

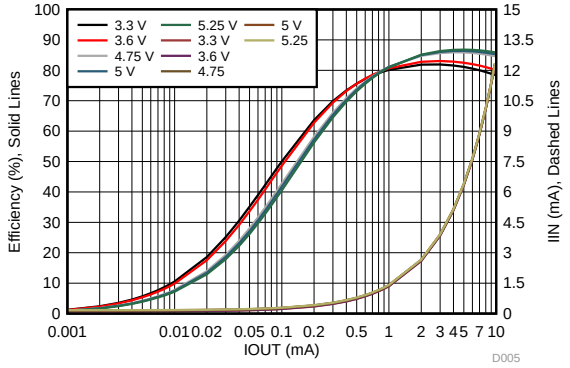
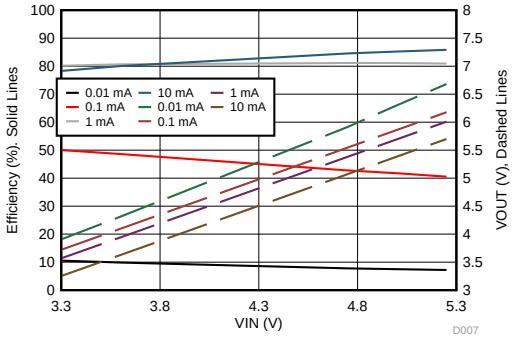


Figure 29. ISO DC/DC Efficiency and VOUT vs VIN, IOUT as Parameter



3.2.2.2 ISO BUCK

With pin 2 and 3 of header J10 shorted and pin 2 and 3 of header J11 shorted, the output voltage of ISO BUCK is 3.3 V.

The output of IsoBuck is loaded by channel 2 of the SMU with a current ranging from 10 μA to 10 mA.

Table 6 shows the connection and jumper setting for the efficiency test of the ISO BUCK .

Table 6. Connection and Jumper Setting for the Efficiency Test of the ISO Buck

POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
SMU-Ch2-Force-High (red)	Test leads banana plug to 0.64-mm square pin socket	J5	1		J5	1	Connect Reverse Protection Diode - Cathode
SMU-Ch2-Sense-High (red))							
SMU-Ch2-Force-Low (black)		J7	3		J7	3	Connect Reverse Protection Diode – Anode
SMU-Ch2-Sense-Low (black)			4				
		J4	6	Jumper Wire	J6	1	
		J13	4	Jumper Wire	J7	4	
		J10	2	Jumper	J10	3	
		J11	2	Jumper	J11	3	

Figure 30 and Figure 31 show the resulting graphs of those measurements.

Figure 30. ISO BUCK: Efficiency and VOUT vs IOUT, 3.3 V Output, VIN as Parameter

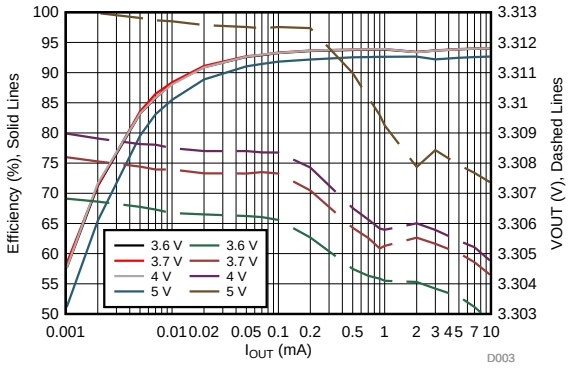
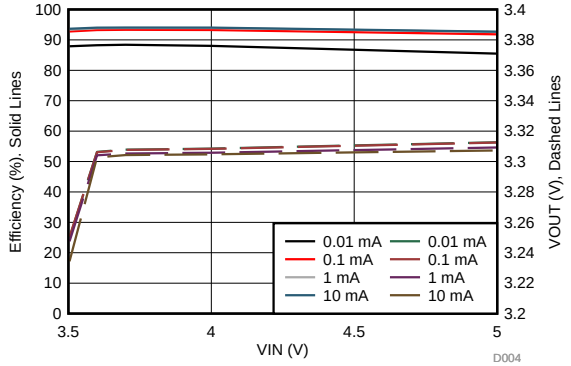


Figure 31. ISO BUCK: Efficiency and VOUT vs VIN, 3.3-V Output, IOUT as Parameter



3.2.2.3 NON-ISO BUCK

The output voltage of the NON-ISO BUCK is set to 3.3 V by the feedback resistors R11 (1.8 MΩ) and R15 (576 kΩ).

The output of NON-ISO BUCK is loaded by channel 2 of the SMU with a current ranging from 10 μA to 10 mA.

Table 7 shows the connection and Jumper Setting for the NON-ISO BUCK efficiency test.

Table 7. Connection and Jumper Setting for NON-ISO BUCK Efficiency Test

POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
SMU-Ch2-Force-High (red)	Test leads banana plug to 0.64-mm square pin socket	J8	1		J8	1	Connect Reverse Protection Diode - Cathode
SMU-Ch2-Sense-High (red)			2				
SMU-Ch2-Force-Low (black)			3		J8	3	Connect Reverse Protection Diode – Anode
SMU-Ch2-Sense-Low (black)			4				
		J4	2	Jumper	J4	4	

Figure 32 and Figure 33 show the resulting graphs of those measurements.

Figure 32. NON-ISO BUCK: Efficiency and VOUT vs IOUT, 3.3-V Output, VIN as Parameter

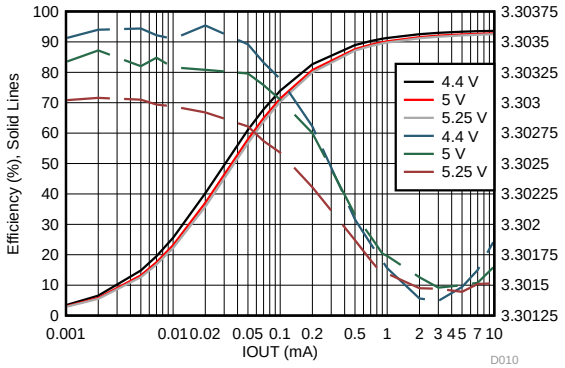
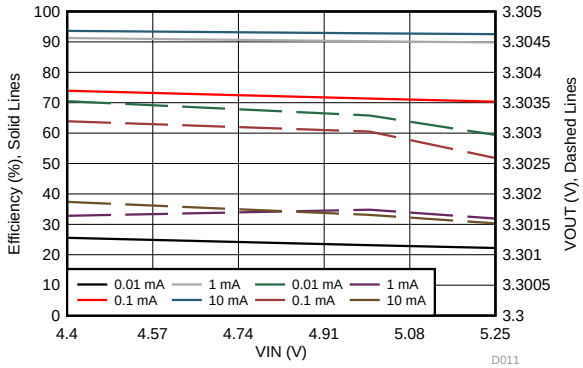


Figure 33. NON-ISO BUCK: Efficiency and VOUT vs VIN, 3.3-V Output, IOUT as Parameter



3.2.2.4 LDOs

The NON-ISO LDO is tested representatively for both - the ISO LDO and the NON-ISO LDO. The output of LDO is loaded by channel 2 of the SMU with a current ranging from 10 μA to 10 mA.

Table 8 shows the connection and jumper setting for LDO efficiency test.

Table 8. Connection and Jumper Setting for LDO Efficiency Test

POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
SMU-Ch2-Force-High (red)	Test leads banana plug to 0.64-mm square pin socket	J12	1		J12	1	Connect Reverse Protection Diode - Cathode
SMU-Ch2-Sense-High (red)			1				
SMU-Ch2-Force-Low (black)		J8	3		J8	3	Connect Reverse Protection Diode – Anode
SMU-Ch2-Sense-Low (black)			4				
		J4	6	Jumper	J4	8	

Figure 34 and Figure 35 show the resulting graphs of those measurements.

Figure 34. LDOs: Efficiency and VOUT vs IOUT, 3 V Output, VIN as parameter

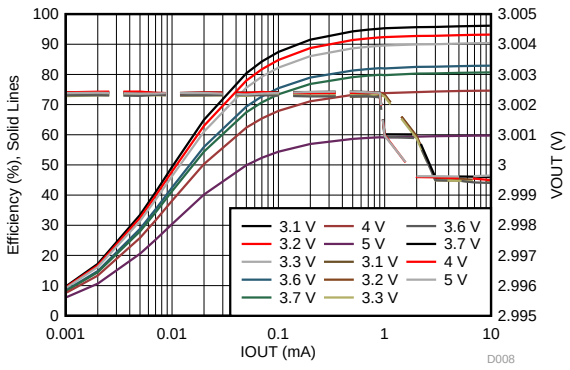
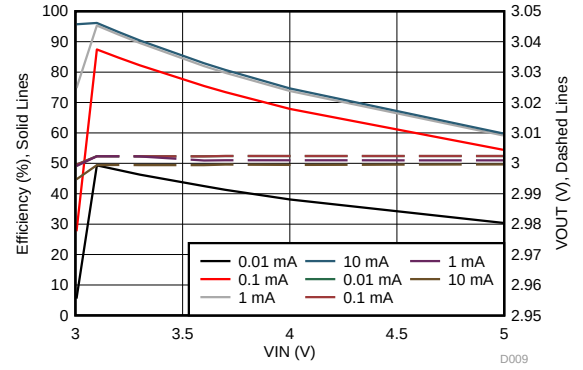


Figure 35. LDOs: Efficiency and VOUT vs VIN, 3V Output, IOUT as parameter



3.2.2.5 Combination (ISO DC/DC, ISO BUCK and NON-ISO BUCK)

The efficiency of combination ISO DC/DC, ISO BUCK, and NON-ISO BUCK have been tested in depth.

Figure 36 shows the combined efficiency and total input current versus output current graphs of test 1. The output current of ISO BUCK is controlled by channel 2 of the SMU, varying from 100 μA to 10 mA. The NON-ISO BUCK is resistively loaded to provide 5 different constant output current levels. The output voltage of both, ISO BUCK and NON-ISO BUCK, is 3.3 V

Figure 37 shows the combined efficiency and total input current versus output current graphs of test 2 in which the output current of the NON-ISO BUCK is controlled by channel 2 of the SMU and the ISO BUCK is loaded resistively. The output voltage of both, ISO BUCK and NON-ISO BUCK, is 3.3 V.

Table 9 shows the connection and jumper setting for combination efficiency test.

Table 9. Connection and Jumper Setting for Combination Efficiency Test

POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
SMU-Ch2-Force-High (red)	Test leads banana plug to 0.64-mm square pin socket	J5 for test 1, J8 for test 2	1		J5 for test 1, J8 for test 2	1	Connect Reverse Protection Diode - Cathode
SMU-Ch2-Sense-High (red)			1 for test 1, 2 for test 2				
SMU-Ch2-Force-Low (black)		J7 for test 1, J8 for test 2	3		J7 for test 1, J8 for test 2	3	Connect Reverse Protection Diode – Anode
SMU-Ch2-Sense-Low (black)			4				
Resistance Decade - red - in series with ammeter		J8 for test 1, J5 for test 2	1				Ammeter in series to the resistance decade, set resistance decade to needed load current
Resistance Decade - black		J8 for test 1, J7 for test 2	3				
		J4	2	Jumper	J4	4	
		J4	5	Jumper	J4	6	
		J3	1	Jumper	J3	2	
		J6	1	Jumper	J6	2	

Figure 36 and Figure 37 show the resulting graphs of those measurements.

Figure 36. Combined Efficiency and Total IIN vs. IOUT of ISO BUCK - Test 1 - IOUT of NON-ISO BUCK as Parameter

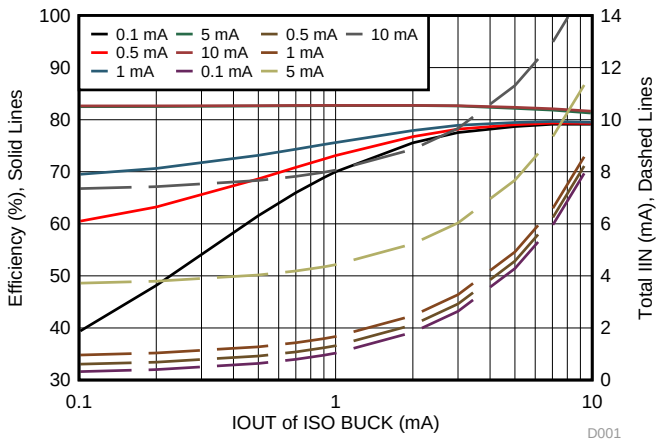
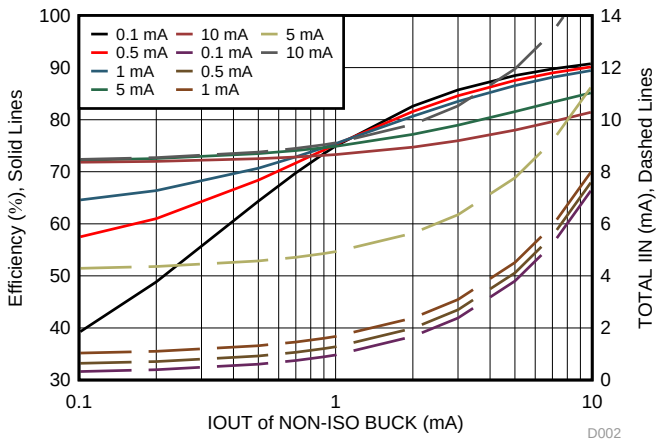


Figure 37. Combined Efficiency and Total IIN vs. IOUT of NON-ISO BUCK - Test 2 - IOUT of ISO BUCK as Parameter



3.2.2.6 Waveforms of ISO DC/DC

The waveforms have been measured at an input voltage of 5 V and 100 µA, 1 mA and 10 mA Iout.

Figure 38 to Figure 40 show the switch node voltage, primary current and output voltage ripple at load currents of 100 µA, 1 mA and 10 mA.

Oscilloscope—channel assignment:

- CH1: Output Voltage Ripple on TP1 - *Vout Iso DCDC*
- CH2: Switch-node voltage measured on TP2 - *HB_SW*
- CH3: Primary current measured with current probe on J3 - *Iprim T1*, see Figure 18

Figure 38. ISO DC/DC Waveforms at Vin = 5 V and Iout = 100 µA

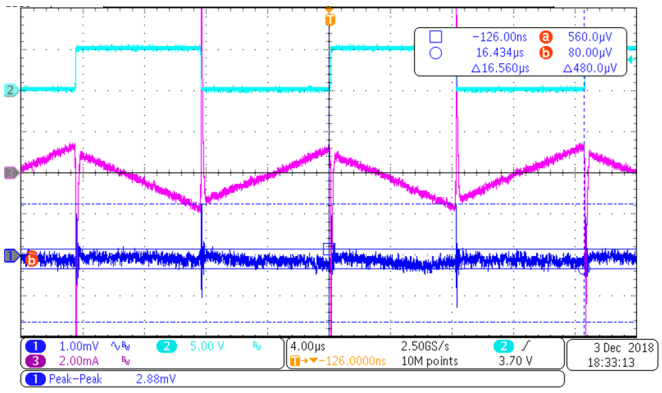


Figure 39. ISO DC/DC Waveforms at Vin = 5 V and Iout = 1 mA

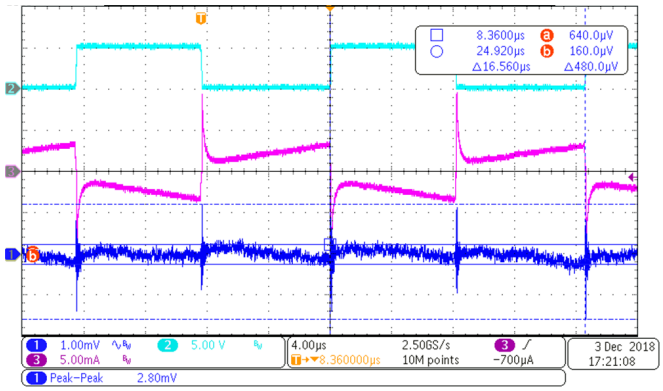
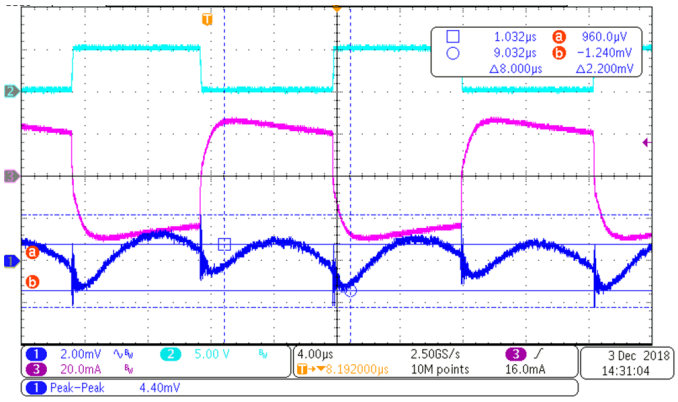


Figure 40. ISO DC/DC Waveforms at Vin = 5 V and Iout = 10 mA



3.2.2.7 Waveforms of ISO BUCK

The waveforms have been measured at input voltages of 3.6 V and 5 V and at output currents of 100 µA and 10 mA.

Figure 41 to Figure 44 show the switch node voltage and output voltage ripple.

Oscilloscope—channel assignment:

- CH1: Output Voltage Ripple on TP8 - *Iso BUCK Vout*
- CH2: Switch-node voltage measured on TP6 - *Iso BUCK SW*

Figure 41. ISO BUCK Waveforms at Vin = 3.6 V and Iout = 100 µA

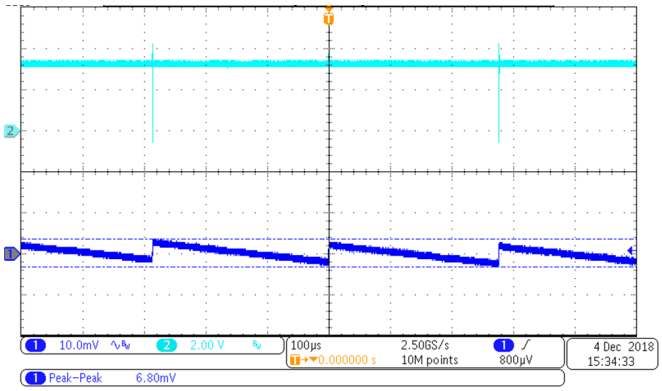


Figure 42. ISO BUCK Waveforms at Vin = 5 V and Iout = 100 µA

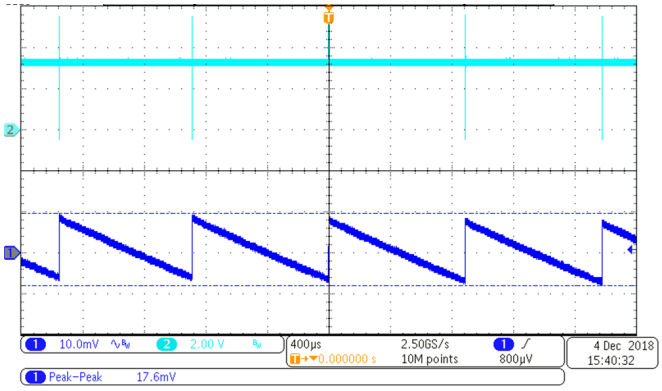


Figure 43. ISO BUCK Waveforms at Vin = 3.6 V and Iout = 10 mA

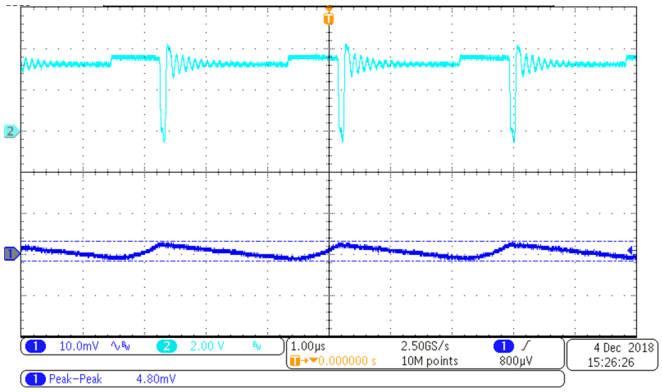
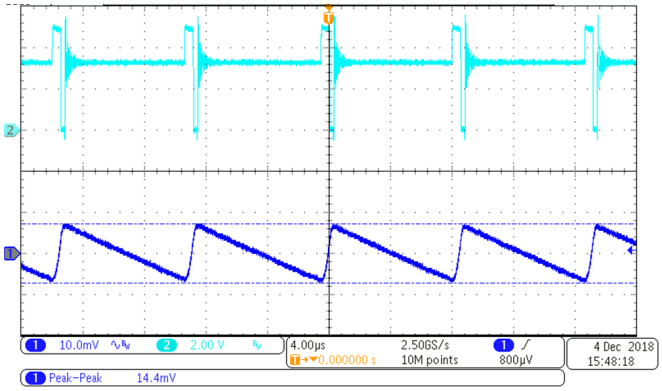


Figure 44. ISO BUCK Waveforms at Vin = 5 V and Iout = 10 mA



3.2.2.8 Waveforms of NON-ISO BUCK

The waveforms have been measured at an input voltage of 5 V and at output currents of 100 µA and 10 mA.

Figure 45 and Figure 46 show the switch node voltage and output voltage ripple.

Oscilloscope—channel assignment:

- CH1: Output Voltage Ripple on TP5 - *Vout non-iso BUCK*
- CH2: Switch-node voltage measured on TP4 - *Non-iso BUCK SW*

Figure 45. NON-ISO BUCK Waveforms at Vin = 5 V and Iout = 100 µA

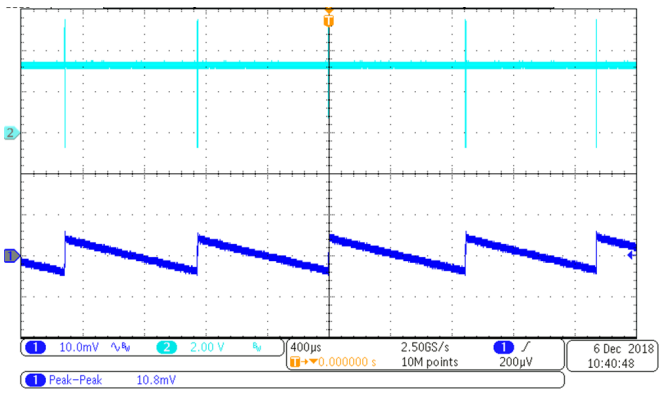
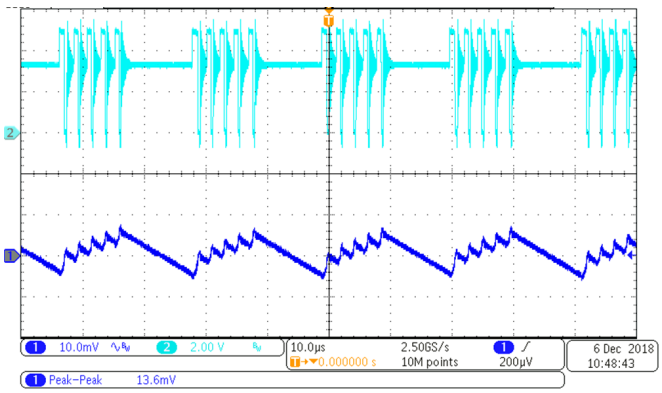


Figure 46. NON-ISO BUCK Waveforms at Vin = 5 V and Iout = 10 mA



3.2.2.9 System Waveforms of Start-up

The start-up waveforms have been measured with a 5-VDC input voltage. The SMU as Power source was current-limited to 30 mA and was connected as described in the table of the section Section 3.2.1. Both system sides had been configured to generate 3.3 V by their BUCK converters and for using their LDOs as post-regulator to generate 3-V rails on the non-isolated side as well as on the isolated-side. Both 3-V rails had been resistively loaded with 10 mA at their nominal 3-V output voltage. The default jumper setting as shown in section Section 3.1.1.2 for standalone test setup had been applied. Resistive loading was done using two resistance decades, see Table 10.

Table 10. Connections for Resistive Loading of *Iso Vout* and *Non-iso Vout*

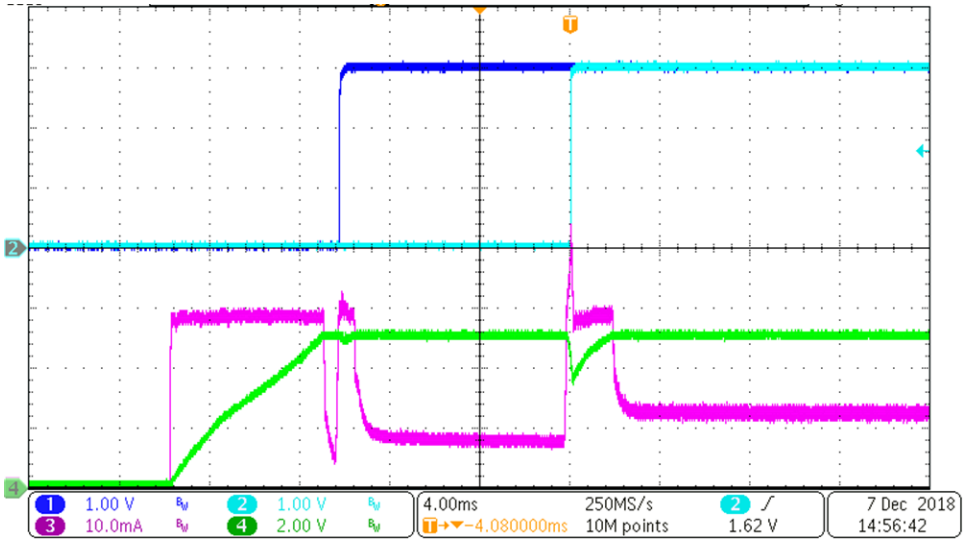
POWER SOURCE, LOAD, MULTIMETER	CONNECTED BY	HEADER		CONNECTED BY	HEADER		COMMENT
			PIN #			PIN #	
Resistance Decade 1 - red - in series with ammeter	Test leads banana plug to 0.64-mm square pin socket	J7	1				Set resistance decades to needed 10 mA of load current
Resistance Decade 1 - black			4				
Resistance Decade 2 - red - in series with ammeter		J13	1				
Resistance Decade 2 - black			4				

Figure 47 shows the output voltage of ISO LDO and NON-ISO LDO, system input current and system input voltage during starting up.

Oscilloscope—channel assignment:

- CH1: Output Voltage of IsoLDO on TP3 - *Iso LDO Vout*
- CH2: Output Voltage of Non-IsoLDO on TP9 - *Non-iso LDO Vout*
- CH3: Input current of system - Measured with current probe on FORCE output of SMU channel 1 which is connected to pin 1 of Power Input header J2 according to Section 3.2.1
- CH4: System input voltage on pin 2 of J2 referenced to pin 4 of J2

Figure 47. System Start-up at Vin = 5 V and Iout = 10 mA



3.2.2.10 ISO DATA - Waveforms and Current Consumption

The ISO7041 is powered with 3 V from LDO at both the isolated side and the non-isolated side. The four channels of ISO7041 are driven with the same channel of a function generator.

Figure 48 shows the propagation delay of INA and OUTA. The waveforms are measured with probe of Tektronix: TPP0250. The input capacitance and resistance of this probe are 3.9 pF and 10 MΩ.

Oscilloscope—channel assignment:

- CH1: Input signal of INA on TP15
- CH2: Output signal of OUTA on TP11

Figure 48. ISO DATA - Propagation delay of INA and OUTA

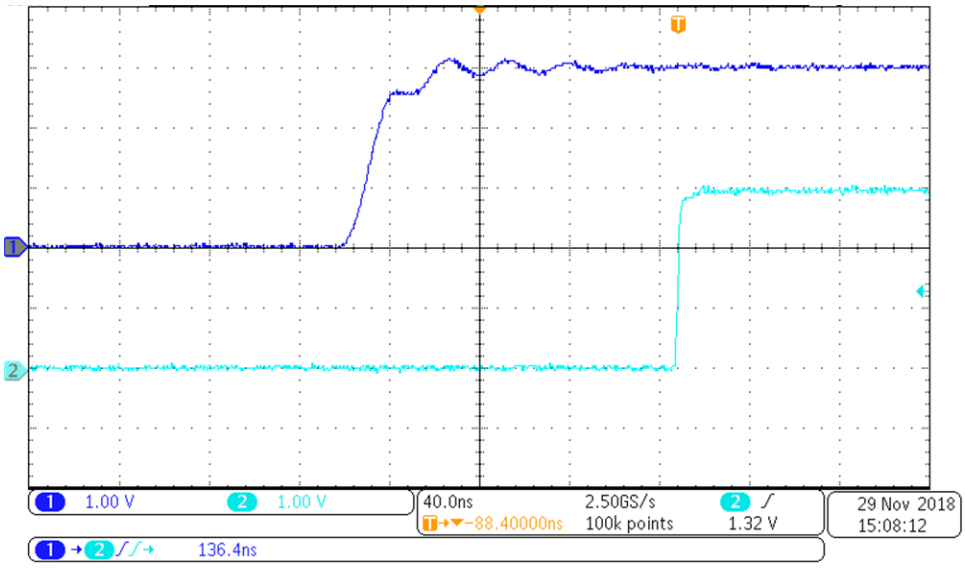


Table 11 and Table 12 show the supply current performance of the ISO DATA circuit blocks at different conditions.

Table 11. Supply Current of ISO DATA circuit block - isolated side and non-isolated side

PARAMETER		TEST CONDITIONS	TEST VALUE	UNIT
Icc1	Non-isolated side Supply Current, Refresh Disabled	1 kbps, No Load	5.12	µA
		10 kbps, No Load	7.52	µA
		100 kbps, No Load	32.71	µA
		1 Mbps, No Load	301.8	µA
		2 Mbps, No Load	598	µA
	Non-isolated side Supply Current, Refresh Enabled	1 kbps, No Load	7.39	µA
		10 kbps, No Load	8.76	µA
		100 kbps, No Load	32.89	µA
		1 Mbps, No Load	302.1	µA
		2 Mbps, No Load	598.2	µA
Icc2	Isolated side Supply Current, Refresh Disabled	1 kbps, No Load	10.01	µA
		10 kbps, No Load	10.2	µA
		100 kbps, No Load	22	µA
		1 Mbps, No Load	146.5	µA
		2 Mbps, No Load	284.4	µA
	Isolated side Supply Current, Refresh Enabled	1 kbps, No Load	10.4	µA
		10 kbps, No Load	11	µA
		100 kbps, No Load	22.1	µA
		1 Mbps, No Load	146.5	µA
		2 Mbps, No Load	284.5	µA

Table 12. Supply Current per Transmitter Channel (T) and per Receiver Channel (R)

PARAMETER	TEST CONDITIONS	TEST VALUE		UNIT
		T	R	
Refresh Disabled	1 kbps, No Load	0.68	2.99	µA
	10 kbps, No Load	1.49	2.81	µA
	100 kbps, No Load	9.51	4.15	µA
	1 Mbps, No Load	94.9	17.19	µA
	2 Mbps, No Load	188.71	31.89	µA
Refresh Enabled	1 kbps, No Load	1.51	3.07	µA
	10 kbps, No Load	1.96	3.09	µA
	100 kbps, No Load	9.57	4.19	µA
	1 Mbps, No Load	94.98	17.18	µA
	2 Mbps, No Load	188.75	31.92	µA

The measured supply current values for the ISO DATA match very well with the values given in the ISO7041 data sheet. The sum of the transmitter channel (T) supply current and receiver channel (R) current (as shown in Table 12) represent what is shown in the graphs of the ISO7041 data sheet as supply current vs data rate graphs, see Figure 49 and Figure 50.

Figure 49. ISO7041 Supply Current vs Data Rate at 3.3 V (With No Load)

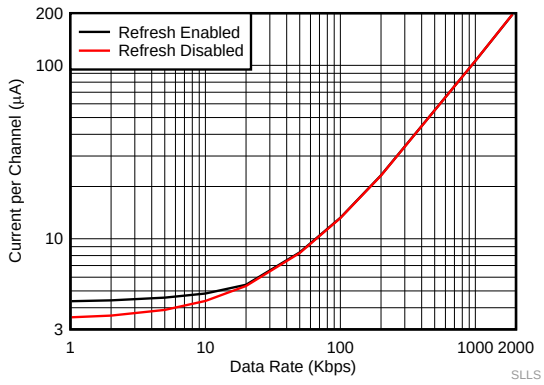
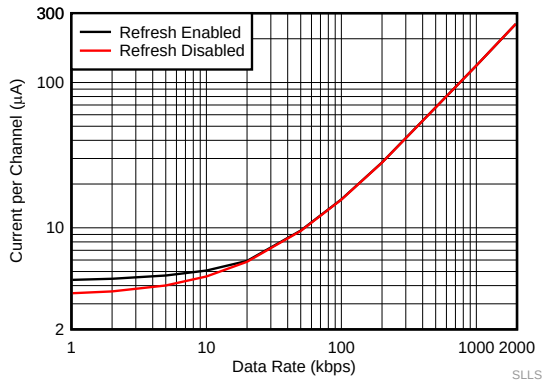


Figure 50. ISO7041 Supply Current vs Data Rate at 3.3 V (With 15-pF Load)



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010018.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010018.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010018.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010018.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010018.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010018.

5 Related Documentation

1. *Current NAMUR Recommendations (NE) and Worksheets (NA):* NE 043: *Standardization of the Signal Level for the Failure Information of Digital Transmitters* 2003-02-03
2. Uniquely efficient isolated DC/DC converter for ultra-low power and low power apps reference design: TIDA-00349
3. WUERTH ELEKTRONIK, 750314839 - Transformer Data

5.1 Trademarks

5.2 Third-Party Products Disclaimer

6 Terminology

SMU— source-measure unit

7 About the Author

JÜRGEN SCHNEIDER is a systems engineer at Texas Instruments, where he is responsible for developing TI Designs for the industrial automation segment. He holds a Dipl.-Ing. (FH) degree in industrial electronics and has worked 13 years as a design engineer for semiconductor manufacturing equipment, telemetry systems, and electro-medical devices before joining TI in 1999. Jürgen has worked with TI as an analog field specialist, FAE, and systems engineer for power solutions. He presents at technical conferences and seminars and has been one of the presenters of the industry-wide known TI Power Supply Design Seminar for multiple years. Jürgen also has the distinguishment of being elected as Senior Member Technical Staff.

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