TI Designs: TIDA-010035
Power Line Communication Using RS-485 Simulation Reference Design

Description

This reference design establishes a simulation model for implementing RS-485 communication over power cabling. Use this simulation model to assess the feasibility of implementing RS-485 communication at a given data rate, cable length, and loading for a specific cable before taking the time-consuming step of building a representative network. A procedure is given for developing a cable model for any given cable and replacing the cable model in the simulation.

Resources

TIDA-010035	Design Folder
SN65HVD1786	Product Folder
TINA-TI™	SPICE Simulator
TIDA-00527	Tool Folder

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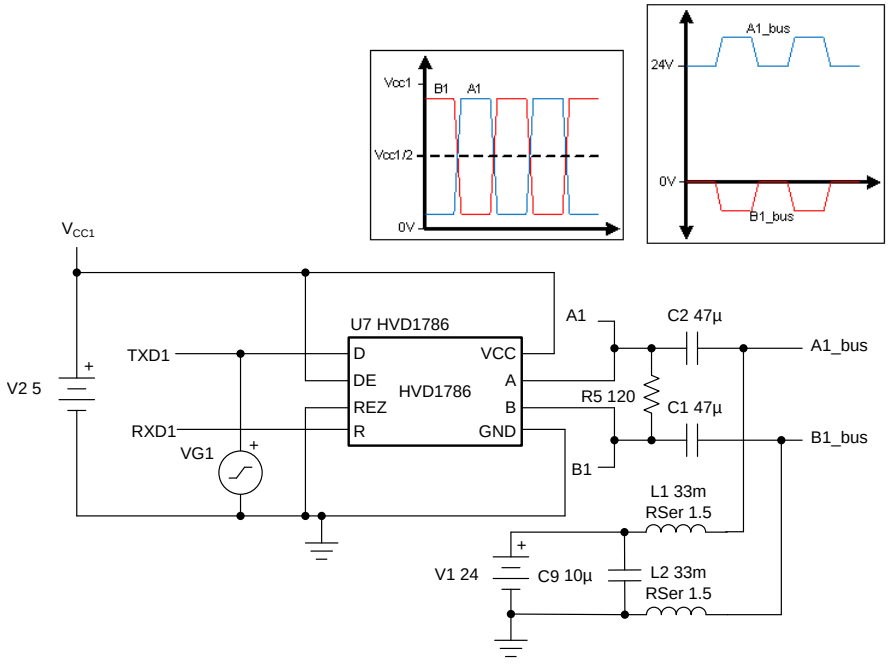
Features

- Simulation model demonstrates feasibility of 64 kbps data rate with cable length up to 1000 feet and a total of 128 nodes
- Sanity-checked against real cable measurements
- Establishes procedure for developing cable model for further simulations

Applications

- Elevator Calling Buttons Operating Panel
- Elevator Main Control Panel
- Electronic Door Locks
- HVAC System Controller



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1 System Description

The communication bus is a key component of many applications. In elevator systems a bus connects the buttons inside the elevator car to the elevator main controller. Existing systems rely on proprietary bus solutions which have served well for many years. However, as new features are added, complexity grows and customers want to a standard interface such as CAN and RS-485 that can provide more throughput and can interface with other networks. Additionally, customers want a wired solution that can simplify installation and reduce cabling costs.

Before selecting the final solution, customers must build a representative network for testing. This step can be very time-consuming and impractical for a network that consists of hundreds of nodes and varying segment lengths. Customers need an easy mechanism to narrow down the list of possible solutions before taking this time-consuming step.

This TI design provides a simulation model that can be used to assess the feasibility of a given wired solution at a given data rate, cable length, and loading for a given cable. RS-485 over power is explored as a possible solution through sub-system level simulations. The results of the simulations are compared against actual measurements for sanity-check. A procedure is given for developing a cable model for any given cable.

1.1 Key System Specifications

Table 1. Key System Specifications

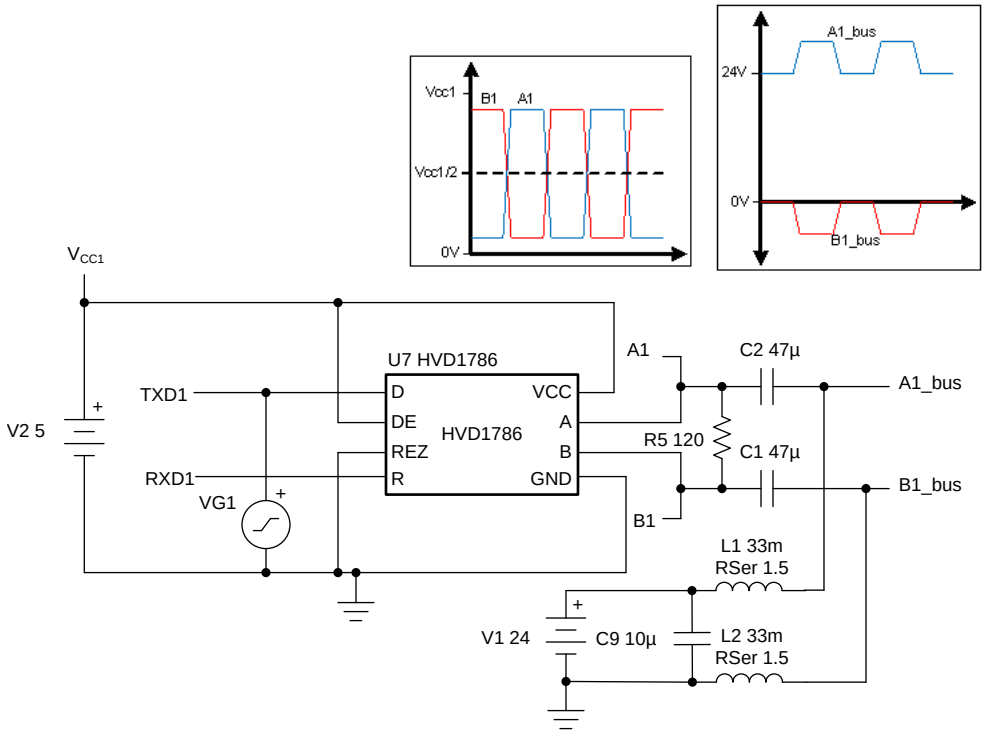
PARAMETER	SPECIFICATIONS	DETAILS
Power Line Voltage	24 V	Section 2.5.3.1
Number of Nodes	128[(1)]	Section 2.5.3.1
Bus Length	1000 feet (300 m)	Section 2.5.3.1
Data Rate	64 kbps	Section 2.5.3.2
Noise Margin	V_{OD} = approximately 715 mV for 128 transceivers at 1/8 unit load	Section 2.5.3.2

(1) Simulation does not include failsafe biasing for a defined DC differential level during idle. Failsafe biasing will reduce the number of nodes (see Section 2.4.1.6 and Section 2.4.1.7).

2 System Overview

2.1 Block Diagram

Figure 1. TIDA-010035 Block Diagram



2.2 Design Considerations

In general, an RS-485 wired network must define several parameters based on the system use case. These parameters ultimately determine if the RS-485 network is able to function properly. These parameters include:

Cable length and data rate— There is an inverse relationship between signal data rate (speed) and cable length. The exact relationship depends on the resistance and inductance of the cable itself.

Number nodes— The output of a driver depends on the current it must supply into a load. Adding nodes to the bus increases the total load current required.

Cable choice— When building an RS-485 network, the choice of cable can be as important as the transceiver to ensure reliable communication over the necessary distance.

Power Line DC voltage— For an RS-485 over power application, the DC voltage of the power rail on which the RS-485 signal is coupled affects the cable model and the transceiver selection. A lower DC voltage will require a thicker wire to carry a higher current. The DC voltage also dictates the minimum bus voltage standoff requirement (input voltage at bus pins) for the transceiver. A high DC voltage will require a transceiver with a high bus voltage standoff.

All of the previously listed parameters affect driver differential output voltage (V_{OD}) at receiver input. The RS-485 standard imposes receivers be able to detect a V_{OD} down to 200 mV. The simulations presented in this design guide focuses on the V_{OD} under the conditions previously outlined to determine if the network can function properly.

The SN65HVD1786 transceiver was used for all the simulations presented in this TI design. The transceiver has a maximum bus pin voltage of 70 V DC which is more than enough to withstand the 24-V DC bus voltage used in this TI design. For lower DC bus voltages, other transceivers can be considered, such as the THVD1450 or THVD1550 which have an maximum bus voltage rating of ±18 V.

NOTE: As Figure 1 shows and Section 2.4.2 explains, the power line voltage is blocked from the transceiver bus pins given that the pins are AC-coupled to the power line. However, the designer should still consider the possibility of direct exposure of the transceiver pins to the DC voltage through a short or AC-coupling capacitor failure.

One point to note is that RS-485 is an electrical-only standard, intended to be referenced by higher level standards. It does not provide for an arbitration mechanism in case of a multi-master use case. However, such a feature can be implemented through software if needed.

2.3 Highlighted Products

This TI design features the SN65HVD1786 RS-485 transceiver. For more information on this device, see the SN65HVD1786 product folder.

2.3.1 SN65HVD1786

This device is designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. It is also robust to ESD events, with high levels of protection to human-body model specifications.

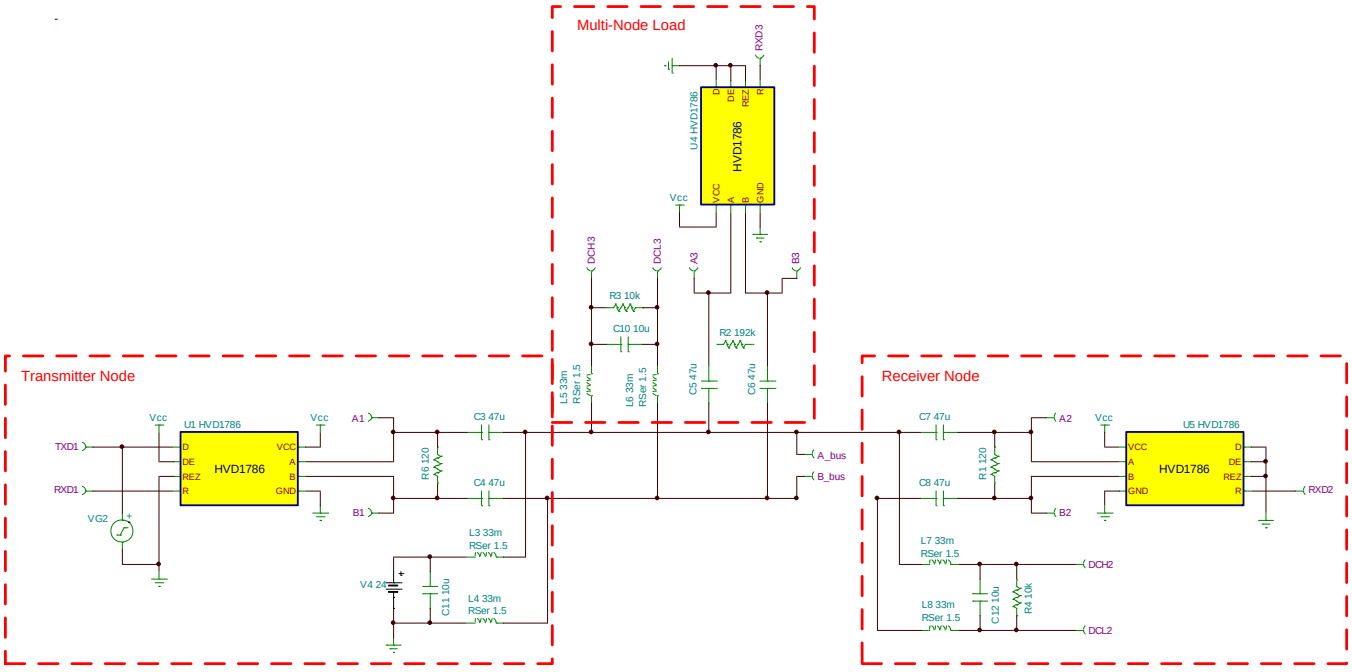
This device combines a differential driver and a differential receiver, which operate from a single power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. These ports feature a wide common-mode voltage range, making the device suitable for multipoint applications over long cable runs. This device is characterized from –40°C to 105°C.

- Bus-pin fault protection to:
  - > ±70 V
- Common-mode voltage range (–20 V to 25 V) more than doubles TIA/EIA 485 requirement
- Bus I/O protection
  - ±16 kV JEDEC HBM protection
- Reduced unit load for up to 256 nodes
- Failsafe receiver for open-circuit, short-circuit and idle-bus conditions
- Low power consumption
  - Low standby supply current, 1 μA typical
  - I_{CC} 5 mA quiescent during operation
- Power-up, power-down glitch-free operation

2.4 System Design Theory

The circuit in Figure 2 shows the model used to simulate a multi-node RS-485 over power-line network. The circuit consists of a transmitter node which includes an RS-485 transceiver and a power source connected to the bus through a coupling network. Similarly, a receiver node consisting of an RS-485 transceiver and a power load is connected at the end of the bus through a coupling network. The multi-node load portion of the circuit simulates multiple nodes connected the to the bus. The total number of nodes simulated is specified by adjusting the passive components values (see Section 2.4.2). Each end of the network is terminated using a 120-Ω resistor.

Figure 2. RS-485 Over Power Line Multi-Node Network Simulation Schematic



The next section presents some introductory material to the RS-485 standard. The following sections describe each portion of the circuit in more detail.

2.4.1 RS-485 Introduction

2.4.1.1 Standard and Features

In 1983, the Electronics Industries Association (EIA) approved a new balanced transmission standard called RS-485. Finding widespread acceptance and usage in industrial, medical, and consumer applications, RS-485 has become the interface workhorse of the industry.

RS-485 is an electrical-only standard. In contrast to complete interface standards, which define the functional, mechanical, and electrical specifications, RS-485 only defines the electrical characteristics of drivers and receivers that could be used to implement a balanced multi-point transmission line. This standard, however, is intended to be referenced by higher level standards.

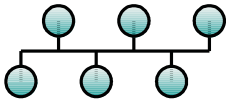
Key features of RS-485 are:

- Balanced interface
- Multi-point operation from a single 5-V supply
- –7-V to +12-V bus common-mode range
- Up to 32 unit loads
- 10-Mbps maximum data rate (at 40 feet)
- 4000-foot maximum cable length (at 100 kbps)

2.4.1.2 Network Topology

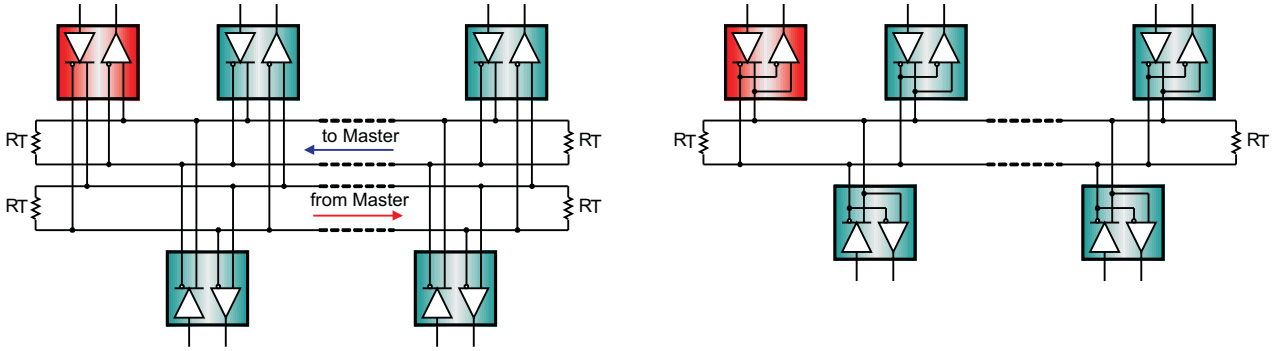
The RS-485 standards suggests that its nodes be networked in a daisy-chain, also known as party line or bus topology (see Figure 3). In this topology, the participating drivers, receivers, and transceivers connect to a main cable trunk via short network stubs. The interface bus can be designed for full-duplex or half-duplex transmission (see Figure 4).

Figure 3. RS-485 Bus Structure



The full-duplex implementation requires two signal pairs (four wires) and full-duplex transceivers with separate bus access lines for transmitter and receiver. Full-duplex allows a node to simultaneously transmit data on one pair while receiving data on the other pair.

Figure 4. Full-Duplex and Half-Duplex Bus Structures in RS-485



In half-duplex, only one signal pair is used, requiring the driving and receiving of data to occur at different times. Both implementations necessitate the controlled operation of all nodes via direction control signals, such as driver and receiver enable signals, to ensure that only one driver is active on the bus at any time. Having more than one driver accessing the bus at the same time leads to bus contention, which, at all times, must be avoided through software control.

2.4.1.3 Signal Levels

RS-485 standard-compliant drivers provide a differential output of a minimum 1.5 V across a 54-Ω load, whereas standard-compliant receivers detect a differential input down to 200 mV. The two values provide sufficient margin for a reliable data transmission even under severe signal degradation across the cable and connectors. This robustness is the main reason why RS-485 is well suited for long-distance networking in noisy environment.

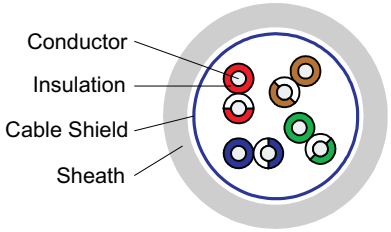
Figure 5. RS-485 Specified Minimum Bus Signal Levels

2.4.1.4 Cable Type

RS-485 applications benefit from differential signaling over twisted-pair cable, because noise from external sources couple equally into both signal lines as common-mode noise, which is rejected by the differential receiver input.

Industrial RS-485 cables are typically of the sheathed, un-shielded, twisted-pair type (UTP) with a characteristic impedance of 120-Ω and 22–24 AWG. Figure 6 shows the cross-section of a four-pair UTP cable typically used for two full-duplex networks. Similar cables in two-pair and single-pair versions are available to accommodate the low-cost design of half-duplex systems.

Figure 6. Example of RS-485 Communication Cable



Cable : Belden 3109A
Type : 4 - pair, 22 AWG PLCT/CM
Impedance : 120 Ω
Capacitance : 11 pF/ft
Velocity : 78% (1.3 ns/ft)

Beyond the network cabling, it is mandatory that the layout of printed-circuit boards and the connector pin assignments of RS-485 equipment maintain the electrical characteristics of the network by keeping both signal lines close and equidistant to another.

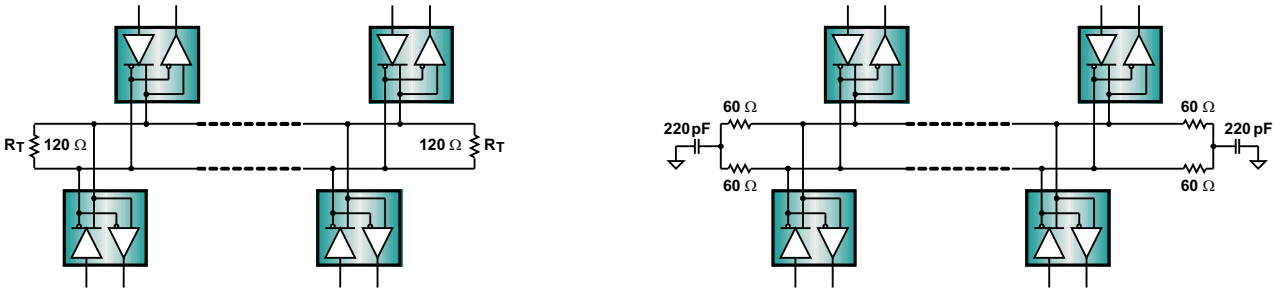
2.4.1.5 Bus Termination and Stub Length

When designing a system that uses drivers, receivers, and transceivers that comply with RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. In general RS-485 requires termination at both ends of the cable.

Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor: cost. The different types of termination techniques discussed are un-terminated lines, parallel termination, AC termination, and multi-point termination.

Proper termination requires the matching of the terminating resistors, R_T , to the characteristic impedance, Z_0, of the transmission cable. Because the RS-485 standard recommends cables with Z_0 = 120 Ω , the cable trunk is commonly terminated with 120-Ω resistors, one at each cable end (see Figure 7, left). Applications in noisy environments often have the 120-Ω resistors replaced with two 60-Ω, low-pass filters to provide additional common-mode noise filtering, (see Figure 7, right).

Figure 7. Proper RS-485 Terminations



2.4.1.6 Failsafe

Failsafe operation is the ability of a receiver to assume a determined output state in the absence of an input signal.

Three possible causes can lead to the loss of signal (LOS):

1. **Open-circuit** caused by a wire break or by the disconnection of a transceiver from the bus.
2. **Short-circuit** caused by an insulation fault connecting the wires of a differential pair to another.
3. **Idle-bus** occurring when none of the bus drivers is active.

Because these conditions can cause conventional receivers to assume random output states when the input signal is zero, modern transceiver designs include biasing circuits for open-circuit, short-circuit, and idle-bus failsafe, that force the receiver output to a determined state, under an LOS condition.

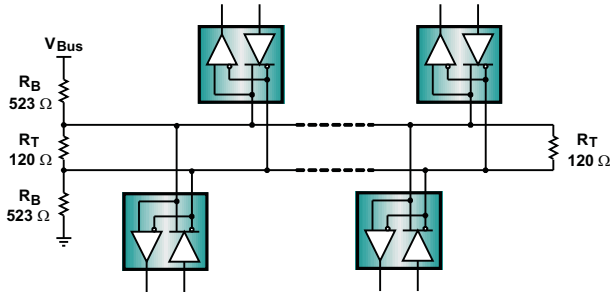
A drawback of these failsafe designs is their worst-case noise margin of 10 mV only, thus requiring external failsafe circuitry to increase noise margin for applications in noisy environments.

An external failsafe circuit consists of a resistive voltage divider that generates sufficient differential bus voltage to drive the receiver output into a determined state. To ensure sufficient noise margin, V_{AB} must include the maximum differential noise measured in addition to the 200-mV receiver input threshold, V_{AB} = 200 mV + V_{Noise}.

$$R_B = \frac{V_{BUS(min)}}{V_{AB} \times \left(\frac{1}{375} + \frac{4}{Z_0}\right)} \quad (1)$$

For a minimum bus voltage of 4.75 V, (5 V – 5%), V_{AB} = 0.25 V, and Z_0 = 120 Ω, R_B yields 528 Ω. Inserting two 523-Ω resistors in series to R_T establishes the failsafe circuit as Figure 8 shows.

Figure 8. External Idle-Bus Failsafe Biasing



2.4.1.7 Bus Loading

Because the output of the driver depends on the current it must supply into a load, adding transceivers and failsafe circuits to the bus increases the total load current required. To estimate the maximum number of bus loads possible, RS-485 specifies a hypothetical term of a unit load (UL), which represents a load impedance of approximately 12 kΩ. Standard-compliant drivers must be able to drive 32 of these unit loads. The latest transceivers often provide reduced unit loading, such as 1/8 UL, thus allowing the connection of up to 256 transceivers on the bus.

Because failsafe biasing contributes up to 20 unit loads of bus loading, the maximum number of transceivers, N, is reduced to:

$$N = \frac{32 * UL_{STANDARD} - 20 * UL_{FAILSAFE}}{UL_{per\ \ transceiver}} \quad (2)$$

Thus, when using 1/8-UL transceivers, it is possible to connect up to a maximum of 96 devices to the bus.

2.4.1.8 Data Rate vs Bus Length

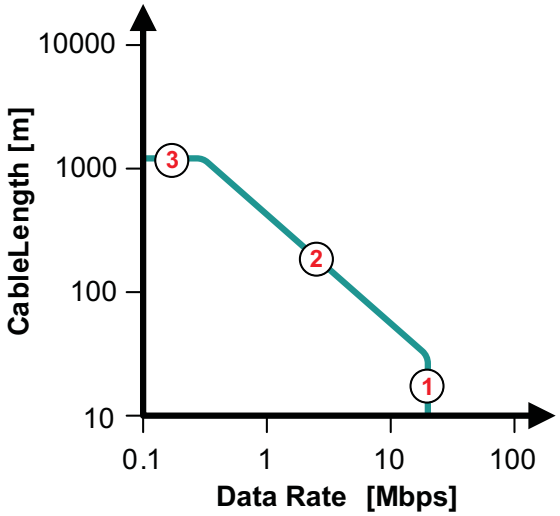
There is an inverse relationship between signal rate (speed) and cable length. The exact relationship depends on the resistance and inductance of the cable itself. When building an RS-485 network, the choice of cable can be as important as the transceiver, to ensure reliable communication over the necessary distance. Figure 9 is a graphical representation of the signal rate to cable length correlation.

Section 1 of the graph presents the area of high data rates over a short cable length. Here, the losses of the transmission line can be neglected and the data rate is mainly determined by the rise time of the driver. Although the standard recommends 10 Mbps, the fast interface circuits of today can operate at data rates of up to 50 Mbps.

Section 2 shows the transition from short to long data lines. The losses of the transmission lines have to be taken into account. Thus, with increasing cable length, the data rate must be reduced.

Section 3 presents the lower frequency range where the line resistance, and not the switching, limits the cable length. Here, the cable resistance causes attenuation in the signal and limits the maximum communication distance.

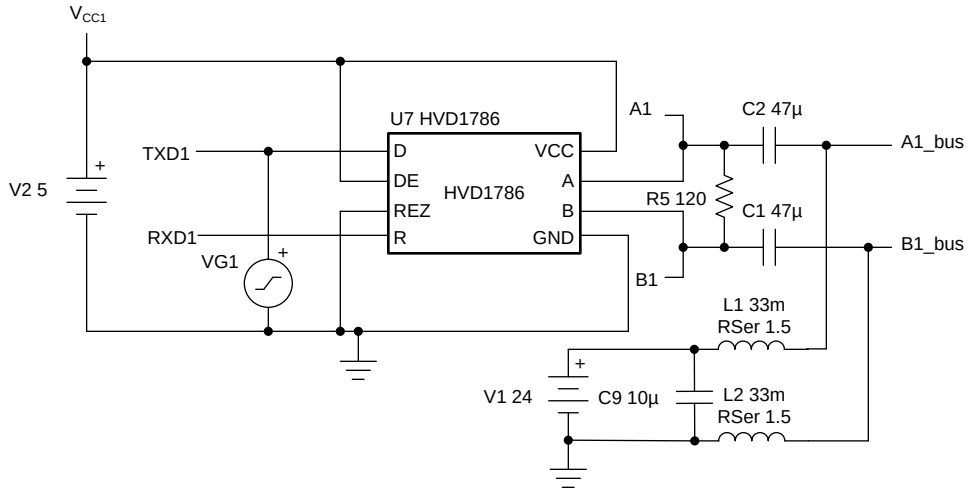
Figure 9. Cable Length vs Data Rate



2.4.2 Coupling Network Design Theory

The circuit presented in Figure 10 shows the basic schematic concept for the transmitter node of the RS-485 network. The RS-485 transceiver (U7) and the power source (V1) are coupled to the bus using a coupling network. The coupling network circuit for the receiver node and multi-node load (for a one-node load) is the same.

Figure 10. Driver Node Schematic



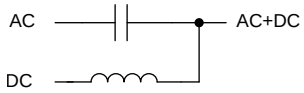
As Figure 11 shows, a coupling network consists of a capacitor that allows the AC signal through while blocking the DC voltage and an inductor which passes the DC voltage but blocks the AC signal. In transmission line environments the impedance of the capacitor (Z_C) is chosen to be much less than the characteristic impedance of the cable, Z_0, and the impedance of the inductor (Z_L) is chosen to be much greater than Z_0:

$$Z_C = \frac{1}{2\pi \cdot f_{min} \cdot C} \ll Z_0$$
$$Z_L = 2\pi \cdot f_{min} \cdot L \gg Z_0 \quad (3)$$

where

- f_{min} is the minimum signal frequency being transmitted (4)

Figure 11. Equivalent Coupling Network Circuit



In order to size the coupling network components, C and L, using Equation 3 and Equation 4 a minimum switching frequency for the data signal must be established. Since the data is random and RS-485 has no inherent protocol to break long sequences of 1's or 0's in the data, a minimum switching frequency cannot be established.

One solution to this problem is to use Manchester encoding on the data stream. Manchester encoding forces a transition for every bit: a logic 0 is encoded as a 0-to-1 transition, while a logic 1 is encoded as a 1-to-0 transition (an opposite encoding may also be used). Figure 12 shows how Manchester encoding works in principle.

Figure 12. Manchester Encoding

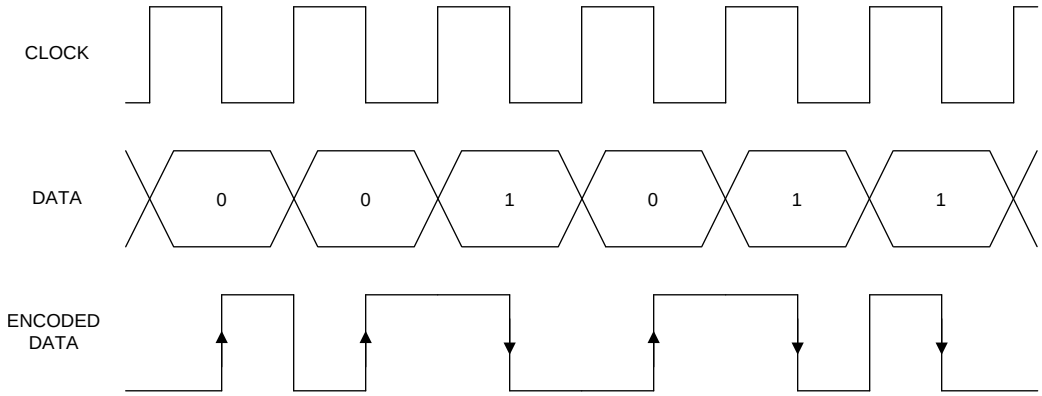
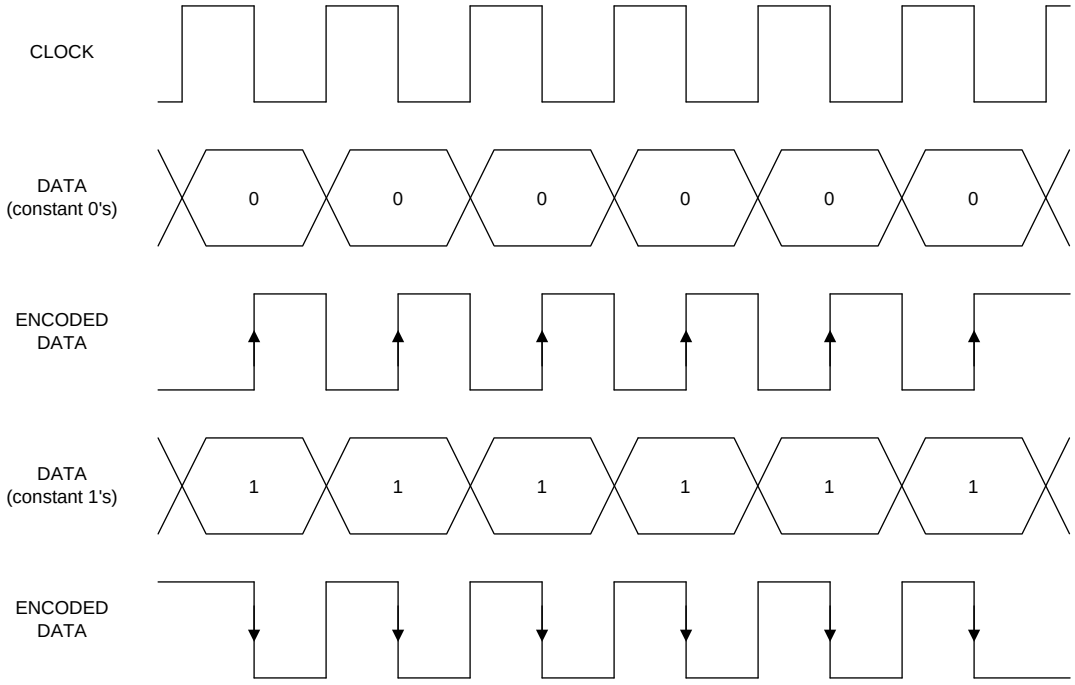


Figure 13 demonstrates a Manchester encoded signal for a sequence of constant 1's and 0's. In both cases, the encoded signal is always transitioning.

Figure 13. Manchester Encoded Output for Constant Digital Signal



Manchester encoding can be performed in software and transmitted through a serial port on a microcontroller. One downside of this approach is the additional memory and CPU cycles required to generate two bits for every bit in the original data. Also, to keep the original data rate, the serial port transmitting clock frequency has to be doubled. If there is an upper limit to the serial port transmit clock frequency, the data rate will must be reduced. These limitations can be avoided by implementing the encoding and decoding using a logic circuit at the expense of additional BOM cost

A Manchester encoded signal will have a lower frequency bound equal to half the clock frequency (alternating 1's and 0's pattern). Using the lower frequency bound, the capacitor and inductor values for the coupling network can be derived using Equation 3 and Equation 4.

By setting $Z_C < Z_0 / 500$, the capacitor value is calculated as follows:

$$\begin{aligned} Z_C &\ll Z_0 \\ Z_C &< \frac{Z_0}{500} \\ (2\pi \cdot f_{min} \cdot C)^{-1} &< \frac{Z_0}{500} \\ 2\pi \cdot f_{min} \cdot C &> \frac{500}{Z_0} \\ C &> \frac{500}{2\pi \cdot Z_0 \cdot f_{min}} \end{aligned} \tag{5}$$

Similarly, by setting $Z_L > 100 \times Z_0$, the inductor value is calculated as follows:

$$\begin{aligned} Z_L &\gg Z_0 \\ Z_L &> 100 \cdot Z_0 \\ 2\pi \cdot f_{min} \cdot L &> 100 \cdot Z_0 \\ L &> \frac{100 \cdot Z_0}{2\pi \cdot f_{min}} \end{aligned} \tag{6}$$

As an example, for a data rate of 64 kbps the minimum switching frequency, f_{min}, is 32 kHz and with $Z_0 = R_T / 2 = 60\ \Omega$, Equation 5 yields C > 41.5 µF. A capacitor value of 47 µF can be used given the wide availability of this size. At this size Z_C is approximately $Z_o / 567$.

Similarly, at the same data rate and Z_0, Equation 6 yields L > 29.8 mH. A value of 33 mH can be used given the wide availability of this size. At this size Z_L is approximately $110 \times Z_0$.

These coupling network component values are used in the simulation sections that follow.

NOTE: An inductor with an equivalent series resistance, R_{ser}, of 1.5 Ω was used in the simulations. This value was used based on average values observed in actual inductor part numbers.

2.5 Simulation and Results

The following sections describe in detail the simulations that were carried out to demonstrate the feasibility of implementing RS-485 over power. It must be stressed that these simulation only demonstrate gross feasibility.

Noise and sources of various disturbances typically present on power lines and their effects on signal integrity for communication signaling were not included in these simulations. However, these typically cannot be reliably simulated. The simulations presented here are limited by system level impedance models, source coupling mechanisms, and also a lack of a cable model and detailed functional level transceiver model.

Before the RS-485 over power-line technique is adopted as the final solution, a representative network that closely matches the final application should be constructed and tested.

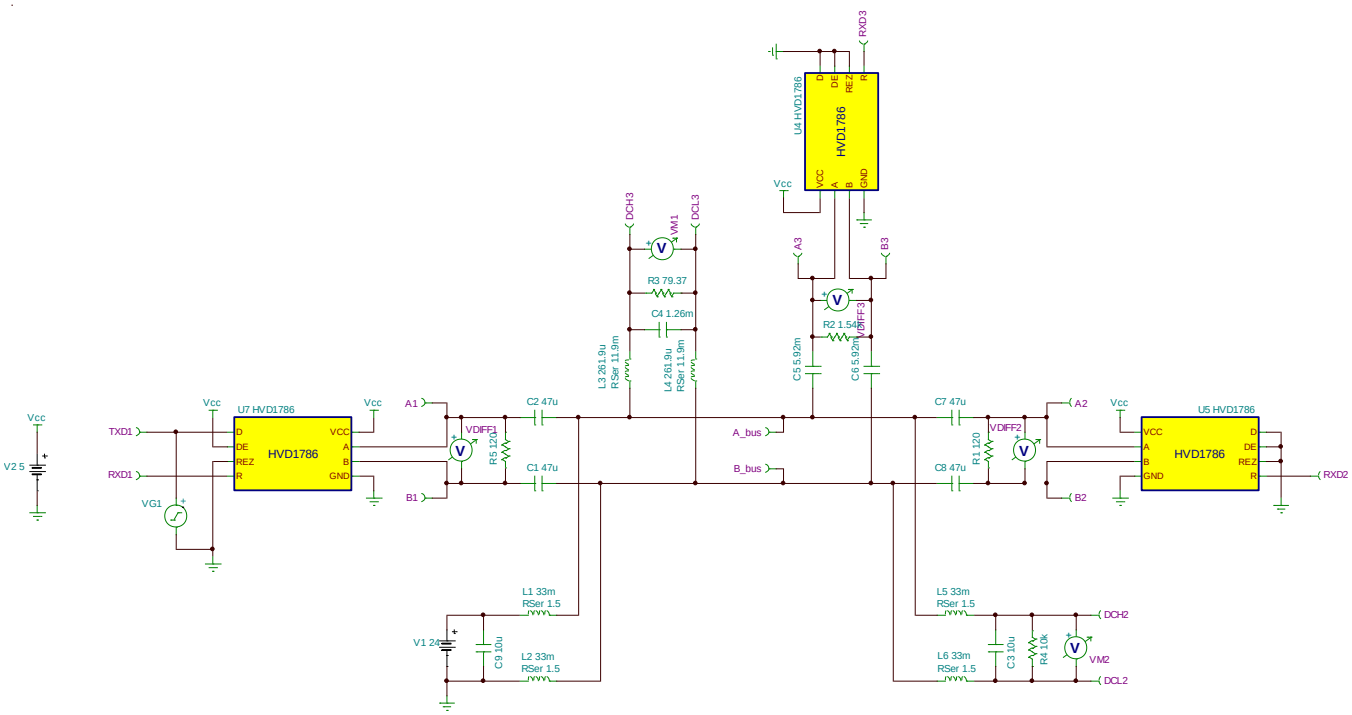
2.5.1 Multi-Node Simulation

A TINA-TI™ software transient analysis was performed to test the multi-node RS-485 over power-line network. The goal of the transient analysis was to understand if the differential output voltage (V_{OD}) at the receiver node provided enough noise margin given the simulated data rate and number of nodes.

2.5.1.1 Simulation Setup

Figure 14 shows the TINA simulation schematic for the multi-node setup. The schematic consists of a transmitter node, a receiver node, and a node intended to mimic the effect of loading the network with multiple nodes. The TINA simulation model uses an excitation source and several voltage probes to analyze the network response over time.

Figure 14. Multi-Node Simulation Model



The simulation has the following main sections:

- Transmitter Node: Consists of the excitation source, transceiver, and power source.
  - Excitation source (VG2): 2.5-V square wave with programmable frequency (set to 32 kHz).
  - 24-V DC power source (V1): Coupled to bus through L1, L2 as calculated in Section 2.4.2.
  - HVD1786 transceiver (U7): Coupled to the bus through C1, C2 as calculated in Section 2.4.2.
- Receiver Node: Consists of transceiver and power rail load.
  - HVD1786 transceiver (U5): Coupled to the bus through C7, C8 as calculated in Section 2.4.2.
  - Power Rail Load (C3, R4): Simulated power load at the receiver end. For this simulation R4 = 10 kΩ and C3 = 10 µF. At 24 VDC, the load is approximately 58 mW. The power load is coupled to the bus through L5, L6 as calculated in Section 2.4.2.
- Multi-node load: Simulated network load on the data bus and the power rail.
  - HVD1786 transceiver (U4): Each transceiver on the network is coupled to the bus through a coupling network (C5, C6). The capacitor value is calculated for one node as in Section 2.4.2 and scaled using C × (#nodes-2), where #nodes is the total number of nodes.
  - Transceiver Load (R2): The component R2 represents the multi-node load looking into all the transceivers on the network. A single HVD1786 has a maximum bus input current spec of 125 µA at 12 V which is equivalent to a 96-kΩ load. For a differential signal the leakage current doubles to 192 kΩ. The total load resistance R2 is scaled as R2 / (#nodes-3).
  - Power Rail Load (C4, R3): The components C4 and R3 represent the load for the multiple nodes on the power rail. These components are scaled as C × (#nodes-2) and R / (#nodes-2), where C and R are taken from the receiver node power load component calculations (C3, R4). Each load is coupled to the bus through a coupling network (L3, L4). The inductor value is calculated for one node as in Section 2.4.2 and scaled using L / (#nodes-2). Similarly, the equivalent series resistance (R_{ser}) of the inductors is calculated for one node and scaled as R_{ser} / (#nodes-2).

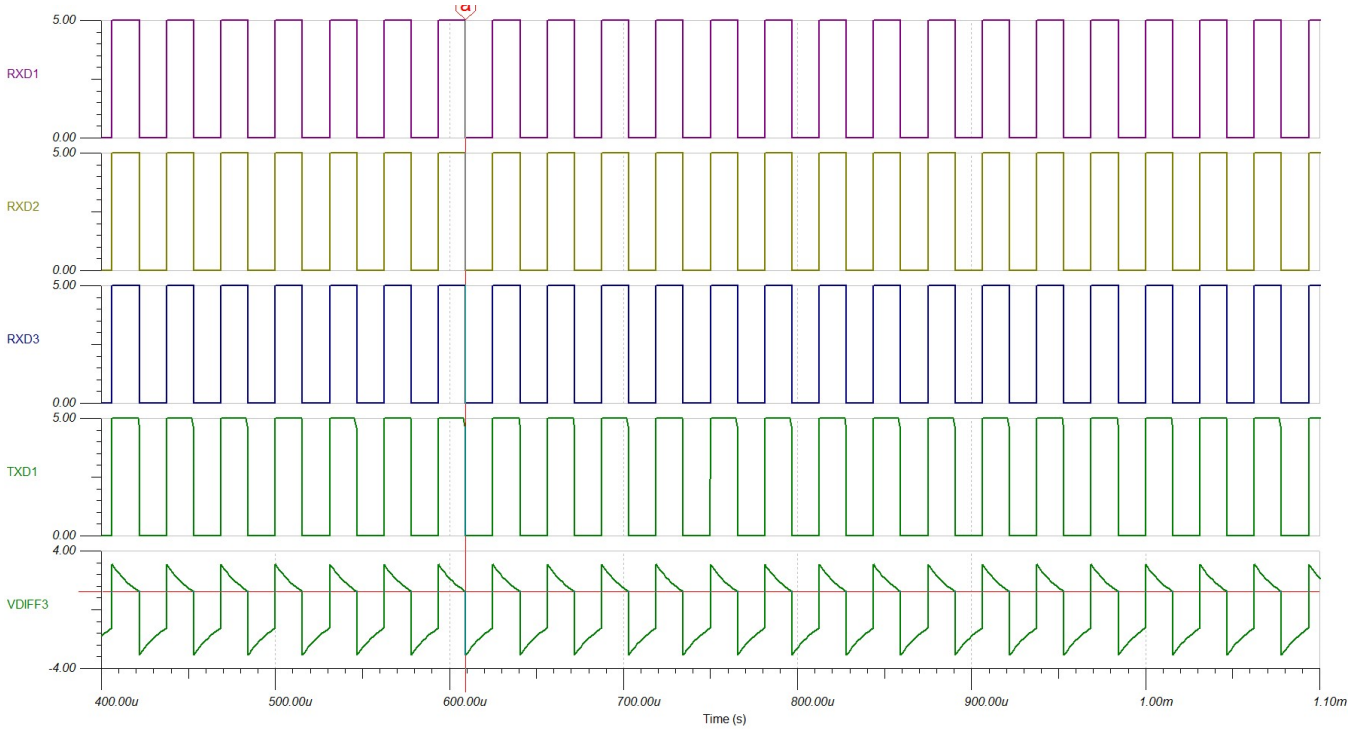
Voltage probes were placed at different points to capture the transient response of the circuit.

NOTE: Simulation does not include failsafe biasing for a defined DC differential level during idle. Failsafe biasing will reduce the number of nodes. See Section 2.4.1.6 and Section 2.4.1.7.

2.5.1.2 Simulation Results

The simulation results in Figure 15 demonstrate that there is a wide margin on VOD at the receiver node with a 128-node network and a data rate of 64 kbps. In this setup the minimum VOD observed is approximately 1.25 V. The output waveform RXD2 shows the transceiver is able to correctly receive the data signal. The output waveform VM2 shows the 24-V DC supply at the receiver node.

Figure 15. Multi-Node Simulation Results (128 Nodes, 64 kbps Data Rate)



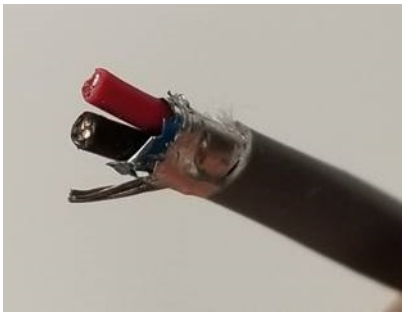
2.5.2 Point-to-Point Simulation with Cable Model

A TINA transient analysis was performed on a point-to-point network using a cable model. The results were compared against measurements made on an actual hardware setup to correlate the transceiver model to an actual system. The procedure used to create the cable model, the simulation setup, the physical measurements, and the comparison of the simulation results to measurements made in a real system are described in the following sections.

2.5.2.1 Cable Model Derivation

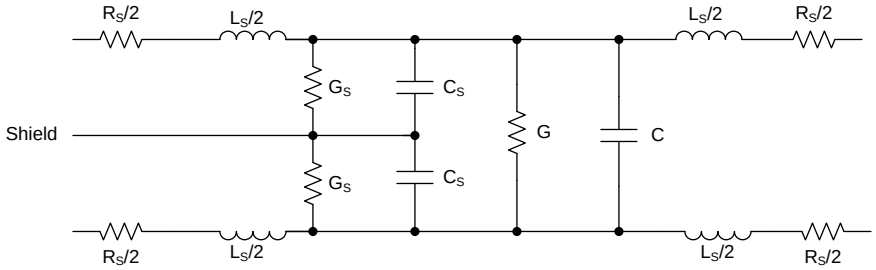
This section describes the procedure for developing a distributed cable model for a shielded, non-twisted pair cable (see Figure 16).

Figure 16. Cross-Section of Shielded, Non-Twisted Pair, 18 AWG Cable



A distributed model uses a lumped-parameter representation for small segments of the overall cable length. The segment length is based on the wavelength of the frequencies being transmitted. Figure 17 shows a general circuit model for a shielded, non-twisted pair cable.

Figure 17. General Circuit Model for Shielded Pairs



Unlike industrial RS-485 cables, this type of low-cost cable does not have a controlled characteristic impedance. A representative model of this type of low-cost cable can still be created, however, because there are no manufacturing controls in place, the cable parameters measured for the model can vary wildly from spool to spool and between manufacturing lots of spools. Therefore these cable models should only be used to investigate feasibility of different network configurations, not as a guarantee of expected performance.

To calculate the component values in the circuit in Figure 17, the following measurements were conducted on a segment of cable using an RLC meter:

- Total resistance and inductance on each wire (red and black)
- Differential impedance, capacitance, and conductance between both wires (red to black) with the both wires open
- Differential impedance between both wires (red to black) with both wires shorted
- Differential capacitance and conductance between each wire (red and black) and ground (shield)

Before any measurements are made, the segment length that is measured must be decided. The maximum segment length is bounded by the wavelength, λ, of the frequencies being transmitted. The segment length must be less than $\lambda / 8$ to avoid transmission line considerations. Also, segment lengths less than 6 feet are not ideal given that this is the nominal stub length in RS-485 networks.

The wavelength is related to the signal frequency through Equation 7:

$$\lambda = c / f \quad (7)$$

where

- c = the speed of light
- f = the signal frequency

A segment length of $\lambda / 8$ = 6 feet, yields a signal frequency of approximately 20 MHz. Note that the maximum frequency point on the RLC meter was 10 MHz. Therefore, a segment length of 6 feet was chosen for the measurements.

The results of the measurements performed on a 6-foot segment of cable are summarized in Table 2.

Table 2. Summary of Measurements Performed On 6-ft Cable Segment

	BLACK		RED		DIFFERENTIAL OPEN (RED-BLACK)				DIFFERENTIAL SHORT (RED-BLACK)		DIFFERENTIAL OPEN (RED-GND)		DIFFERENTIAL OPEN (BLACK-GND)	
FREQ (Hz)	R (Ω)	L (µH)	R (Ω)	L (µH)	|Z| (kΩ)	THETA (DEGREES)	C (pF)	G (µS)	|Z| (Ω)	THETA (DEGREES)	C (pF)	G (µs)	C (pF)	G (µs)
DC	0.041		0.0405											
1 k							376.57	0.1097			754.33	0.2177	689.24	0.1987
10 k	1.67	4.495	1.8	4.72	45.483	–86.955	349.2	1.172	3.3	7.22	701.86	2.293	641.42	2.107
20 k	1.692	2.668	1.803	2.719	23.302	–86.864	340.65	2.353	3.71	4.47	685.24	4.589	626.13	4.224
40 k	1.611	2.09	1.706	2.16	11.958	–86.85	331.85	4.66	2.87	4.37	668.66	9.08	610.83	8.36
100 k	1.758	2.087	1.8	2.1285	4.9432	–86.804	321.04	11.15	3.21	8.65	647.48	21.78	591.24	20.04
200 k	1.86	1.965	1.902	2.008	2.5335	–86.847	313.19	21.16	3.58	10.8	632.14	41.38	577.05	37.97
400 k	2.069	1.8635	2.11	1.9022	1.2965	–86.88	306.22	39.8	4.56	9.17	618.52	78.1	564.52	71.1
1 M	2.271	1.7725	2.341	1.8016	0.5332	–86.86	297.76	90.6	4.713	12.32	600.58	179.8	548.22	160.5
2 M	2.363	1.7285	2.484	1.7512	0.27134	–86.52	292.16	179.7	4.87	20.63	584.12	354.8	533.75	308.4
4 M	2.838	1.6742	3.012	1.695	0.13817	–85.474	285.32	395	6.16	27.45	550.9	783	505.7	651
10 M	0.908	1.335	1.187	1.3597	0.059187	–83.883			4.82	22.7	374.3	841	354.44	703

The following graphs illustrate the measured values for the 6-foot segment of cable.

Figure 18. Cable Resistance Across Frequency

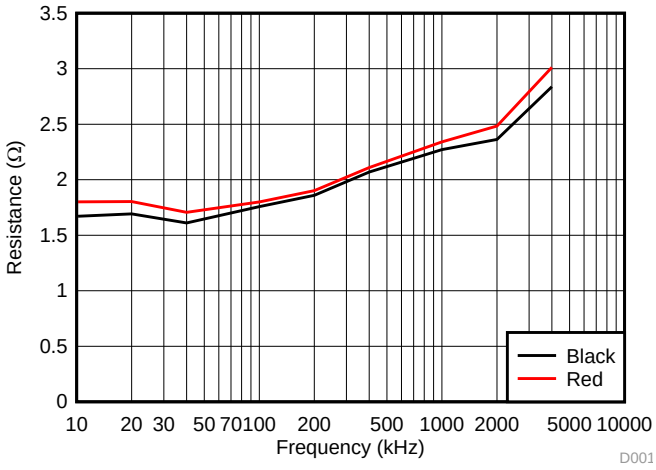


Figure 19. Cable Inductance Across Frequency

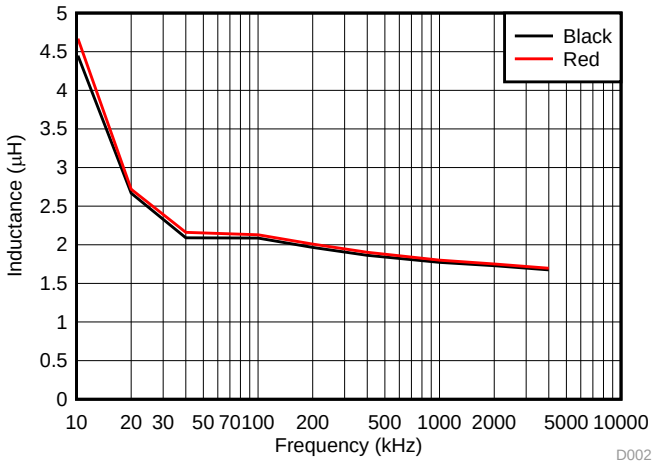


Figure 20. Cable Capacitance Across Frequency

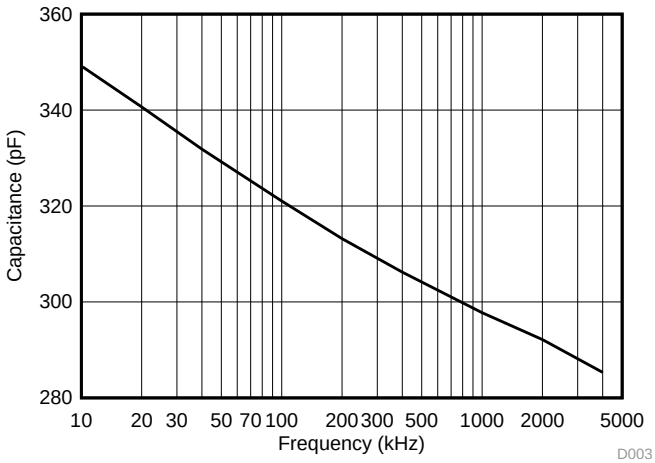
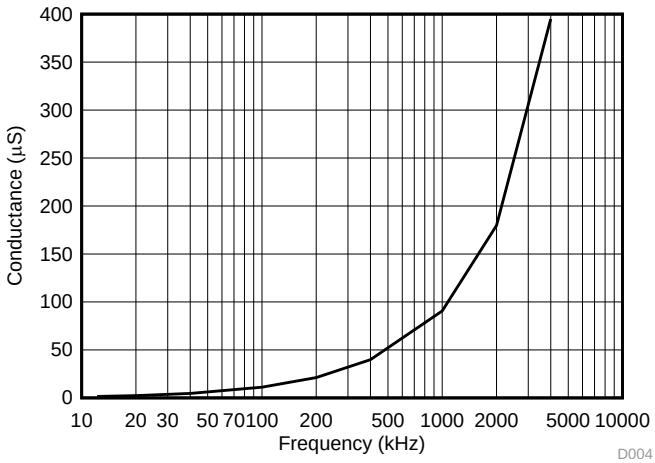


Figure 21. Cable Conductance Across Frequency



The characteristic impedance of a transmission line is defined by (see Reference #3 in Section 3):

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{8}$$

where

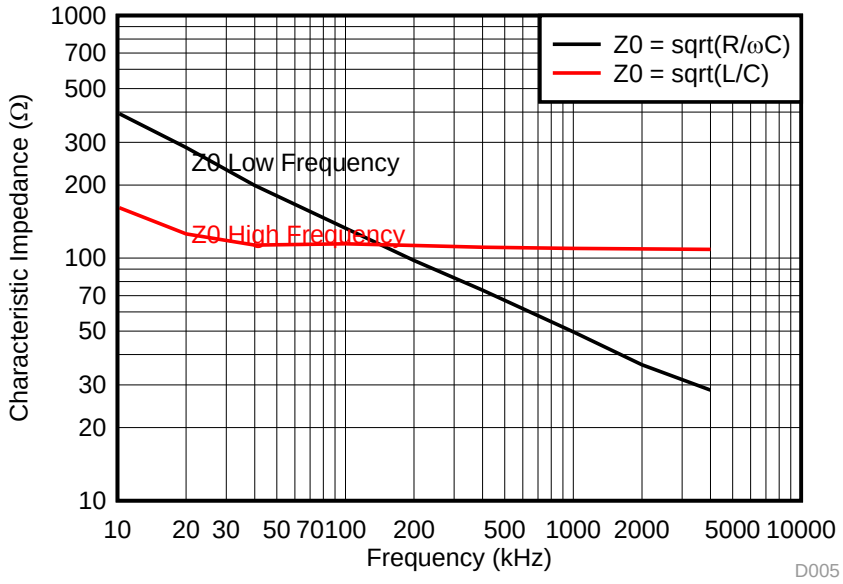
- R is the conductor series resistance per unit length
- G is the shunt conductance per unit length
- C is the capacitance per unit length

At low frequencies, the equation is reduced to:

$$Z_0 = \sqrt{\frac{R}{\omega C}} = \sqrt{\frac{R_{BLACK} + R_{RED}}{2\pi f C_{DIFF}}} \tag{9}$$

The characteristic impedance for the cable is calculated using these equations. Figure 22 plots the low frequency and high frequency curves for Z_0.

Figure 22. Characteristic Impedance Across Frequency



The cable model parameter values were calculated as described in Table 3.

Table 3. Final Cable Model Parameter Values(1)

Parameter	Value	Calculation
R	6.8 mΩ/ft	Average R per unit length for red and black wires at DC for 6-ft segment length.(2)
L	351.3 nH/ft	Average L per unit length for red and black wires at 100 kHz for 6-ft segment length.(3)
C (diff)	66.24 pF/ft	Average C per unit length for differential open capacitance (red-black) at 1 kHz for 6-ft segment length.
G (diff)	50.5 mΩ × ft	Average G per unit length for differential open conductance (red-black) at 1 kHz for 6-ft segment length; converted to ohms.
C (sig-Gnd)	125.59 pF/ft	Average C per unit length for differential open capacitance (reg-gnd and black-gnd) at 1 kHz for 6-ft segment length.
G (sig-Gnd)	26.56 mΩ × ft	Average G per unit length for differential open conductance (reg-gnd and black-gnd) at 1 kHz for 6-ft segment length.
Z_o	130 Ω at 100 kHz	Z_0 at 100 kHz from low frequency line on Figure 22.

(1) All the values calculated in Table 3 are derived from Figure 18 through Figure 22. The goal of this document is not to create a frequency-dependant model. Therefore, a baseline value was selected from the data figures to approximate a frequency-independent model. For example, at high frequencies the cable conductance (Figure 21) increases exponentially, while the cable capacitance (Figure 20) decreases. Therefore, a low-frequency conductance and capacitance value is used.

(2) As the data in Table 2 shows, there is a considerable difference between the low-frequency resistance, R, measurements at DC and at low frequencies. Since the model in Figure 17 does not have a dependence on frequency, the decision was made to use R instead R_S / 2 in the model.

(3) At f = 100 kHz, the L value is flat in Figure 19.

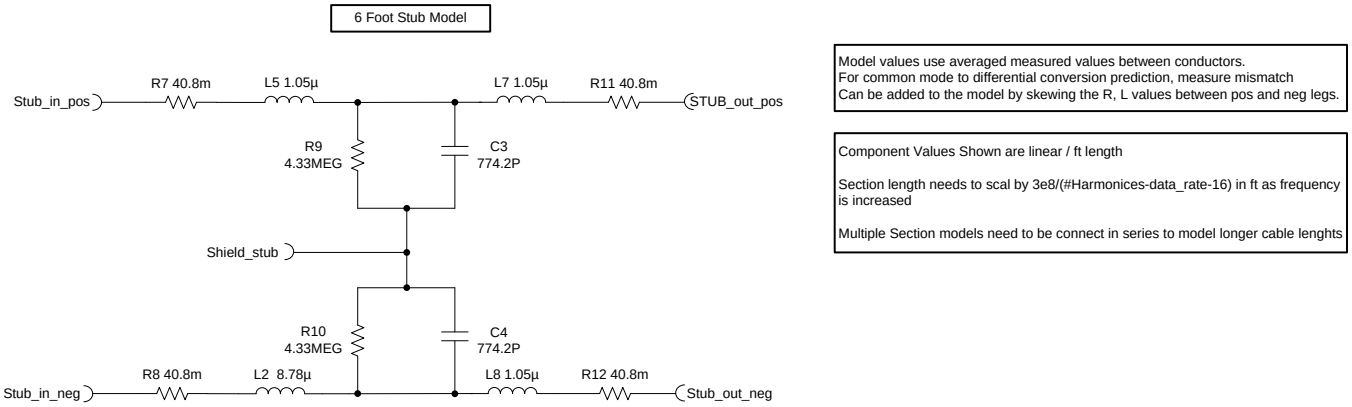
The bandwidth of the cable being modeled also needs to be characterized primarily to determine the practical limits of the cable in terms of data rate. However, for model development, knowing the maximum bandwidth of the cable also determines where in the characteristic impedance curve you will be operating and therefore what the termination of the cable needs to be. Additionally, knowing the maximum frequency makes it possible to determine the appropriate section length needed for the model.

For this particular cable, the frequency at which 3 dB of signal is lost (also referred to as the cable insertion loss) at the end of a 500-ft section of cable was measured to be 196 kHz. Assuming a simple inverse square law for cable loss versus distance relationship, then for 1000 ft of cable we would expect to see 3-db insertion loss at roughly 50 kHz. Similarly, for an insertion loss of 6 dB with 1000 ft of cable, expect a maximum frequency of approximately 196 kHz. Conservatively, we can assume in this case that for 1000 ft of cable, a maximum frequency of 100 kHz is a good target.

While there are many measurement techniques available to determine the maximum cable bandwidth, a very simple method was used here. A more accurate way to determine the maximum cable bandwidth would be to measure the bit error rate (BER) of a representative network while increasing frequency. Since this technique is more closely related to the way the cable is used, inaccuracy due to equivalent loads, improper termination, and arbitrary maximum insertion loss can all be eliminated.

Figure 23 and Figure 24 show the models created for a 6-foot cable stub and a 50-foot section of cable, respectively. The models were created by scaling the parameters in Table 3.

Figure 23. 6-Foot Stub Cable Model



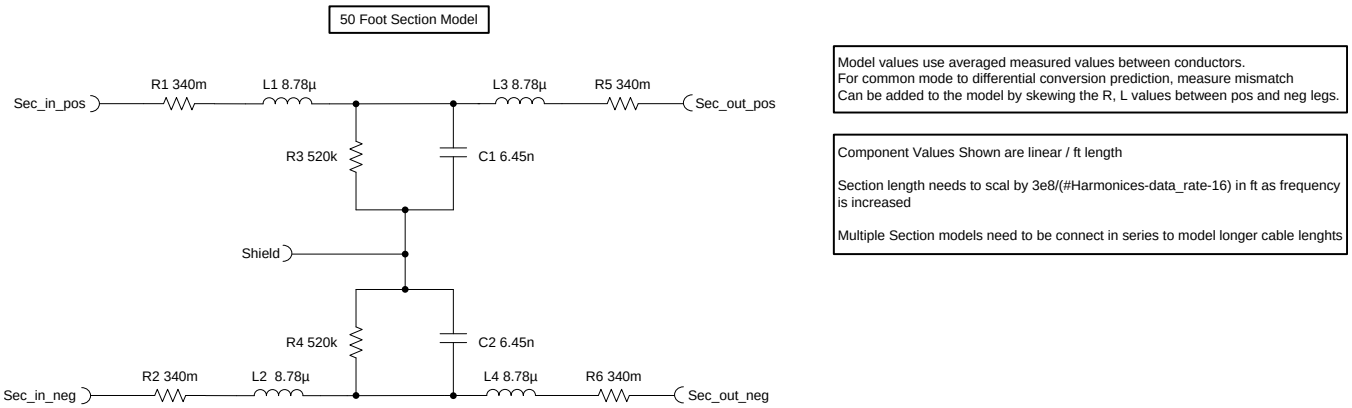
(1) R_S = 6.8 mΩ/ft × 6 ft = 40.8 mΩ (see Note 1 on Table 3)

(2) L_S / 2 = (351.3 nH/ft × 6 ft) / 2 = 1.05 µH

(3) C_S = AVG[(C (sig-Gnd), 2 × C (diff)] × 6 = 774.2 pF (see discussion on removal of C and G from component model)

(4) G_s = AVG[(G (sig-Gnd), G (diff) / 2] / 6 = 4.32 MΩ (see discussion on removal of C and G from component model)

Figure 24. 50-Foot Section Cable Model



(1) R_S = 6.8 mΩ/ft × 50 ft = 340 mΩ (see Note 1 on Table 3)

(2) L_S / 2 = (351.3 nH/ft × 50 ft) / 2 = 8.78 µH

(3) C_S = C_S (6 ft) / 6 ft × 50 ft = 6.45 nH (see discussion on removal of C and G from component model)

(4) G_S = G_S (6 ft) × 6 ft / 50 ft = 520 kΩ (see discussion on removal of C and G from component model)

The models in Figure 23 and Figure 24 have been simplified by removing the G and C components from the original model (see Figure 17). Note that with the shield signal open the total differential capacitance in Figure 17 is given with:

$$C(diff) = \frac{C_S}{2} + C \tag{10}$$

For the 6 foot model, C (diff) = 66.24 pF × 6 = 397.44 pF. C_S using the C (sig-gnd) parameter is 125.59 pF × 6 = 753.54 pF. Using these two values and solving for C:

$$C = C(diff) - \frac{C_S}{2} = 397.44pF - \frac{753.33pF}{2} = 20.67pF \tag{11}$$

Compared to C_S / 2, C is > 18 × smaller so it can safely be removed. Averaging C (diff) and C (sig-gnd) for the C_S calculation makes up for the small error from simply ignoring C in the model.

Similarly, the total for differential conductance, G, (in Ω) is given using Equation 12:

$$G(diff) = \frac{G(2G_S)}{(2G_s + G)} \tag{12}$$

For the 6 foot model, G (diff) = 50.5 MΩ / 6 = 8.41 MΩ. G_S using the G (sig-gnd) parameter is 26.56 MΩ / 6 = 4.43 MΩ. Using these two values and solving for G:

$$G = \frac{(G(diff) \cdot 2G_s)}{(2G_S - G(diff))} \quad (13)$$

$$G = \frac{(2 * 8.41M\Omega * 4.43M\Omega)}{(2 * 4.43M\Omega - 8.41M\Omega)} = 165.58M\Omega \quad (14)$$

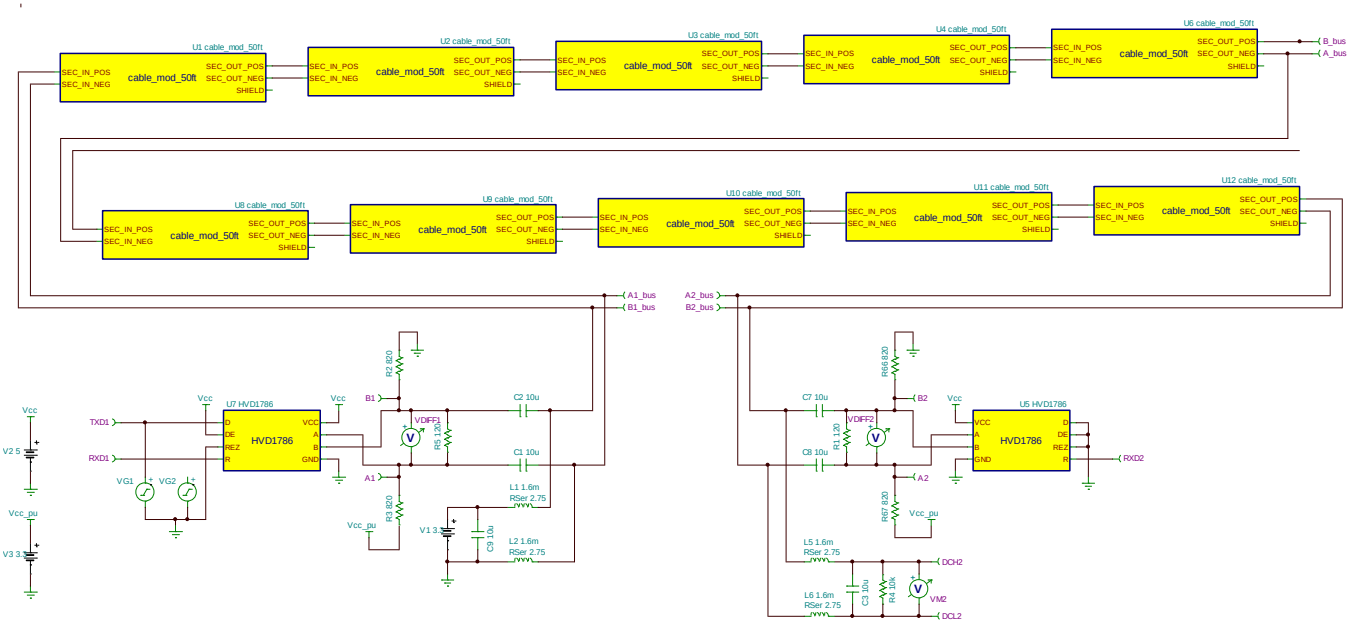
This is nearly 19 × larger than 2 × Gs which is in parallel with it, so it can also be safely removed. Similar to the capacitance in the previous case, averaging G (diff) and G (sig-gnd) makes up for the small error from simply ignoring G in the model.

To validate this simplification, note that from Figure 23, C4 in series with C3 is 387.1 pF. Compare this value to the curve in Figure 20 and note that the values are very close. Similarly for 1 / (R9 + R10) compared to the curve in Figure 21. Note that these model simplifications may not apply to all types of cable configurations.

2.5.2.2 Simulation Setup

Figure 25 shows the TINA-TI schematic used to simulate the point-to-point system connected through a 1000-foot cable. Ten 50-foot cable segments are used to mimic the 500 feet of cable. Note that the coupling network component values (C1, C2, L1, and L2) match the component values used in the physical setup.

Figure 25. Point-to-Point System Using Cable Model Simulation Schematic



2.5.2.3 Hardware Measurements

A point-to-point physical network was created using a pair of TIDA-00527 boards and 1000-foot section of cable. The following modifications were made to the TIDA-00527 board:

- 820-Ω pullup resistor was added to VCC at U1 pin 7 for failsafe biasing
- 820-Ω pulldown resistor was added to GND at U1 pin 6 for failsafe biasing
- 600-µH inductors were added between pins 8 and 5 on JMP8 and JMP9

A micro-controller was used to generate a Manchester encoded bit stream on a UART serial port at a baud rate of 115200.

2.5.2.4 Simulation Results

Figure 26, Figure 27, and Figure 28 compare the simulation results based on a cable model to the measurements made on an actual 500 ft section of cable for a point-to-point system. The waveforms compare the transmit (TXD), receive (RXD), and bus signals (A/B bus) of the simulation to the measurements. Note that the A/B bus and RXD signals have been aligned for comparison by shifting the TXD signal.

The results show good agreement between the simulation and the hardware test. Some of the differences between simulation and the cable measurements include:

1. Measurement uses a 3-V RS-485 transceiver while the simulations use a 5-V transceiver.
2. Simulation uses ideal component values while actual measurements use components with real tolerances.
3. Simulation model for RS-485 transceiver is idealized for driver edge rate. This is likely the source of the ringing in the simulation waveforms for the bus nodes. Also, the transceiver simulation model is meant to be a functional representation so there are other aspects of the model which do not match data sheet performance parameters.
4. The cable used in the hardware test is likely not very close in lot number to cable used to develop simulation model. The spools used to develop the cable model and for the measurements were purchased in different locations and many months apart. Because the impedance of this type of cable is not controlled, transmission line performance characteristics are expected to vary significantly.
5. Scope settings or probe bandwidth of equipment used in the hardware test may be filtering measurement results.

The simulations appear to be pessimistic on both attenuation and delay. This may be due to the transceiver model or a difference in speed rating of transceivers used in the hardware test (20 Mbps) versus simulation (1 Mbps).

Figure 26. TXD Master Simulation Results Compared to Actual Cable Measurements

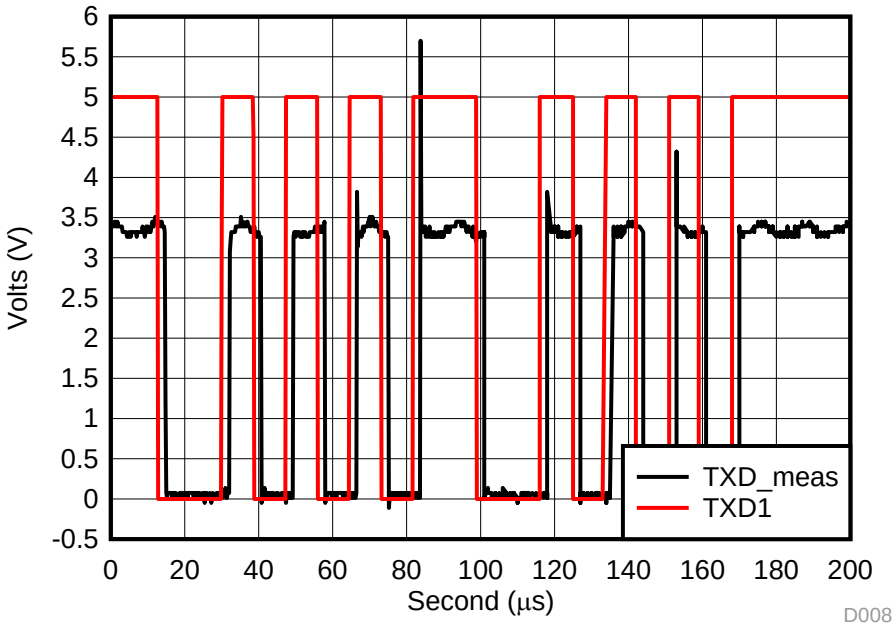


Figure 27. RXD Slave Simulation Results Compared to Actual Cable Measurements

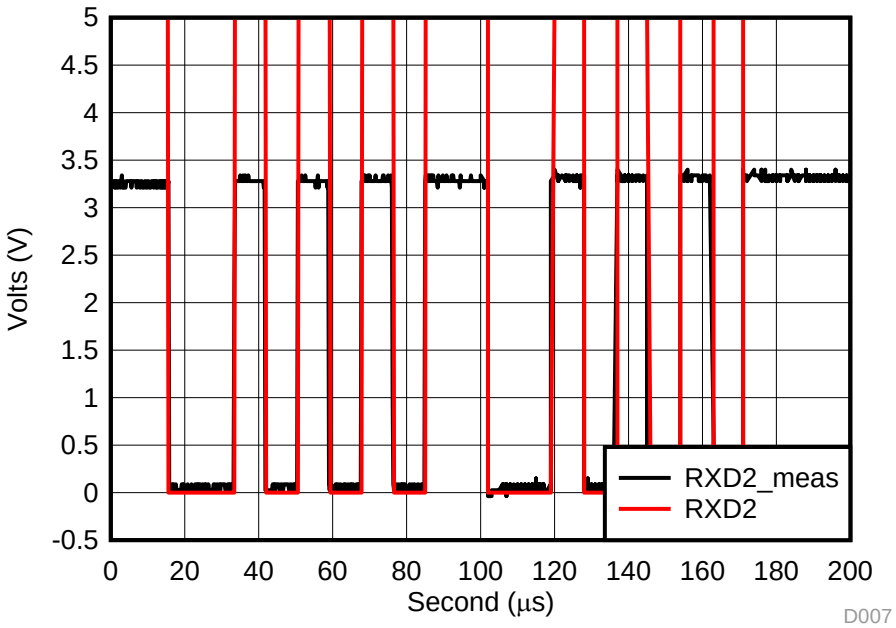
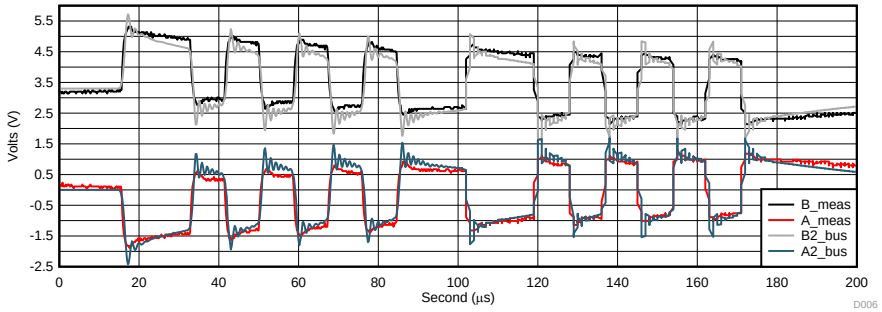


Figure 28. Bus Node At Input To Slave Simulation Results Compared to Actual Cable Measurements



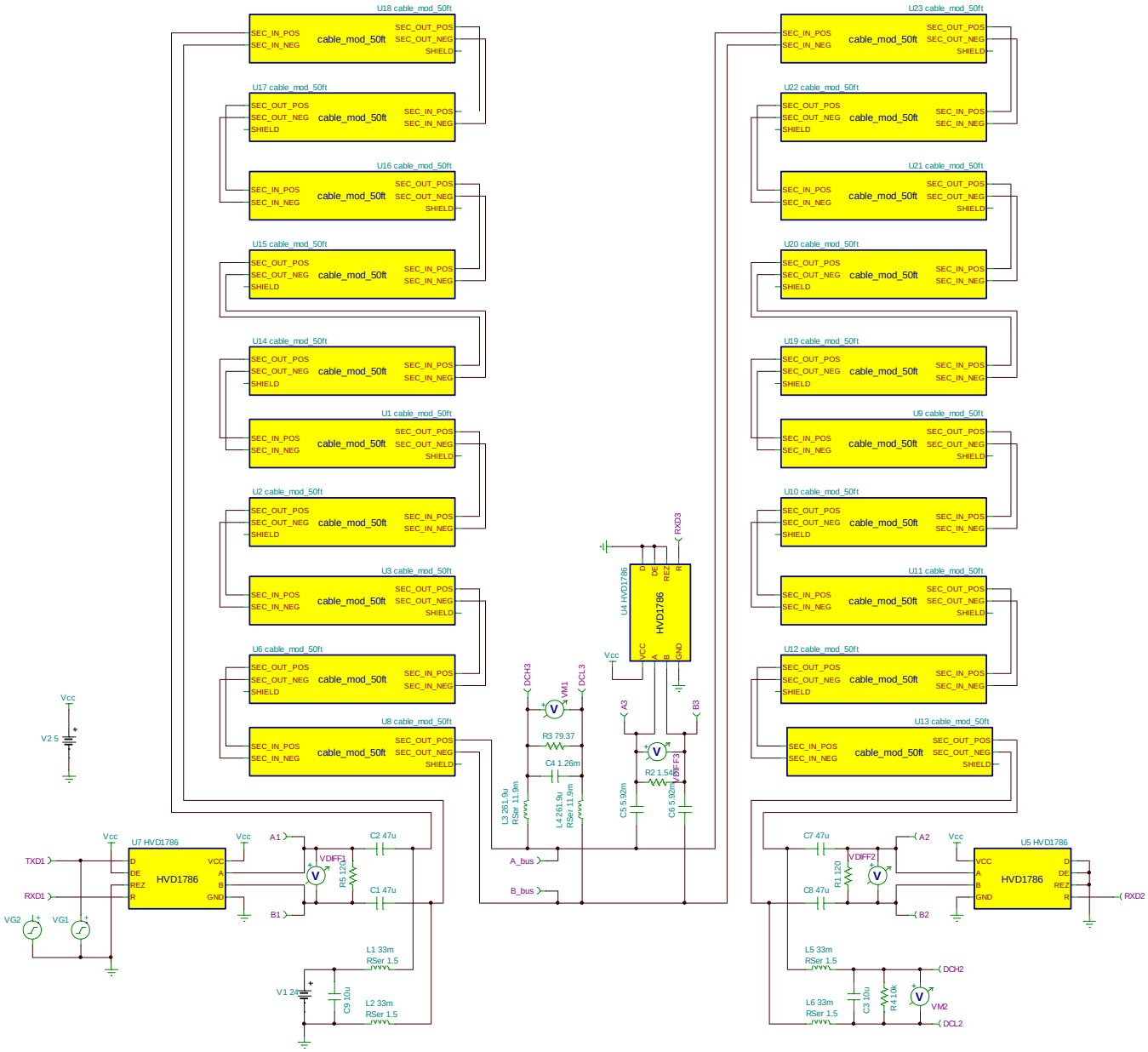
2.5.3 Multi-Node Simulation With Cable Model

A TINA transient analysis was performed on a multi-node network using a cable model. The goal of the transient analysis was to understand if the differential output voltage (V_{OD}) at the receiver node provided enough noise margin given the simulated data rate and number of nodes.

2.5.3.1 Simulation Setup

Figure 29 shows the TINA simulation schematic for the multi-node setup using a cable model. The schematic consists of a transmitter node, a receiver node, and a node intended to mimic the effect of loading the network with multiple nodes. There is 500 feet of cable between the transmitter node and the multi-node load, and another 500 feet of cable between the multi-node load and the receiver node. The cable model was developed as described in Section 2.5.2. The TINA simulation model uses an excitation source and several voltage probes are also used to analyze the network response over time.

Figure 29. Multi-Node Network With Cable Model Simulation



The simulation has the following main sections:

- Transmitter node: Consists of the excitation source, transceiver, and power source.
  - Excitation Source (VG2): 2.5-V square wave with programmable frequency (set to 32 kHz).
  - 24-V DC power source (V1): Coupled to bus through L1, L2 as calculated in Section 2.4.2.
  - HVD1786 transceiver (U7): Coupled to the bus through C1, C2 as calculated in Section 2.4.2.
- Receiver node: Consists of transceiver and power rail load.
  - HVD1786 transceiver (U5): Coupled to the bus through C7, C8 as calculated in Section 2.4.2.
  - Power rail load (C3, R4): Simulated power load at the receiver end. For this simulation R4 = 10 kΩ and C3 = 10 µF. At 24 VDC, the load is approximately 58 mW. The power load is coupled to the bus through L5, L6 as calculated in Section 2.4.2.
- Multi-Node Load: Simulated network load on the data bus and the power rail.
  - HVD1786 transceiver (U4): Each transceiver on the network is coupled to the bus through a coupling network (C5, C6). The capacitor value is calculated for one node as in Section 2.4.2 and scaled using C × (#nodes-2), where #nodes is the total number of nodes.
  - Transceiver Load (R2): The component R2 represents the multi-node load looking into all the transceivers on the network. A single HVD1786 has a maximum bus input current spec of 125 µA at 12 V which is equivalent to a 96-kΩ load. For a differential signal the leakage current doubles to 192 kΩ. The total load resistance R2 is scaled as R2 / (#nodes-3).
  - Power Rail Load (C4, R3): The components C4 and R3 represent the load for the multiple nodes on the power rail. These components are scaled as C × (#nodes-2) and R / (#nodes-2), where C and R are taken from the receiver node power load component calculations (C3, R4). Each load is coupled to the bus through a coupling network (L3, L4). The inductor value is calculated for one node as in Section 2.4.2 and scaled using L / (#nodes-2). Similarly, the equivalent series resistance (R_{ser}) of the inductors is calculated for one node and scaled as R_{ser} / (#nodes-2).
- Cable Segments: Two 500-foot cable segments connect the transmitter node, the multi-node load, and the receiver node.

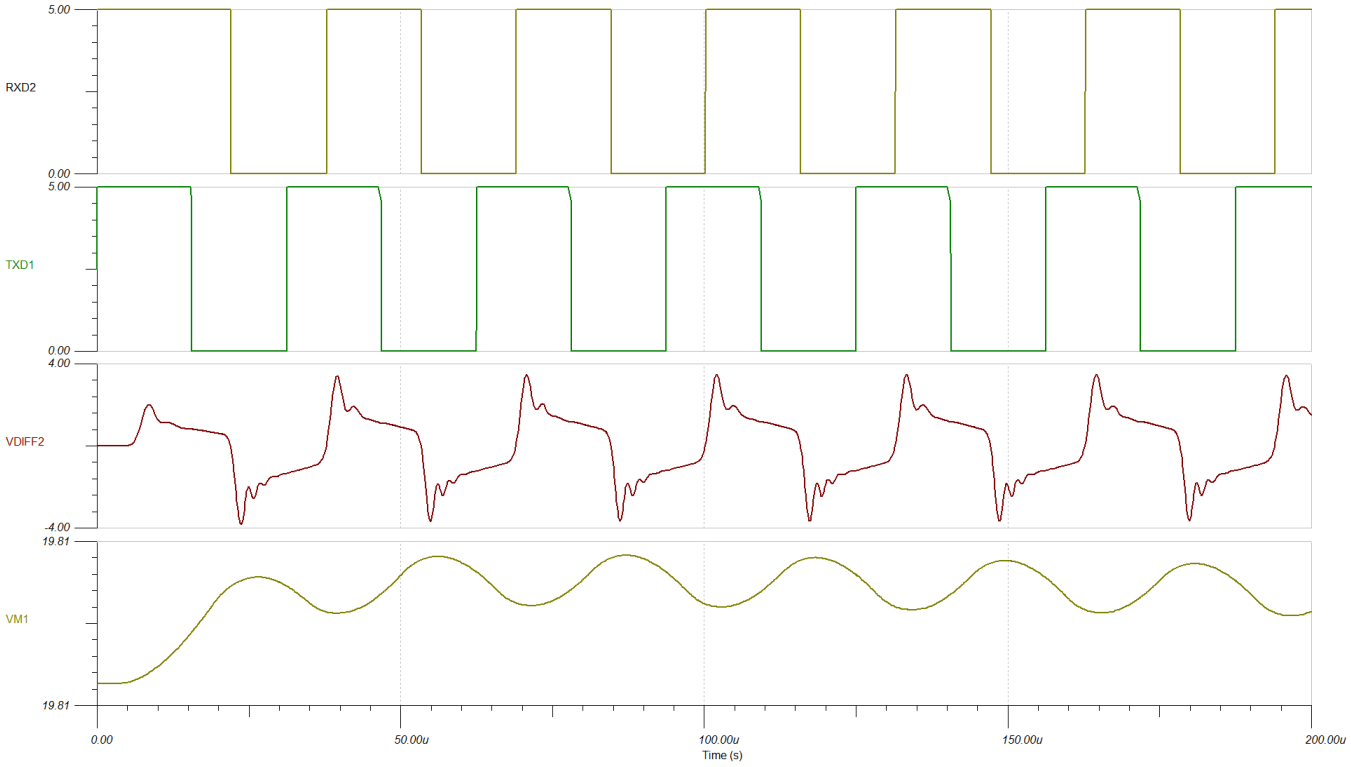
Voltage probes were placed at different points to capture the transient response of the circuit.

NOTE: Simulation does not include failsafe biasing for a defined DC differential level during idle. Failsafe biasing will reduce the number of nodes. See Section 2.4.1.6 and Section 2.4.1.7.

2.5.3.2 Simulation Results

The simulation results in Figure 30 show that V_{OD} = 715 mV at the receiver node. Also, the receiver node output, RXD2, equals the transmitter node input. The output waveform VM2 shows the 24-V DC supply at the receiver node.

Figure 30. Multi-Node Simulation With Cable Model Results (128 Nodes, 64 kbps Data Rate)



2.6 Design Files

2.6.1 Simulation Files

To download the TINA-TI simulation files, see the design files at TIDA-010035.

3 Related Documentation

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8. Texas Instruments, *RS-485 Power Over Bus Reference Design*

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