

Three-phase inverter reference design for 200–480 VAC drives with opto-emulated input gate drivers



Description

This reference design realizes a reinforced isolated three-phase inverter subsystem using isolated IGBT gate drivers and isolated current/voltage sensors. The UCC23513 gate driver used has a 6-pin wide body package with optical LED emulated inputs which enables its use as pin-to-pin replacement to existing opto-isolated gate drivers. This design shows that the UCC23513 input stage can be driven using all existing configurations used to drive opto-isolated gate drivers. In-phase shunt resistor based motor current sensing is done using AMC1300B isolated amplifier and DC link voltage, IGBT module temperature sensing using the AMC1311 isolated amplifier. The design uses a C2000™ LaunchPad™ for inverter control.

Resources

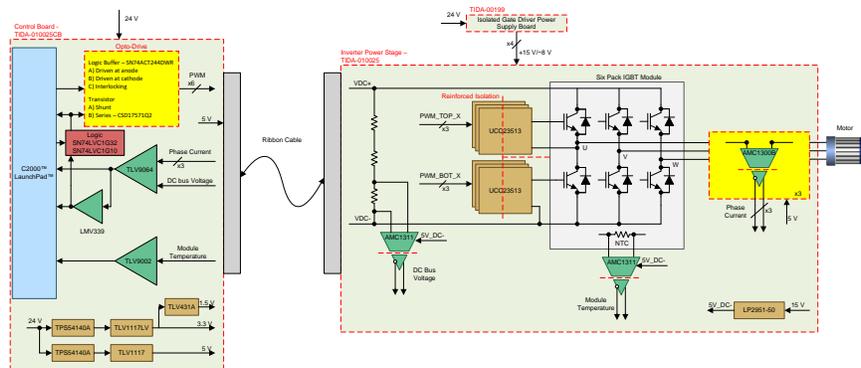
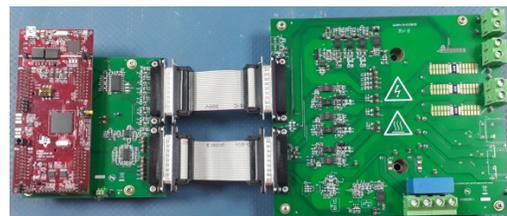
TIDA-010025	Design Folder
UCC23513	Product Folder
AMC1300, AMC1311	Product Folder
TLV9002, TLV9064	Product Folder
LMV339	Product Folder
SN74ACT244, SN74LVC1G10, SN74LVC1G32	Product Folder
CSD17571Q2	Product Folder
TPS54140A	Product Folder
TLV1117, TLV1117LV	Product Folder
TLV431A	Product Folder
LP2951	Product Folder
LAUNCHXL-F28379D	Tool Folder

Features

- Three-phase inverter power stage suited for 200–480 VAC powered drives with output current rating up to 14 Arms
- Reinforced isolated gate driver with opto-emulated inputs and 6-pin wide body package which can be used as pin to pin replacement for opto-isolated gate drivers
- Gate driver with wide operating ambient temperature up to 125°C with low parametric variations, high CMTI and working isolation voltage rating of 1500 Vdc results in improved system robustness
- Reinforced isolated In-phase shunt resistor based motor current sensing up to 25 Apk for all three phases with overcurrent protection response of < 5 μs
- Reinforced isolated DC link voltage sensing up to 800 V and temperature sensing up to 120°C using NTC integrated inside IGBT module using isolated amplifiers
- Inverter control using C2000 LaunchPad

Applications

- AC Inverter & VF Drives
- Servo CNC & Robotics
- Three-Phase UPS





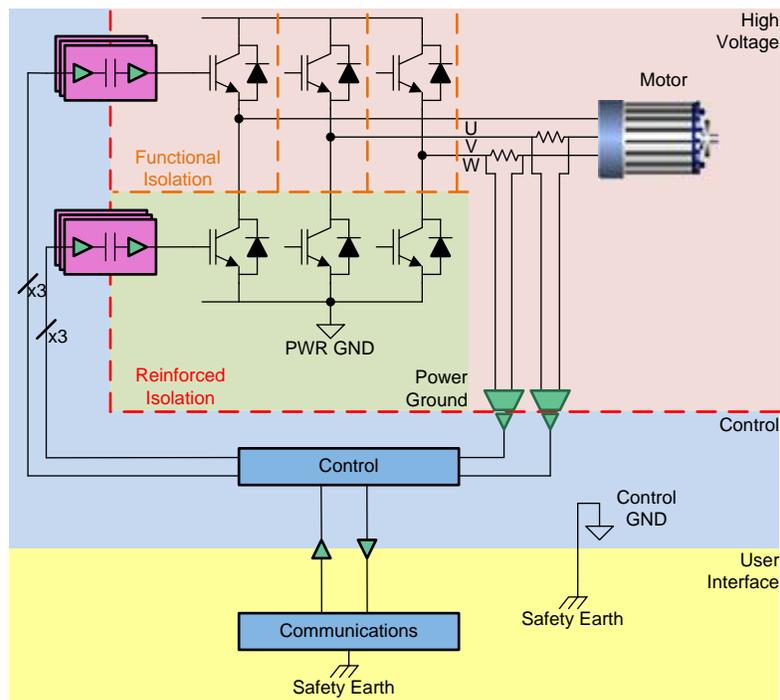
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1 System Description

A variable frequency drive (VFD) is a type of motor controller that drives an AC induction motor (ACIM) or permanent magnet synchronous motor (PMSM) by varying the frequency and amplitude of current supplied to the electric motor. The basic components of a VFD are:

- Input section, which draws AC electric power from the utility and converts the AC into DC power
- Inverter section, which converts DC back into a controllable AC waveform

Figure 1. Three-Phase Inverter With Isolated Gate Driver



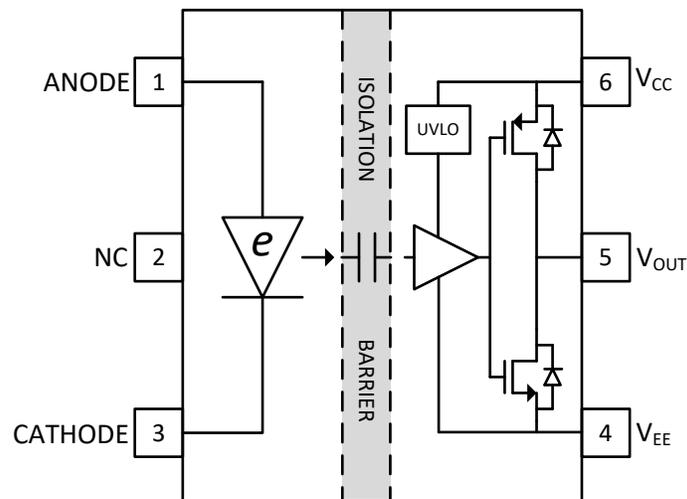
The three-phase inverter uses insulated gate bipolar transistor (IGBT) switches which have advantages of high input impedance as the gate is insulated, has a rapid response ability, good thermal stability, simple driving circuit, good ability to withstand high voltage, snubber-less operation and controllability of switching behavior providing reliable short-circuit protection. The IGBT is a voltage controlled device, which gives it the ability to turn on and off very quickly.

Figure 1 shows a typical application of a 3-phase inverter using six isolated gate drivers. This design uses the UCC23513 reinforced isolated gate driver device from TI. PWM control signals are required to turn the IGBT devices on and off which at the system level eventually may determine the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a MCU and are at low voltage levels such as 3.3 V or 5 V. The gate controls required by the IGBTs are in the range of 15 to 20 V and need high current capability to be able to drive the large capacitive loads offered by the IGBT gates. Also the gate drive needs to be applied with reference to the emitter of the IGBT and by inverter construction, the emitter node of top IGBT swings from 0 to the DC bus voltage, which is several hundreds of volts in magnitude. As the IGBT can float with respect to ground at the power stage, both the power supply and the gate circuitry should be isolated from the inverter ground. Isolated current sensors are used to measure the motor phase currents. The controller samples the current waveform and modulates the inverter output waveform to ensure that the motor phase current follows the current reference set-point inside the controller.

The UCC23513 is a capacitive isolated gate driver whose inputs emulate an opto-isolated gate driver input LED stage. The device is current controlled without any requirement for primary side power supply. Thus the gate driver can be used as a pin to pin replacement to opto-isolated gate drivers. Use of capacitive isolation provides additional benefits when compared to opto-isolation like:

- Wide operating ambient temperature range up to 125°C
 - Lower parametric variations with temperature and age
 - Higher working isolation voltage of 1500 Vdc
 - Higher common mode transient immunity (CMTI) and > 40 years isolation rating
- These benefits result in increased robustness at the system level.

Figure 2. UCC23513



This reference design demonstrates the following:

- UCC23513 works exactly like opto-gate drivers in a three-phase motor-drive inverter system and can be driven in all possible ways that opto-isolated gate drivers use presently
- Switching performance of gate driver, gate source/sink current waveforms, gate voltages and switch node voltage waveforms at hard and soft switching conditions

1.1 Key System Specifications

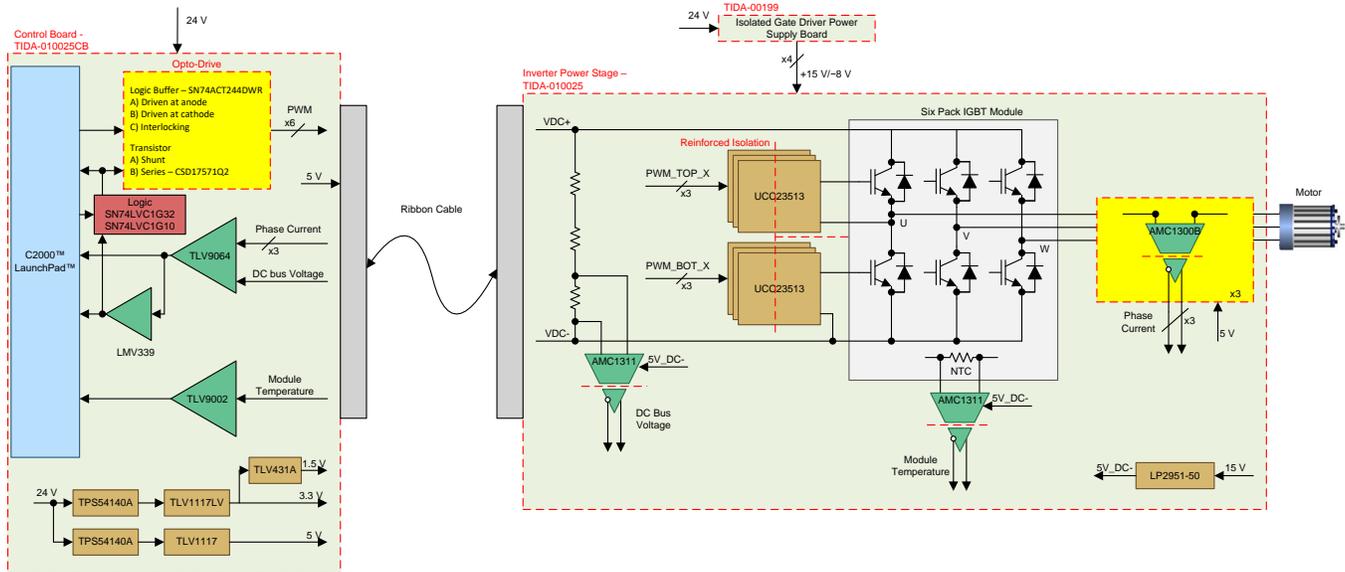
Table 1. TIDA-010025 Key System Specifications

SUBSECTION	PARAMETER	SPECIFICATIONS	COMMENTS
Inverter	DC bus voltage input	200 to 800 VDC	
	Continuous nominal output current rating	14 Arms	
	PWM switching frequency	Up to 20 kHz	Inverter tested with specified range
	Power switch used	1200-V, 25-A, converter inverter brake (CIB) module with integrated NTC	Part number: 7MBR25VA120-50
Motor current sensing	Measurement range	25 Apk	Shunt resistor used is 10 mΩ
DC bus voltage sensing	Measurement range	800 VDC	Resistor divider ratio is 2.5 mV/V
IGBT module temperature sensing	Measurement range	0°C to 120°C	
Protection	DC bus voltage	Overvoltage and undervoltage detection	User software implementation
	IGBT module temperature	Overtemperature shutdown and temperature derating	User software implementation
	Isolation	Reinforced isolation	Reinforced isolated gate drivers, current and voltage sensors. 8-mm creepage between the control side and high-voltage side
Connector interfaces	MCU interface	LaunchPad interface using berg stick connectors	See schematic for pin assignments on the connector
	Power	24 V, 200 mA	For powering the control side
		4 × +15 V, –8 V isolated from each other	For powering the six gate drivers. Individual isolated power supplies for the 3 high-side switches and one single supply for the 3 low-side switches and the brake IGBT
PCB information	PCB layer stack	Power board: 4 layer – 2-oz outer, 1-oz inner copper layers Control board: 4 layer – 1-oz copper	
	Laminate	FR4, high Tg	
	PCB thickness	1.6 mm	
	PCB size	Power board – 190.5 mm × 165.1 mm, control board – 113.03 mm × 114.3 mm	

2 System Overview

2.1 Block Diagram

Figure 3. TIDA-010025 Block Diagram



This reference design is a three-phase inverter drive for controlling AC and Servo motors. It comprises of two boards: a power stage module and a control module.

Power-stage module: This board performs the function of DC/AC conversion. A CIB IGBT module 7MBR25VA120-50 is used for the power conversion. This module has a three-phase diode based rectifier input stage, a three-phase IGBT based inverter output stage, an IGBT based brake chopper and an NTC thermistor integrated inside the module. In this design the rectifier stage is unused and provision is given to power the three-phase inverter stage directly with a DC power supply.

Six UCC23513 isolated gate driver devices are used to control the six IGBT switches of the inverter and 1 gate driver is used to control the braking chopper IGBT. The gates of the IGBTs are driven with +15-V, -8-V power supplies. 3 × individual isolated +15-V, -8-V power rails are used for controlling the high side IGBT gates and a single power rail is used to control the 3 low side IGBT gates and 1 brake chopper IGBT gate. The gate driver power supplies are generated using either TIDA-00199 isolated flyback converter or TIDA-010026 isolated flyback converter. Both these TIDs generate 4 × isolated +15-V, -8-V supplies from a single 24-V input rail. The inputs of UCC23513 emulate the inputs of an opto-isolated gate driver. They are current controlled and the control signals are driven from the control module. UCC23513 provides UVLO capability and in case of the gate drive power rails falling below the UVLO threshold the IGBT gate drive signals are cutoff.

Motor in-phase current sensing is done in all three phases using shunt resistors and isolated amplifier AMC1300B. The output differential signals are sent to the control module for further processing. The AMC1300B secondary side is powered from 5 V. This 5 V is generated using Zener diode from corresponding high-side 15-V IGBT gate control rail. The DC link voltage is measured using a voltage divider across the DC link and isolated amplifier AMC1311. The IGBT module temperature is measured using the NTC integrated inside the IGBT module. A voltage divider is formed using an external resistor and the NTC. The voltage drop across the NTC is sensed using isolated amplifier AMC1311. Both the AMC1311 amplifier secondary sides are powered using a 5-V supply. This supply is generated from the 15-V low-side IGBT control rail using LDO LP2951. Primary sides of the isolated amplifiers are powered using 5-V rail.

Control module: This board performs the function of the controlling the power module. It captures the current and voltage feedback signals from the power module, processes them and generates PWM signals to control the IGBT gate drivers. This board comprises of the MCU, analog signal conditioning, PWM signal buffering and the control side DC/DC power supply generation circuitry.

The TMS320F28379D based C2000 LaunchPad LAUNCHXL-F28379D is used for inverter control. Berg stick headers are provided on the control module for mounting the LaunchPad. The controller generates the 3.3-V PWM pulses for controlling the IGBT gate drivers. The IGBT gate driver UCC23513 is current controlled and the 3.3-V PWM pulses need to be converted into approximately 10-mA current signals. Multiple circuit configurations are provided for this conversion and the user can evaluate any of the following configurations (there are more details in the [Section 2.3.3.1](#)):

- SN74ACT244D buffer drives anode of UCC23513
- SN74ACT244D buffer drives cathode of UCC23513 (SN74ACT240 can replace SN74ACT244 incase PWM inversion is required)
- SN74ACT244D is used to interlock high side and low side gate drivers
- MCU directly drives CSD17571Q2 NMOS in series with UCC23513 input
- MCU directly drives NPN BJT which is in parallel with UCC23513 input

NOTE: The input of the SN74ACT244D is 3.3-V input logic compatible while being powered from the 5-V supply.

TLV9064 is used in the difference amplifier configuration to convert the differential current and voltage sense signals from the isolated amplifiers to single ended. The single ended output signals drive the single ended ADC inputs on the LaunchPad. Note that the outputs of TLV9064 used for sensing motor phase currents are level shifted to allow sensing of bipolar currents. A slower amplifier TLV9002 is used for converting the module temperature sense signal from differential to single ended. TLV431A is used for generating the 1.5-V reference signal for level shifting and this reference signal is buffered using TLV9002 before distributing it to different amplifiers. LMV339 is set in the window comparator configuration to detect overcurrent. In-case of overcurrent in any of the three motor phases the comparator output goes low and triggers the enable pin of the PWM buffer. The output of the buffer is tri-stated which turns off the gate driver outputs resulting in inverter shutdown.

A single 24-V power supply rail input is required for the control board. Two TPS54140A DC/DC buck converters generate intermediate rails for downstream LDOs which generate 3.3 V and 5 V. LDO TLV1117LV generates the 3.3-V rail and the LDO TLV1117 generates the 5-V rail. The 3.3-V rail is used to power the LaunchPad and the analog signal conditioning circuit on the control board. The 5-V rail is used to power the PWM buffer and also sent across to the power stage module for powering the primary sides of the isolated amplifiers. Power supply sequencing is done by interconnecting the PowerGood and enable pins on the TPS54140A devices. First the 3.3-V rails comes up and then the 5-V rail.

2.2 Highlighted Products

2.2.1 UCC23513

The UCC23513 is an opto compatible, single channel, isolated IGBT, SiC, and MOSFET gate driver with 3-A peak output current and 5 kV_{RMS} reinforced isolation rating. UCC23513 can drive both high side and low side power switches. Key features and characteristics bring significant performance and reliability upgrades over standard opto-coupler based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design. Performance highlights include high CMTI, low propagation delay and small pulse width distortion. Tight process control means small part-to-part skew. The input stage is an emulated diode (ediode) which means long term reliability and excellent aging characteristics over traditional LEDs. Additionally, the material group 1 mold compound and the resulting comparative tracking index (CTI) of > 600 V means robust insulating material. The high performance and reliability of the UCC23513, along with its stretched SO-6 package, > 8.5-mm clearance and creepage makes it suitable for inverter applications in motor drive, solar, industrial power supplies and appliances. The higher operating temperature opens up opportunities for applications not previously supported by traditional opto-couplers.

In this design UCC23513 is used to drive the 6 inverter IGBT gates and the brake chopper IGBT gate.

2.2.2 AMC1300

The AMC1300 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the AMC1300 is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings and especially in motor control applications, lower torque ripple. The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1300 simplify system level design and diagnostics.

In this design the AMC1300B version of the device which has lower offset, gain error and temperature drift is used to sense current in the 3 motor phases. The higher accuracy of the B version enables more precise and smoother control of the motor across operational ambient temperature.

2.2.3 AMC1311

The AMC1311 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The high-impedance input of the AMC1311 is optimized for connection to high voltage resistive dividers or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate, low temperature drift voltage or temperature sensing and control in closed-loop systems. The integrated missing high-side supply voltage detection feature simplifies system level design and diagnostics.

In this design AMC1311 is used to sense the inverter DC link voltage using a high impedance resistor divider network. The 2-V input range of the device makes it less sensitive to inverter switching noise and the high impedance input does not alter the resistor divider ratio. The device is also used to measure the voltage across the NTC resistor integrated inside the IGBT module.

2.2.4 TLV9064

The TLV9064 is a quad low voltage op amp with rail to rail input and output swing capabilities. This device is a highly cost effective solution for applications where low voltage operation, a small footprint and high capacitive load drive are required. Although the capacitive load drive of the TLV9064 is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler.

In this design the device is used to convert differential ended signals from the isolated amplifier into single ended signals which then drive the MCU ADC. Unity GBW of 10 MHz and slew rate of 6.5 V/ μ s enable fast transient response for the motor control loops. Internal RFI and EMI filters enable accurate measurements inside the noisy electrical environment within a drive.

2.2.5 TLV9002

The TLV9002 is a dual low voltage op amp with rail to rail input and output swing capabilities. This device provides a cost effective solution for applications where low voltage operation and high capacitive load drive are required. The capacitive load drive of TLV9002 is 500 pF and the resistive open loop output impedance makes stabilization easier with much higher capacitive loads. The robust design of the TLV9002 simplifies circuit design. The op amps feature unity gain stability, an integrated RFI and EMI rejection filter and no phase reversal in overdrive conditions.

In this design it is used to convert differential ended signal from the NTC voltage measurement isolated amplifier into single ended signal which drives MCU ADC. The TLV9002 has a lower unity gain bandwidth of 1 MHz and slew rate of 2 V/ μ s which makes it ideal for measuring the slow moving temperature signal. Internal RFI and EMI filters enable accurate measurements inside the noisy electrical environment within a drive.

2.2.6 LMV339

The LMV339 is a low voltage quad comparator. This device provides a cost effective solution for applications where low voltage operation, low power, space savings and fast response are required.

In this design the LMV339 is used in the window comparator configuration for detection of overcurrent in the motor phases. The fast response time (prop delays less than 500 ns) enables fast turn off of the inverter in cases of short-circuit faults.

2.2.7 TLV431A

The TLV431 device is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. The output voltage can be set to any value from V_{ref} (1.24 V) to 6 V with two external resistors. These devices have a typical output impedance of 0.25 Ω . Active output circuitry provides a very sharp turnon characteristic, making them excellent replacements for low-voltage Zener diodes in many applications.

The motor phase current is a bipolar signal whereas the MCU ADC is unipolar. A reference signal is required to level shift the measured current signal into the ADC. In this design the reference signal is generated using TLV431A.

2.2.8 SN74ACT244A

The SN74ACT244 is an octal buffer which operates with a 5-V supply and has TTL compatible inputs. These devices are organized as two 4 bit buffers and drivers with separate output enable inputs. When OE is low, the device passes non-inverted data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

The UCC23513 has a current driven ediode input stage. The PWM outputs of the MCU are 3.3-V signals which are converted into approximately 10-mA current signals using the buffer device. The buffer can also disable the gate drivers in case of fault conditions. The active low enable pin of the buffer is pulled high and the buffer outputs turn high impedance.

2.2.9 SN74LVC1G32

This single 2-input positive OR gate is designed for 1.65 V to 5.5 V_{CC} operation. The device performs the Boolean function $Y = A + B$. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

2.2.10 SN74LVC1G10

The SN74LVC1G10 performs the Boolean function $Y = \overline{A \times B \times C}$. The device is fully specified for partial power down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

2.2.11 CSD17571Q2

This device is a 30-V, 20-m Ω $R_{DS(on)}$, SON2 \times 2 NexFET™ power MOSFET designed to minimize losses in load management applications while offering excellent thermal performance for the size of the package. In this design the FET is used to control the current flow through input ediode of the UCC23513.

2.2.12 TPS54140A

The TPS54140A device is a 42-V, 1.5-A, step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low ripple-pulse skip mode reduces the no-load, regulated output supply current to 116 μ A. Using the enable pin, shutdown supply current is reduced to 1.3 μ A.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow start pin that can also be configured for sequencing/tracking. An open drain power good signal indicates the output is within 94% to 107% of its nominal voltage. A wide switching frequency range allows efficiency and external component size to be optimized. Frequency fold back and thermal shutdown protects the part during an overload condition.

In this design the device is used for generating intermediate voltage rails for the 3.3-V and 5-V LDO post regulators. The input voltage is 24 V.

2.2.13 TLV1117LV

The TLV1117LV series of low-dropout (LDO) linear regulators is a low input voltage version of the popular TLV1117 voltage regulator. The TLV1117LV family of LDOs is also stable with 0 mA of load current; there is no minimum load requirement. The device offers excellent line and load transient performance resulting in very small magnitude undershoots and overshoots of output voltage when the load current requirement changes.

A precision bandgap and error amplifier provides 1.5% accuracy. A very high PSRR enable the use of the device for post-regulation after a switching regulator. Other valuable features include low output noise and low dropout voltage.

The device is internally compensated to be stable with 0- Ω equivalent series resistance (ESR) capacitors. These key advantages enable the use of cost effective small size ceramic capacitors. Cost effective capacitors that have higher bias voltages and temperature derating can also be used if desired.

In this design the TLV1117LV LDO acts as a post regulator on the buck converter and generates the 3.3-V rail for the control module

2.2.14 TLV1117

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V and adjustable output voltage options. All internal circuitry is designed to operate down to 1-V input to output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA decreasing at lower load currents.

In this design the TLV1117 LDO acts as a post regulator on the buck converter and generates the 5-V rail for driving the opto-tron input stage and for powering the primary side of the isolated amplifiers.

2.2.15 LP2951

The LP2951 device is a bipolar low dropout voltage regulator that can accommodate a wide input supply-voltage range of up to 30 V. The 8-pin LP2951 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together and the FEEDBACK and VTAP pins together, the LP2951 outputs a fixed 5 V, 3.3 V, or 3 V, depending on the version.

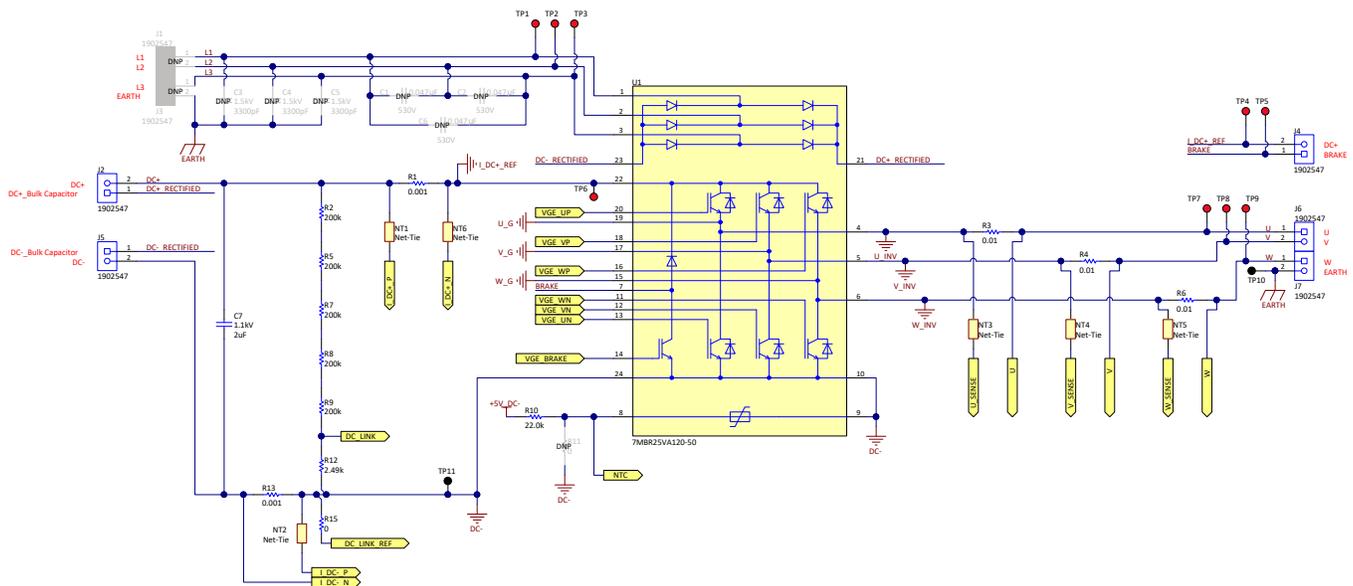
In this design the device is used to generate 5-V rail from 15-V gate driver power supply for powering the secondary side of DC- referenced isolated amplifiers.

2.3 System Design Theory

2.3.1 Three-Phase Inverter

This reference design uses a converter inverter brake (CIB) IGBT module to implement the three phase inverter. A CIB IGBT module has a diode based three phase rectifier front end, IGBT based three-phase inverter output stage and a brake chopper stage all integrated within a single module. The IGBT module part number used is the 1200-V, 25-A module 7MBR25VA120-50.

Figure 4. Three-Phase Inverter



The TIDA-010025 inverter designed using the IGBT module has a nominal output current rating of 14 Arms. Note that in this design provision has been given for three-phase mains voltage rectification but is not tested. 200 to 480 VAC mains input is given to connectors J1 and J3. C3, C4, C5 are the Y caps and C1, C2, C6 are the X caps used for AC line filtering. The output of the rectifier stage (DC+_RECTIFIED and DC-_RECTIFIED) is given to connector J2 and J5. User should use an external PCB with appropriately designed bulk capacitors to smooth the rectified AC waveform. This PCB should also contain bleeder resistors and inrush current control circuitry. The smoothed DC waveform should be rerouted to J2 and J5 as shown in schematic.

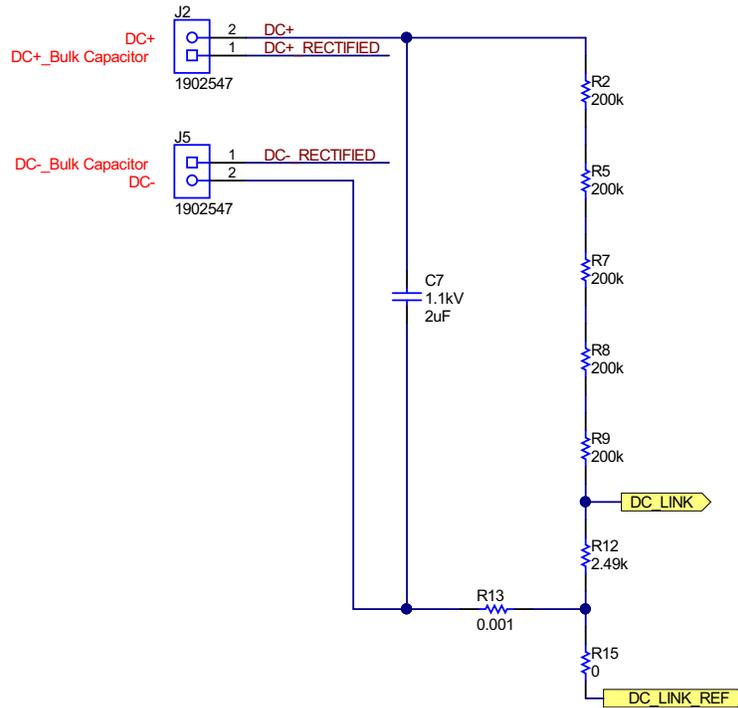
For TIDA-010025 design testing DC link voltage is directly provided to the inverter through J2 and J5 using an external current limited DC source and the rectifier front end is not used. C7 is the high frequency decoupling capacitor. Resistor chain comprising of R2, R5, R7, R8, R9 and R12 is used for measuring the DC link voltage. The output of the inverter is passed through shunt resistors R3, R4 and R6 to connectors J6 and J7 to which the motor phase terminals are connected. Shunt resistors are used to measure the motor phase current. The gates of the IGBT switches are controlled using isolated gate driver UCC23513.

An NTC integrated inside the IGBT module is used to measure the module temperature. A resistor divider is formed using R10 and the NTC. The voltage drop measured across the NTC is proportional to IGBT module temperature.

2.3.2 DC Bus Voltage Sensing

The TIDA-010025 design is designed to operate from a DC bus voltage of up to 800-Vdc maximum which covers most of the low-voltage drives with grid voltage input up to 480 VAC. A 2- μ F, 1.1-kV film capacitor is placed close to the IGBT module DC bus inputs. This capacitor minimizes the loop area for the high-frequency switching currents. This helps minimize switch node overshoots and high frequency ringing, which in turn help reduce EMI.

Figure 5. DC Link Voltage Sensing



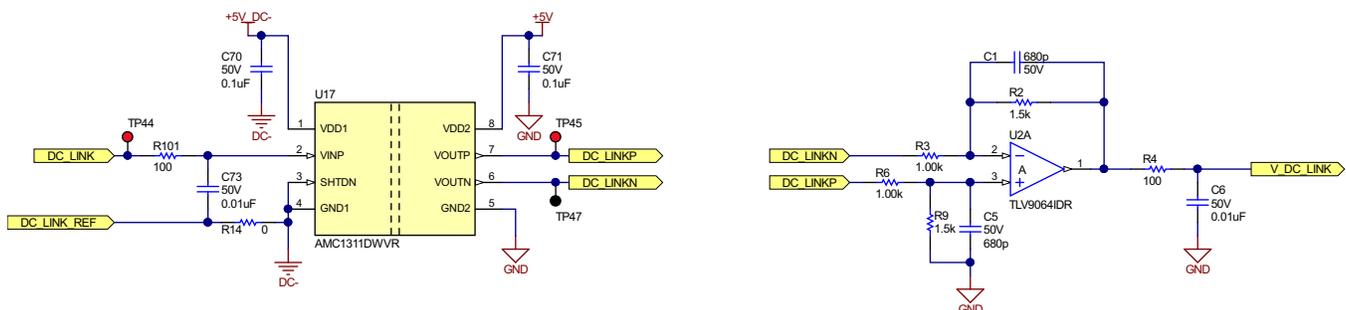
The DC bus voltage feedback is necessary for over and under voltage protection as well as for regulating the PWM duty cycles to maintain a constant RMS voltage to the motor. A voltage divider comprising of resistors R2, R5, R7, R8, R9 and R12 is used to down convert the DC bus voltage to the input voltage range of the isolated amplifier. This reference design uses the AMC1311DWV which has a linear input voltage range of -0.1 to 2 V. The scaling factor of the divider is calculated in Equation 1:

$$\text{Scaling factor} = \frac{R12}{(R12 + R2 + R5 + R7 + R8 + R9)} = 0.002484 \text{ V/V} \quad (1)$$

The 0 to 2-V input to the AMC1311 corresponds to 0 to 800 V with a scaling factor of 0.002484 V/V. Each resistor in the divider network is rated for 200 V and will be derated by 20% in case of the maximum DC bus voltage of 800 V. The maximum power dissipated across each resistor is 0.128 W when DC bus voltage is 800 V. Each resistor is rated for 0.25 W.

Figure 6 shows the AMC1311 circuit used for sensing the scaled voltage across the resistor divider network. R101 and C73 form the input filter. The secondary side is powered using a 5-V supply referenced to DC-. C70 is the secondary side supply noise decoupling capacitor. C71 is used for power supply noise decoupling on the primary side 5-V supply which is referenced to GND. The AMC 1311 has a gain of 1 and a differential output stage. 0 to 2-V input is converted into ±1-V signals around 1.44-V common mode on the output.

Figure 6. DC Bus Voltage Sensing Using AMC1311



2.3.3 Isolated IGBT Gate Driver

The TIDA-010025 inverter requires 7 isolated gate drivers for IGBT switch control. Six drivers are used for controlling the IGBT inverter switches and the seventh driver is used for controlling the brake chopper IGBT. The isolated gate driver used in this design is the UCC23513. This driver has an opto-LED emulated ediode input stage and is current controlled. The gate driver is designed to be pin to pin compatible to existing opto-isolated gate drivers and is available in wide body stretched SO6 package.

2.3.3.1 Gate Driver Input Stage

The gate driver input low to high threshold is 4 mA(max) and high to low threshold is 0.8 V(min). It is recommended that the input diode ON forward current be from 7 to 16 mA. In this design, the ON forward current is designed to be approximately 10 mA.

The output of an inverter control MCU is 3.3-V PWM signal. This has to be converted into a 10-mA current signal. Multiple circuit configurations can be implemented for this conversion. TIDA-010025 has provisions on board to evaluate each of the input drive methods. The design is tested with each configuration to show that UCC23513 can be used as pin to pin replacement for opto-isolated gate drivers.

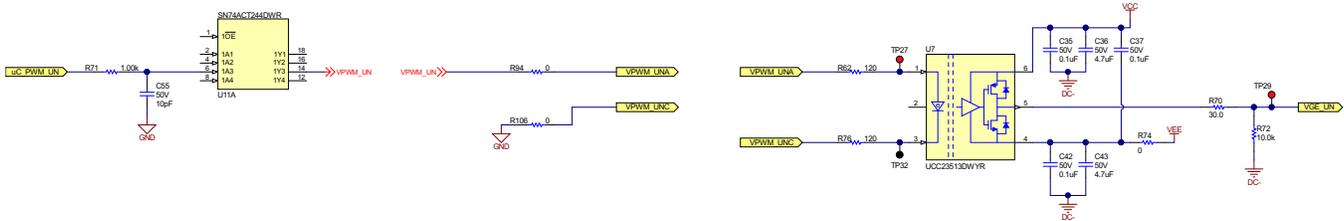
The different input drive circuit configurations implemented on TIDA-010025 are:

- Buffer drives anode of UCC23513
- Buffer drives cathode of UCC23513
- Buffer used to interlock high-side and low-side gate drivers
- MCU drives an NMOS FET in series with UCC23513 input
- MCU drives an NPN BJT which is in parallel with UCC23513 input

2.3.3.1.1 UCC23513 Buffer-Drives Anode

In this configuration SN74ACT244 buffer is used to drive the anode of the ediode while the cathode is grounded. The buffer used has a recommended output drive capability of ±24 mA. ACT logic family buffers have inputs which are compatible with 3.3-V TTL signals while being powered by 5-V supply. This ensures that the buffer can drive 5-V output signals while being controlled by 3.3-V MCU logic.

Figure 7. Buffer-Drives Anode



The input to the buffer is filtered by RC filter comprising R71 and C55. The output of the buffer is connected to ediode anode through resistor R62. The cathode is connected to GND through resistor R76. The resistor values are calculated using Equation 2:

$$R62 + R76 = \frac{(V_{buff} - V_f)}{I_{fon}} = \frac{(4.6 - 2.2)}{10mA} = 240\Omega$$

where

- V_{buff} is the buffer output high voltage at 10 mA taken from the data sheet
- V_f is the maximum input forward voltage of ediode
- I_{fon} is the ediode forward current

(2)

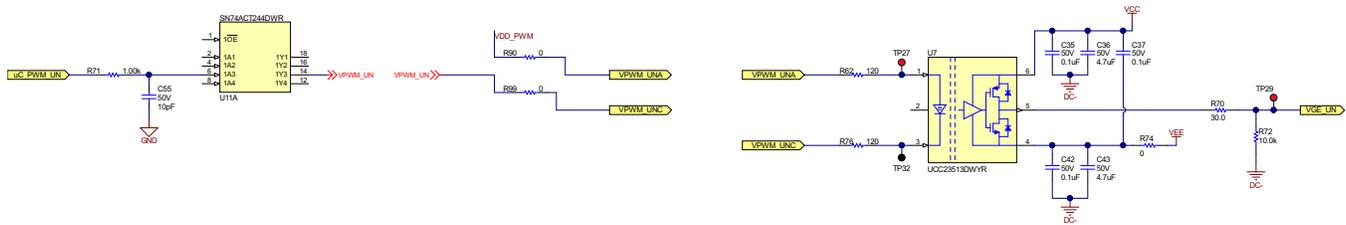
R62 and R76 are selected to be 120 Ω each.

In case 5-V buffer supply is not available or the buffer active low enable pin is pulled high the outputs of the buffer get tri-stated. In this state no current is driven through the ediode and the gate driver outputs are held low.

2.3.3.1.2 UCC23513 Buffer-Drives Cathode

In this configuration SN74ACT244 buffer is used to drive the cathode of the ediode through resistor R76 and the anode is pulled to 5 V through R62. If PWM signal is high the buffer drives the cathode to 5 V, which reduces the voltage across the ediode to < 0.8 V driving the output of the gate driver low. If PWM signal is low the buffer pulls the cathode to ground, which drives a current through the ediode turning on the output of the gate driver. Thus in this configuration the PWM signals are inverted. If inversion is not acceptable an inverting buffer like SN74ACT240 which is pin to pin compatible to the SN74ACT244 can be used.

Figure 8. Buffer-Drives Cathode



Resistors R62 and R76 are calculated using Equation 3:

$$R62 + R76 = \frac{(V_{supply} - V_f - V_{buff})}{I_{fon}} = \frac{(5 - 2.2 - 0.25)}{10mA} = 255\Omega$$

where

- V_{buff} is the buffer low output voltage at 10 mA taken from the data sheet
- V_f is the maximum input forward voltage of ediode
- I_{fon} is the ediode forward current

(3)

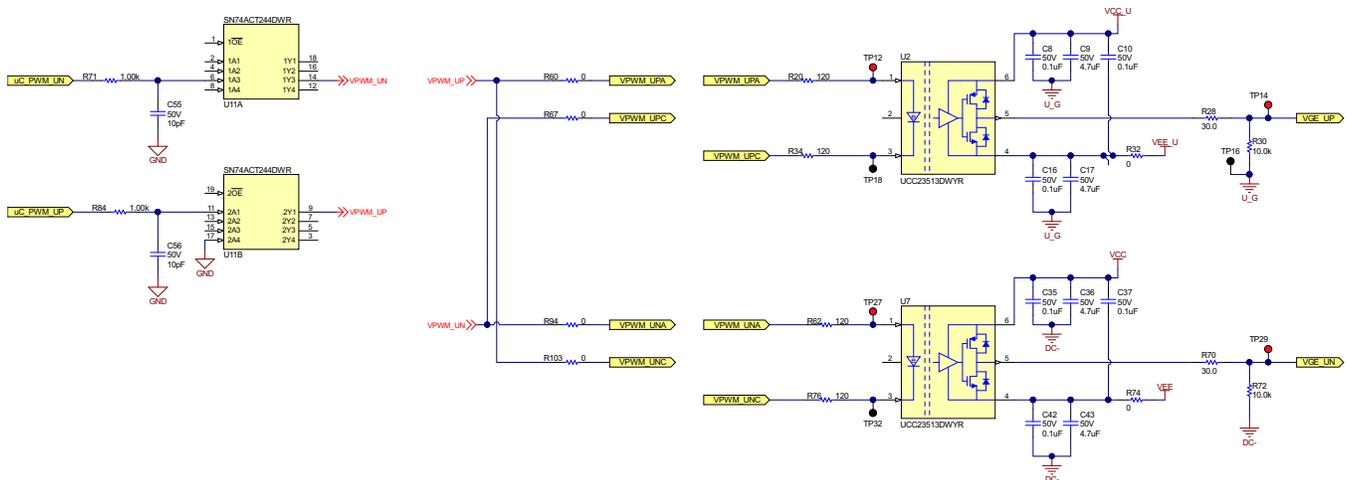
R62 and R76 are selected to be 120 Ω each

In case 5-V buffer supply is not available or the buffer active low enable pin is pulled high the outputs of the buffer get tri-stated. In this state no current is driven through the ediode and the gate driver outputs are held low.

2.3.3.1.3 Buffer Used to Interlock High-Side and Low-Side Gate Drivers

In this configuration SN74ACT244 buffer high side PWM signal is used to drive the anode of the high side gate driver ediode through resistor R20 and the cathode of the low side gate driver ediode through R76. The buffer low side PWM signal is used to drive the cathode of the high side gate driver ediode through resistor R34 and the anode of the low side gate driver ediode through R62.

Figure 9. Buffer Used to Interlock High-Side and Low-Side Gate Drivers



The output of the gate drivers follow Table 2:

Table 2. PWM Logic Table for Interlocking

CASE	HIGH-SIDE PWM INPUT	LOW-SIDE PWM INPUT	HIGH-SIDE PWM OUTPUT	LOW-SIDE PWM OUTPUT
1	High	High	Low	Low
2	High	Low	High	Low
3	Low	High	Low	High
4	Low	Low	Low	Low
5	Tri state	Tri state	Low	Low

The high-side and low-side PWM signals are complementary during normal operation and thus cases 2 and 3 from Table 2 occur. During the dead time period (case 4) both the PWM signals are low. No current flows through either of the ediode's and the gate driver outputs are low. In case 5-V buffer supply is not available or the buffer active low enable pin is pulled high the outputs of the buffer get tri-stated (case 5). In this state no current flows through the ediodes and the gate driver outputs are low. Sometimes due to MCU malfunction, motor control software bug or noise there is a possibility that both the PWM signals turn on (case 1). In this state both the anode and cathode of gate drivers are driven high and no current flows through the diodes. Both the gate drivers are turned off.

Resistors R62 and R76 are calculated using Equation 4:

$$R62 + R76 = \frac{(V_{buff_{on}} - V_f - V_{buff_{off}})}{I_{fon}} = \frac{(4.6 - 2.2 - 0.25)}{10mA} = 215\Omega$$

where

- $V_{buff_{on}}$ is the buffer high output voltage at 10 mA taken from the data sheet
- $V_{buff_{off}}$ is the buffer low output voltage at 10 mA taken from the data sheet
- V_f is the maximum input forward voltage of ediode
- I_{fon} is the ediode forward current

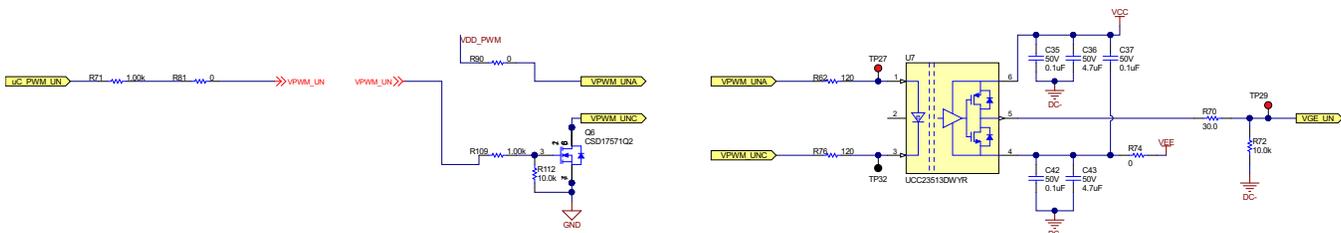
(4)

In this design R62 and R76 are selected to be 120 Ω each. Gate current will still be higher than 7 mA.

2.3.3.1.4 MCU Drives NMOS FET in Series With Gate-Driver Input

A lower cost option is to use an NMOS FET in series with the ediode instead of using a buffer IC. The advantage is that a higher input drive voltage ($V_{dd} > 5V$) can be used but interlocking is not possible. The anode of the ediode is connected to V_{dd} supply through resistor R62 and the cathode is connected to ground through resistor R76 and FET Q6. If PWM signal from MCU is high the FET is turned on and current flows through ediode turning the gate driver output ON. If PWM signal is low the FET blocks current flow through the ediode and the gate driver turns off.

Figure 10. MCU Drives NMOS FET in Series With Gate-Driver Input



Resistors R62 and R76 are calculated using Equation 5:

$$R62 + R76 = \frac{(V_{supply} - V_f - V_{FETDS})}{I_{fon}} = \frac{(5 - 2.2)}{10mA} = 280\Omega$$

where

- V_{FETDS} is the voltage drop across the FET at 10 mA which is negligibly small
- V_f is the maximum input forward voltage of ediode
- I_{fon} is the ediode forward current

(5)

In this design R62 and R76 are selected as 120 Ω each. Gate current will still be lower than 16 mA

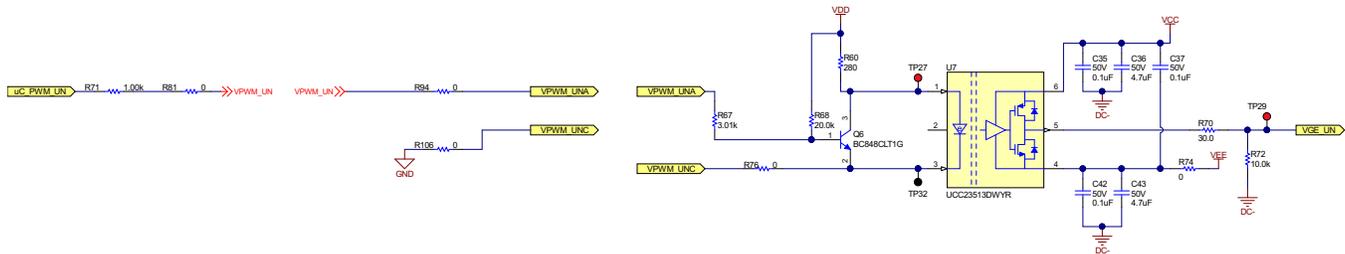
If the PWM input to the FET is floating due to fault conditions the resistor R112 pulls the gate of Q6 low turning off the FET.

2.3.3.1.5 MCU Drives NPN FET in Parallel With Gate-Driver Input

Another option is to use an NPN transistor in parallel with the ediode and drive the base of the NPN BJT directly from MCU. When PWM signal is high Q6 is turned on and the current flows through R60 and Q6. The voltage across the ediode is equal to V_{sat} of the NPN transistor. The gate driver output is pulled low. If the PWM signal is low Q6 is turned off, the current flows from VDD through R60 and the ediode, gate driver output is high.

The advantage of this configuration is that as the NPN is in parallel with the ediode and can be placed close to the gate driver input stage on the PCB, it strongly drives the ediode below 0.8 V when the BJT is saturated and is a high noise immunity circuit configuration. Also a higher input drive voltage (Vdd) can be used. The disadvantage is that a current will always be flowing either through the ediode or through the NPN BJT.

Figure 11. MCU Drives NPN FET in Parallel With Gate-Driver Input



Resistor R60 is calculated using Equation 6:

$$R60 = \frac{(V_{dd} - V_f)}{I_{fon}} = \frac{(5 - 2.2)}{10mA} = 280\Omega$$

where

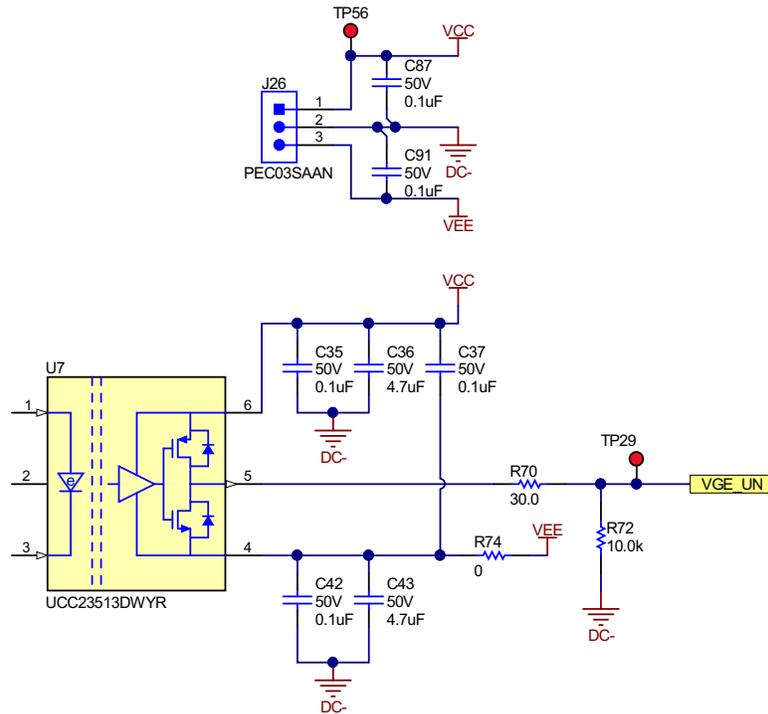
- Vdd is the supply voltage
- Vf is the maximum input forward voltage of ediode
- Ifon is the ediode forward current

(6)

Select R60 as 280 Ω.

2.3.3.2 Gate-Driver Supply

The UCC23513 input is current controlled and does not require any primary side power supply rail. In this design the secondary side is powered by a +15-V and -8-V rail which are referenced to the IGBT emitter. As Figure 12 shows the 15-V rail (VCC) is connected to the VCC pin and -8-V rail (VEE) is connected to the VEE pin of the gate driver. The total secondary voltage is 23 V which is used for biasing the gate driver internal circuit as well as to drive the IGBT gate. A 4.7-μF bulk capacitor C36 and C43 provides the IGBT gate currents and helps minimize the parasitic inductance due to gate current loops allowing for faster switching. 0.1-μF noise decoupling capacitors C35 and C42 are used to filter the power input.

Figure 12. Gate-Driver Power-Supply Rail


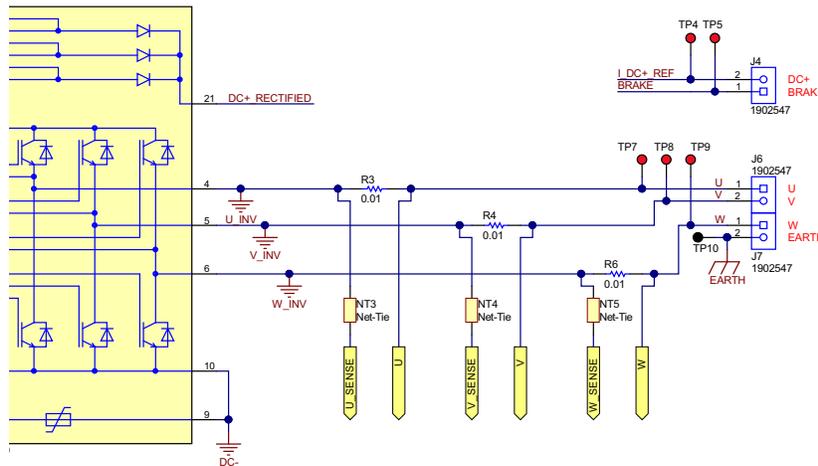
2.3.3.3 Gate Driver Output Stage

The UCC23513 has a single gate driver output for controlling the IGBT switching time. A gate resistor R70 equal to 30 Ω is selected as recommended in the IGBT module data sheet. This results in a maximum peak source and sink currents of 0.766 A at +15-V, -8-V rail. In case independent control of the IGBT switching ON and OFF is required components D9 and R64 can be mounted in parallel to R70. A 10-k Ω resistor R72 is connected between the IGBT gate to emitter pins close to the IGBT module. This is to ensure that the IGBT remains in the off state in case the gate driver gets disconnected from the IGBT due to faults.

2.3.4 Motor-Phase Current Sensing

Motor-phase current is sensed in all three phases using shunt resistors R3, R4 and R6. The voltage drop across the resistor is measured using an isolated amplifier. This reference design uses the ± 250 mV input voltage range of the AMC1300B device. The design can measure up to 25-Apk current. Shunt resistors are selected to be 10 m Ω and a 1%, 4-W rated resistor is selected.

Figure 13. Shunt Resistors for In-Phase Motor-Current Measurement



Value of shunt resistor = Input voltage range of U3 / Peak current value to be measured = 250 mV / 25 A = 10 mΩ

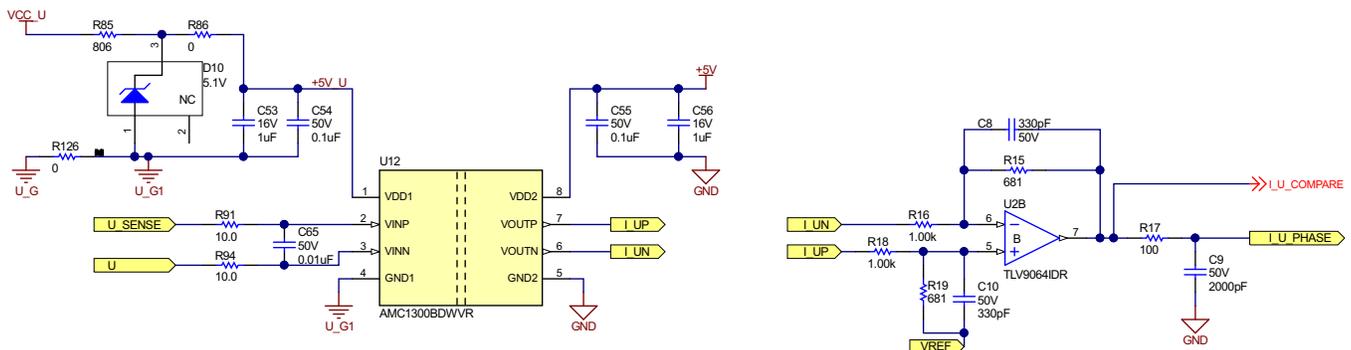
Inverter nominal current rating = 14 Arms

Nominal power dissipation = 14 × 14 × 10 m = 1.96 W

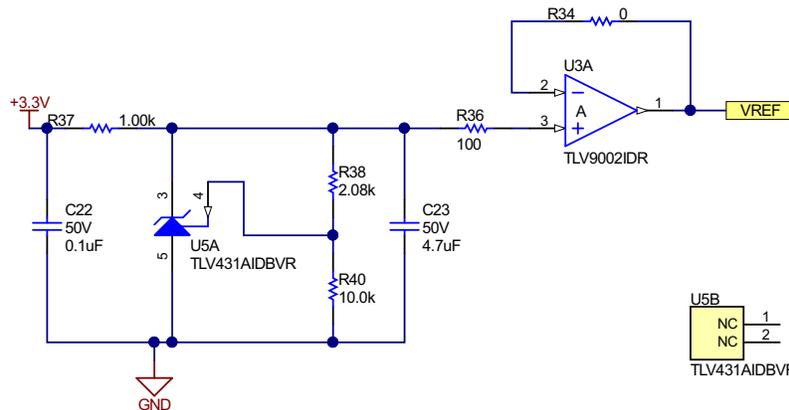
Figure 14 shows the circuit configuration for measuring current using the AMC1300B. R91, R94, and C65 form the input differential filter. This prevents high frequency noise on the input from getting aliased on the measured frequency range. The secondary side of the amplifier is powered from +5-V_U which is referenced to the inverter phase node U_{G1}. This supply is generated from the 15-V VCC_U isolated gate drive power supply using Zener diode. C54 is the supply noise decoupling capacitor.

The isolated amplifier has a gain of 8.2 and the output is a differential signal over a common mode of 1.44 V. ±250 mV is amplified to ±2.05. The input of the MCU ADC is single ended with a FS input range of 3 V. To measure the bipolar current signal the FS output of the isolated amplifier is mapped to the FS input of the ADC. A difference amplifier is implemented using TLV9064 with a gain of (3-0.2) / (2 × 2.05) = 0.6829. Note that a margin of 0.1 V is provided from the ground and 3V to ensure that the output is within the output voltage swing range of the op amp. The output of the amplifier is level shifted to 1.5-V for bidirectional current measurement. R17 and C9 form the ADC input RC filter.

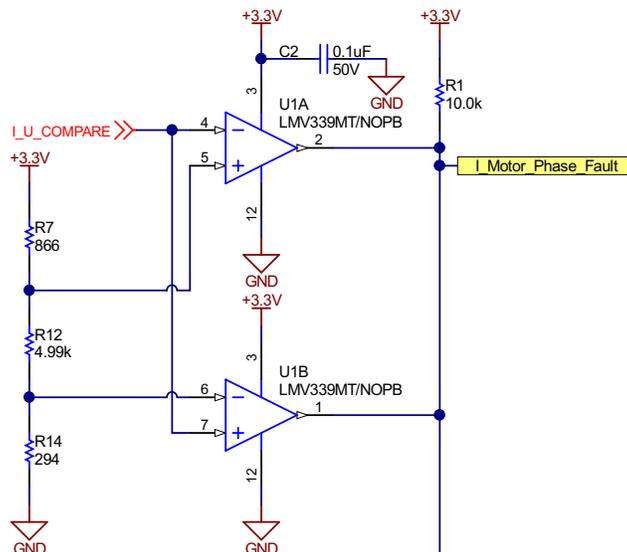
Figure 14. Motor-Phase Current Measurement



The 1.5-V reference for level shifting the op-amp output is generated using TLV431A and buffered using TLV9002.

Figure 15. 1.5-V Reference Generation


Overcurrent detection: A window comparator is implemented for overcurrent detection using LMV339. The overcurrent threshold is set to ± 24 Apk which corresponds to difference amplifier output of 2.84 V and 0.1597 V. These thresholds are set using resistors R7, R12, and R14. Note that the input to the window comparators is taken before the ADC antialiasing filter to reduce the response time to overcurrent faults. The output of the comparator is open drain, whenever fault occurs it is pulled low. The output of the comparator is connected to the active low enable pin of PWM drive buffer through logic blocks to ensure that the PWM buffer is tri-stated in case of overcurrent faults. Tri-stating the PWM buffers turns off the gate driver outputs.

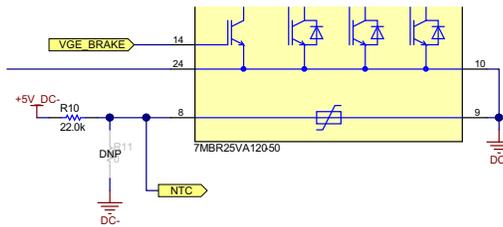
Figure 16. Overload Detect Comparator


2.3.5 IGBT Module Temperature Sensing

Temperature feedback of the IGBT power module is necessary for overtemperature shutdown as well as derating the output of the inverter at higher temperatures. Module temperature is measured using the NTC integrated inside the module.

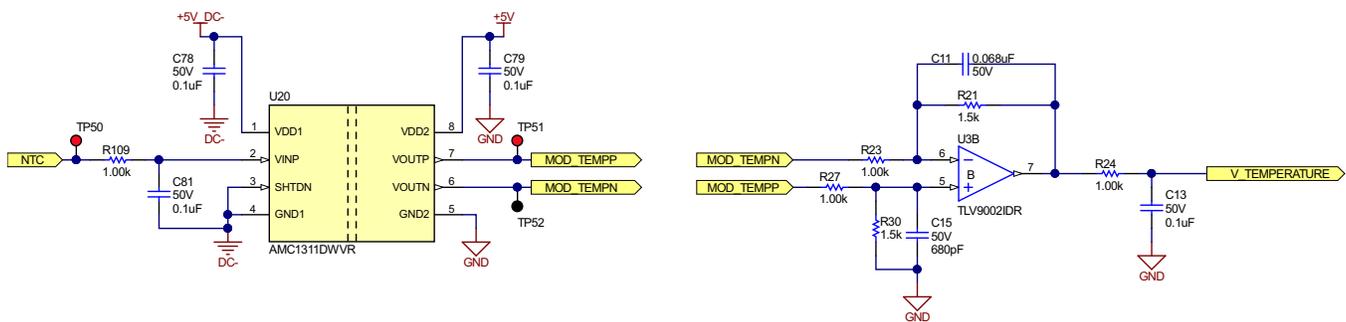
A resistor divider is formed using R10 and the NTC resistor as [Figure 17](#) shows.

Figure 17. Temperature Sensing Using IGBT Module Integrated NTC



The voltage across the NTC resistor is measured using isolated amplifier AMC1311. The NTC voltage is filtered using R109 and C81 before feeding in to the amplifier. The output is a differential signal over common mode of 1.44 V which is converted into single ended using difference amplifier TLV9002. A gain of 1.5 is used to map the 2-V FS range of AMC1311 to the 3V FS range of ADC MCU.

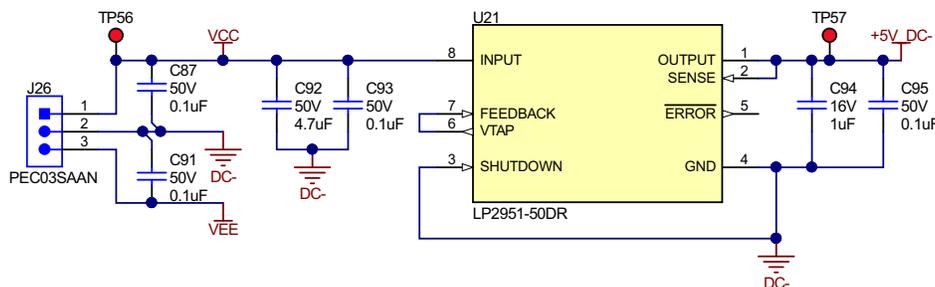
Figure 18. Isolated Amplifier for Temperature Measurement



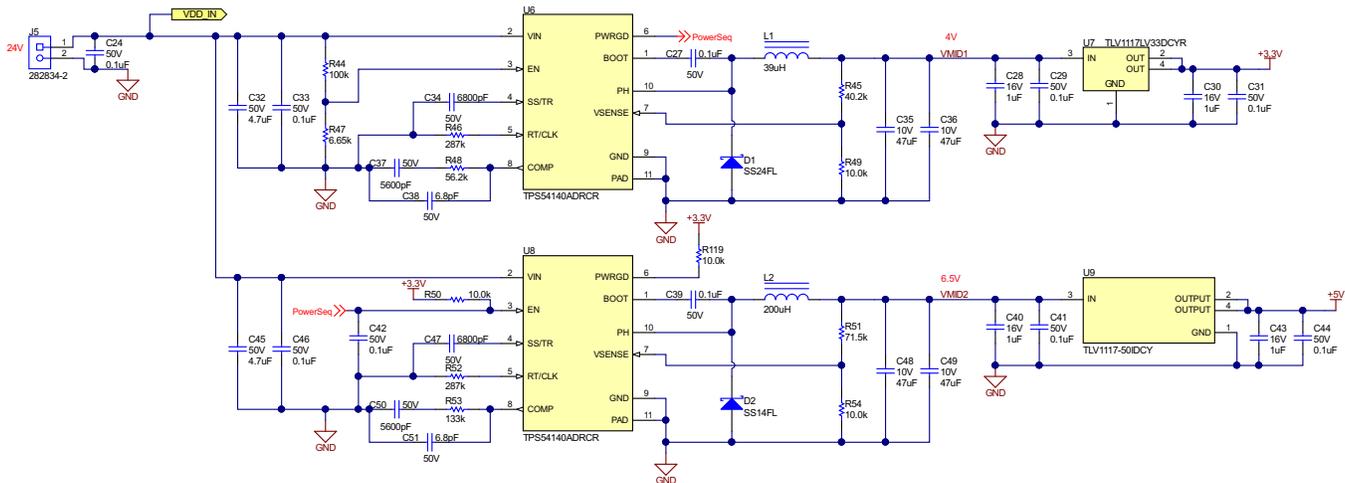
2.3.6 Power Supply

The AMC1311 isolated amplifiers used for DC link voltage and temperature sensing needs secondary side 5-V supply which is referenced to DC-. This is generated from the low side IGBT gate driver 15-V supply. The AMC1311 requires a secondary side power supply current of 9.7 mA maximum. LP2951 LDO is used to generate the 5-V supply as Figure 19 shows. C92 is the input bulk capacitor and C93 is the noise decoupling capacitor. The output voltage sense pin is directly connected to the output voltage and the internal resistor divider Vtap is connected to the feedback pin. The shutdown pin is connected to ground resulting in the LDO being always on.

Figure 19. Generation of 5-V Referenced to DC-



The control card requires a 3.3-V rail and a 5-V rail which are referenced to primary side ground. The 3.3-V rail is used to power the LaunchPad, analog signal conditioning circuit and the comparator circuit on the control card. The 5-V rail is used to power the PWM drive buffer and sent from the control card to the inverter power board where it is used to power the primary side of the isolated amplifiers.

Figure 20. Low-Voltage Side DC Power-Supply Rails Generation


Both these rails are generated using buck converter TPS54140A. The input to these devices is 24 V (VDD_IN) through connector J5. The enable pin of U6 is connected to VDD_IN through resistor divider network R44 and R47. The enable pin threshold is 1.25 V, this ensures that U6 starts functioning only if VDD_IN is greater than approximately 20 V. The feedback network of the converter R45 and R49 is set so that the output VMID1 is 4 V. This 4 V is fed to a downstream LDO TLV1117LV to generate 3.3-V rail. The power good pin of U6 is an open drain output which asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shutdown. In this design this pin is connected to the Enable pin of U8 to do power sequencing. Initially the power good pin will be low till the VSENSE pin is below 94% of the internal reference voltage. Once this is exceeded, the PWRGD pin de-asserts itself and the pull up resistor R50 enables device U8. U8 is designed to generate VMID2 which is 6.5 V. This feeds a downstream 5-V LDO TLV1117-50. The sequencing order on power up is 3.3 V and then 5-V rail. This ensures that the controller is powered up before any of the feedback circuits and PWM drive buffer. The soft start time can be set using C34 and C47 on the SS pin. This design uses 6800 pF which results in a soft start time of approximately 2 ms. The TI WEBENCH™ software is used to design the buck converter and select the components.

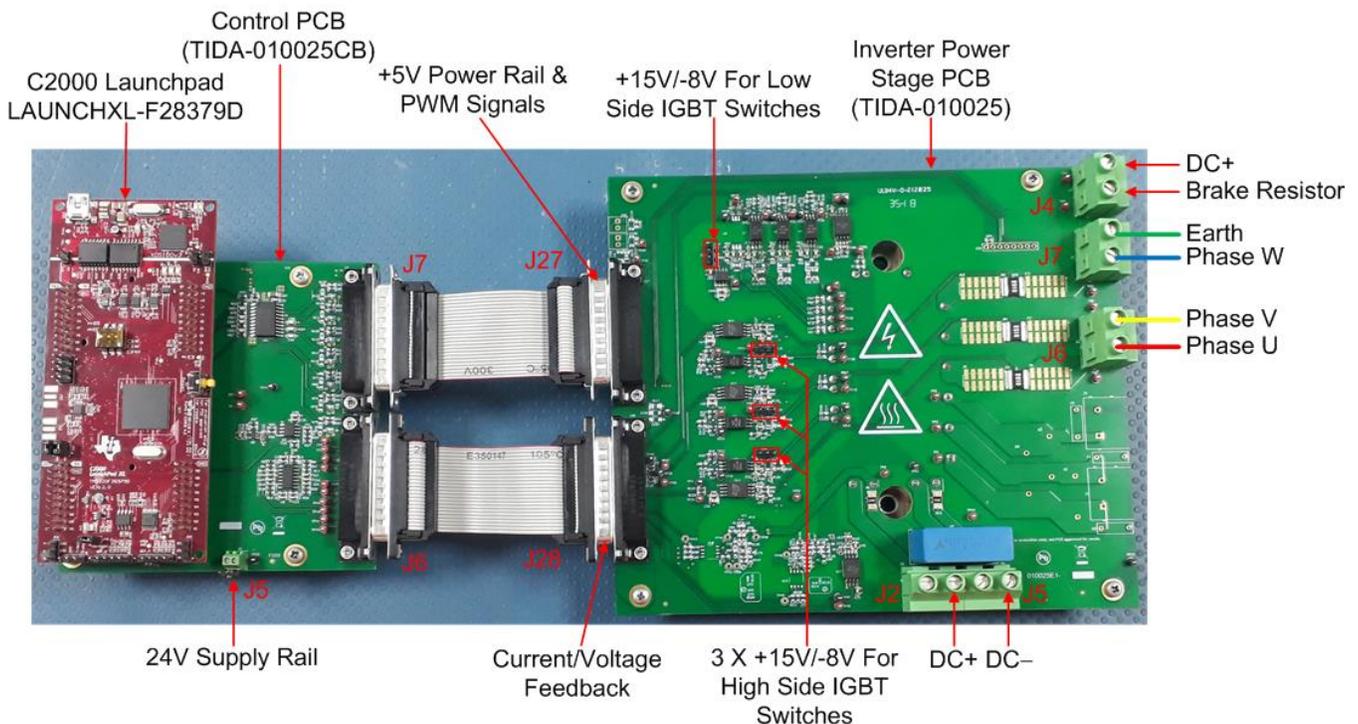
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 TIDA-010025 PCB Overview

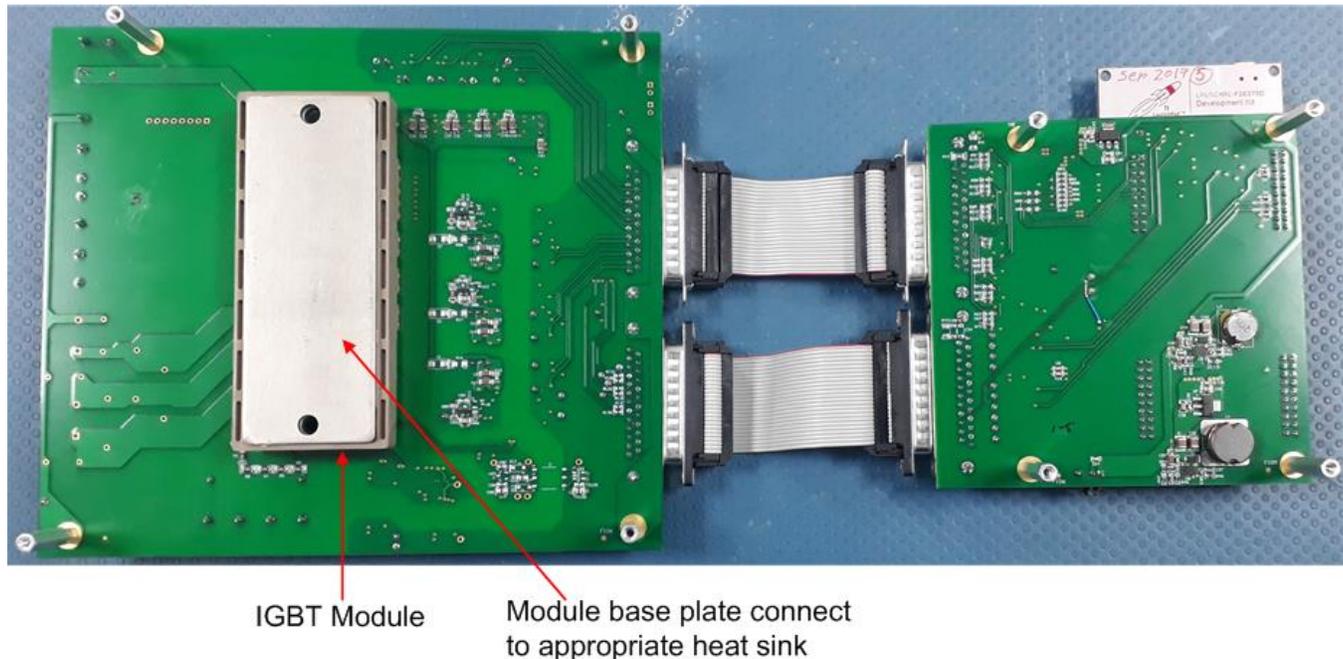
The TIDA-010025 design comprises of two PCB's. A control module (TIDA-010025CB) and an inverter power stage (TIDA-010025). Both the PCBs are interfaced through 25 pin D-subminiature connectors using ribbon cables. One cable is used between J7 on the control board and J27 on the inverter board to send 5-V power rail and PWM signals and the other cable is used between J28 on the inverter board and J6 on the control board to feedback motor phase current, DC link voltage and IGBT module temperature measurements. Motor is controlled using a C2000 LaunchPad mounted onto the control module. External 24-V supply is connected to J5 on the control board. The 3 motor phases are connected to J6 and J7. Provision is given to connect external brake resistor to J4. The DC link input to the inverter is through connectors J2 and J5.

Figure 21. TIDA-010025 Top View



An IGBT module with integrated rectifier, brake chopper and inverter is mounted on the bottom of the PCB. The base plate of the IGBT module needs to be connected to a heat sink using thermal compound. An appropriate heat sink needs to be selected based on the power dissipation in the application and cooling mechanism available.

Figure 22. TIDA-010025 Rear View



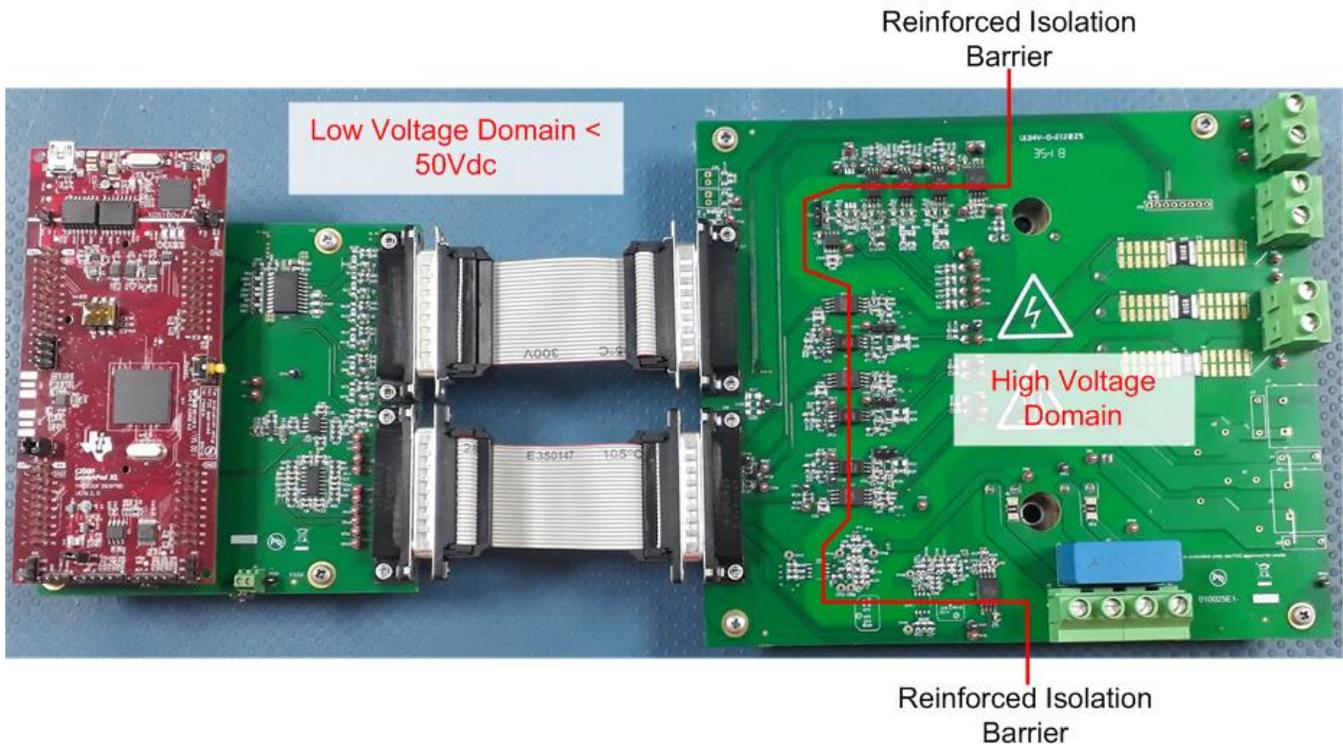
3.1.2 Safety Precautions During Testing

High-Voltage Warning: TIDA-010025 can work with a HV DC link input of up to 800 VDC. These HV sections can be exposed to human contact and extreme care needs to be exercised while testing and should be handled by a professional only. Electric shock is possible when connecting board to live wire. Therefore all exposed terminals (high voltage or otherwise) should not be handled directly when power is turned on – all connections should be done only in powered down state. For safety, use of isolated test equipment with overvoltage/overcurrent protection is recommended. The HV area on the PCB is shown in [Figure 24](#) and marked on the PCB with the symbol in [Figure 23](#).

Figure 23. High-Voltage Warning



Figure 24. High-Voltage Locations on PCB



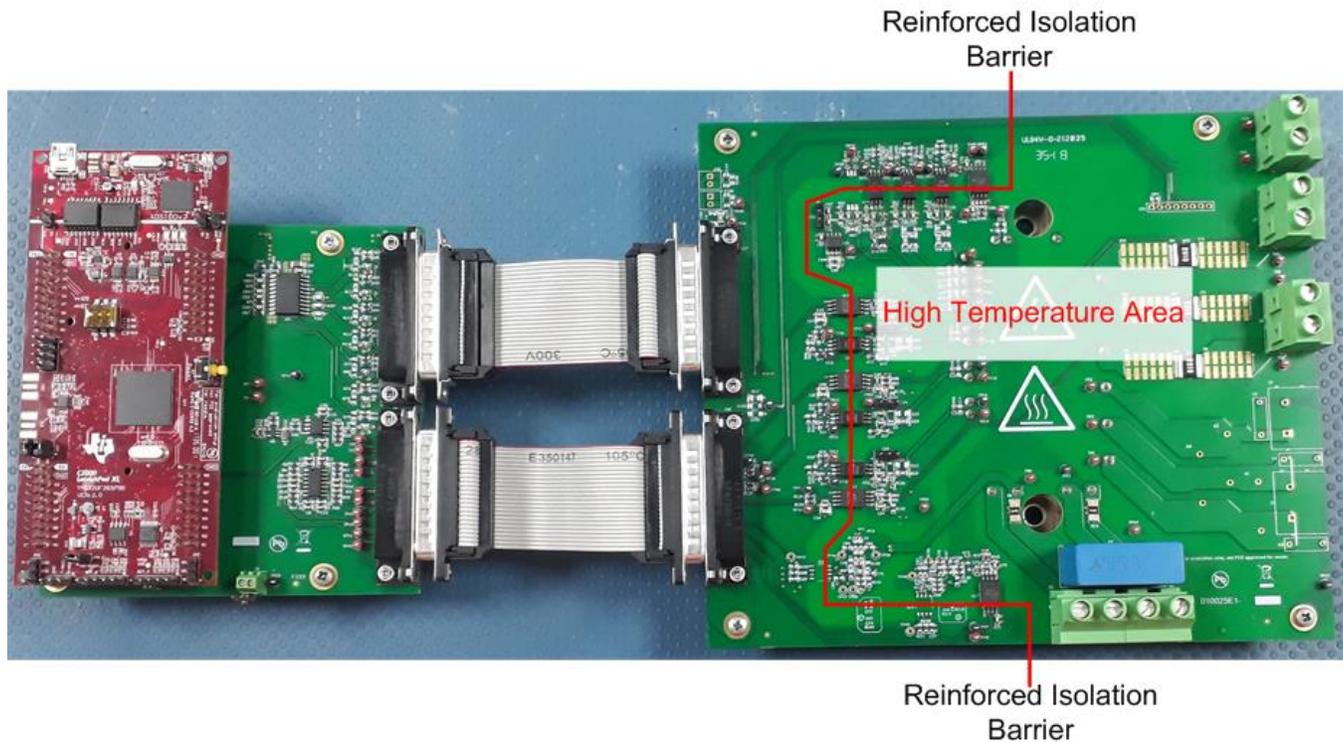
Never leave a powered board unattended. Please note that on inverter turn off the DC link capacitor can hold some residual charge. Ensure that the DC link capacitor is completely discharged before handling the board again.

The high- and low-voltage domains are separated by a reinforced isolation barrier as [Figure 24](#) shows. A minimum of 8-mm creepage and clearance is provided across the domains.

High-Temperature Warning: During operation especially at high ambient temperatures and when the inverter is fully loaded some components and parts of the PCB can reach high temperatures. Do not touch the PCB as contact may cause burns. On inverter turn off let the PCB cool down for some time before handling it again. [Figure 26](#) shows the high-temperature location on the PCB and marked on the PCB with the symbol in [Figure 25](#).

Figure 25. High-Temperature Warning



Figure 26. High-Temperature Locations on PCB


3.1.3 Controller Interface

TIDA-010025CB is interfaced with the LAUNCHXL-F28379D LaunchPad. The pin functions used are shown in [Table 3](#) through [Table 6](#).

Table 3. TIDA-010025CB J1 Interface to LaunchPad™ J1, J3

TIDA-010025 FUNCTION	LaunchPad™ FUNCTION USED	J1 PINS	J3 PINS	LaunchPad™ FUNCTION USED	TIDA-010025 FUNCTION
+3.3 V	3.3 V	1	21		
		2	22	GND	GND
		3	23	ADCIN14	V_DC_LINK
		4	24		
		5	25		
		6	26		
		7	27	ADCINC2	I_U_PHASE
		8	28	ADCINB2	I_V_PHASE
		9	29	ADCINA2	I_W_PHASE
		10	30		

Table 4. TIDA-010025CB J2 Interface to LaunchPad™ J4, J2

TIDA-010025 FUNCTION	LaunchPad™ FUNCTION USED	J4 PINS	J2 PINS	LaunchPad™ FUNCTION USED	TIDA-010025 FUNCTION
uC_PWM_UP	EPWM1A	40	20		GND
uC_PWM_UN	EPWM1B	39	19		
uC_PWM_VP	EPWM2A	38	18		
uC_PWM_VN	EPWM2B	37	17		
uC_PWM_WP	EPWM3A	36	16		
uC_PWM_WN	EPWM3B	35	15		
		34	14		
		33	13	GPIO124	OVERLOAD_FAULT
		32	12	GPIO125	Fault_Control
		31	11		

Table 5. TIDA-010025CB J3 Interface to LaunchPad™ J5, J7

TIDA-010025 FUNCTION	LaunchPad™ FUNCTION USED	J5 PINS	J7 PINS	LaunchPad™ FUNCTION USED	TIDA-010025 FUNCTION
+3.3 V	3.3 V	41	61		
		42	62	GND	GND
		43	63	ADCIN15	V_TEMPERATURE
		44	64		
		45	65		
		46	66		
		47	67		
		48	68		
		49	69		
		50	70		

Table 6. TIDA-010025CB J4 Interface to LaunchPad™ J8, J6

TIDA-010025 FUNCTION	LaunchPad™ FUNCTION USED	J8 PINS	J6 PINS	LaunchPad™ FUNCTION USED	TIDA-010025 FUNCTION
uC_PWM_BRAKE	EPWM4A	80	60	GND	GND
		79	59		
		78	58		
		77	57		
		76	56		
		75	55		
		74	54		
		73	53		
		72	52		
		71	51		

3.2 Testing and Results

The focus of the tests is to evaluate the functionality and performance of the UCC23513 gate drive subsystem for the three-phase inverter.

3.2.1 Test Setup

Figure 27 through Figure 29 show the test setup. Follow all the safety precautions mentioned in Section 3.1.2. The F28379D LaunchPad is mounted on the TIDA-010025 control module. The control module is then connected to the TIDA-010025 inverter power stage using ribbon cables. The motor is connected to the inverter terminal blocks and DC link connection is provided. Note that a current limited external DC supply has to be used. TIDA-00199 (TIDA-010026 can also be used) is used to generate the +15-V, -8-V isolated gate driver power rails. An external 24-V DC supply is used to power both the control card and the TIDA-00199. The controller is debugged through an USB cable. Basic isolated connection is provided on the LaunchPad.

Use the following power-up sequence, the power-down sequence is the inverse.

- 24-V control card power supply
- 24-V supply for TIDA-00199
- 565 Vdc (corresponds to 400-VAC grid voltage) supply to inverter

Figure 27. Test Setup

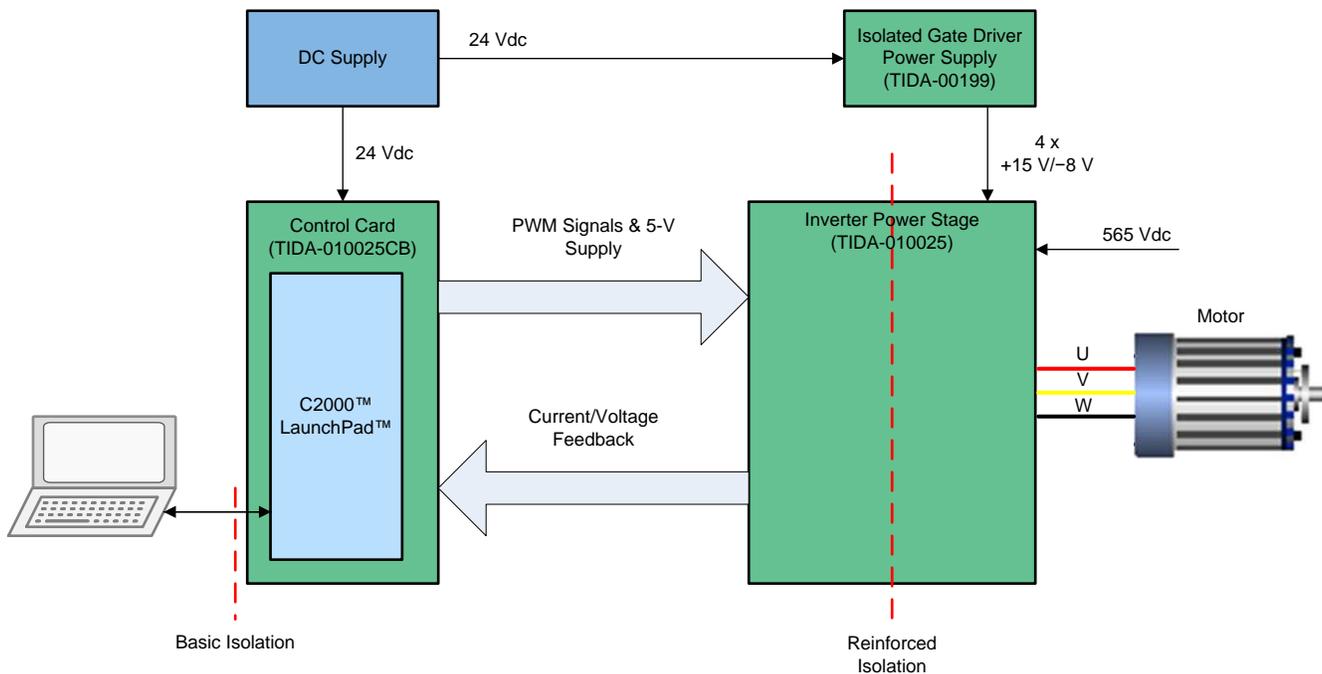


Figure 28. Lab Test Setup

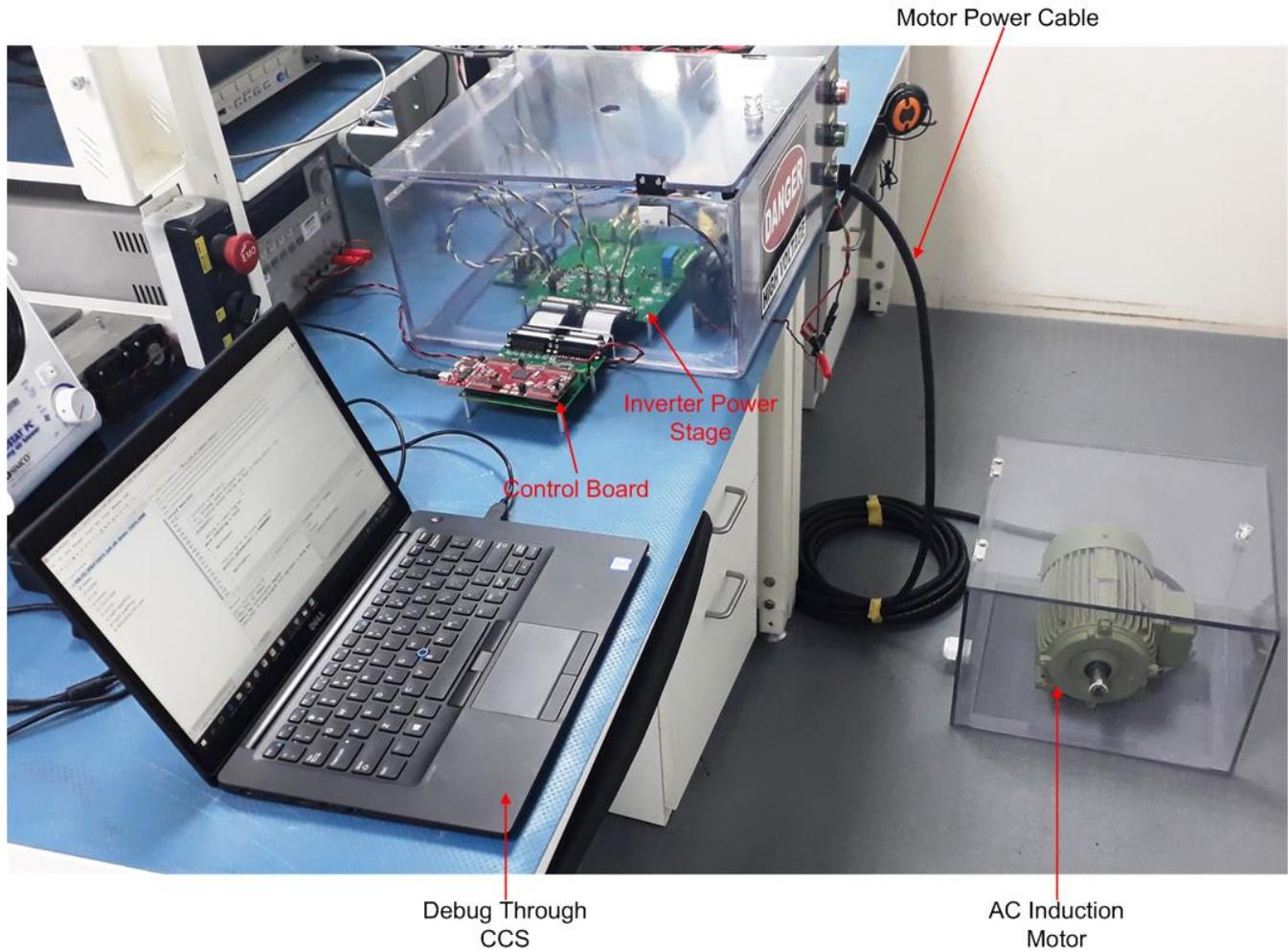
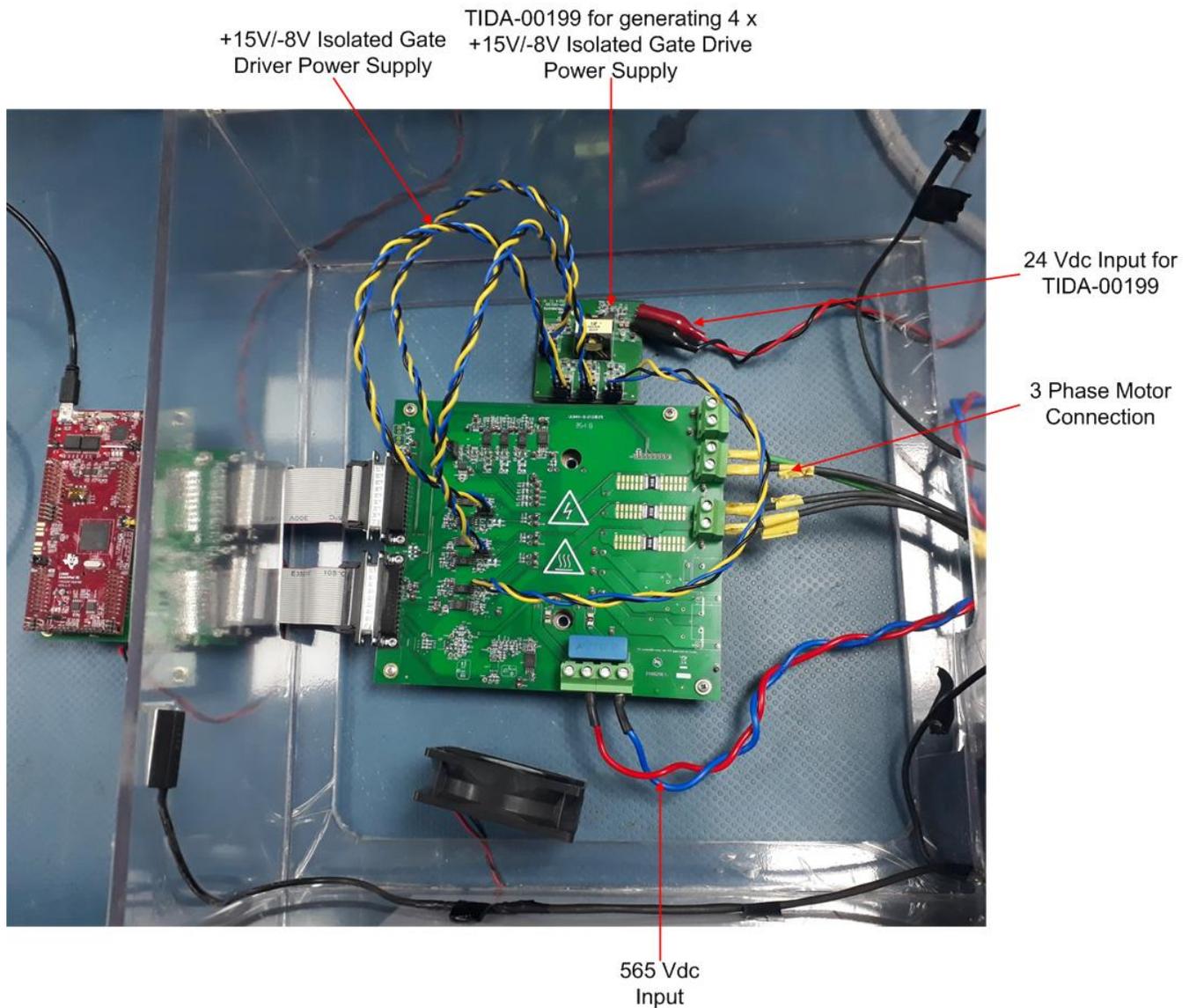


Figure 29. Lab Test Setup (Zoomed)


3.2.2 Test Results

3.2.2.1 Inverter Switch Node Waveforms

This section shows the inverter functional switching waveforms. Hard switching behavior of the inverter switch node is captured at a negative current (current flowing into phase node) of -2 A. Soft switching is captured at a positive current (current flowing out of phase node) of 2 A. For all waveforms a DC bus voltage of 565 Vdc is used.

Figure 30 to Figure 35 show the turn on and turn off behavior of the inverter switch node

- Channel 1: PWM output from MCU
- Channel 2: Voltage across ediode of U phase low side IGBT gate driver
- Channel 3: V_{ge} of U phase low side IGBT
- Channel 4: Inverter switch node for phase U referenced to DC-

Figure 30. Hard Switch Turn On

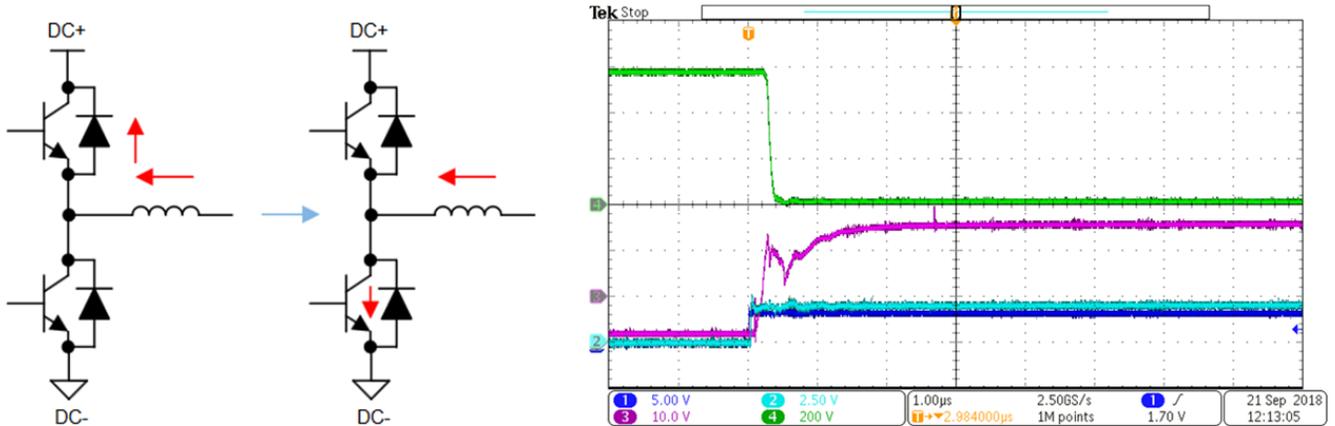


Figure 31. Hard Switch Turn Off

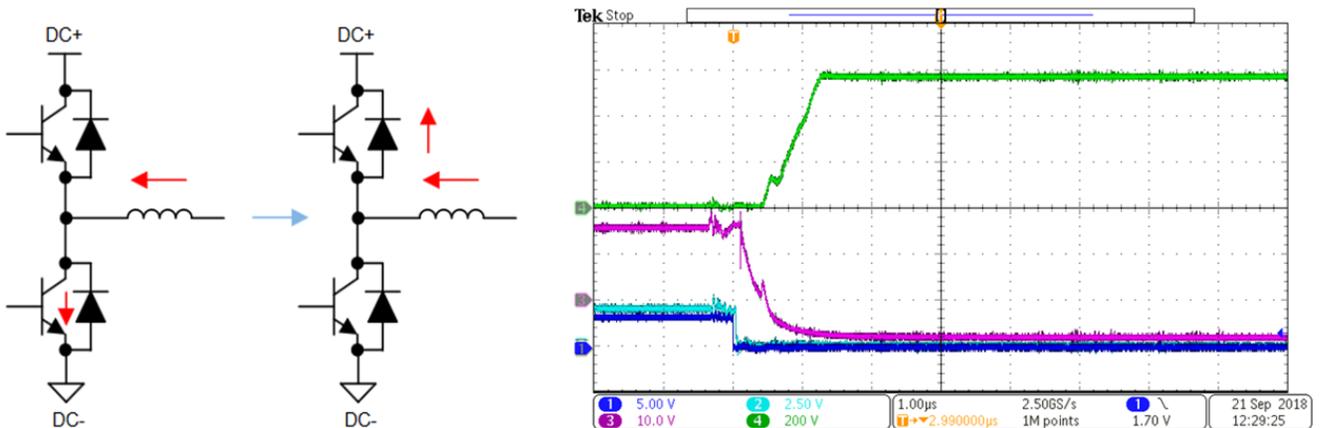


Figure 32. Soft Switch Turn On

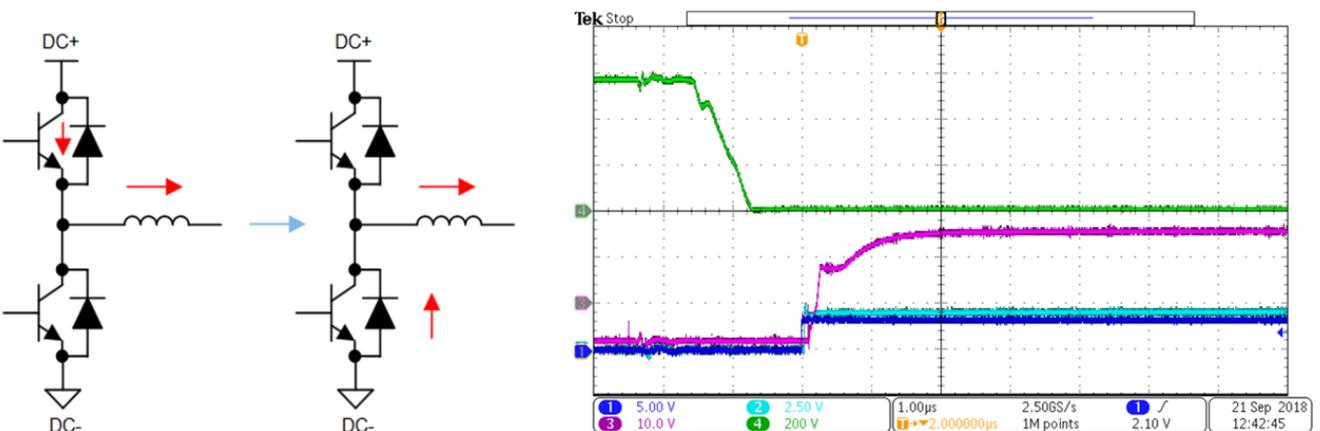


Figure 33. Soft Switch Turn Off

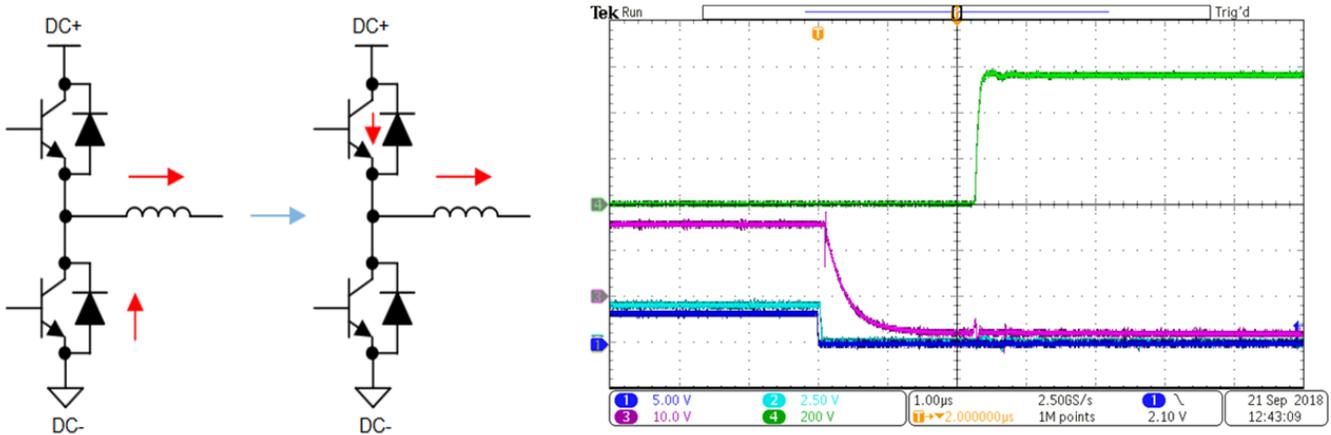


Figure 34 and Figure 35 show the turn on and turn off dv/dt of the inverter switch node captured at 2-A phase current at a DC link voltage of 565 V. Note that the turn off dv/dt depends on the phase current and the output capacitance C_{oss} of the IGBT. Higher the phase current faster the voltage builds up across the C_{oss} .

Figure 34. Turn On dv/dt

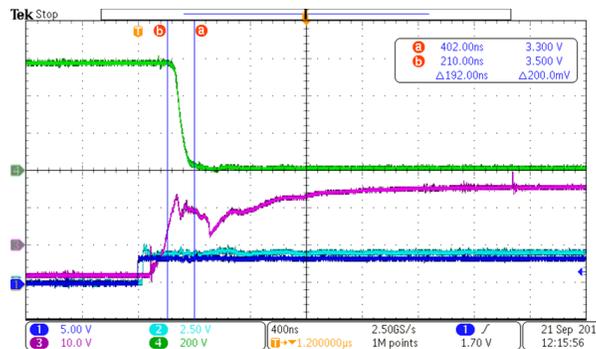
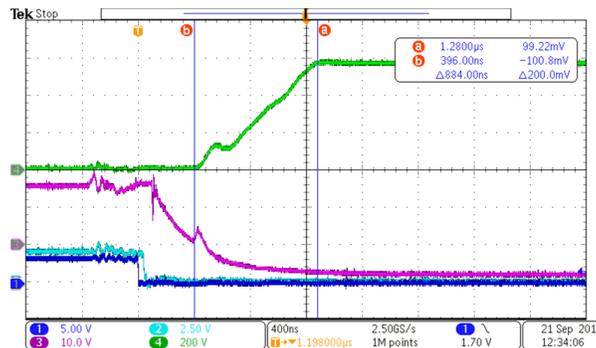


Figure 35. Turn Off dv/dt



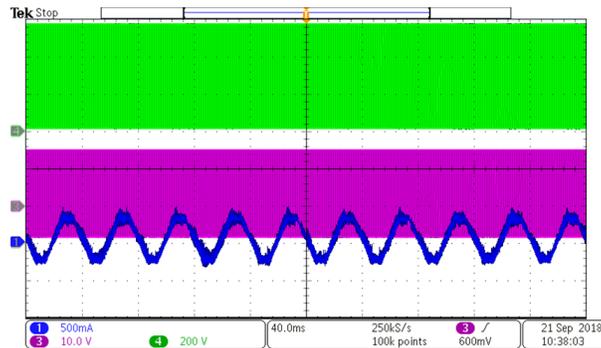
3.2.2.2 Motor-Current Waveform When Running Open Loop

Note that open loop testing is done to characterize the inverter. Motor shaft is not loaded and the inverter driven without the current control loop. The phase U current is captured.

- Channel 1: Phase U motor current
- Channel 3: V_{ge} of U phase low side IGBT

- Channel 4: Inverter switch node for phase U referenced to DC–

Figure 36. Motor-Current Waveform



3.2.2.3 Gate-Current Waveform

This section captures the source and sink gate current waveforms. The source current is measured to be approximately 0.66 Apk and the sink current is approximately 0.8 Apk

Figure 37 to Figure 40 show the turn on and turn off behavior of the inverter switch node

- Channel 1: PWM output from MCU
- Channel 2: Gate current (Note: The channel 2 waveform is measured across the gate resistor and therefore shown in volts. To convert from voltage to current divide the scale by 30)
- Channel 3: Vge of U phase low side IGBT
- Channel 4: Inverter switch node for phase U referenced to DC–

Figure 37. Gate-Source Current With DC Link 0 V

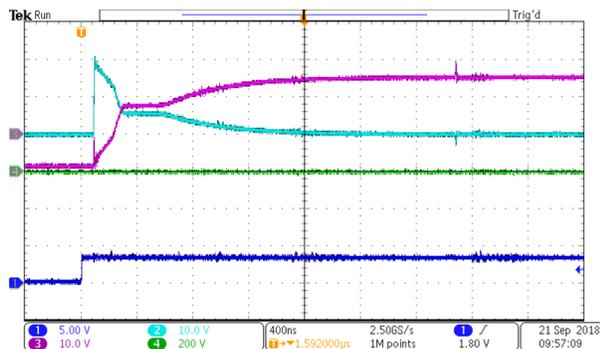


Figure 38. Gate-Sink Current With DC Link 0 V

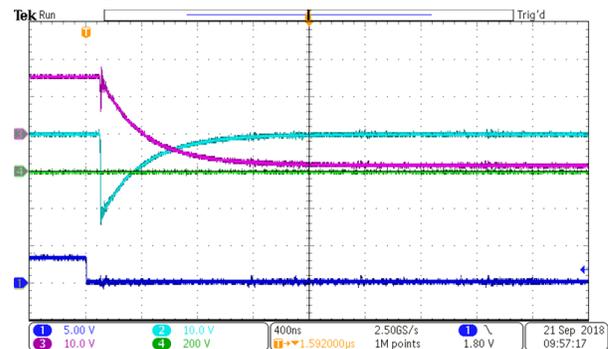


Figure 39. Gate-Source Current With DC Link Powered With 565 V

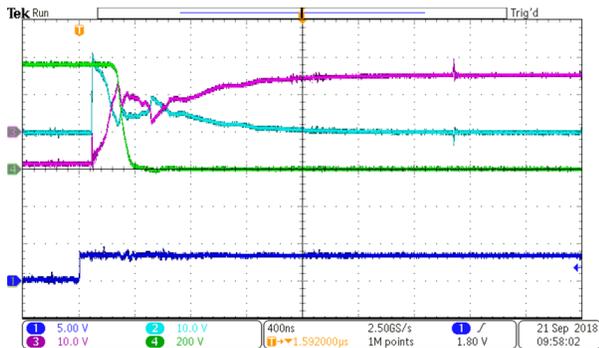
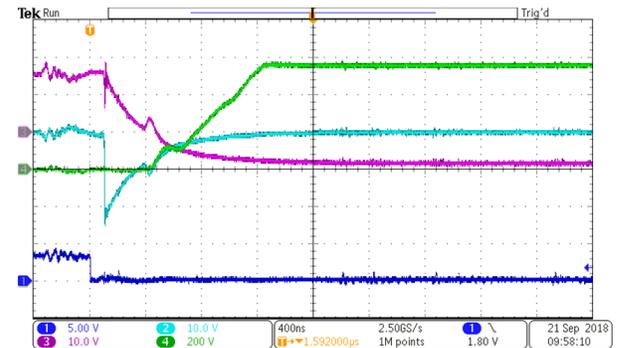


Figure 40. Gate-Sink Current With DC Link Powered With 565 V



3.2.2.4 Measured Pulse-Width Distortion

Pulse width distortion is the difference in input to output PWM pulse width of the gate driver. In this design it is measured to be approximately 20 ns.

- Channel 1: PWM output from MCU
- Channel 2: PWM output from gate driver
- Channel 3: V_{ge} of U phase low side IGBT

Figure 41. Input PWM Pulse Width

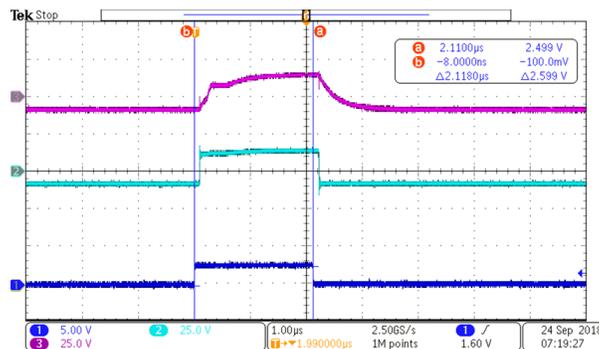
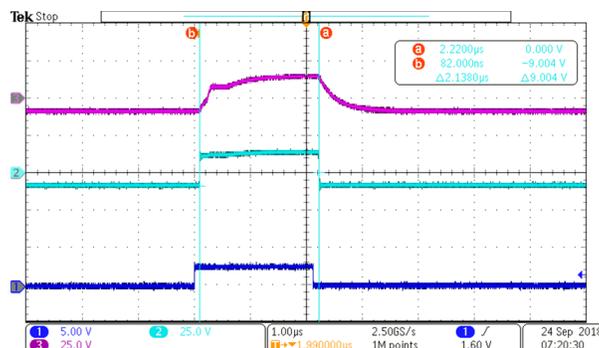


Figure 42. Output PWM Pulse Width



3.2.2.5 Minimum Pulse Rejection

Minimum pulse width rejection parameter helps in deciding the minimum PWM which can be applied by the MCU to the inverter.

- Channel 1: PWM output from MCU

- Channel 2: PWM output from gate driver
- Channel 3: Vge of U phase low side IGBT

Figure 43 shows the PWM input which is passed by the gate driver to the output. If the input PWM width is reduced further as Figure 44 shows, the pulse is rejected by the gate drive. Figure 45 shows that the input PWM should be approximately 1.5 μ s for the IGBT gate to emitter voltage to reach its final value for this TI design. This time is proportional to the RC time constant of the gate circuit.

Figure 43. Pulse Width Passed by Gate Driver

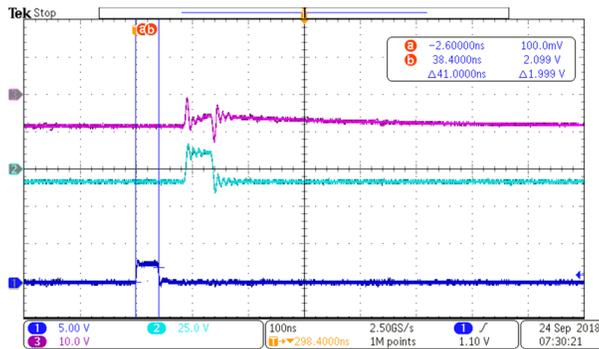


Figure 44. Pulse Width Rejected

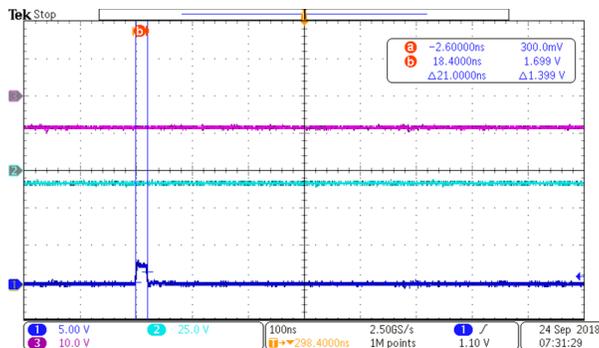
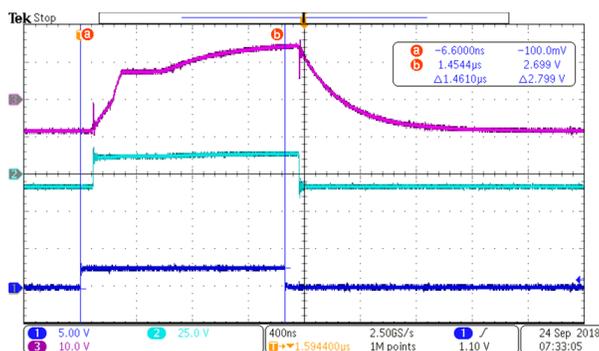


Figure 45. Minimum Pulse Width at Gate of IGBT



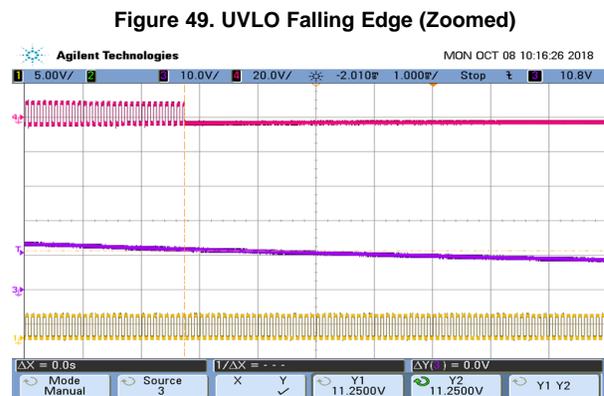
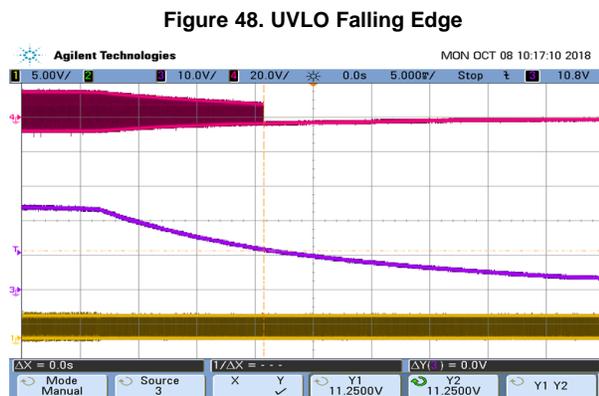
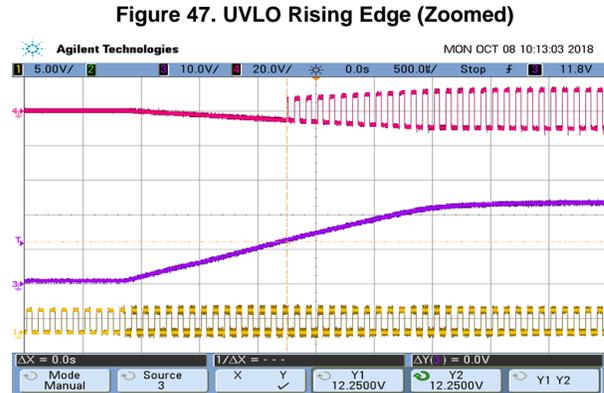
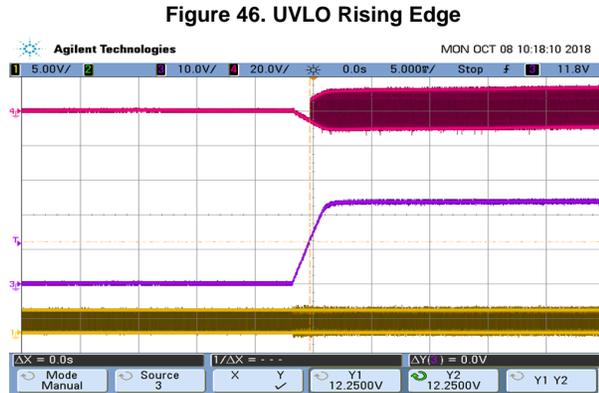
3.2.2.6 UVLO of Gate Driver

The UVLO function is implemented between the V_{CC} and Vee pins of the gate driver to prevent an underdriven condition on the IGBT. When V_{CC} is lower than $UVLO_R$ at device start-up or lower than $UVLO_F$ after start-up, the voltage supply UVLO feature holds the effected output low, regardless of the input forward current.

- Channel 1: PWM output from MCU

- Channel 2: Gate driver power supply (Vcc-Vee) for U phase low side IGBT
- Channel 3: Vge of U phase low side IGBT

Figure 46 shows the measured rising edge UVLO at 12.25 V and Figure 48 shows the falling edge UVLO at 11.25 V.



3.2.2.7 Interlocking High Side and Low Side Gate Drivers

TIDA-010025 board has provision to interlock the high side and low side gate drivers as shown in Section 2.3.3.1.3. The components required to be populated and unpopulated to test this configuration are shown in schematic.

For testing interlocking a fault is purposely inserted into the PWM signals so that there is overlap between the high-side and low-side PWM signals from the MCU. Figure 50 and Figure 51 show that whenever both PWM signals are high, then the output PWM signals of the gate driver are low.

- Channel 1: Low-side IGBT PWM signal from MCU
- Channel 2: High-side IGBT PWM signal from MCU
- Channel 3: Vge of low-side IGBT
- Channel 4: Vge of high-side IGBT

Figure 50. Interlocking of High-Side and Low-Side Gate Drivers

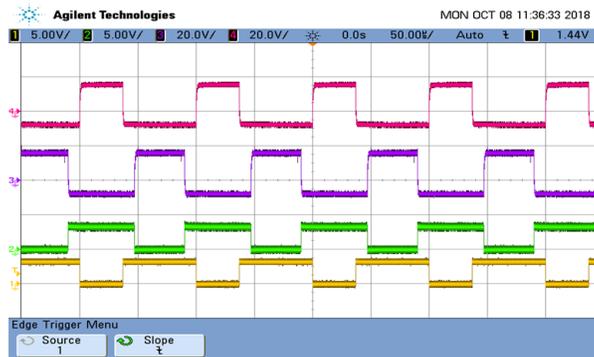
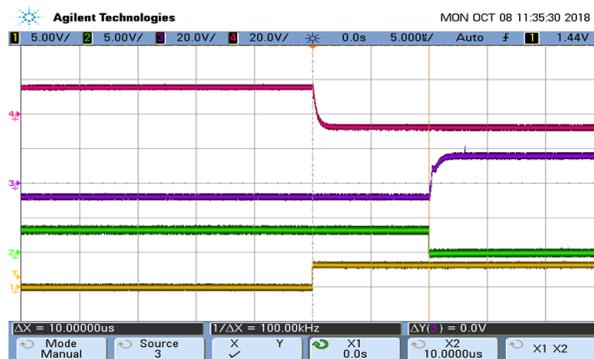


Figure 51. Interlocking of High-Side and Low-Side Gate Drivers (Zoomed)



4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-010025](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-010025](#).

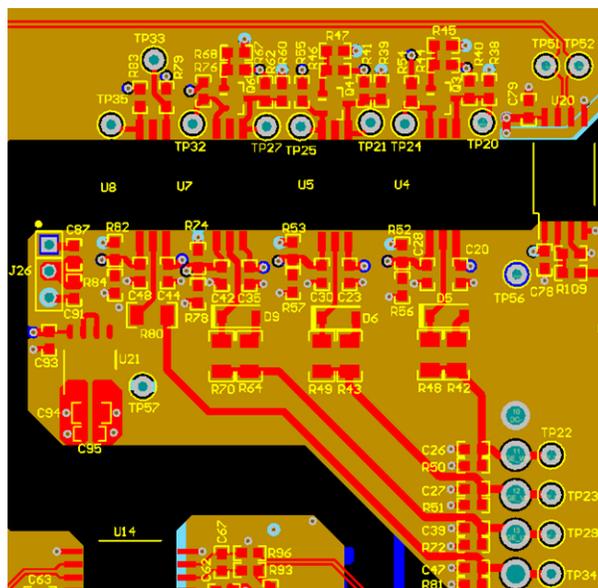
4.3 PCB Layout Recommendations

4.3.1 UCC23513

The layout guideline is provided for device U7. Similar guidelines apply to all other gate drivers.

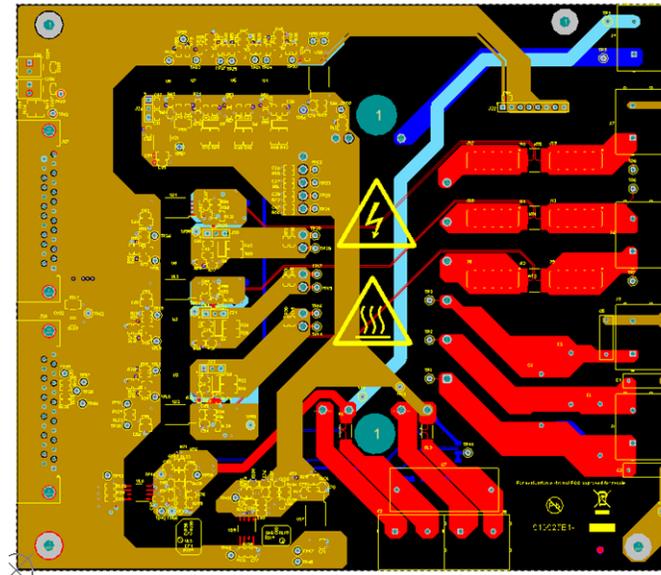
- Place gate drive supply bypass capacitors C42, C35 close to the device power supply pins
- The IGBT gate turn on and turn off loop areas should be kept to a minimum. Gate tracks are made wide to reduce parasitic track inductances.
- R62 and R76 are ediode current limit resistors should be kept close to the device

Figure 52. UCC23513 Layout



4.3.2 Creepage and Clearance Between High-Voltage Nets

Note that the controller side and the inverter side are reinforced isolated from each other. Plane to plane creepage and clearance is kept to a minimum of 8 mm across the isolation barrier. Reinforced isolated devices UCC23513, AMC1300B, AMC1311 are placed across the isolation barrier for interfacing signals across the high voltage and low voltage side.

Figure 53. Creepage and Clearance Spacing


4.3.3 Layout Prints

To download the layer plots, see the design files at [TIDA-010025](#).

4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-010025](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-010025](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-010025](#).

5 Related Documentation

1. Texas Instruments, Wide-Input Isolated IGBT Gate-Drive Fly-Buck Power Supply for Three-Phase Inverters, [TIDA-00199](#)
2. Texas Instruments, Isolated IGBT Gate-Drive Power Supply Reference Design with Integrated Switch PSR Flyback Controller, [TIDA-010006](#)

5.1 Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2018) to A Revision	Page
• Changed 1414 Vpk to 1500 Vdc	1
• Changed 1414 V to 1500 Vdc	3

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