Design Guide: TIDA-010009

Compact, efficient, 24-V input auxiliary power supply reference design for servo drives

Description

This design showcases a method to generate power supplies required in a servo or AC drive including the analog and digital I/O interfaces, encoder supply, isolated transceivers, and digital processing block. The design also implements protection against input reverse polarity, output overload, and short-circuit conditions.

Resources

TIDA-010009	Design Folder
TPS2663	Product Folder
LM5180-Q1	Product Folder
LP2951-N	Product Folder
TPS62125	Product Folder
LMR33630	Product Folder
TPS25200	Product Folder
LM3880	Product Folder
TLV62569	Product Folder
TPS62821	Product Folder
TPS61170	Product Folder
CSD19533Q5A	Product Folder
CSD16301Q2	Product Folder

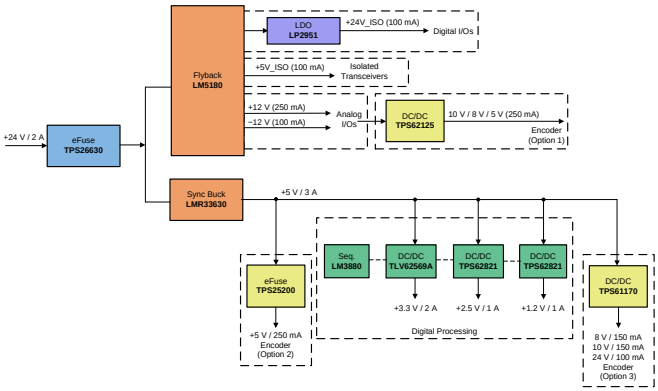
TI E2E™ Community — ASK Our E2E™ Experts

Features

- Powered from an external protective extra-low voltage (PELV) power supply of 24 V ±20%
- Industrial eFuse at supply input providing programmable UV/OV, reverse polarity protection, output overload and SC protection
- Synchronous buck DC/DC converter with integrated switch optimized for > 90% efficiency and compact size
- PSR flyback with integrated switch to generate isolated voltage rails for communication and digital I/Os
- Programmable voltage output to support multiple encoder types
- Output voltage rails: 24VISO, 5VISO, ±12 V, 5 V, 3.3 V, 2.5 V, 1.2 V with load and line regulation of < ±1%

Applications

- Variable Speed AC/DC Drives
- Servo Drives



Copyright © 2019, Texas Instruments Incorporated

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

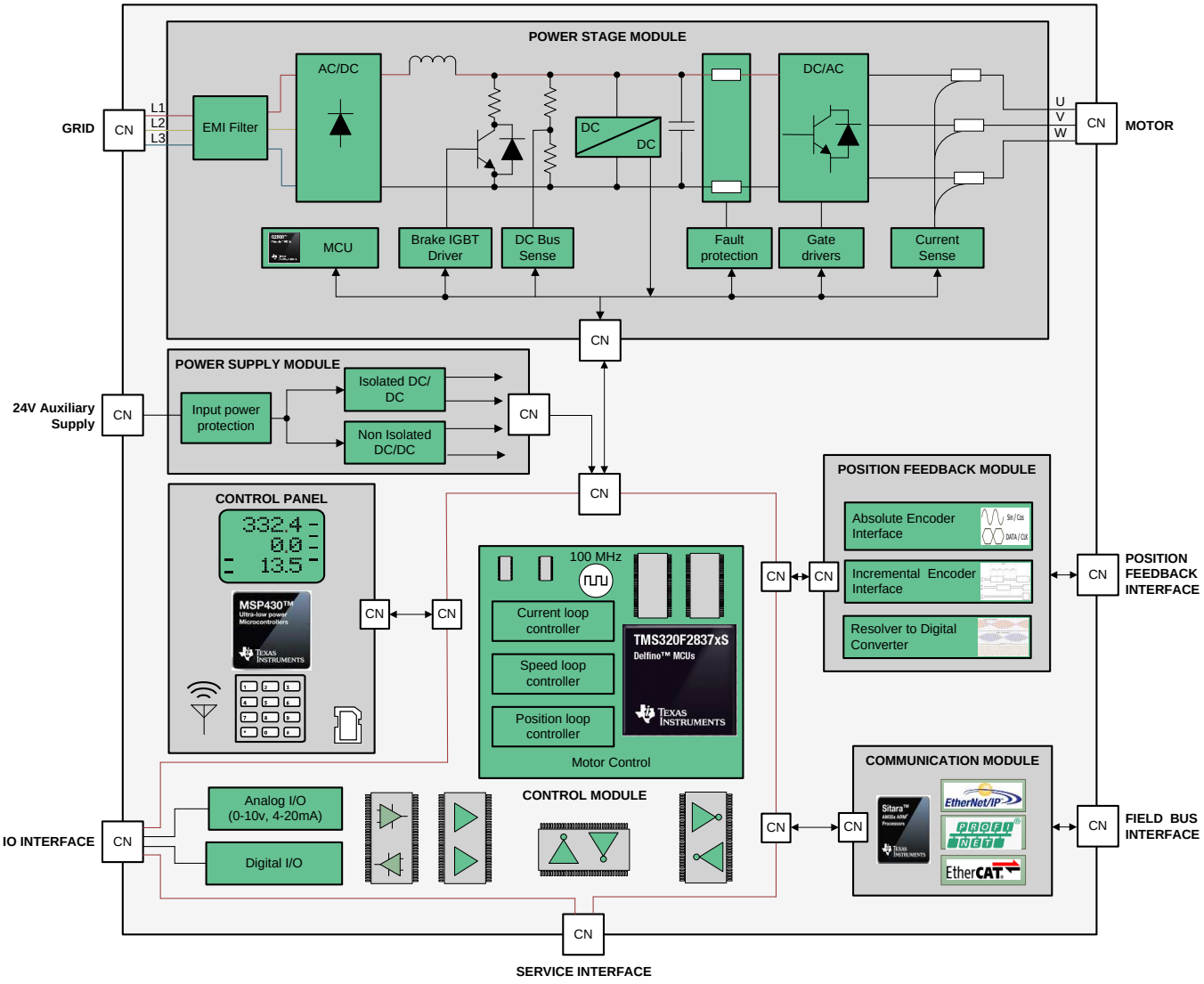
Servo drives consist of a power section, controller, position sensor and feedback, user IO, display, and communication module. Multiple voltage rails are required for the operation of all the control electronics in the drive which can be generated from a single-phase supply terminal, the DC link, or using an 24-V external power supply. The advantage of using an external power supply is that in an event of 3-phase power failure, the supply to the control electronics is not lost and the communication and diagnostic features are maintained. In situations where the drive is mounted in a cabinet, the 3-phase power cannot be supplied when the cabinet door is open. By providing an external +24-V supply, cabinet doors can be opened without resetting the controller of the drive.

While using a 24-V external supply, the system has to be robust against miswiring, EMC immunity, and overvoltage transients at the input. Protection against reverse polarity, reverse power flow, over- and undervoltage and overcurrent are necessary. The power supply for the system should also be compact, cost effective, and efficient. The system is designed keeping in mind that external 24-V supply is a protective extra low voltage (PELV) supply where the voltage cannot exceed 60 V DC in normal or single fault conditions. A single fault condition is where the basic insulation is short-circuited and the current- or voltage-limiting device is short-circuited or open-circuited, whichever is less favorable.

The 24-V supply can be used to generate multiple isolated and non-isolated power rails for the digital processing and memory, the analog and digital I/Os, communication interfaces, and encoder.

Copyright © 2019, Texas Instruments Incorporated

Figure 1. Typical Motor Drive Architecture



1.1 Key System Specifications

Table 1 highlights the key system specifications of the TIDA-010009.

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage range	24VDC ±20%
Output voltage rails	24 V, 1-A (Unregulated output from eFuse for fan or gate driver supply) Isolated 24 V, 100-mA (Regulated supply for Digital IOs) Isolated 5 V, 100 mA 12 V, 250 mA –12 V, 100 mA 3.3 V, 2 A 1.2 V, 1 A 2.5 V, 1 A Configurable encoder supply: Option 1: 5 V, 8 V, 10 V, 250 mA Option 2: 8 V, 10 V, 150 mA 24 V, 100 mA Option 3: 5 V, 250 mA
Efficiency	> 90% for DC/DC converters

Copyright © 2019, Texas Instruments Incorporated

Table 1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS
Inrush current limit	225 mA
Maximum input voltage withstand capability	60 V
Reverse polarity protection capability at the input	Up to –60 V
Programmable under and over-voltage at the input	UVLO trip point: 18 V OVLO trip point: 28 V
Current limit on 5 V, 250-mA encoder supply rail	320 mA
Current limit on 24-V, 100-mA digital IO supply rail	200 mA
Sequencing of power rails for digital processing	3.3 V, 1.2 V, 2.5 V with 10-ms delay between power up of each rail
Operating temperature	–25ºC to 85ºC Max
Form factor	114 mm × 77.47 mm

Copyright © 2019, Texas Instruments Incorporated

2 System Overview

2.1 Block Diagram

Figure 2. TIDA-010009 Block Diagram

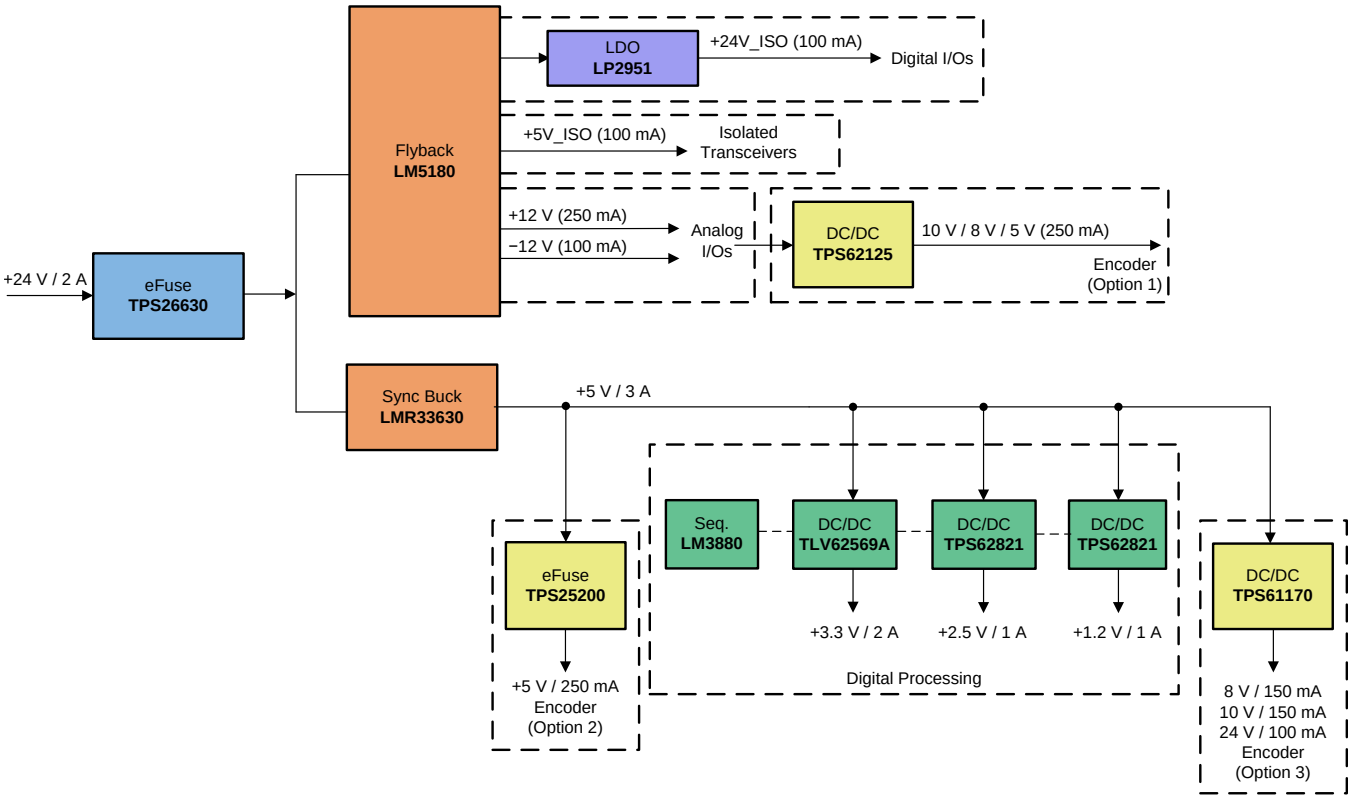


Figure 2 shows the TIDA-010009 block diagram. The design is capable of operating at a nominal input voltage of 24-V. An EMI filter is used at the input to suppress the common-mode noise generated by the converters in the design. The TPS26630 is an eFuse with integrated FET which is used to limit current and protect downstream DC/DC converters against overvoltage during fault conditions. The 24-V output from the eFuse is given to the VIN pin of the flyback controller, LM5180 which further generates isolated 24 V, isolated 5 V, and ±12 V at the output. The isolated 5 V is used to power up the isolated transceivers of various industrial fieldbus interfaces. The isolated 24-V is used for digital IO. The ±12-V rail is used for the analog IO in drive. The 12-V rail at the output of the flyback can be down-converted to 5 V, 8 V, or 10 V using the TPS62125 device for powering up the encoder in the system. The LM5180 device uses primary-side regulation (PSR), which offers better cross-regulation between the multiple outputs when compared with the auxiliary winding feedback method. The 24-V output from the eFuse also feeds into a simple switcher, the LMR33630 device which down-converts the 24-V rail to 5-V. The LMR33630 device is capable of driving up to 3 A of load current from an input of up to 36 V. The 5-V, 3-A output of the LMR33630 device is further down-converted to 3.3 V, 1.2 V, and 2.5 V for powering the digital processing block of the system. The power rails to the digital processing block are sequenced using a LM3880 sequencer. The 5-V output from the LMR33630 device passes through a highly-integrated boost converter, the TPS61170 device which steps up the voltage to either 8 V, 10 V, or 24 V by using different feedback resistors. The output from the TPS61170 device is used to power up the encoder.

Copyright © 2019, Texas Instruments Incorporated

2.2 Highlighted Products

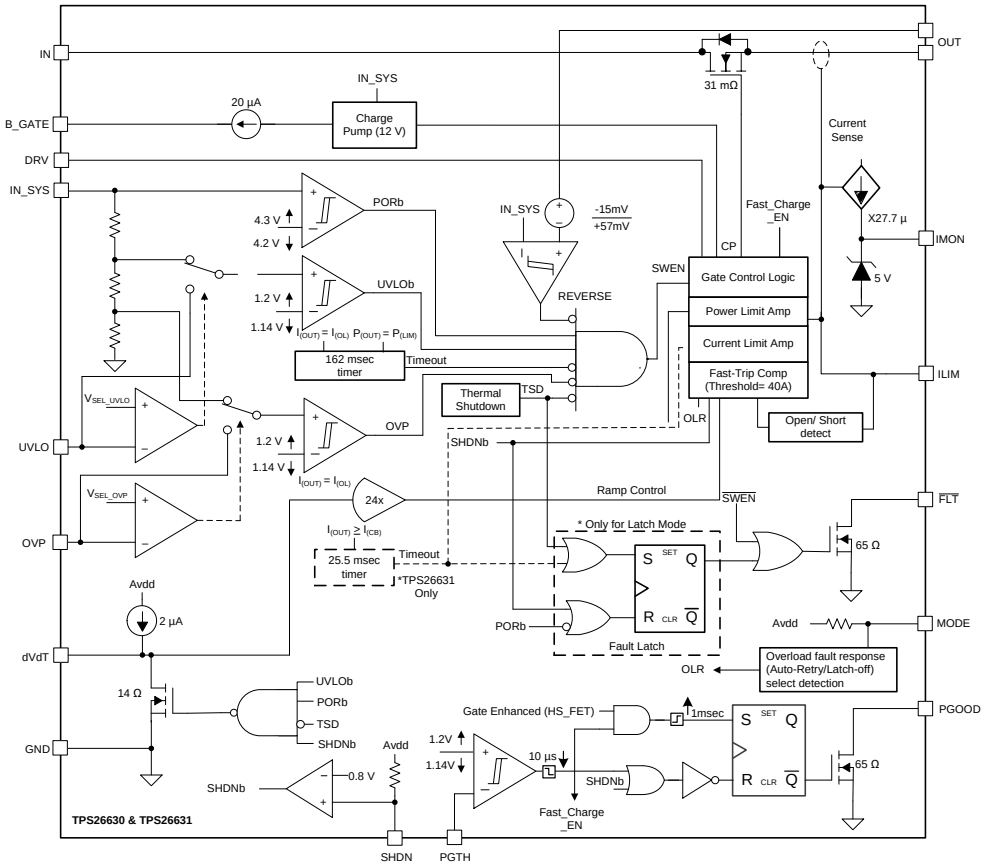
2.2.1 TPS2663

The TPS2663x devices are easy to use, positive 60-V and 6-A eFuse with a 31-mΩ integrated FET. It features a B-FET driver to control an external N-channel FET in the system designs that require protection from input reverse polarity faults and reverse current blocking. The device incorporates robust protection features that simplify system designs requiring class-A performance (no supply interrupts) during system tests like IEC61000-4-5 Surge tests as well as input supply brown-out tests.

Inrush current control during hot-plug operation can be achieved with the help of the dVdT feature. The TPS26630 and TPS26631 devices feature adjustable overvoltage cutoff functionality. The devices also feature adjustable overcurrent functionality. An analog current monitor can be used to sense the real time load current. The device features fault indicator output. PGOOD with adjustable detection threshold (PGTH) and can be used for enable and disable control of the downstream DC/DC converters.

The servo drive is powered using an external PELV supply where the TPS26630 eFuse protects against overvoltage transients and controls inrush current.

Figure 3. TPS26630 Block Diagram



Copyright © 2019, Texas Instruments Incorporated

2.2.2 LM5180-Q1

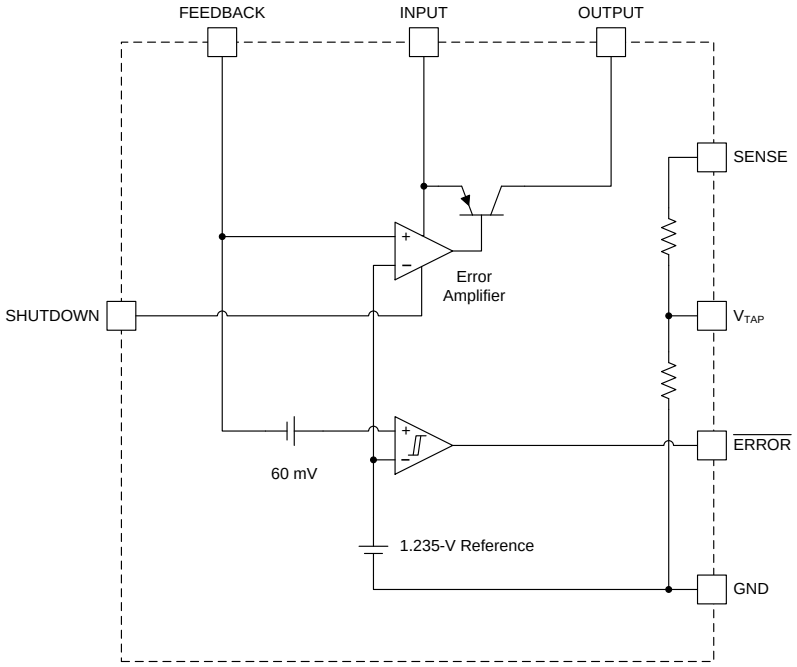
The LM5180 is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 70 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. The high level of integration results is a simple, reliable and high-density design with only one component crossing the isolation barrier. Boundary conduction mode (BCM) switching enables a compact magnetic solution and better than ±1% load and line regulation performance. An integrated 100-V power MOSFET provides output power up to 7 W with enhanced headroom for line transients.

2.2.3 LP2951-N

The LP2950 and LP2951 devices are bipolar, low-dropout voltage regulators that can accommodate a wide input supply-voltage range of up to 30 V. The 8-pin LP2951 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and VTAP pins together, the LP2951 outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and VTAP pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

In this design, the LP2951 device is used to regulate the 24-V supply to digital IOs. It limits the output current to 200 mA, in case of short-circuit conditions.

Figure 4. LP2951 Functional Diagram



2.2.4 TPS62125

The TPS62125 device is a high-efficiency synchronous step-down converter optimized for low and ultra-low power applications providing up to 300-mA output current. The device has a wide input voltage range of 3 V to 17 V. The device includes a precise low-power enable comparator which can be used as an input supply voltage supervisor (SVS) to address system specific power-up and power-down requirements. The enable comparator consumes only 6-µA quiescent current and features an accurate threshold of 1.2 V typical as well as an adjustable hysteresis. With this feature, the converter can generate a power supply rail by extracting energy from a storage capacitor fed from high impedance sources such as solar panels or current loops. With its DCS-Control scheme the converter provides power-save mode

Copyright © 2019, Texas Instruments Incorporated

operation to maintain highest efficiency over the entire load current range. At light loads the converter operates in pulse frequency modulation (PFM) mode and transitions seamlessly and automatically in pulse width modulation (PWM) mode at higher load currents. The DCS-Control™ scheme is optimized for low-output ripple voltage in PFM mode to reduce output noise to a minimum and features excellent AC load regulation. An open-drain power good output indicates once the output voltage is in regulation.

The TPS62125 device has a greater than 90% efficiency and is used for generating encoder supplies 5-V, 8-V, or 10-V rail by varying the feedback resistor.

2.2.5 LMR33630

The LMR33630 SIMPLE SWITCHER® regulator is an easy-to-use, synchronous, step-down DC/DC converter that delivers best-in-class efficiency for rugged industrial applications. The LMR33630 device is capable of driving up to 3 A of load current from an input of up to 36 V. The LMR33630 device provides high light-load efficiency and output accuracy in a very small solution size. Features such as a power-good flag and precision enable provide both flexible and easy-to-use solutions for a wide range of applications. The LMR33630 device automatically folds back frequency at light load to improve efficiency. Protection features include thermal shutdown, input undervoltage lockout, cycle-by-cycle current limit, and hiccup short-circuit protection.

In this design, the LMR33630 device is used to down-convert the 24-V rail to 5-V rail. It shows a line regulation of less than 1% across varying input voltage.

2.2.6 TPS25200

The TPS25200 device is a 5-V eFuse with precision current limit and overvoltage clamp. The device provides robust protection for load and source during overvoltage and overcurrent events. The TPS25200 device is an intelligent protected load switch with VIN tolerant to 20 V. In the event that an incorrect voltage is applied at IN, the output clamps to 5.4 V to protect the load. If the voltage at IN exceeds 7.6 V, the device disconnects the load to prevent damage to the device, or load, or both.

The TPS25200 device has an internal 60-mΩ power switch and is intended for protecting source, device, and load under a variety of abnormal conditions. The device provides up to 2.5 A of continuous load current. Current limit is programmable from 85 mA to 2.9 A with a single resistor to ground. During overload events output current is limited to the level set by R_{ILIM}. If a persistent overload occurs the device eventually goes into thermal shutoff to prevent damage to the TPS25200.

In this design TPS25200 is used for encoder power supply protection where the output current limit is set to 320 mA.

2.2.7 LM3880

The LM3880 simple power supply sequencer offers the easiest method to control power up sequencing and power down sequencing of multiple independent voltage rails. By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in a 6-pin SOT-23-6 package, the Simple Sequencer contains a precision enable pin and three open-drain output flags. The open-drain output flags permit that they can be pulled up to distinct voltage supplies separate from the sequencer VDD, so as to interface with ICs requiring a range of different enable signals. When the LM3880 is enabled, the three output flags will sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags will follow a reverse sequence during power down to avoid latch conditions.

In this design, the power supply sequencer LM3880 is used to sequence the power up of the digital processing block.

Copyright © 2019, Texas Instruments Incorporated

2.2.8 TLV62569

The TLV62569 device is a synchronous buck DC-DC converter optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 2 A. At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 1.5-MHz switching frequency. At light load, the device automatically enters Power Save Mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is reduced to less than 2 µA. The TLV62569 provides an adjustable output voltage via an external resistor divider. An internal soft start circuit limits the inrush current during startup. Other features like over current protection, thermal shutdown protection and power good are built-in. The device is available in a SOT23 and SOT563 package.

In this design, the TLV62569 device generates 3.3 V for the digital processing block. It shows an efficiency greater than 90% across varying loads.

2.2.9 TPS62821

The TPS62821 device is a part of the TPS6282x family of devices. The TPS6282x is an all-purpose and easy to use synchronous step-down DC/DC converter with a very low quiescent current of only 4 µA. It supplies up to 3-A output current (TPS62823) from a 2.4-V to 5.5-V input voltage. Based on the DCS-Control™ topology it provides a fast transient response. The internal reference allows to regulate the output voltage down to 0.6 V with a high-feedback voltage accuracy of 1% over the junction temperature range of –40°C to 125°C. The TPS6282x include an automatically entered power save mode to maintain high efficiency down to very light loads. The device features a Power Good signal and an internal soft start circuit. For fault protection, it incorporates a HICCUP current limit as well as a thermal shutdown. The TPS6282x are packaged in a 2 × 1.5 mm QFN-8 package.

The TPS62821 device is used to generate 1.2-V and 2.5-V voltage rails in this design used in the digital processing block.

2.2.10 TPS61170

The TPS61170 is a monolithic, high-voltage switching regulator with integrated 1.2-A, 40-V power MOSFET. The device can be configured in several standard switching-regulator topologies, including boost and SEPIC. The device has a wide input-voltage range to support applications with input voltage from multi-cell batteries or regulated 5-V, 12-V power rails.

The TPS61170 operates at a 1.2-MHz switching frequency, allowing the use of low-profile inductors and low-value ceramic input and output capacitors. External loop compensation components give the user flexibility to optimize loop compensation and transient response. The device has built-in protection features, such as pulse-by-pulse overcurrent limit, soft start, and thermal shutdown. The TPS61170 is available in a 6-pin 2-mm × 2-mm QFN package, allowing a compact power-supply solution.

In this design, the TPS61170 device is used to generate 8 V, 10 V, or 24 V by varying the feedback resistor. This voltage rail can be used to power up the encoder in the drive.

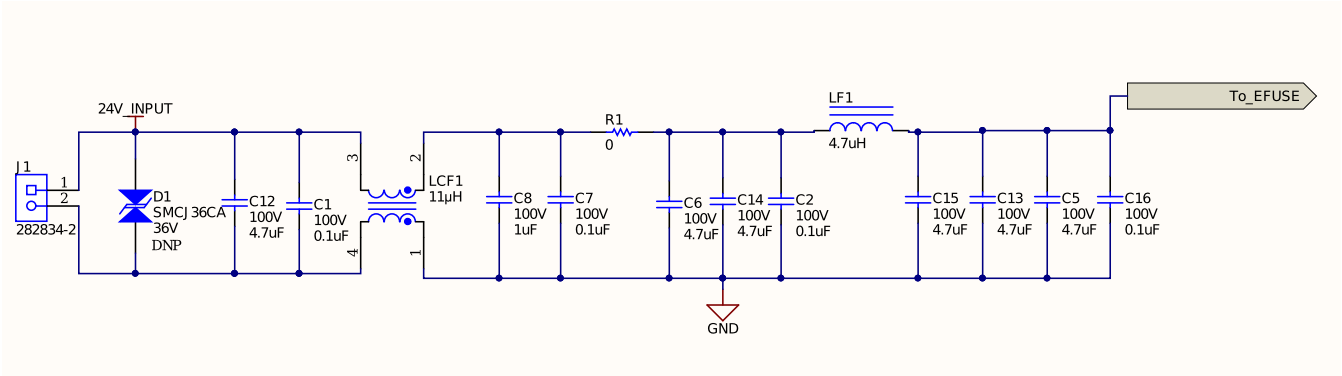
Copyright © 2019, Texas Instruments Incorporated

2.3 System Design Theory

2.3.1 Input Filter Design

In this design, the input supply voltage passes through a common mode and differential mode filter. The advantage of the differential mode is two-fold. First, the filter has two-poles at its cutoff frequency, resulting in a slope of –40 dB/decade, giving rise to a steeper cutoff. Second, owing to its bidirectional nature, this not only filters out high-frequency noise from entering the system, but also protects the line from EMI noise generated in the system. The differential filter used in this reference design uses ceramic capacitors of 4.7 µF, 100-V, X7R and a 4.7-µH inductor. For further input filtering and damping, an electrolytic capacitor of 0.1 µF, 100 V is added. This is a cheap and compact solution to construct a low cutoff frequency filter.

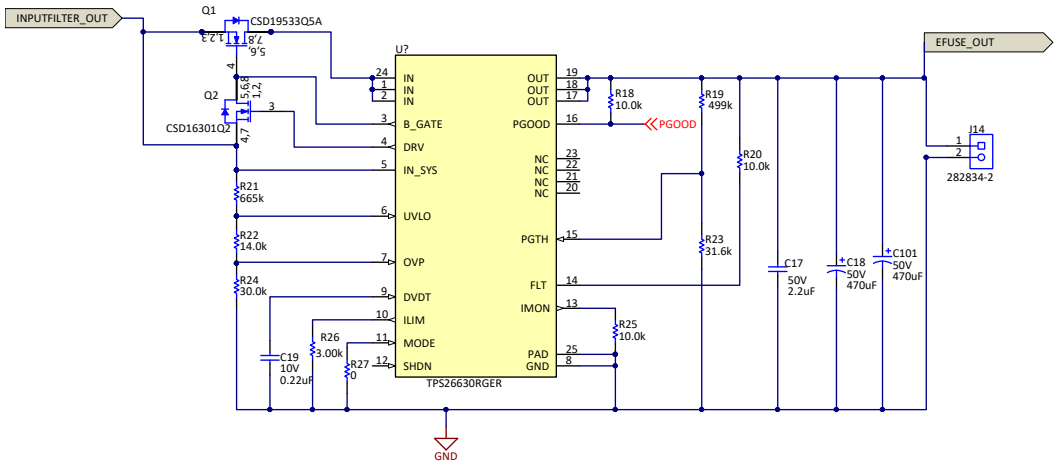
Figure 5. Input Filter Schematic



2.3.2 Protection at Input by eFuse

The power supply module is usually connected to an auxiliary 24-V DC or to rectified AC Mains to provide power to the controller, different interfaces, encoder supply and I/O modules. Input protection circuits are required to protect the module from faults such as overvoltage, undervoltage, and overload. In an auxiliary system, protection circuits should block the reverse polarity to protect the power supply from possible negative voltages. The eFuse TPS26630 offers a plug-and-play input protection solution for such applications.

Figure 6. TPS26630 eFuse Schematic



Copyright © 2019, Texas Instruments Incorporated

2.3.2.1 Programming the Current-Limit Threshold—R_{ILIM} Selection

The TPS26630 device provides an accurate overload current limiting and fast short-circuit protection feature. The current limit threshold can be decided by an external resistor using Equation 1.

$$I_{OL} = \frac{18}{R_{ILIM}} \quad (1)$$

where

- I_{OL} is the overload current limit in Ampere
- R_{ILIM} is the current limit resistor in kΩ

The current limit threshold is set at 6 A, thus requiring the R_{ILIM} (R26) to be 3 kΩ.

2.3.2.2 Undervoltage Lockout and Overvoltage Set Point

The TPS26630 device protects the system during overvoltage and undervoltage conditions. The UVLO and overvoltage trip points can be set using an external voltage divider network. As the devices in the design operate at a voltage range of 20 V to 27 V, the UVLO trip point (V(UV)) is set at 18 V and the overvoltage point (V(OV)) is set at 28 V using the following equations:

$$V_{OV} = \frac{R21 + R22 + R24}{R24} \times V_{OVPR} \quad (2)$$

$$V_{UV} = \frac{R21 + R22 + R24}{R22 + R24} \times V_{UVLOR} \quad (3)$$

where

- the value of device overvoltage threshold voltage V_{OVPR} and undervoltage threshold voltage V_{OVLR} is 1.2 V.

Solving the equations gives R21 = 665 kΩ, R22 = 14 kΩ, and R24 = 30 kΩ.

2.3.2.3 Output Buffer Capacitor – C_{OUT}

During the power interruption time TFAIL_TR, the output capacitor C_{OUT} of the TPS26630 provides energy to the load. The required buffer capacitor C_{OUT} can be computed as follows:

$$C_{OUT} = \frac{2 \times P(DC-DC) \times TFAIL_TR}{V(IN-SYS)^2 - V(UV_DC-DC)^2} \quad (4)$$

where

- P(DC-DC) = 70.1 W/η, assuming efficiency of 85%, P(DC-DC) = 82.47 W
- TFAIL_TR = 1.5 ms
- V(IN_SYS) = 24 V
- V(UV_DC-DC) = 18 V

The C_{OUT} is computed to be 0.98 mF. This design uses two 470-µF electrolytic capacitors C18 and C101 with 20% tolerance.

2.3.2.4 Power Good Threshold (PGTH) Set Point

The Power Good feature of the device can be used to enable or disable the device downstream in the design. The power-good threshold point is set according to the UVLO threshold of the downstream device in the design. The UVLO threshold of the DC/DC converter downstream is 18 V. Hence, the PGTH set point is calculated as:

$$V(PGTHF) = \frac{R23}{R19 + R23} \times V_{UVLO_DC-DC} \quad (5)$$

where

- V(PGTHF) = 1.14 V

Assuming R19 = 499 kΩ, R4 comes out to be approximately 33.7 kΩ.

Copyright © 2019, Texas Instruments Incorporated

2.3.2.5 Setting Output Voltage Ramp Time—(tdVdT)

The TPS26630 device uses an external capacitor connected at the dVdT pin for a controlled start-up and to control the inrush current. The inrush current is calculated as follows:

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{OUT} \times \frac{V_{(IN_SYS)}}{t_{dVdT}}$$

where

- $t_{dVdT} = 20.8 \times 10^3 \times V_{(IN_SYS)} \times C_{(dVdT)}$ (6)

In this design, the inrush current is limited to 225 mA by placing a 200-nF capacitor C19 at dVdT pin. The fastest output slew rate can be achieved by leaving the dVdT pin floating.

2.3.2.6 Selecting Q1, Q2 and TVS Clamp for Surge Protection

The TPS26630 device supports the reverse input polarity protection feature. Connecting an N-channel power FET (Q1) with the source to IN_SYS, drain to IN and GATE to B-GATE forms a back to back FET topology in power path that is required to protect the load from input reverse polarity faults. Connecting an external signal FET (Q2) across BGATE, DRV and IN_SYS creates a pulldown gate switch for Q1 during reverse current and reverse polarity fault events.

In case of a negative surge strike, the input voltage will be clamped to –58.1 V by D1 resulting in a voltage stress of –(58.1 V + 24 V) = 82.1 V, across the external blocking FET Q1. In this design a 100-V rated N-channel FET is chosen.

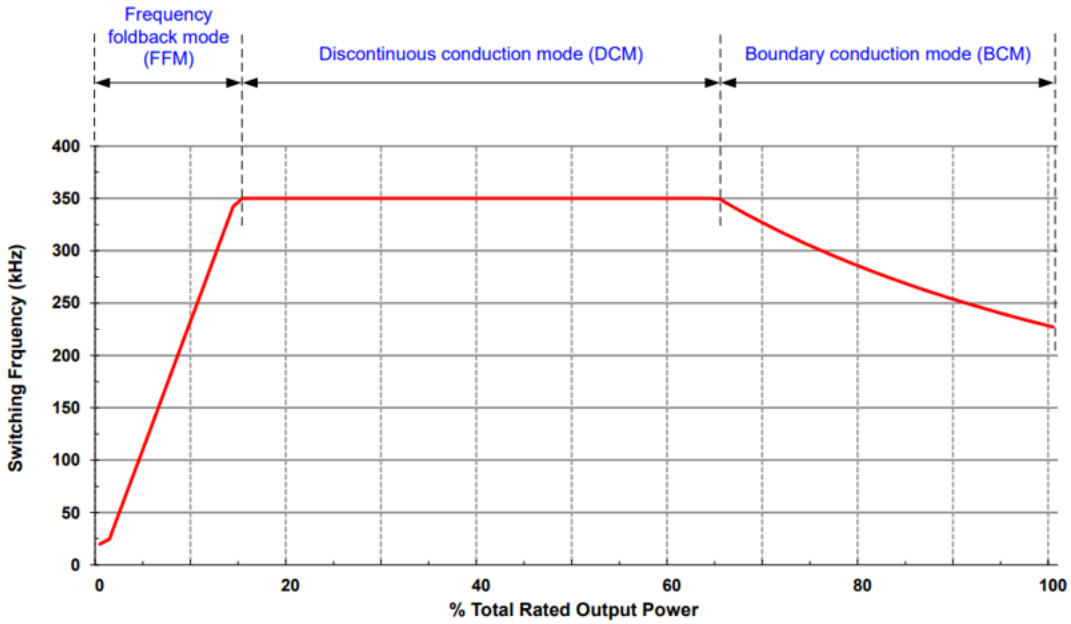
The B_GATE drive is in the range of 10 V – 14 V thus a suitable FET with the target $R_{DS(on)}$ specified at this gate drive voltage is selected. Q2 should be at least 15 V VDS rated FET with a maximum VGS rating of 20 V, Ciss ≤ 50 pF and VGTH(min) ≤ 3V. The CSD19533Q5A and CSD16301Q2 are selected for Q1 and Q2, respectively.

2.3.3 Designing Flyback Power Supply

2.3.3.1 LM5180 Operation

The LM5180 flyback controller works in three different modes depending on the load as Figure 7 shows.

Figure 7. Three Modes of Operation Illustrated by Variation of Switching Frequency With Load



Copyright © 2019, Texas Instruments Incorporated

At high loads, the LM5180 device operates in *Quasi-Resonant Boundary Conduction Mode*. The power MOSFET turns on when the current in the secondary winding reaches zero at the first valley on the SW node, to minimize switch-on losses. The MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the peak current decreases and the frequency increases to maintain BCM operation. The duty cycle (D) remains constant with the load in this mode, and is determined by Equation 7. The peak current I_{SW-PK} for a given load can be estimated using Equation 8.

$$D = \frac{(V_{OUT} + V_{FWD}) \times NPS}{(V_{OUT} + V_{FWD}) \times NPS + V_{IN}} = 0.507 \quad (7)$$

$$I_{SW-PK} = \frac{2 \times P_{OUT}}{V_{IN} \times D \times \eta} = 1.37A \quad (8)$$

$$\frac{1}{2} \times V_{IN} \times I_{PK,PRI} \times D \times \eta = P_{OUT}$$

where

- NPS is the primary-to-secondary turns ratio
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{FWD} is the forward voltage drop of the flyback secondary diode, which is 0.7 V for the diode used in this reference design
- η is the efficiency which is estimated as 85% at full load for calculations (9)

At medium loads, the LM5180 device operates in *Discontinuous Conduction Mode* (DCM), where it clamps the maximum switching frequency to 350 kHz and as the load decreases, the peak current reduces to maintain regulation at 350 kHz.

At even lighter loads, the system operates in *Frequency Fold-Back Mode* (FFM), and the switching frequency decreases as the load current is reduced. The primary-side peak current fixed by the internal error amplifier decreases to a minimum level of 0.27 A and the MOSFET off-time extends to maintain the output load requirement. The LM5180 device has a minimum frequency of operation at 10 kHz.

2.3.3.2 Transformer Design

The transformer design includes making key decisions on the turns ratio and primary inductance. Further specifications like the switching frequency, saturation current, leakage inductance, isolation, primary and secondary DCRs, and mechanicals – pinout, footprint, and height also need to be optimized to minimize losses, size, and cost.

The constraint on the minimum value of the turns ratio (primary to secondary) is set by the maximum output power yielded by a particular turns ratio to be greater than 7 W. Whereas, the maximum possible value of the turns ratio is constrained by the voltage rating of the built-in MOSFET in the LM5180 device. The initial estimate of turns ratio can be calculated according to Equation 10:

$$NPS = \frac{N_P}{N_S} = \frac{D}{1-D} \times \frac{V_{IN(MIN)}}{(V_{OUT} + V_{FWD})} \quad (10)$$

Thus, the turns ratio calculated for the following rails is:

$$NPSmin\ (24V) = 0.99;\ \text{approximately}\ 1$$
$$NPSmin\ (12V) = 1.94;\ \text{approximately}\ 2$$
$$NPSmin\ (5V) = 4.33;\ \text{approximately}\ 4.5 \quad (11)$$

The built-in MOSFET is rated at 100 V. In the off cycle, when the secondary (flyback) diode is on, the voltage on the drain (VDS) is as Equation 12 shows.

$$VDS = V_{IN} + V_{REF} + V_{RING} = 24 + 25 + 20 = 69V \quad (12)$$

Copyright © 2019, Texas Instruments Incorporated

Also, the voltage across the secondary diode when the switch is on can be calculated as shown.

$$VDIODE(24V\ \ rail) = V_{OUT} + \left(\frac{V_{IN}}{NPS}\right) + VD_SPIKE = 24 + 24 + 20 = 68\ \ V$$

$$VDIODE(12V\ \ rail) = V_{OUT} + \left(\frac{V_{IN}}{NPS}\right) + VD_SPIKE = 12 + 12 + 20 = 44\ \ V$$

$$VDIODE(5V\ \ rail) = V_{OUT} + \left(\frac{V_{IN}}{NPS}\right) + VD_SPIKE = 5 + 5.3 + 20 = 30.3\ \ V$$

where

- V_{IN} is the input voltage
- V_{REF} = NPS × (V_{OUT} + V_{FWD}) = 1 × (24 + 0.7) = 24.7 V approximately 25 is the primary voltage reflected across the transformer
- V_{OUT} is the output voltage
- V_{RING} and VD-SPIKE is the spike in voltage due to resonance (assumed to be 20 V) (13)

To provide the maximum possible output power for a given turns ratio, the controller will work in the BCM with the maximum possible IPK,PRI(MAX) that can be withstood by the primary MOSFET (1.5 A). As the primary-to-secondary turns ratio is increased, the duty cycle increases according to Equation 7. In BCM, the output power can be estimated with Equation 14.

$$POUT_MAX = \frac{I_{SW-PK}}{2 \times \left(\frac{1}{V_{IN(MAX)}} + \frac{1}{NPS \times (V_{OUT} + V_{FWD})}\right)} = 8.34\ \ W \quad (14)$$

The inductance of the transformer primarily determines the modes of operation in the LM5180 device as the load is varied from the minimum load to full load. An increase in the magnetic inductance generally leads to an increase in the leakage inductance of the transformer. The LM5180 device has a minimum off time ($T_{OFF(MIN)}$) of 500 ns: the magnetizing current should not decrease to zero in less than 500 ns. Equation 15 calculates the minimum inductance value (LPRI) as 46 µH.

$$L_{PRI} \geq \frac{(V_{OUT} + V_{FWD}) \times NPS \times T_{OFF_MIN}}{I_{PK,PRI(MIN)}} \geq 46\ \ \mu H$$

where

- V_{OUT} is the output voltage
- The minimum peak primary current ($I_{PK,PRI(MIN)}$) is 0.27 A for the LM5180 device
- The primary to secondary turns ratio is NPS (15)

Thus, this reference design uses a transformer with primary magnetic inductance of 75 µH.

2.3.3.3 Input and Output Capacitor Selection

Without input capacitors, a high ripple current in the converter is supplied by the unregulated power source. Stray inductance and resistance causes high-voltage ripple. Input capacitors provide a bypass for this ripple current and stabilize the supply bus voltage during a transient event. This design uses a ceramic capacitor at the input, since the ESR of aluminum electrolytics and most tantalums is too high to allow for effective ripple reduction and causes excessive power dissipation in the ESR parasitic. The capacitance value can be calculated with Equation 16:

$$C_{IN} > \frac{I_{SW-PK} \times D \times (1-D)^2}{2 \times f_{SW} \times \Delta V_{IN}}$$

where

- I_{SW-PK} is the peak primary current
- ΔV_{IN} is variation in the input voltage (16)

The minimum value of the output capacitor can be calculated as follows:

$$C_{OUT} > \frac{I_{OUT} \times \left(I_{PK-PR(MAX)} - \frac{I_{OUT}}{NPS}\right)^2}{I_{PK-PR(MAX)}^2 \times f_{SW} \times \Delta V_{OUT}}$$

where

- $I_{PK-PRI(MAX)}$ is the maximum primary current that can be taken by MOSFET
- NPS is the turns ratio
- ΔV_{OUT} is the variation in output voltage (17)

Copyright © 2019, Texas Instruments Incorporated

2.3.3.4 Flyback Diodes

The secondary (flyback) diodes used in the design should withstand the maximum secondary current peak ($I_{PK,SEC}$) as well as the maximum reverse voltage across the diode. The diode should also have low leakage current to avoid losses and hence a decrease in the efficiency; this can be achieved by using ultra-fast switching diodes.

The maximum primary peak current of the LM5180 device is 1.65 A which translates to a secondary peak current of 1.65 A with a turns ratio of 1:1. The maximum output average current to be provided by a rail in the design is 0.250 A. Thus, the flyback diode should have a surge current greater than 3 A at 350 kHz, and an average current rating greater than 0.3 A. The reverse voltage across the diode when the primary side MOSFET is turned on is given by Equation 18:

$$\left(\frac{V_{IN(MAX)}}{NPS} + V_{OUT} + V_{RING}\right) = \left(\frac{28}{1} + 20 + 20\right) = 68 \text{ V} \quad (18)$$

Hence, the diode is rated at 100 V.

2.3.4 Power Supply for Analog IO

Analog inputs are used to communicate speed, position, and torque control reference set points from the motion controller or PLC to the drive. Analog outputs are used to monitor and feedback key drive parameters back to the motion controller or PLC or to drive display meters. Analog IOs can be ±10 V, 0-V to 10-V signals or 4- to 20-mA current signals.

In this design, ±12-V rail is generated using the flyback to provide power supply to the analog I/Os in the drive.

2.3.5 Power Supply for Digital IO

Digital I/O Interfaces are designed for the PLC-based system which requires an isolated power supply of 24 V. In this design, an isolated 24-V rail is generated using the flyback and LP2951 low-dropout voltage regulator. The output of the LDO is set at 24 V using an external resistor divider pair. The resistor divider is tied to VOUT, and the divided-down voltage is tied directly to the FEEDBACK pin for comparison against the internal 1.235-V reference.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R30}{R34}\right) - I_{FB}R30 \quad (19)$$

where

- V_{REF} = 1.235 V
- I_{FB} = FEEDBACK bias current, typically 20 nA

In this design, R30 = 2.05 MΩ and R34 = 105 kΩ.

The LP2951 device has an active-low error output signal if the output voltage drops by 6% of its nominal value. The device has an output current limit of 200 mA to limit the output current in case of short-circuit conditions.

Copyright © 2019, Texas Instruments Incorporated

2.3.6 Power Supply for Isolated Transceivers

Wired signal interfaces like RS-485, CAN or interface translators are important for deterministic, secure and reliable communication between drive and external systems like PLC, motion controllers, or other drives on the factory floor. To achieve a robust data communications in harsh industrial environments, this reference design provides power isolation to protect against voltage spikes and ground loops within the noisy environment and improve system reliability. An isolated 5-V rail is generated using flyback.

2.3.7 Designing SIMPLE SWITCHER®, LMR33630

In this design, the LMR33630 device down-converts the 24-V rail to 5 V. The LMR33630 device is capable of driving up to 3 A of load current from an input of up to 36 V. The 5-V, 3-A output of the LMR33630 device is further down-converted to 3.3 V, 1.2-V, and 2.5-V through a sequencer for powering the digital processing block in the drive.

2.3.7.1 Choosing Switching Frequency and Setting Output Voltage

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, therefore, a more compact design. In this design, the output current drawn from the LMR33630 device is 3 A, thus it is necessary to minimize losses to limit the temperature rise of the converter. Hence, we choose a switching frequency of 400 kHz.

The output voltage of the LMR33630 device is externally adjustable using a resistor divider network comprised of R58 and R60 which closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF} = 1 V. The resistance of the divider is a compromise between excessive noise pick-up and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value of R58 is 100 kΩ.

$$R60 = \frac{R58}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)} = \frac{100\ k\Omega}{\left(\frac{5\ V}{1\ V} - 1\right)} = 25\ k\Omega \quad (20)$$

For this design, R58 = 100 kΩ and R60 = 24.9 kΩ are chosen.

2.3.7.2 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current should be used. The following equation can be used to determine the value of inductance:

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times IOUT_{max}} \times \frac{V_{OUT}}{V_{IN}} = \frac{(24 - 5)}{400\ kHz \times 0.3 \times 3} \times \frac{5}{24} = 11\ \mu H \quad (21)$$

The constant K is the percentage of inductor current ripple. For this example we choose K = 0.3 and find an inductance L = 11 µH.

Ideally, the saturation current rating of the inductor should be at least as large as the high-side switch current limit, ISC. This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly.

To avoid sub-harmonic oscillation, the inductance value should not be less than that given in Equation 22. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. Generally, the minimum inductor ripple current should be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq 0.28 \times \frac{V_{OUT}}{f_{SW}} = 3.5\ \mu H \quad (22)$$

Copyright © 2019, Texas Instruments Incorporated

2.3.7.3 Input and Output Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the LMR33630 device. This capacitance can be increased to help reduce input voltage ripple, or maintain the input voltage during load transients, or both. In addition a small case size 220-nF ceramic capacitor must be used at the input, as close as possible to the regulator. This provides a high-frequency bypass for the control circuits internal to the device. This design uses a 10-µF, 35-V, X7R ceramic capacitor and two 220-nF, 50-V, X7R ceramic capacitors.

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. In this design, a bank of 4 × 22-µF, 16-V ceramic capacitors in the 1206 case size are used. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high-frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics. This design uses a 0.1-µF ceramic capacitor.

2.3.8 Power Supply for Digital Processing

Digital processing block receives processed current, voltage, temperature feedback signals and implements the control algorithm, monitors for fault conditions, communicates with external systems, generates gate signals to drive the power devices, stores critical information like fault parameters among other functions.

The power supplies for the digital processing block are generated by down-converting the 5-V, 3-A output of the LMR33630 device.

Copyright © 2019, Texas Instruments Incorporated

2.3.8.1 3.3-V Supply

The 3.3-V supply is used to power up the I/O in the digital processing module. 5 V is down-converted to 3.3 V using a high-efficiency synchronous buck converter, the TLV62569 device. The device operates with an adaptive off time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. An external resistor divider is used to set the output voltage according to the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R47}{R48}\right) \quad (23)$$

where

- Feedback voltage V_{FB} is 0.6 V.

Thus, the values chosen for R47 and R48 are 453 kΩ and 100 kΩ, respectively.

The inductor L6 and output capacitor C33 form an output low pass filter. The main parameters for inductor selection are inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, the following equation is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta IL}{2} = 2.17 \text{ A}$$
$$\Delta IL = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} = 0.34 \text{ A} \quad (24)$$

where

- $I_{OUT,MAX}$ = 2 A is the maximum output current
- ΔIL = 0.34 A is the inductor current ripple
- f_{SW} = 1.5 MHz is the switching frequency
- L, the inductor value is 2.2 µH

An output capacitor 10 µF, 10 V with low ESR is chosen to maintain low output voltage ripple. The TLV62529 device has a power-good feature which is used for sequencing the other voltage rails. The device has a 3-A output current limit.

2.3.8.2 2.5-V Supply

In this design, 5 V is down-converted to 2.5-V using a high-efficiency synchronous buck converter, the TPS62821 device. A 2.5-V rail can be used to power up processor cores, FPGA, or the memory module in a drive. The device operates in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. It operates at a nominal switching frequency of 2.2 MHz and provides a continuous output current of 1 A.

The TPS62821 device has a soft-start feature where about 250 µs after EN goes high, the internal circuitry controls the output voltage during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time of about 1 ms. An external resistor divider is used to set the output voltage according to the following equation:

$$R64 = \left(\frac{0.6 \text{ V}}{I_{FB}}\right) \qquad R63 = \left(\frac{V_{OUT}}{I_{FB}} - R64\right) \quad (25)$$

where

- the recommended value of I_{FB} is 5 µA

In this design R63 and R64 are set to 475 kΩ and 150 kΩ. A 470-nF inductor and 22-µF capacitor form the output filter. Connecting a 120-pF feed-forward capacitor between the output and feedback pin of the device improves the regulation speed.

2.3.8.3 1.2-V Supply

The 1.2-V rail is used to power up the processor core in the digital processing module of the drive. In this design, the TPS62821 device is used to generate 1.2-V from 5 V. According to Equation 25, the output voltage is set to 1.2-V using R53 = 100 kΩ and R59 = 100 kΩ.

Copyright © 2019, Texas Instruments Incorporated

2.3.9 Sequencing of Power Supplies

The digital processing module requires different power supply voltages with the correct power sequence. Power supply voltages turned on with an incorrect power sequence can cause reliability problems such as characteristics degradation, inrush currents, and latch-up conditions. This reference design addresses the challenge to design the power tree with the correct sequencing without trading off factors such as power tree architecture, efficiency, cost and size.

2.3.9.1 Using the Sequencer, LM3880

The LM3880 simple power supply sequencer provides a simple solution for sequencing multiple rails in a controlled manner. Integrated timers control the timing sequence (power up and power down) of three open-drain output flags which are connected to the enable pin of switchers to control the operation of the power supplies. When the EN pin is asserted, the power-up sequence starts. An internal counter delays the first flag (FLAG1) from rising until a fixed time period has expired. When the first flag is released, another timer will begin to delay the release of the second flag (FLAG2). This process repeats until all three flags have sequentially been released.

In this design, the output flags are asserted sequentially from FLAG1, FLAG2, to FLAG3 (1-2-3) with a 10-ms delay between each flag. A device can be chosen from the LM3880 family according to the sequence and delay desired.

2.3.9.2 Using the Power Good Signal

In this design, the Power Good of the TLV62569 (PG1) generating the 3.3 V is tied to the enable pin of the TPS62821 (EN2) generating a 1.2-V rail. The Power Good of the TPS62821 (PG2) generating the 1.2-V is tied to the enable pin of the TPS62821 (EN3) generating a 2.5-V rail. The power-good pin goes high when the output voltage rail reaches 95% of its value. The converter downstream is only enabled when the power good goes high ensuring the correct power-up sequence is followed.

2.3.10 Power Supplies for Encoder

This reference design showcases multiple methods for generating power supplies for different types of encoders.

2.3.10.1 5-V Encoder Supply

2.3.10.1.1 5-V, 250-mA Supply Using TPS62125

A 5-V, 250-mA supply for encoders is generated using flyback and synchronous step-down converter, the TPS62125 device. The output voltage is set to 5 V using external resistors according to the following equation:

$$V_{OUT} = 0.8\ V \times \left(\frac{R36}{R42} + 1\right) \quad (26)$$

For a 5-V output, R36 = 1.05 MΩ and R42 = 200 kΩ. The device has a short-circuit protection feature where it limits the current to up to 300 mA in case of short circuit.

2.3.10.1.2 5-V, 250-mA Supply Using TPS25200

In this design a 5-V, 250-mA supply for encoders is also generated using the LMR33630 SIMPLE SWITCHER® and TPS25200 eFuse. The TPS25200 device is a 5-V eFuse with precision current limit and overvoltage clamp. The device provides robust protection for load and source during overvoltage and overcurrent events. The TPS25200 device is an intelligent protected load switch with VIN tolerant to 20 V. In the event that an incorrect voltage is applied at IN, the output clamps to 5.4 V to protect the load. If the voltage at IN exceeds 7.6 V, the device disconnects the load to prevent damage to the device, or load, or both. Current limit is programmable from 85 mA to 2.9 A with a single resistor RILIM to ground. During overload events output current is limited to the level set by RILIM. In this design the current limit is set to 320 mA.

Copyright © 2019, Texas Instruments Incorporated

The TPS25200 device has a FAULT open-drain output which is asserted (active low) during an overcurrent, over-temperature, or overvoltage condition. The TPS25200 device asserts the FAULT signal until the fault condition is removed and the device resumes normal operation.

2.3.10.2 8-V and 10-V Encoder Supply

2.3.10.2.1 8-V, 250-mA Supply Using TPS62125

A 8-V, 250-mA encoder supply is generated using a flyback and synchronous step-down converter, the TPS62125. The output voltage is set to 8 V using external resistors according to Equation 27:

$$V_{OUT} = 0.8\ V \times \left(\frac{R39}{R42} + 1\right) \quad (27)$$

For an 8-V output, R39 = 1.8 MΩ and R42 = 200 kΩ. For a 10-V, 250-mA output, R37 = 2.32 MΩ and R42 = 200 kΩ The device has a short-circuit protection feature where it limits the current to up to 300 mA in case of short circuit.

2.3.10.2.2 8-V and 10-V, 150-mA Supply Using TPS61170

A 8-V, 150-mA and 10-V, 150-mA encoder supply is generated using a boost converter, the TPS61170. The device operates at a 1.2-MHz switching frequency, allowing the use of low-profile inductors and low-value ceramic input and output capacitors. The output voltage is set to 8 V using external resistors according to the following equation:

$$V_{OUT} = 1.229\ V \times \left(\frac{R103}{R104} + 1\right) \quad (28)$$

Considering the leakage current through the resistor divider and noise decoupling to the feedback FB pin, an optimum value for R104 is selected at 10 kΩ. For an 8-V output, R103 = 54.9 kΩ and a 10-V output, R102 = 71.5 kΩ. The capacitor in the range of 1 μF to 4.7 μF is recommended for the input side. The output typically requires a capacitor in the range of 1 μF to 10 μF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Thus this design uses a 4.7-μF capacitor at input and a 10-μF capacitor at output.

2.3.10.3 24-V Encoder Supply Using TPS61170

A 24-V, 100-mA supply for encoders is generated using a high-voltage boost converter, the TPS61170. The device operates at a 1.2-MHz switching frequency, allowing the use of low-profile inductors and low-value ceramic input and output capacitors.

The output voltage is set to 24 V using external resistors according to the following equation:

$$V_{OUT} = 1.229\ V \times \left(\frac{R101}{R104} + 1\right) \quad (29)$$

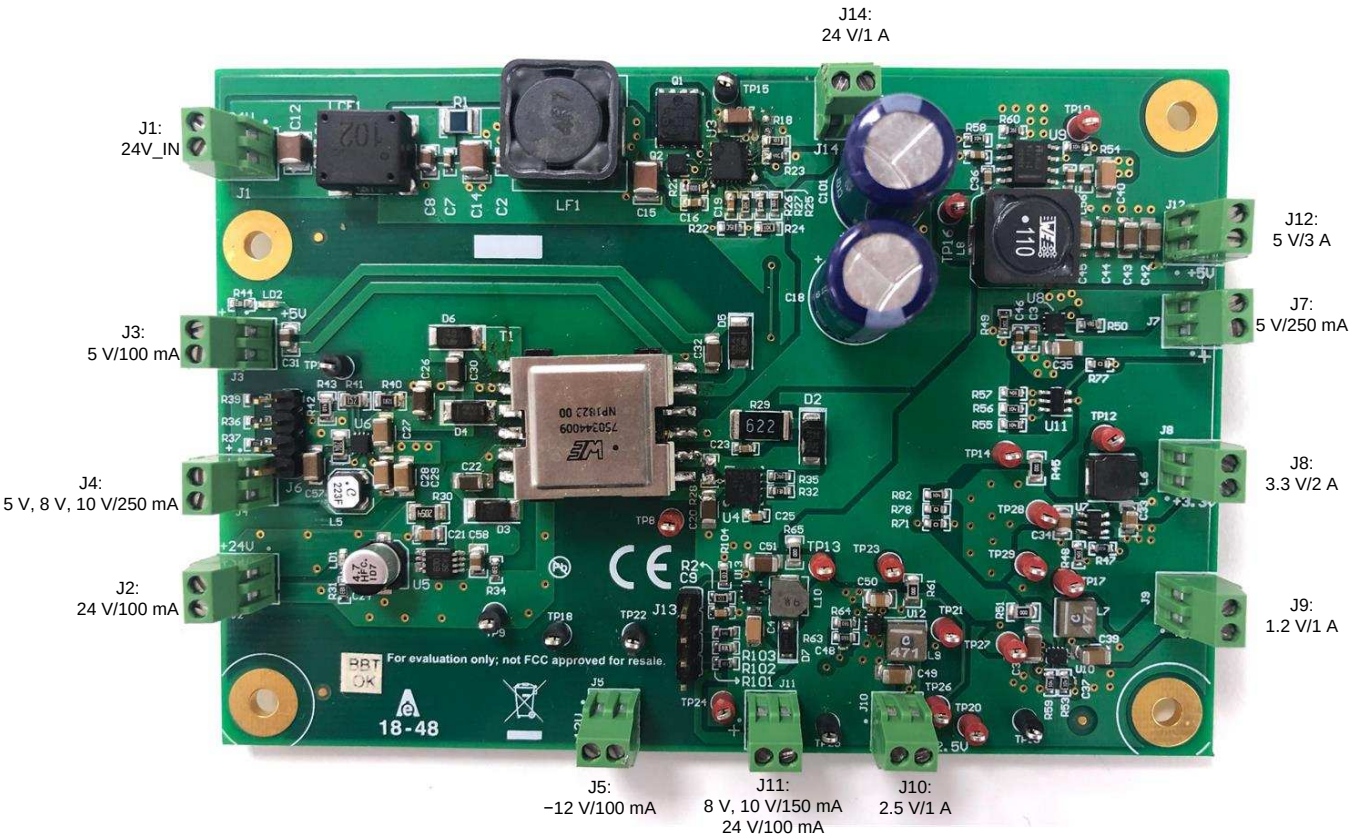
Considering the leakage current through the resistor divider and noise decoupling to feedback FB pin, an optimum value for R104 is selected at 10 kΩ. For a 24-V output, R101 = 187 kΩ. The capacitor in the range of 1 μF to 4.7 μF is recommended for the input side. The output typically requires a capacitor in the range of 1 μF to 10 μF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Thus, this design uses a 4.7-μF capacitor at input and a 10-μF capacitor at output.

Copyright © 2019, Texas Instruments Incorporated

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Getting Started Hardware

Figure 8. TIDA-010009 Top View



The TIDA-010009 is a compact board with 114-mm × 77.47-mm dimensions. Table 2 provides details on the connectors used in the design.

Table 2. Connector Functions

CONNECTOR	FUNCTION
J1	24-V nominal input power supply
J2	24-V, 100-mA output to digital I/O
J3	5-V, 100-mA output to isolated transceivers
J4	5-V, 8-V, 10-V, 250-mA VDD external supply to the encoder
J5	–12 V, 100-mA output to analog I/O
J6	Selection of the TPS62125 buck converter feedback resistor
J7	5-V, 250-mA VDD supply to the encoder
J8	3.3-V, 2-A output to digital processing block
J9	1.2-V, 1-A output to digital processing block
J10	2.5-V, 1-A output to digital processing block
J11	8-V, 10-V, 150-mA, 24-V, 100-mA VDD supply to the encoder
J12	5-V, 3-A output for encoder supply
J13	Selection of the TPS61170 boost converter feedback resistor
J14	24-V, 1-A unregulated output for fan or gate driver supply

Copyright © 2019, Texas Instruments Incorporated

3.2 Testing and Results

3.2.1 Functional Validation of eFuse

3.2.1.1 Soft Start and Inrush Current

Figure 9 highlights the inrush current control feature of the eFuse. An external capacitor of 200 nF connected at the dVdT pin to GND defines the slew rate of the output voltage at power on. In this design, the inrush current is limited to 225 mA according to Equation 6. The output of eFuse rises to 24 V in approximately 100 ms.

Figure 9. Hot Plug In and Inrush Current Control at 24-V Input

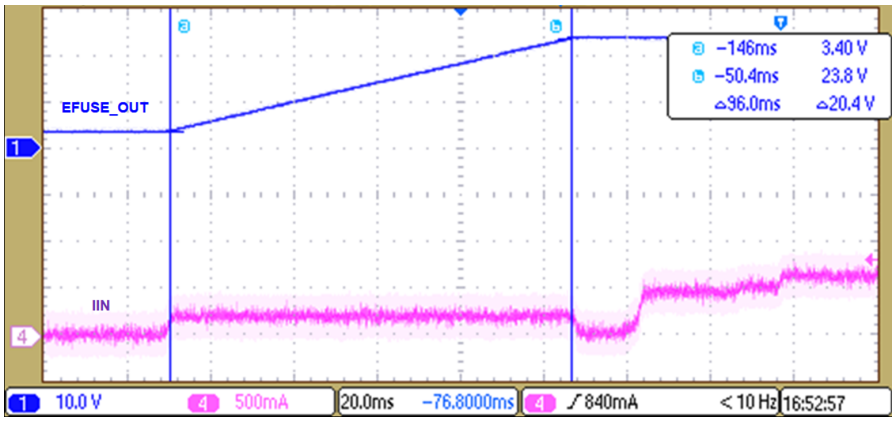


Figure 10 shows the controlled increase in input current as the sequencer LM3880 in the design enables the buck converters downstream. Figure 11 shows the decrease in current corresponding to power down of DC/DC converters

Figure 10. Input Current During Power Up of Power Supplies

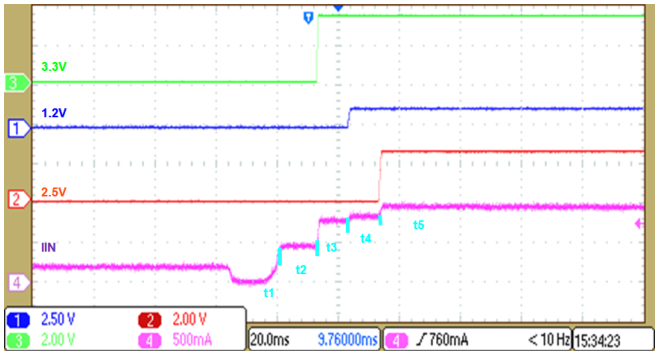


Figure 11. Input Current During Power Down of Supplies

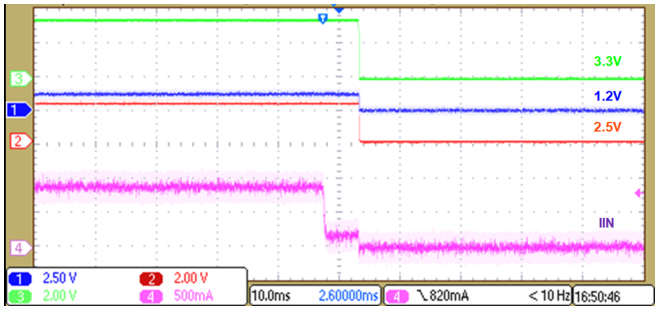


Table 3. Power Up of Power Supplies

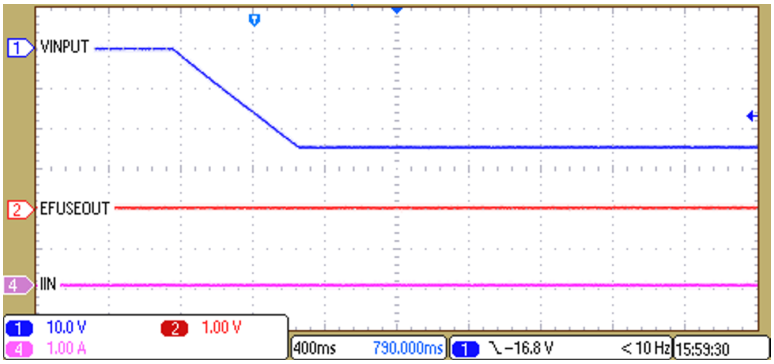
STATE	CONDITION
t1	All DC/DC converters are disabled
t2	LMR33630 generating 5 V is enabled
t3	TLV62569 generating 3.3 V is enabled
t4	TPS62821 generating 1.2 V is enabled
t5	TPS62821 generating 2.5 V is enabled

Copyright © 2019, Texas Instruments Incorporated

3.2.1.2 Input Reverse Polarity Protection

Figure 12 highlights the reverse polarity protection feature of the eFuse where the output of the eFuse remains unaffected by the application of reverse polarity voltage at the input.

Figure 12. Input Reverse Polarity Response



3.2.1.3 Undervoltage Lockout and Overvoltage Protection

Figure 13 highlights the undervoltage lockout feature of the eFuse and Figure 14 highlights the overvoltage protection feature of the eFuse. The undervoltage lockout is triggered at 18.4 V and the overvoltage protection starts at 28.8 V.

Figure 13. Undervoltage Lockout Feature

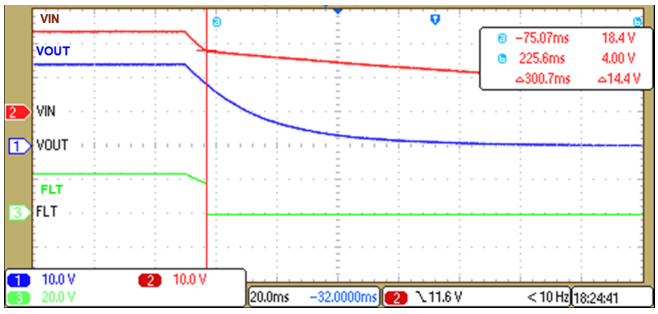
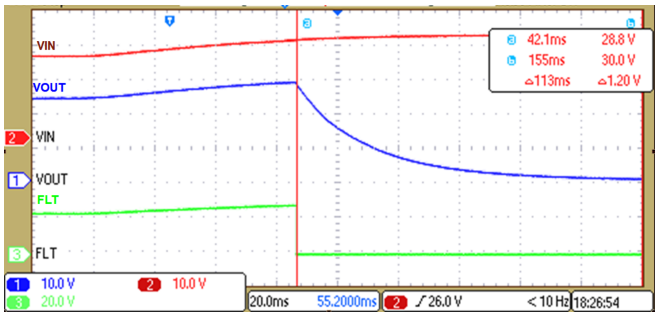


Figure 14. Overvoltage Protection Feature



Copyright © 2019, Texas Instruments Incorporated

3.2.2 Efficiency of Power Supplies

The efficiency is measured at loads varying from 10% to 100%. When the system is loaded at 50% for example, each rail is loaded at 50% of its maximum load.

Figure 15 through Figure 17 show the efficiency of DC/DC converters generating 3.3 V at 2 A, 2.5 V at 1 A, and 1.2 V at 1 A.

Figure 15. Efficiency of 3.3-V, 2-A Rail

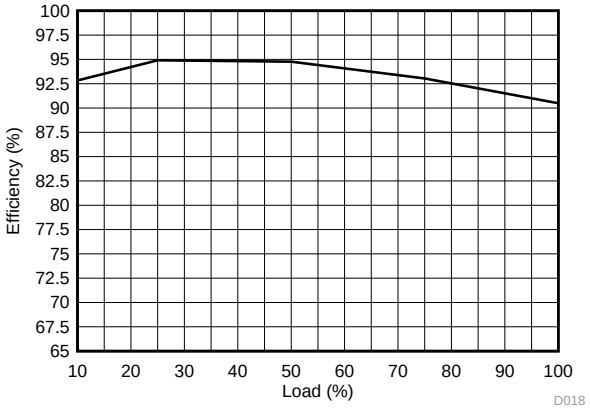


Figure 16. Efficiency of 2.5-V, 1-A Rail

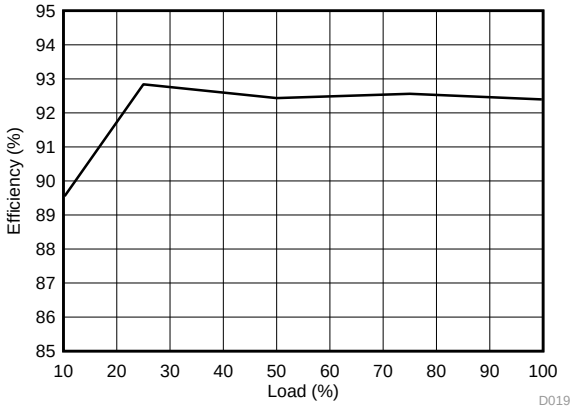
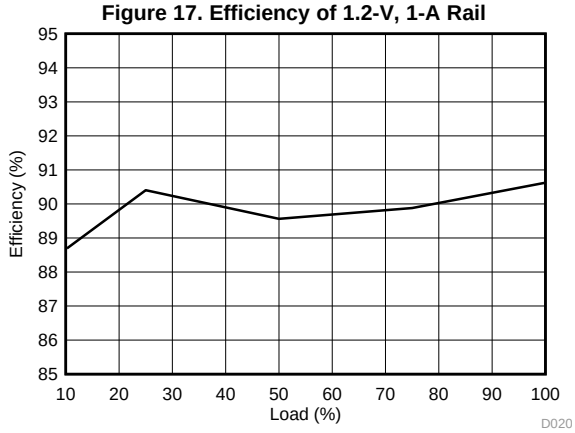


Figure 17. Efficiency of 1.2-V, 1-A Rail



Copyright © 2019, Texas Instruments Incorporated

Figure 18 through Figure 20 show the efficiency of the TPS61170 device generating 8 V at 150 mA, 10 V at 150 mA, and 24 V at 100 mA.

Figure 18. Efficiency of 8-V, 150-mA Rail

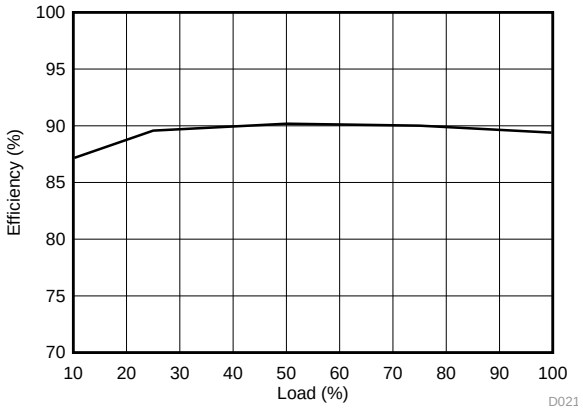


Figure 19. Efficiency of 10-V, 150-mA Rail

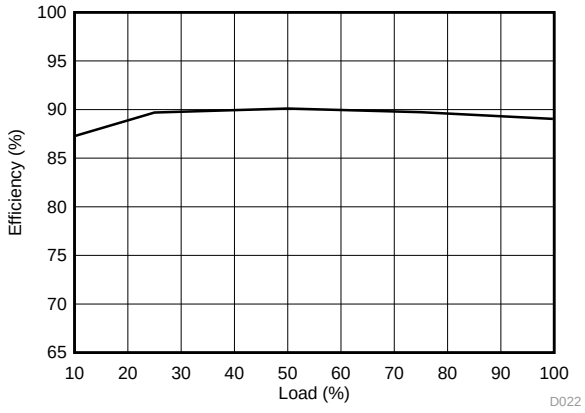
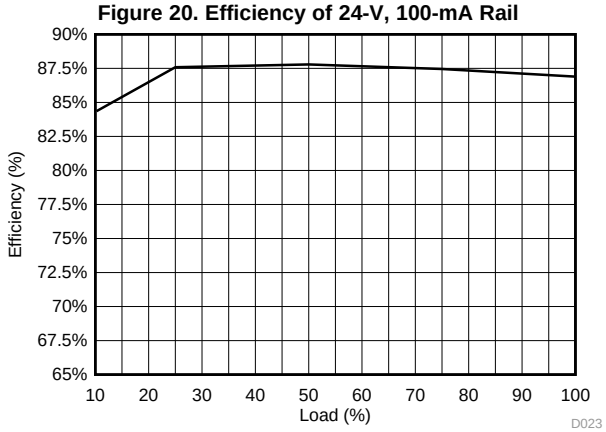


Figure 20. Efficiency of 24-V, 100-mA Rail



Copyright © 2019, Texas Instruments Incorporated

3.2.3 Load Regulation of Power Supplies

Load regulation is measured for power supplies where the load is varied from 10% to 100% and the output voltage noted.

Figure 21 through Figure 23 show the load regulation of 3.3-V, 2.5-V, and 1.2-V output rails.

Figure 21. Load Regulation of 3.3-V, 2-A Rail

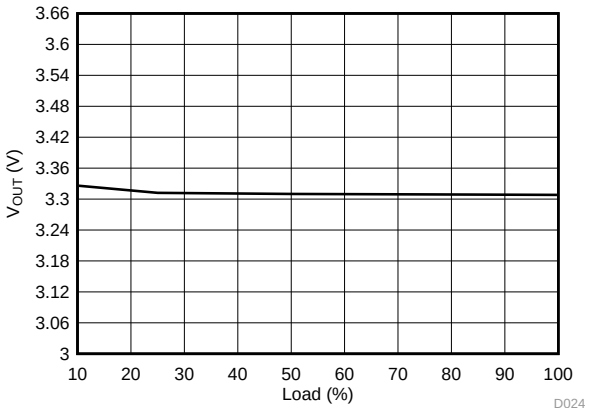


Figure 22. Load Regulation of 2.5-V, 1-A Rail

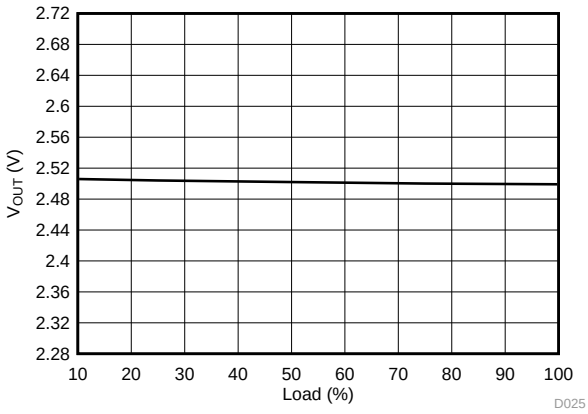
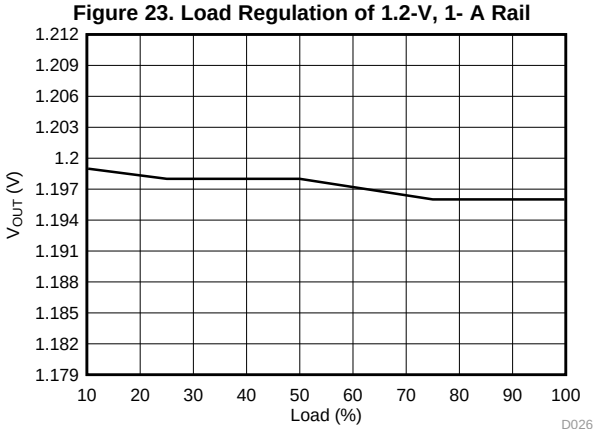


Figure 23. Load Regulation of 1.2-V, 1- A Rail



Copyright © 2019, Texas Instruments Incorporated

Figure 24 through Figure 26 show the load regulation of 8-V and 10-V at 150-mA rail, and 24-V at 100-mA rail generated by the TPS61170 device.

Figure 24. Load Regulation of 8-V, 150-mA Rail

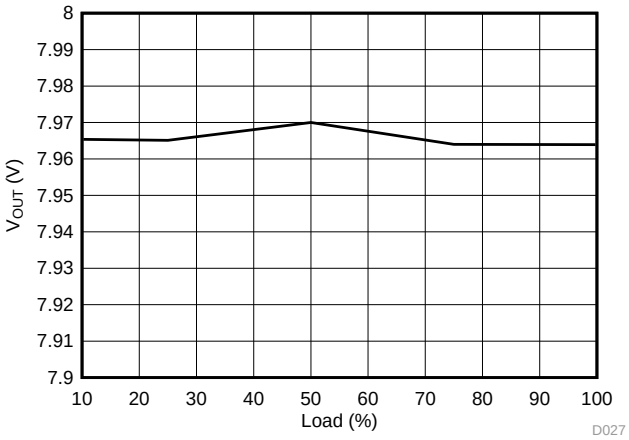


Figure 25. Load Regulation of 10-V, 150-mA Rail

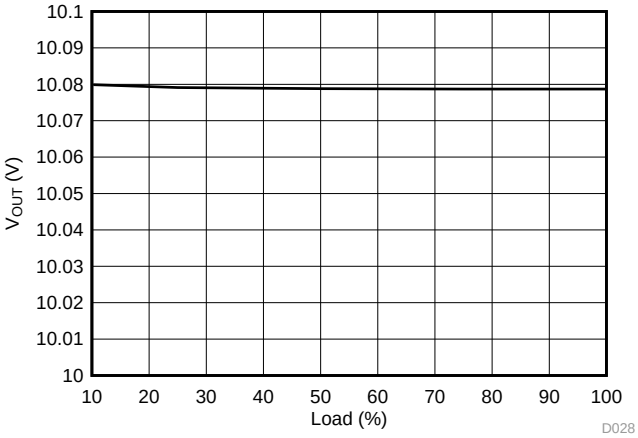
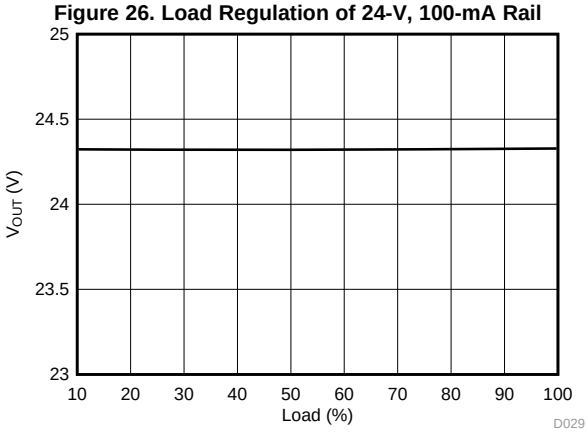


Figure 26. Load Regulation of 24-V, 100-mA Rail



Copyright © 2019, Texas Instruments Incorporated

3.2.4 Line Regulation at Full Load by LMR33630 and LM5180

Line regulation is measured for the LMR33630 and LM5180 device at full load where the input voltage is varied from 19 V to 29 V and the output voltage noted.

Figure 27 through Figure 29 show the line regulation of isolated 24-V rail, isolated 5-V and ±12-V rail generated by the LM5180.

Figure 27. Line Regulation of Isolated 24-V, 100-mA Rail

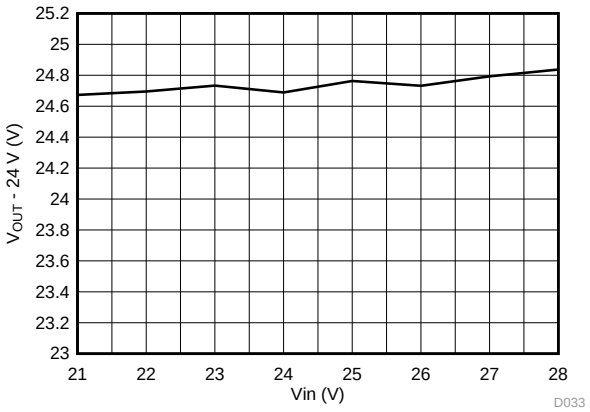


Figure 28. Line Regulation of Isolated 5-V, 100-mA Rail

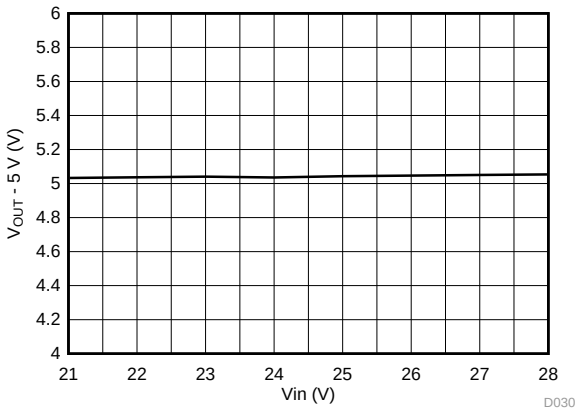


Figure 29. Line Regulation of 12-V, 250-mA Rail

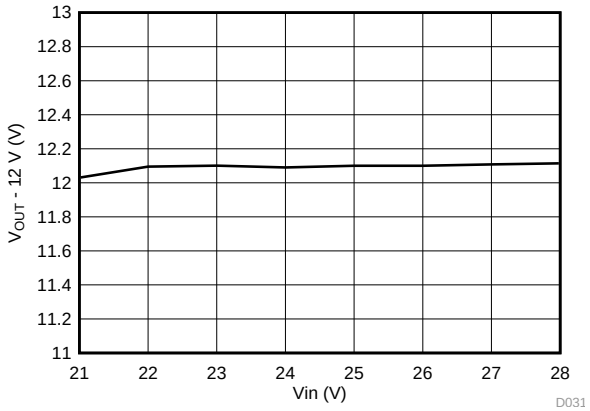


Figure 30. Line Regulation of –12-V, 100-mA Rail

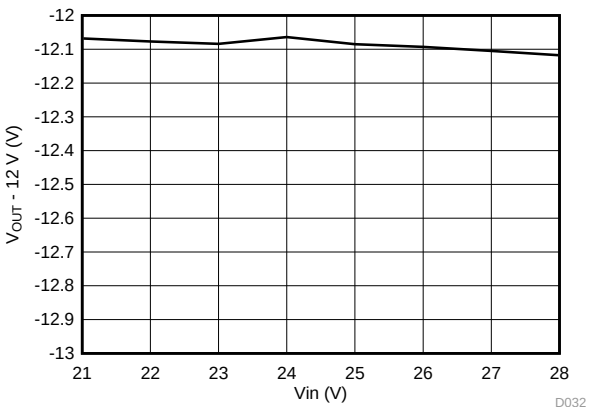
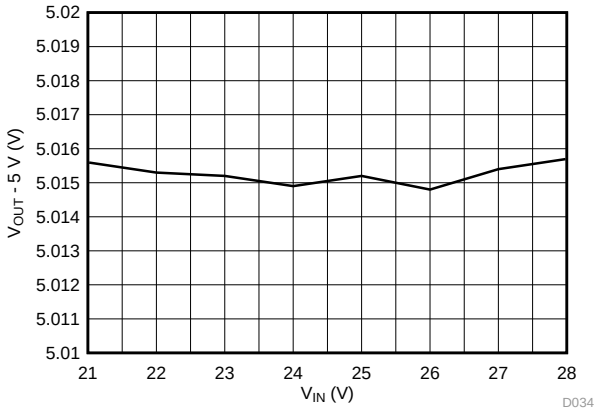


Figure 31 shows the line regulation of a 5-V rail generated by the LMR33630 device.

Figure 31. Line Regulation of LM33630 5-V Rail



Copyright © 2019, Texas Instruments Incorporated

3.2.5 Switch Node Waveforms of Supplies

The following figures show the switch node performance of buck converters in the design.

Figure 32 through Figure 34 show the switch node performance of power supplies for the digital processing block in the design.

Figure 32. Switch Node of TLV62569 3.3-V Rail at Full Load

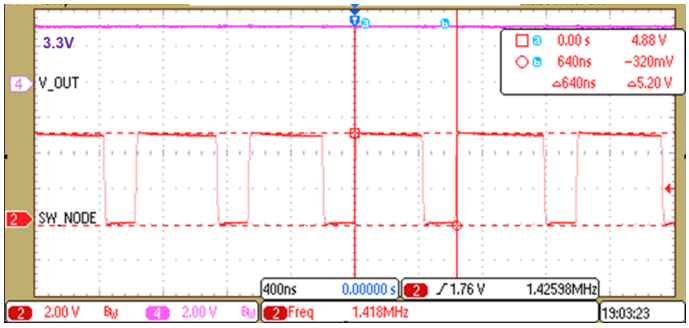


Figure 33. Switch Node of TPS62821 2.5-V Rail at Full Load

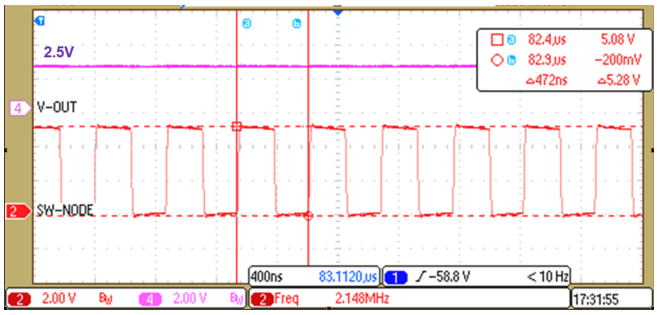
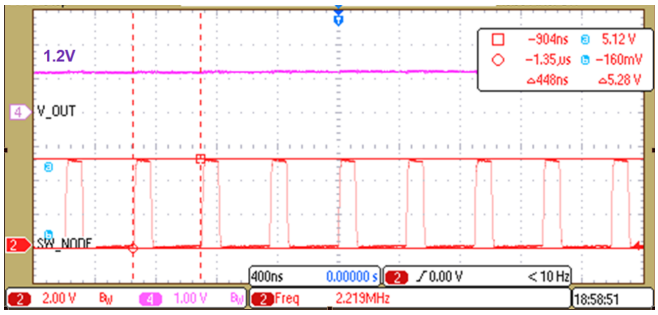


Figure 34. Switch Node of TPS62821 1.2-V Rail at Full Load



The following figures show the switch node performance of the buck converter, TPS62125, generating 5 V, 8 V, and 10 V for encoder supply.

Figure 35. Switch Node of TPS62125 5-V Rail at Full Load

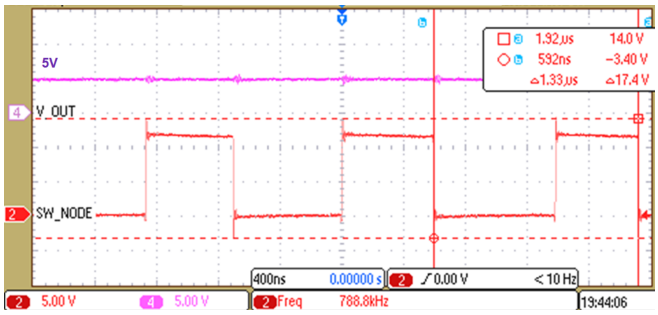
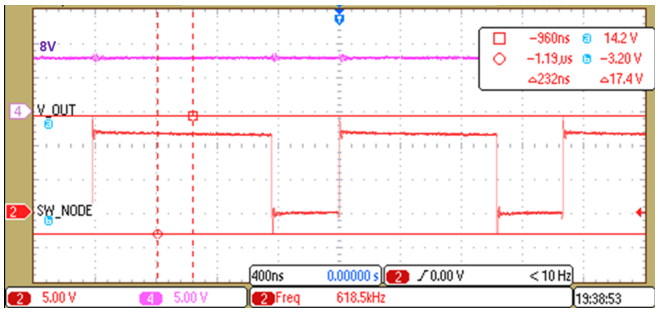


Figure 36. Switch Node of TPS62125 8-V Rail at Full Load



Copyright © 2019, Texas Instruments Incorporated

Figure 37. Switch Node of TPS62125 10-V Rail at Full Load

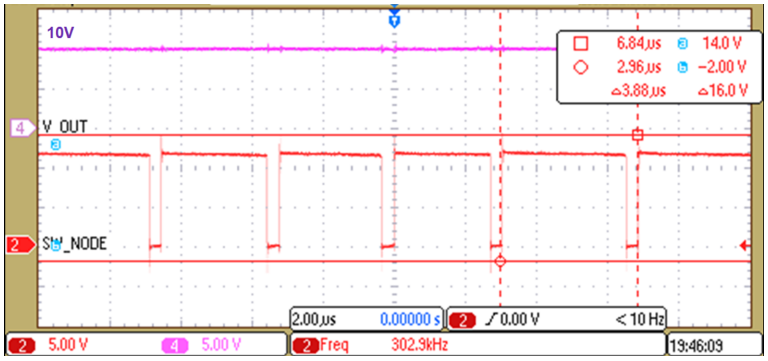


Figure 38 through Figure 40 show the switch node performance of the boost converter, TPS61170, generating 8 V, 10 V, and 24 V for encoder supply.

Figure 38. Switch Node of TPS61170 8-V Rail at Full Load

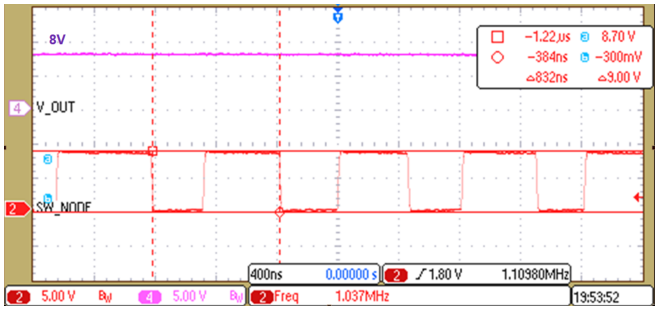


Figure 39. Switch Node of TPS61170 10-V Rail at Full Load

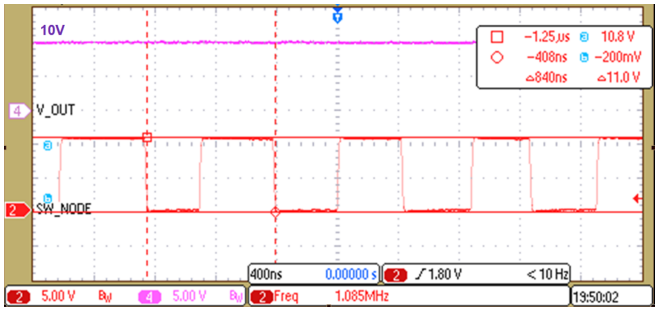
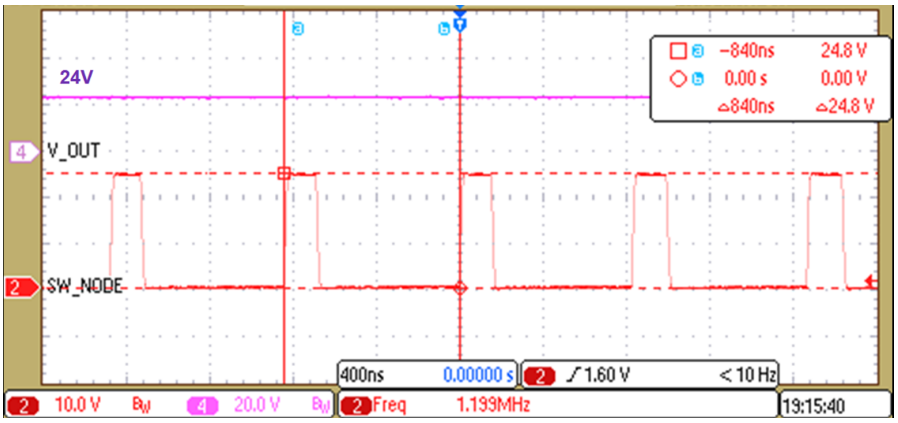


Figure 40. Switch Node of TPS61170 24-V Rail at Full Load



Copyright © 2019, Texas Instruments Incorporated

3.2.6 Sequencing of Voltages by Sequencer

Figure 41 and Figure 43 show sequencing by the sequencer LM3880, by the voltage rails where the voltage rails power up with a gap of 10 ms. Figure 42 and Figure 44 show the power down of the voltage rails. The power down behavior of the voltage rails depends on the discharging of the output capacitor through the connected load. 1.2-V and 2.5-V rails generated by TPS62821 are discharged through the SW pin by a current sink.

Figure 41. Power Up Sequencing by LM3880 at No Load

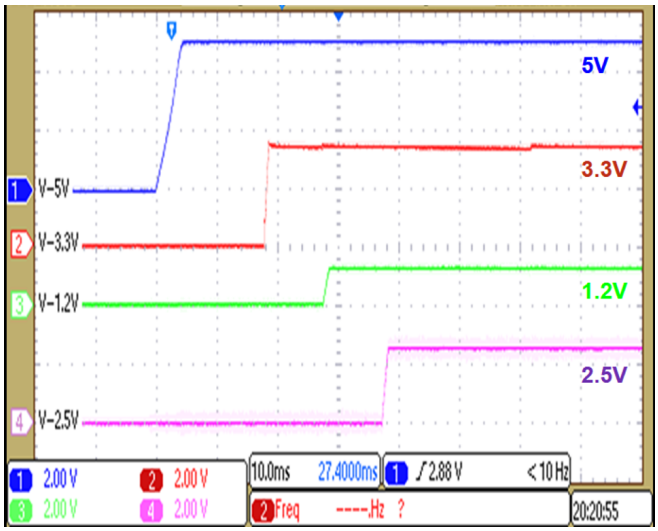


Figure 42. Power Down Sequencing by LM3880 at No Load

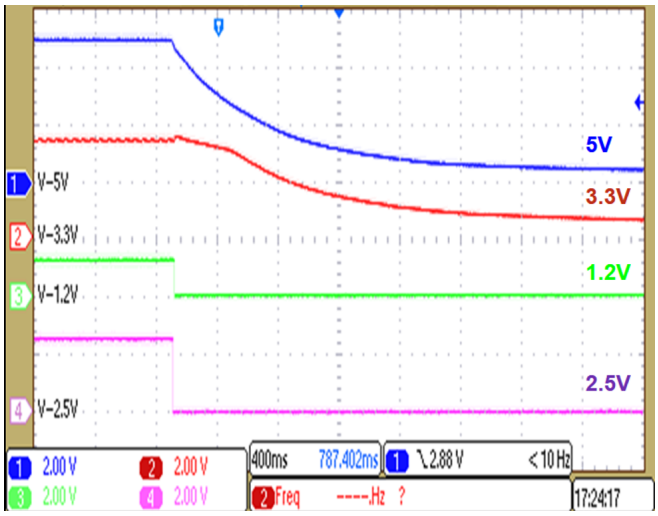


Figure 43. Power Up Sequencing by LM3880 at Full Load

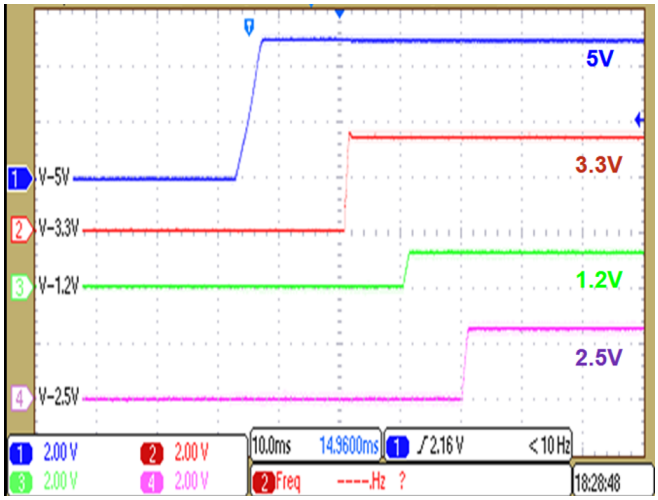
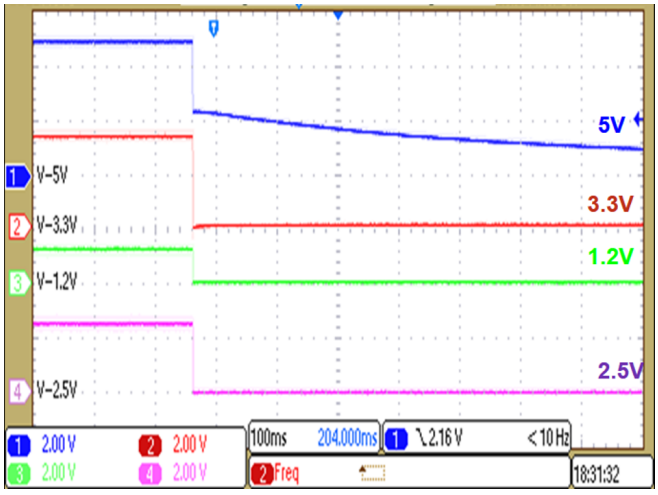


Figure 44. Power Down Sequencing by LM3880 at Full Load



3.2.7 Sequencing of Voltages by Power Good

Figure 45 and Figure 47 show sequencing through power good by the voltage rails where the voltage rail powers up only if the power good condition is met of the converter upstream. The power good of the 3.3-V rail is tied to the enable of the TPS62821 generating 1.2 V and the TPS61170 generating 24-V encoder supply. The power good of the 1.2-V rail is tied to the enable of the TPS62821 generating 2.5 V.

Figure 46 and Figure 48 show the power down of the voltage rails. The power down behavior of the voltage rails depends on the discharging of the output capacitor through the connected load. The 1.2-V and 2.5-V rails generated by the TPS62821 are discharged through the SW pin by a current sink.

Copyright © 2019, Texas Instruments Incorporated

Figure 45. Power Up Sequencing by Power Good at No Load

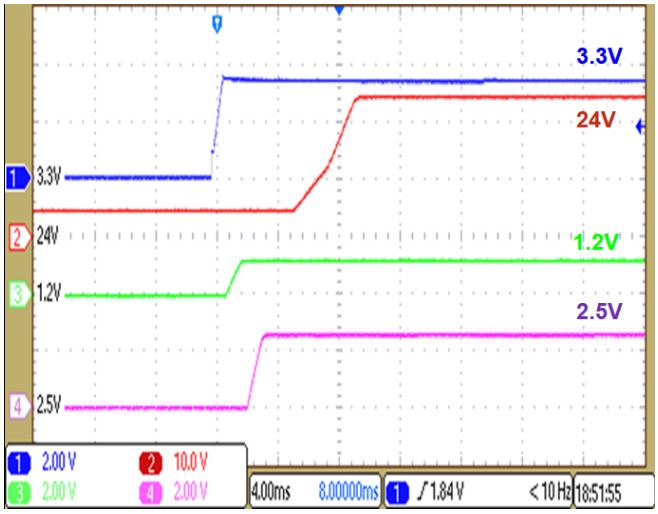


Figure 46. Power Down Sequencing by Power Good at No Load

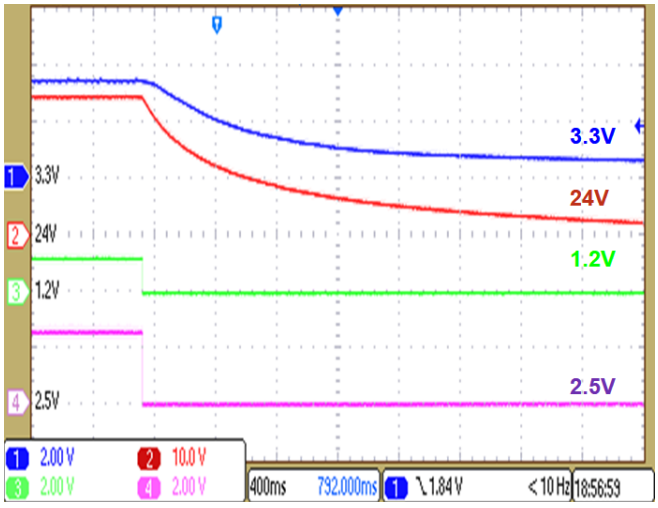


Figure 47. Power Up Sequencing by Power Good at Full Load

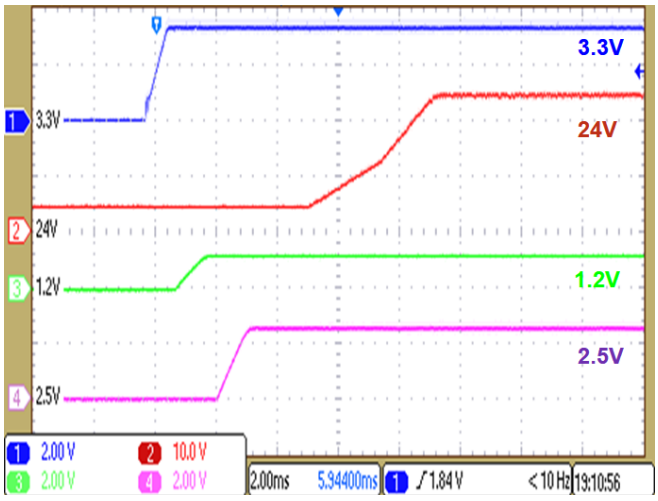
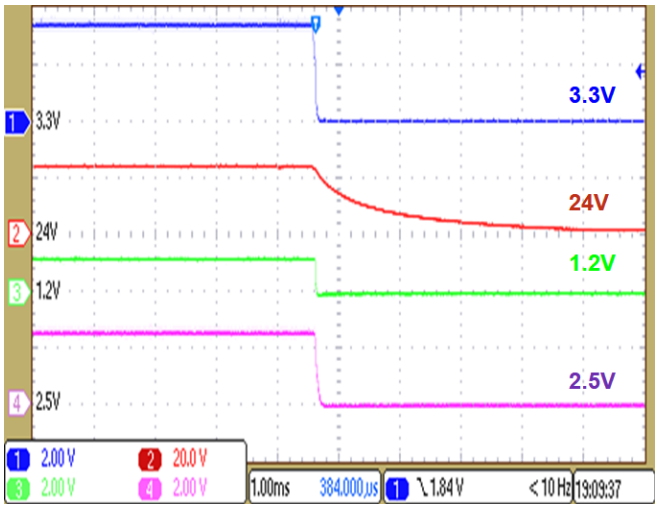


Figure 48. Power Down Sequencing by Power Good at Full Load



3.2.8 Step Response

Figure 49 through Figure 54 show the step response of the voltage rails where the load is varied from no load to full load and back to no load again.

Figure 49. Step Response of TLV62569 3.3-V Rail

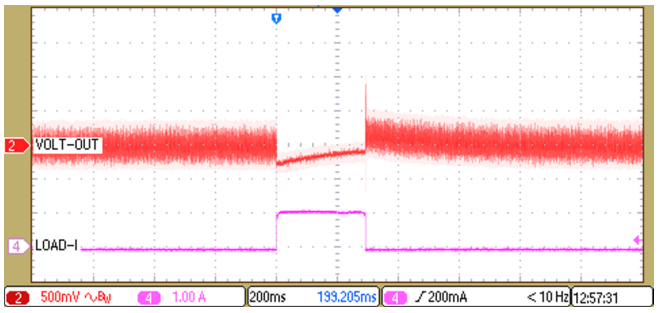
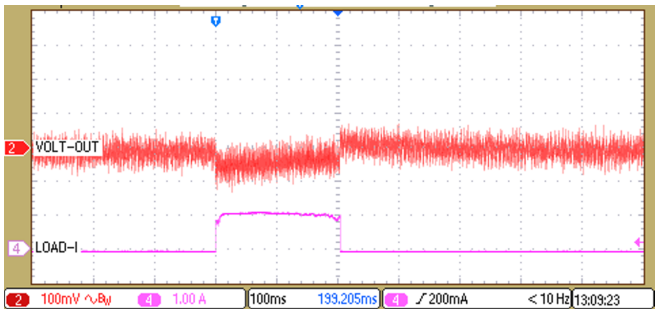


Figure 50. Step Response of TPS62821 2.5-V Rail



Copyright © 2019, Texas Instruments Incorporated

Figure 51. Step Response of TPS62821 1.2-V Rail

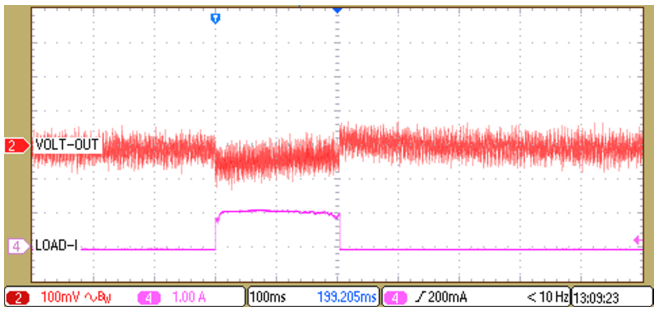


Figure 52. Step Response of TPS61170 8-V Rail

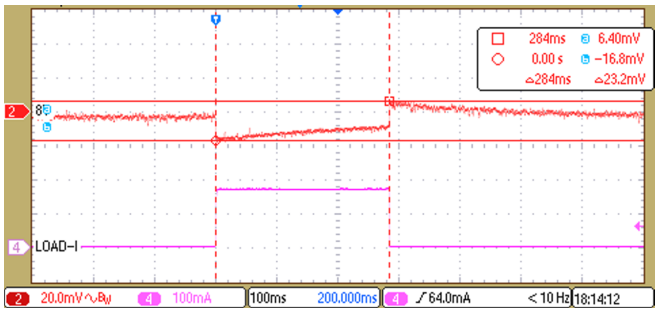


Figure 53. Step Response of TPS61170 10-V Rail

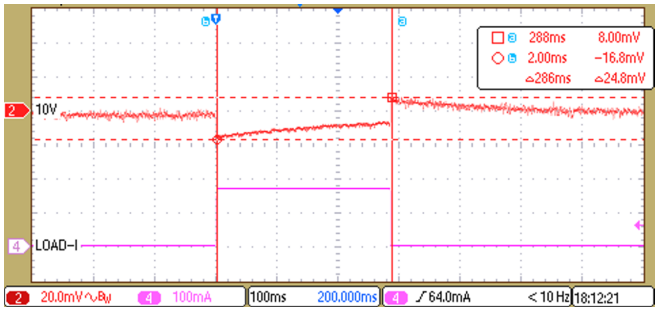
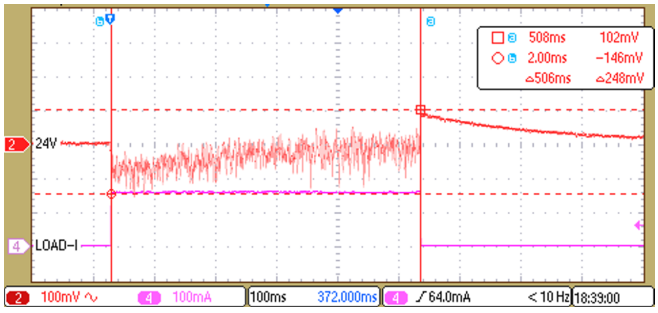


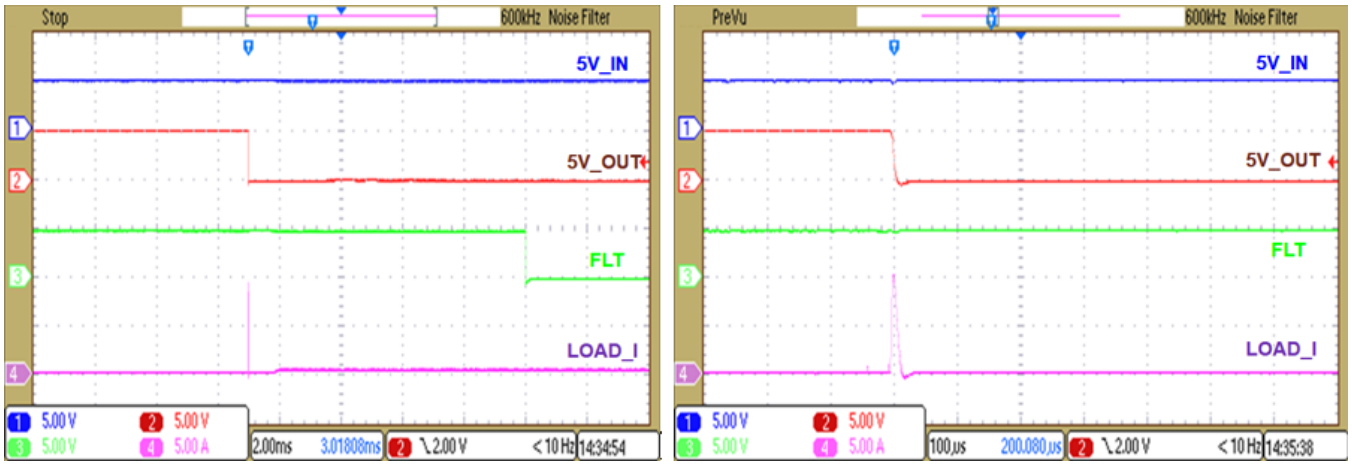
Figure 54. Step Response of TPS61170 24-V Rail



3.2.9 Short Circuit on 5-V, 250-mA Encoder Supply

The 5-V, 250-mA output TPS25200 device is shorted in Figure 55. The TPS25200 device limits the current to 320 mA in short-circuit conditions and the fault output is asserted low.

Figure 55. Short Circuit on 5-V, 250-mA Encoder Supply



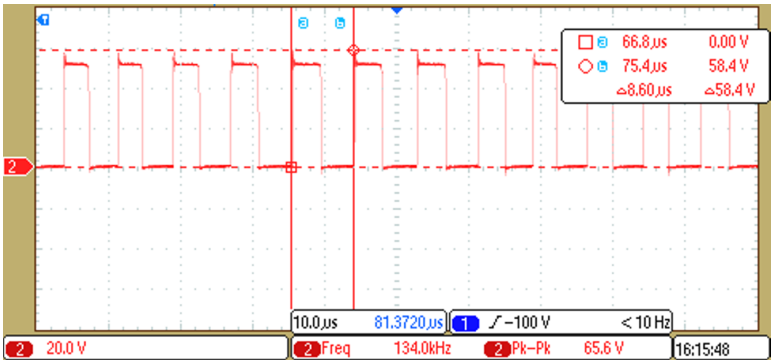
Copyright © 2019, Texas Instruments Incorporated

3.2.10 Functional Validation of LM5180

3.2.10.1 Switch Node Voltage at Full Load

Figure 56 shows the switch node waveform of the flyback converter LM5180. The maximum switch node voltage is 58.4 V which is within the 100-V rating of the LM5180 MOSFET.

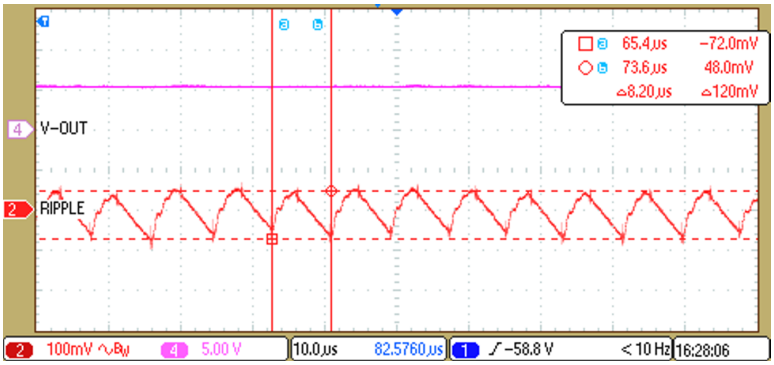
Figure 56. Switch Node of LM5180 at Full Load



3.2.10.2 Output Ripple on Isolated 5-V, 100-mA at Full Load

Figure 57 shows the output ripple on the 5-V, 100-mA rail generated by the flyback. The output is loaded at 100%. The maximum output ripple across the 5-V rail is 120 mV.

Figure 57. Output Ripple on Isolated 5-V Rail at Full Load

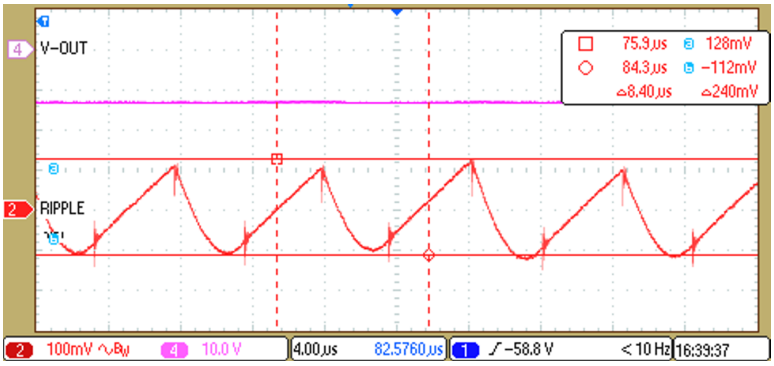


Copyright © 2019, Texas Instruments Incorporated

3.2.10.3 Output Ripple on -12 V at Full Load

Figure 58 shows the output ripple on the -12-V, 100-mA rail generated by the flyback. The output is loaded at 100%. The maximum output ripple across the -12-V rail is 240 mV.

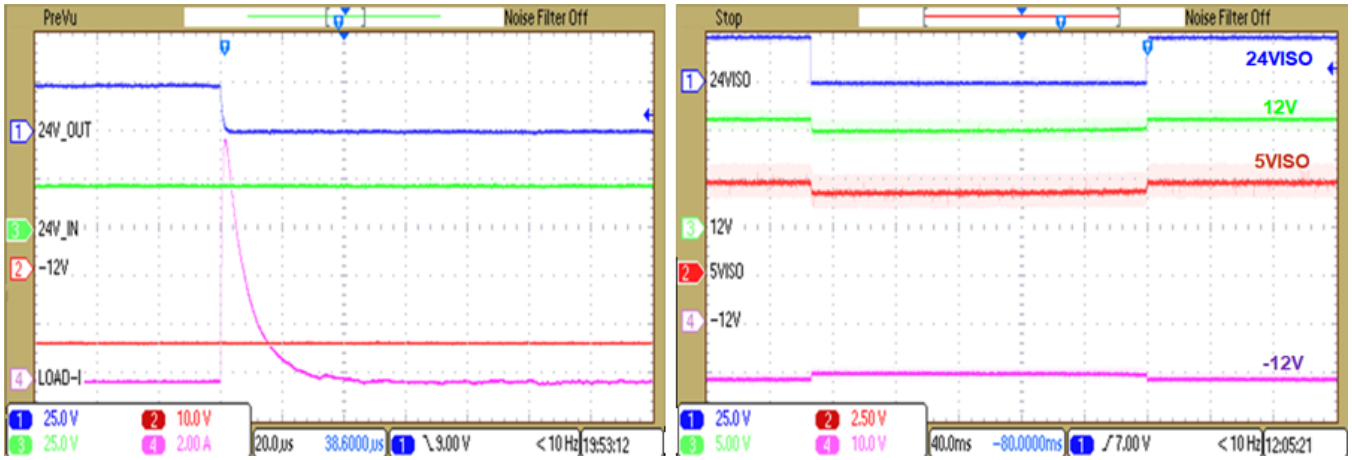
Figure 58. Output Ripple on -12-V Rail



3.2.10.4 Short Circuit on Flyback Output Rails

The 24-V rail of the flyback is shorted to observe the short-circuit behavior of all the voltage rails of the flyback. The LDO LP2951 generating the 24-V rail limits the current to 200 mA during short circuit. After the removal of the short condition, the voltage rail returns to their normal operating condition as the waveform on the right of Figure 59 shows.

Figure 59. Shorting 24-V, 100-mA Output Rail of Flyback



Copyright © 2019, Texas Instruments Incorporated

The 5-V, 8-V, and 10-V at 250-mA power supply to encoder is shorted in the following figures. After the removal of the short condition, the voltage rail returns to their normal operating condition as the waveform on the right of Figure 60, Figure 61, and Figure 62 show. The TPS62125 limits the current to 300 mA in short-circuit conditions.

Figure 60. Shorting 5-V, 250-mA Supply to Encoder

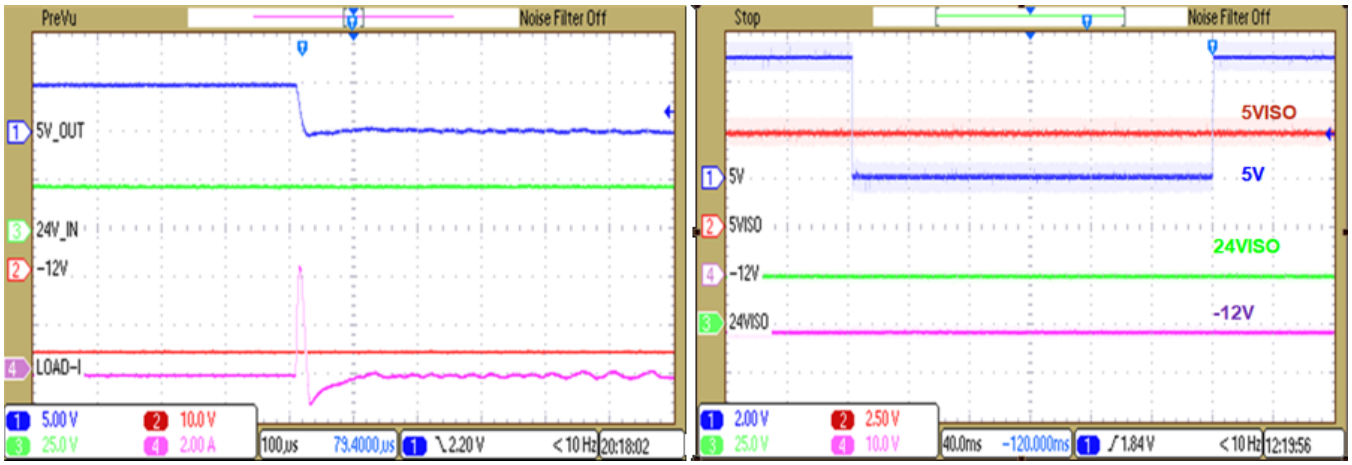


Figure 61. Shorting 8-V, 250-mA Supply to Encoder

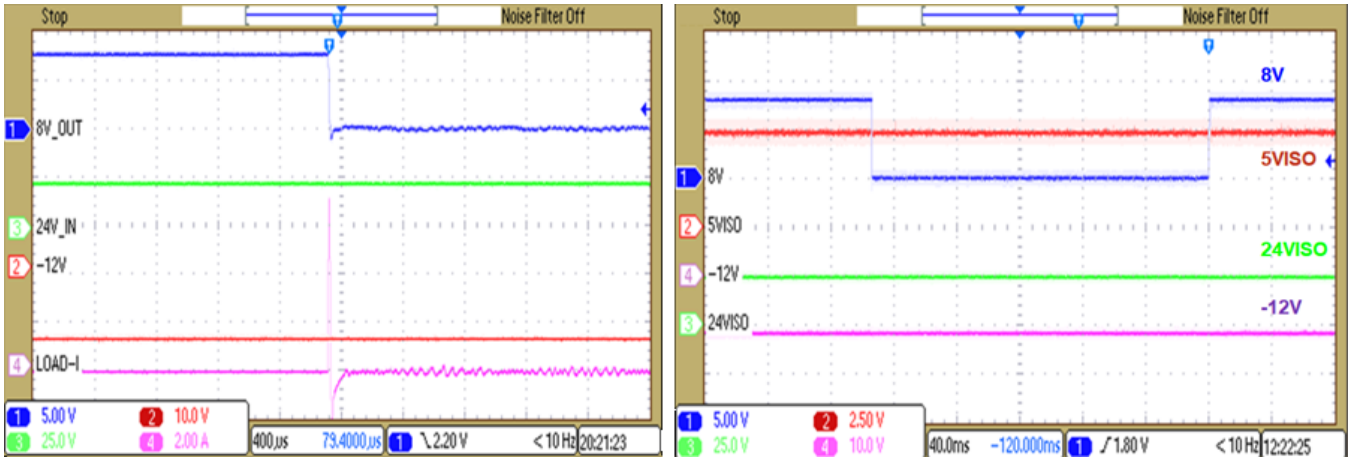
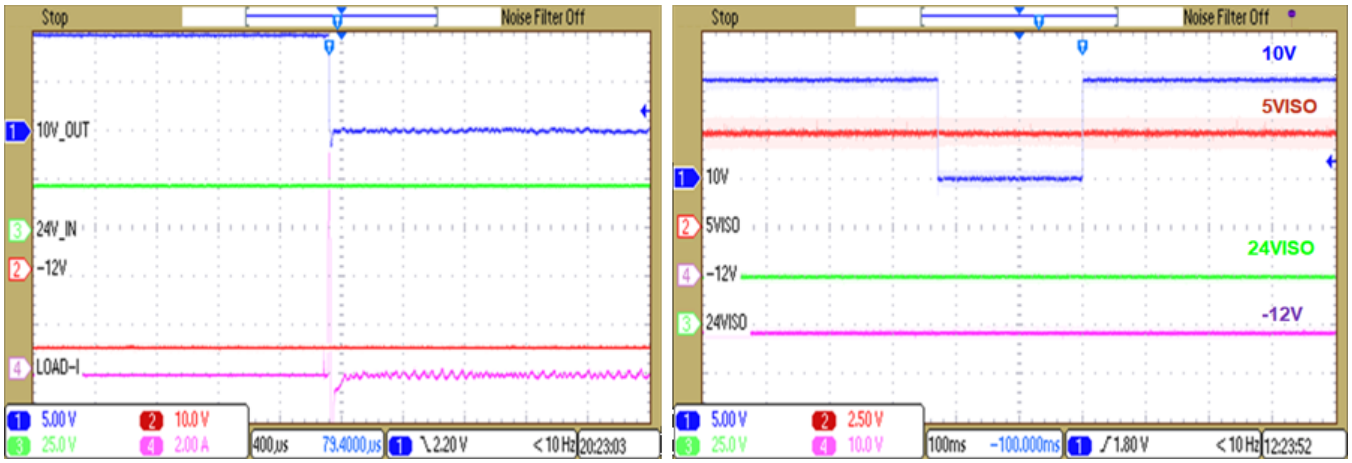


Figure 62. Shorting 10-V, 250-mA Supply to Encoder

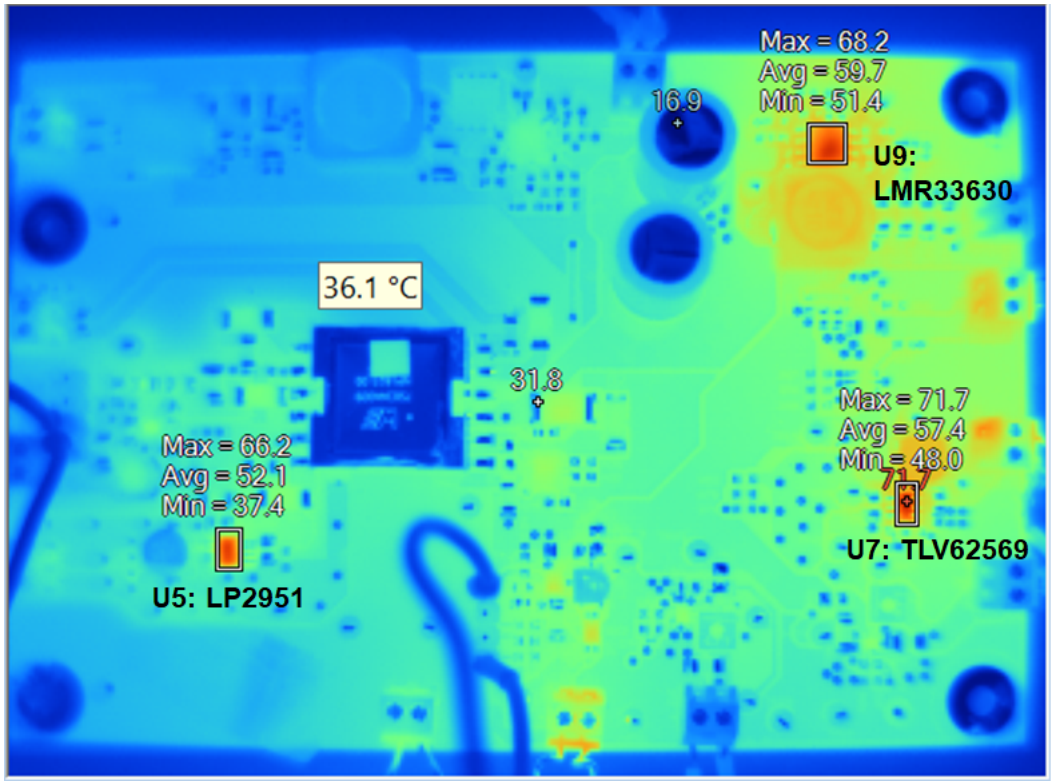


Copyright © 2019, Texas Instruments Incorporated

3.2.11 Thermal Image of the Board

Figure 63 shows the thermal image of the board when all the rails are loaded at 100% and ambient temperature is kept at 25°C. The board is kept in operation for 15 minutes to bring the package temperature rise to equilibrium.

Figure 63. TIDA-010009 Thermal Image



Copyright © 2019, Texas Instruments Incorporated

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010009.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010009.

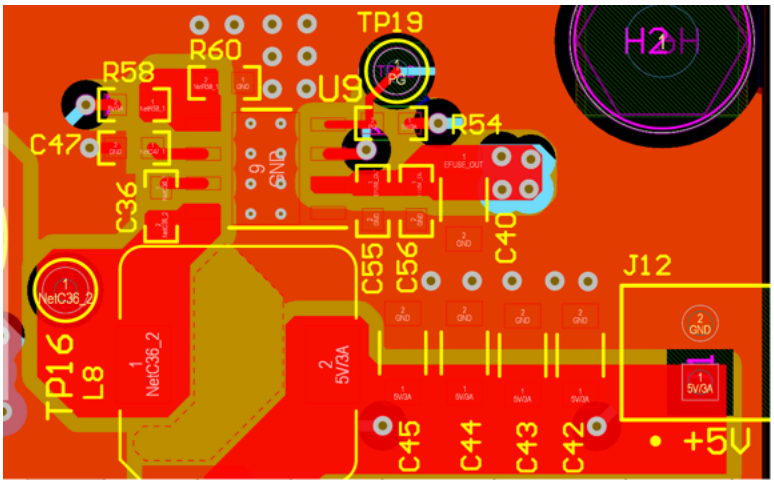
4.3 PCB Layout Recommendations

4.3.1 LMR33630

The layout guidelines are given for LMR33630 and shown in Figure 64. Similar guidelines apply to the DC/DC converters in the design.

- Place the input capacitors C55, C56 as close as possible to the VIN and GND terminals.
- Place bypass capacitor C47 for VCC close to the VCC pin. This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
- Connect the thermal pad to the ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator.
- Provide enough PCB area for proper heat sinking.

Figure 64. LMR33630 Layout

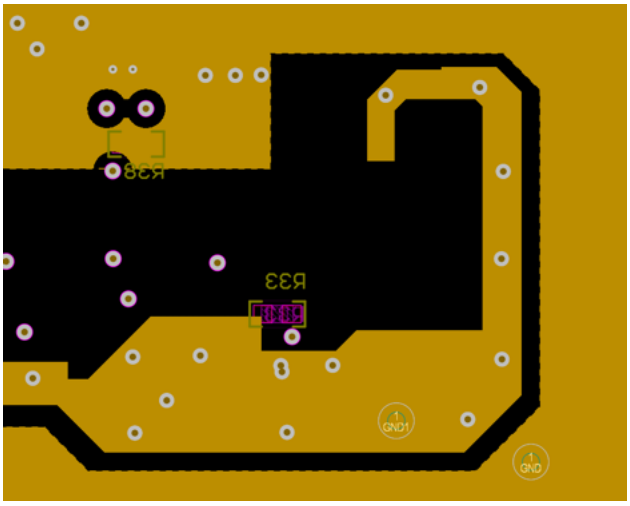


Copyright © 2019, Texas Instruments Incorporated

4.3.2 Isolation

Figure 65 depicts that a minimum distance of 40 mils is maintained between two grounds to maintain isolation.

Figure 65. Isolated Grounds Layout



4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010009.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010009.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010009.

5 Related Documentation

1. Texas Instruments, *400-V to 690-V AC Input, 50-W Flyback Isolated Power Supply Reference Design for Motor Drives*
2. Texas Instruments, *TPS2663x 60-V, 6-A Power Limiting, Surge Protection Industrial eFuse*
3. Texas Instruments, *LM5180 70-VIN PSR Flyback DC/DC Converter With 100-V, 1.5-A Integrated Power MOSFET*
4. Texas Instruments, *LMR33630 SIMPLE SWITCHER® 3.8-V to 36-V, 3-A Synchronous Step-Down Voltage Converter*

6 Trademarks

E2E, DCS-Control are trademarks of Texas Instruments.
SIMPLE SWITCHER is a registered trademark of Texas Instruments.
Altium Designer is a registered trademark of Altium LLC or its affiliated companies.
All other trademarks are the property of their respective owners.

7 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

Copyright © 2019, Texas Instruments Incorporated

8 About the Authors

Vaibhavi Shanbhag is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions with a focus on Motor Drive segment within Industrial Systems. Vaibhavi received her bachelor of engineering in Electrical and Electronics from BITS Pilani, Goa campus.

Aishwarya Bhatnagar is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems. Aishwarya earned her bachelor of technology in electronics and communication engineering from MNNIT, Allahabad.

Copyright © 2019, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated