

# TI Designs: TIDA-010013

## RGB to OLDI/LVDS Display Bridge Reference Design for Sitara™ Processors



### Description

Higher resolution displays are now in larger demand than ever before. This results in a higher pixel clock which can lead to challenges such as high EMI emission and noise immunity. As a result, the video interface now transitions from a traditional RGB to LVDS video interface. As microprocessors with an integrated graphics unit may output single-ended RGB video data only, this reference design demonstrates the simplicity of converting RGB to LVDS.

### Resources

<a href="#">TIDA-010013</a>	Design Folder
<a href="#">SN65LVDS93B</a>	Product Folder
<a href="#">TL431</a>	Product Folder



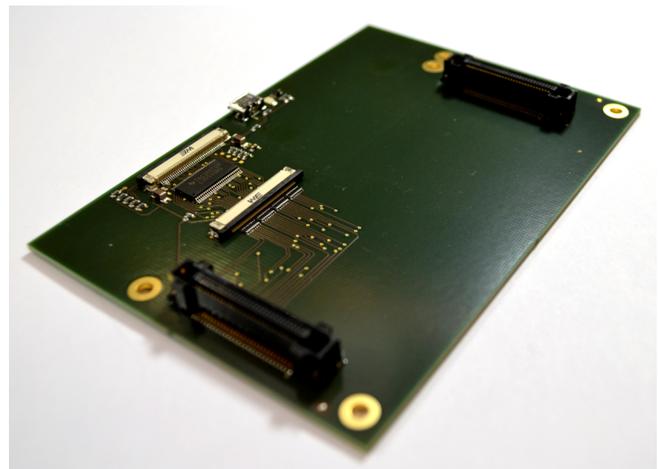
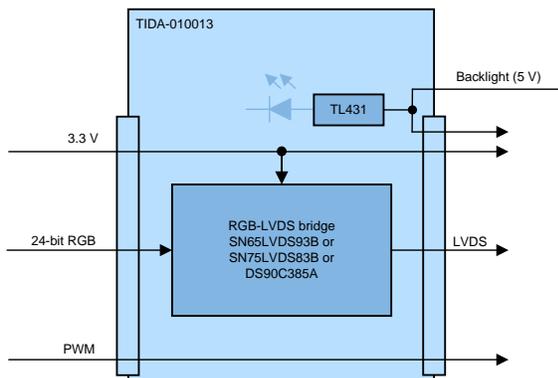
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### Features

- Compact 24-bit RGB to open LVDS display interface (OLDI) or LVDS interface
- Supports *AM335x Starter Kit* and *AM572x Evaluation Module*
- High resolution 10.1-inch wide super video graphics array (WSVGA) LCD display module (1024×600 pixel)
- Display brightness control by Sitara

### Applications

- [Panel PLC](#)
- [Portable Monitor](#)
- [Industrial Robot Teach Pendant](#)
- [Logistics Robot Teach Pendant](#)



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## 1 System Description

The solution proposed is applicable when the video source interface (for example, video processor) is incompatible with the video sink interface (for example, display). An example is to connect a AM335x or AM572x Sitara microprocessor with 24-bit single-ended LVCMOS outputs to an LCD with differential LVDS input. Dedicated integrated circuits are available for this purpose, such as the SN65LVDS93B, SN75LVDS83B, or the DS90C385A, which are investigated in this reference design. The SN75LVDS83B video bridge supports a pixel clock of up to 135 MHz, which translates to a super-extended graphics array (SXGA) of 1280×1024 pixel display resolution at a frame rate of 75 Hz.

The video source interface, the video bridge, and the video sink interface use the same voltage to power up or power down at the same time to make data buffers redundant. In addition, the voltage level of the three components are kept equal at the benefit of signal integrity.

The backlight power is not the focus of this design and is delivered from an external power supply unit. A low voltage indicator is added to easily observe the correct voltage level. Inside the LCD module, this constant voltage is input to a power supply with constant output current to precisely set the LED brightness. An additional PWM signal provided to the LCD module controls the duty cycle of the LED current, which directly sets the backlight brightness.

Another option is to use an LCD glass instead of an LCD module, which exposes the terminals of the backlight LED strings directly to the outside. All backlight power generation is moved from the LCD to the main board with same functionality as previously shown.

The focus of this reference design is the video signal conversion. It is shown that only the video bridge and a few passive components are required to accomplish this task.

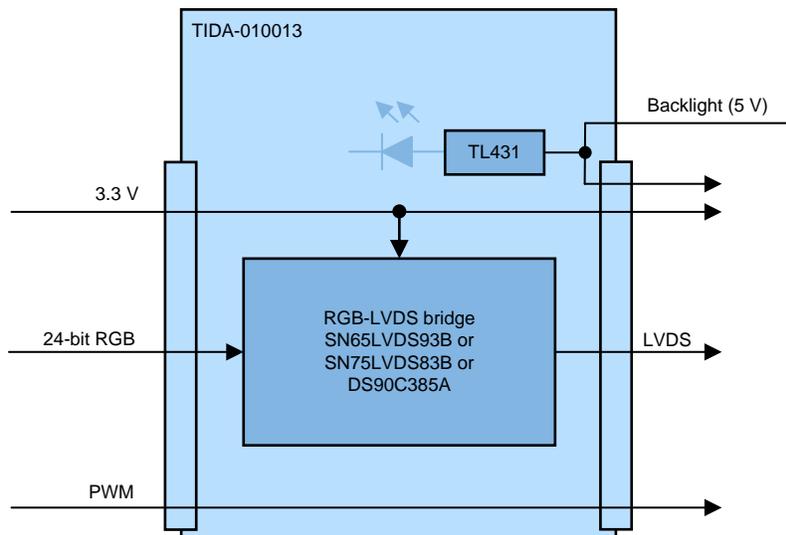
### 1.1 Key System Specifications

**Table 1. Key System Specifications**

PARAMETER	SPECIFICATIONS	DETAILS
Video input	Up to 24-bit RGB (CMOS)	<a href="#">Section 2.4.1</a>
Video output	4 LVDS pairs (3 data + 1 clock)	<a href="#">Section 2.4.1</a>
Pixel clock	Up to 135 MHz (SN75LVDS83B)	<a href="#">Section 2.3.1.2</a>
Power consumption (LVDS bridge)	130 mW at 3.3 V	<a href="#">Section 3.3.2.1</a>
LCD backlight power consumption (full brightness)	4.6 W at 7 V	<a href="#">Section 3.3.2.2</a>
Operating temperature	0°C to +50°C	<a href="#">Section 2.4.5</a>
Form Factor	122 mm × 87 mm	<a href="#">Section 3.1.3</a>

## 2 System Overview

### 2.1 Block Diagram



**Figure 1. TIDA-010013 Block Diagram**

### 2.2 Design Considerations

This design solely serves the purpose of resolving interface incompatibilities of the video source and video sink. With a careful board layout, the video port becomes more robust with lower EMI emission at the same time. This is accomplished by minimizing the trace length of the single-ended 24-bit RGB video interface. The layout for this design is not able to follow this rule due to mechanical constraints as two Sitara platforms (AM335x and AM572x) are supported. The focus is more on the functionality than layout optimization. See the video bridge data sheets for layout considerations.

The video source and video are assumed in close proximity, as seen in a panel PLC, for instance. In applications where the video signal must overcome longer distances, for example in a remote display application, dedicated transmitter and receiver devices are available. The FPD-III link video protocol serves this purpose, which is able to transmit the video signal and an auxiliary bidirectional channel over up to 15 m with a pixel clock of up to 170 MHz. See the Texas Instruments Web page ([www.ti.com](http://www.ti.com)) for more information about FPD-III link technology.

### 2.3 Highlighted Products

#### 2.3.1 SN65LVDS93B, SN65LVDS83B, or DS90C385A

The SN65LVDS93B, SN75LVDS83B, and DS90C385A have been tested with this design. Only one part is used at a time. These three parts have the same functions and are pin-to-pin compatible.

##### 2.3.1.1 SN65LVDS93B

The SN65LVDS93B LVDS SerDes (serializer, deserializer) transmitter contains four 7-bit parallel load serial-out shift registers, a 7 × clock synthesizer, and five low-voltage differential signaling (LVDS) drivers in a single integrated circuit. These functions allow synchronous transmission of 28 bits of single-ended LVTTTL data over five balanced-pair conductors.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected through the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS93B device requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the users. The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input and the possible use of the shutdown, clear (SHTDN) signal. SHTDN is an active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers at a low level.

The input pixel clock range is 10 MHz to 85 MHz.

The SN65LVDS93B is characterized for operation over ambient air temperatures of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### 2.3.1.2 SN75LVDS83B

The SN75LVDS83B shares the same functionality, but has a more narrow operation over ambient air temperatures of  $-10^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  and a higher pixel clock frequency of up to 135 MHz, compared to the SN65LVDS93B.

### 2.3.1.3 DS90C385A

The DS90C385A transmitter converts 28 bits of LVCMOS, LVTTTL data into four low-voltage differential signaling (LVDS) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over the fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 87.5 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 612.5Mbps per LVDS data channel. Using a 87.5-MHz clock, the data throughput is 306.25Mbytes/sec. This transmitter can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge or falling edge strobe transmitter will interoperate with a falling edge strobe FPDLink receiver without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces with added spread spectrum clocking support.

### 2.3.2 TL431

The TL431 is a three-terminal adjustable shunt regulator, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between  $V_{\text{REF}}$  (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of  $0.2\ \Omega$ . Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

The TL431 is offered in three grades, with initial tolerances (at  $25^{\circ}\text{C}$ ) of 0.5%, 1%, and 2%, for the B, A, and standard grade, respectively. In addition, low output drift versus temperature ensures good stability over the entire temperature range.

The TL431 variant used in this design is characterized for operation from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## 2.4 System Design Theory

### 2.4.1 LVDS Video Bridge

The main component of the design is the video bridge, U1. It converts the 24-bit wide RGB video signal, including the control signal HSYNC, VSYNC, DE, and the pixel clock (all single-ended LVCMOS) to an LVDS signal with four signals and one clock lane. The LVDS output clock is  $7\times$  the incoming pixel clock. The LVDS video output consists of four data lanes and one clock lane. See [Figure 2](#) for a functional diagram of the SN65LVDS93B, as an example.

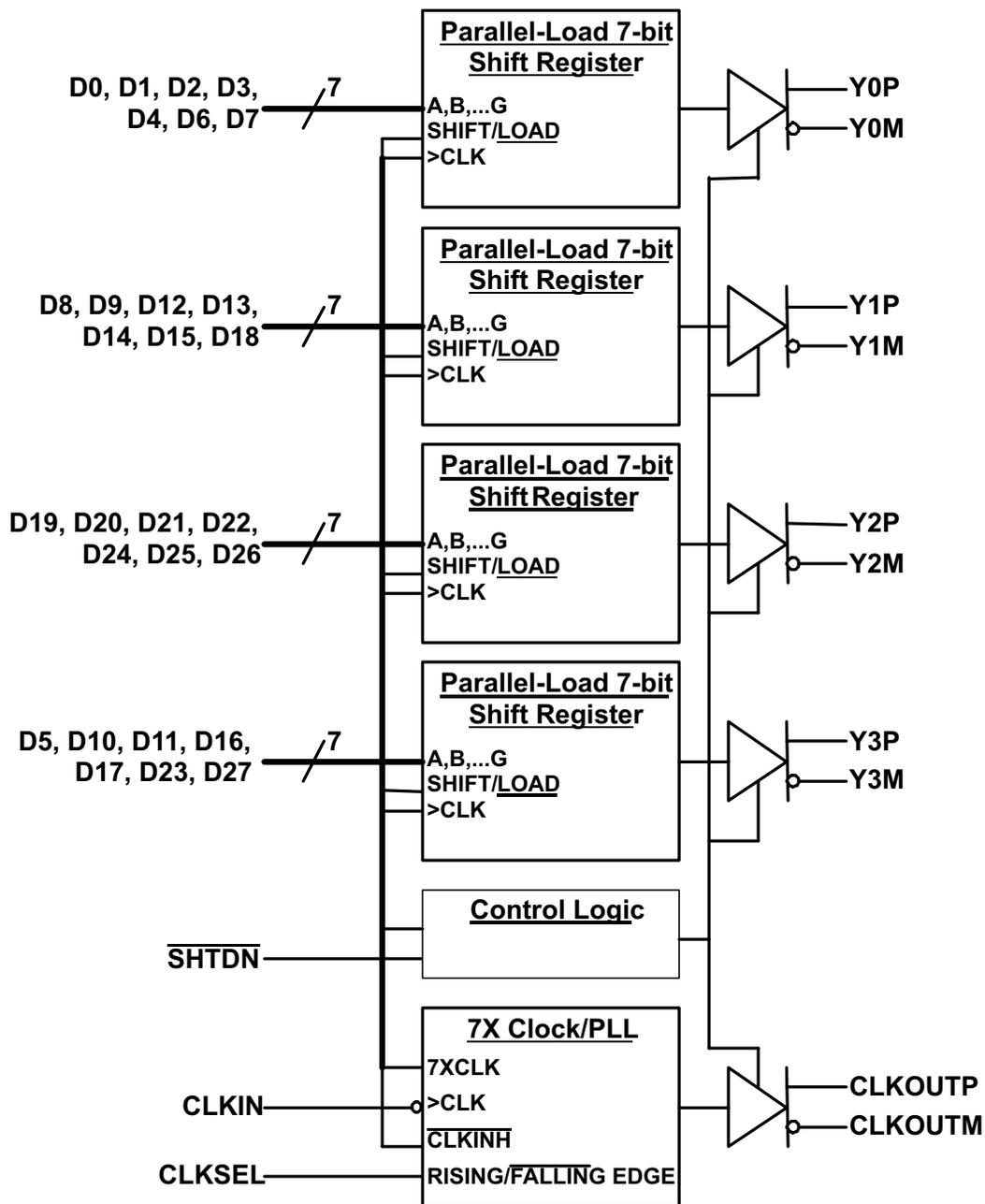
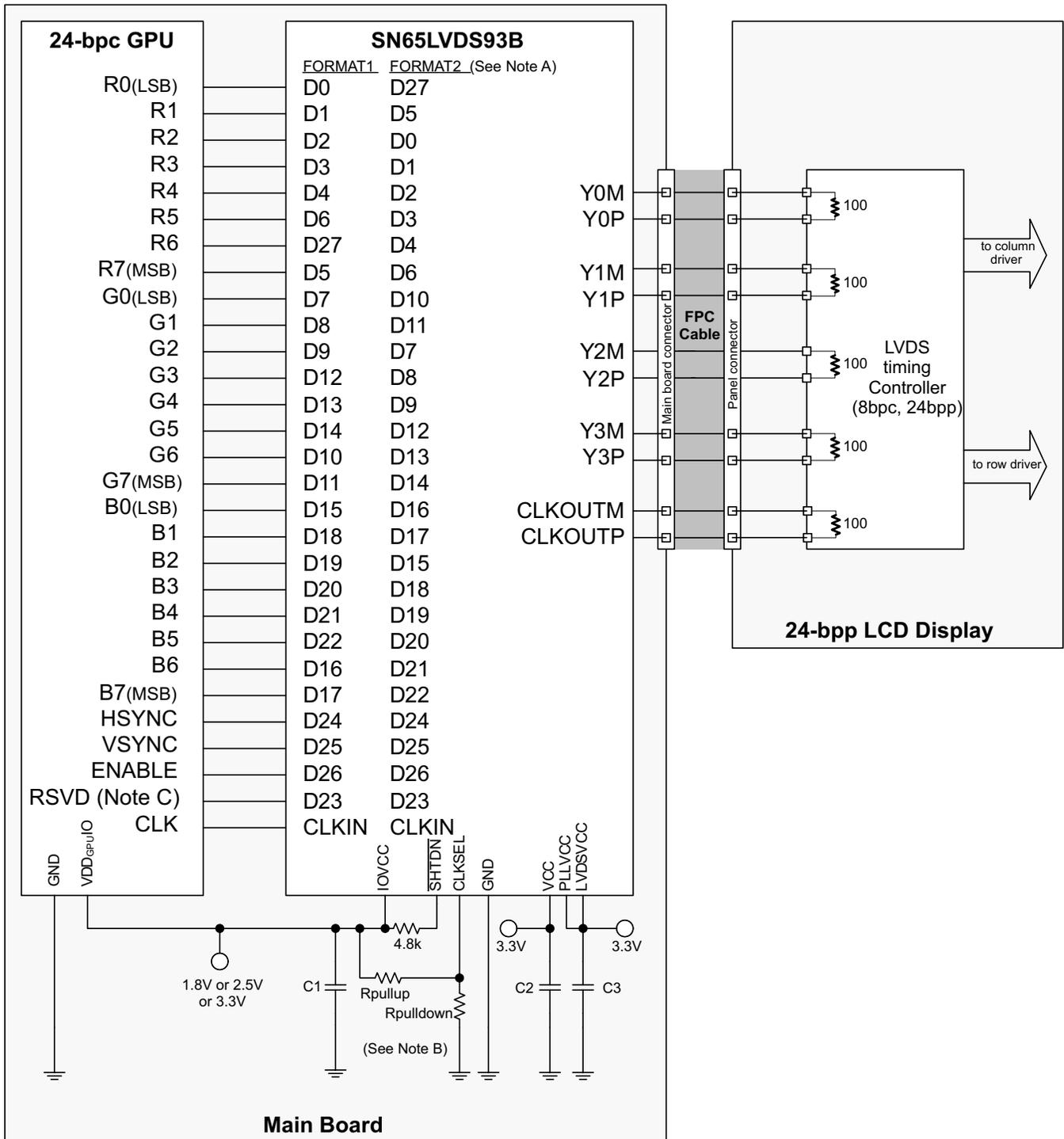


Figure 2. SN65LVDS93B Functional Block Diagram

The color mapping of the 24-bit RGB signal to the LCD\_DATA terminals for the AM335x Sitara family is not intuitive. Please refer to erratum *LCD: Color Assignments of LCD\_DATA Terminals* in the [AM335x Sitara™ Processors Silicon Revisions 2.1, 2.0, 1.0 Silicon Errata](#) document. The color mapping of the AM572x Sitara processor is straight forward. See the *DSS Output Data Signals to RGB Color Components Mapping* table in the [AM572x Sitara Processors Technical Reference Manual](#). Figure 3 shows the mapping of the RGB and control signals to the input of the video bridge.



Note A. Connection format 1 is used in this design (see also [Section 3.1.3](#)).

Note B. Data bits are latched on the falling pixel clock edge (CLKSEL = LOW).

**Figure 3. Sitora™ to Video Bridge Signal Mapping**

## 2.4.2 Power Supply

The 3.3-V power rail for the video bridge is provided by the Sitara development platforms. This keeps the design simple (no additional supply rail generation and data buffers) and close to the real application. The development platforms are capable of supplying the additional power for the video bridge and the digital part of the LCD. See [Section 3.3.2](#) for power consumption measurements.

The backlight power for the LCD is supplied from an external power supply. The LCD accepts an input range of 4 V to 7.3 V. A standard micro-USB connector allows for simple voltage delivery of 5 V. In addition, no overvoltage and reverse polarity protection is implemented as it is common sense that a micro-USB delivers 5 V with a standardized power connection. The indicator LED, D1, lights if the voltage is 4.6 V and above. This is useful if the power source cannot deliver the required 1 A as standard USB ports may deliver up to 0.5 A only. A common wall plug charger with USB output usually supplies more than 1 A.

## 2.4.3 Brightness Control

The LCD module accepts a PWM at signal LED\_PWM to control the backlight brightness. The allowed frequency range of the PWM is from 500 Hz to 20 kHz with a duty cycle range of 10% to 100%.

## 2.4.4 LCD Control Pins

The LCD module has 8 control pins. [Table 2](#) shows their meanings and the modes selected.

**Table 2. LCD Control Pins Setting**

SIGNAL	DESCRIPTION	SELECTED MODE
BIST	Built-in self test	Deasserted (LOW)
LED_EN	Backlight LED on or off	Asserted (HIGH)
LED_PWM	Backlight LED control	PWM brightness
STBYB	LCD standby	Deasserted (HIGH)
RESET	LCD reset	Deasserted (HIGH)
SHLR	Gate driver left or right scan	Normal scan (HIGH)
UPDN	Gate driver up or down scan	Normal scan (LOW)
INSEL	Data input format	8-bit input (LOW)

## 2.4.5 Operating Temperature

The limiting factor in the system in terms of operating temperature is the LCD with an operating range of 0°C to +50°C. The industrial version of the video bridge, the SN65LVDS93B, can operate in a temperature range of -40°C to +85°C.

## 3 Hardware, Software, Testing Requirements, and Test Results

### 3.1 Hardware

This design requires a video source and a video sink to operate. The video source is provided by a Sitara processor. The *AM3558 Starter Kit* and the *AM572X Evaluation Module* is supported by this design from a mechanical point of view. Other Sitara subfamilies are supported electrically only and can be blue-wired.

#### 3.1.1 AM335x Starter Kit

The *AM335x Starter Kit* provides a stable and affordable platform to quickly start evaluation of Sitara Arm® Cortex®-A8 AM335x Processors (AM3351, AM3352, AM3354, AM3356, AM3358) and accelerate development for smart appliance, industrial, and networking applications. It is a low-cost development platform based on the ARM Cortex-A8 processor that is integrated with options such as Dual Gigabit Ethernet, DDR3, and LCD touch screen.

#### 3.1.2 AM572x Evaluation Module

The *AM572x Evaluation Module* provides an affordable platform to quickly start evaluation of Sitara ARM® Cortex®-A15 AM57x Processors (AM5728, AM5726, AM5718, AM5716) and accelerate development for HMI, machine vision, networking, medical imaging, and many other industrial applications. It is a development platform based on the dual ARM Cortex-A15, dual C66x DSP processor that is integrated with lots of connectivity such as PCIe, SATA, HDMI, USB 3.0, USB 2.0, Dual Gigabit Ethernet, and more.

The *AM572x Evaluation Module* also integrates video and 3D, and 2D graphics acceleration, as well as a dual-core Programmable Real-time Unit (PRU) and dual ARM Cortex-M4 cores.

#### 3.1.3 Reference Design

The reference design takes the RGB video interface signals from the Sitara development platforms. The *AM335x Starter Kit* provides the video port over a 40-pin FFC, which connects to J1 of the reference design. The *AM572x Evaluation Module* provides the video port over J18, a 30x2 pin connector designed for high-speed signals (Hirose FX-18 series). J17 is introduced for mechanical stability reasons only.

The RGB video signal is connected to the video bridge in a way that the generated LVDS data are understandable by the LCD. The connection follows the more common *Format 1*, which maps the 2 MSB of each color to the LVDS output Y3. With the pixel clock of 51.2 MHz, the LVDS clock is seven times higher, 358.4 MHz. This allows to map 24+3 incoming signals to 4 LVDS outgoing signals.

The LVDS signal is provided to the LCD over FFC connector J2.

The backlight power is provided over the micro-USB connector J3 and is directly passed to J3 to supply the LCD. A indicator LED, D1, is introduced to visually indicate the correct voltage. If the voltage is 4.6 V, the shunt regulator reference voltage pin U2.3 is 2.5 V. At this voltage, U2 starts to conduct current from the cathode to the anode and D1 lights.

The board width of 122 mm is derived from the width of the *AM335x Starter Kit*. The board height of 87 mm is for no particular reason, but to take measurements at the video bridge while the *AM572x Evaluation Module* is plugged on top of the reference design.

#### 3.1.4 Display

The display used in this design is the 10.1-inch TFT color LCD module NHD-10.1-1024600AF-LSXV# from Newhaven Display®. It features a 1024x600 pixel resolution and runs at a pixel clock of about 51.2 MHz. The LCD uses the HX8282-A01 from Himax as a source driver. The HX8282-A01 data sheet provides the display timings, which were adopted in this design. Refer to [HX8282-A01 TXT LCD Source Driver with LVDS TCONF Data Sheet](#) for timings.

### 3.2 Software

This design uses standard software components available from the Texas Instruments Web page ([www.ti.com](http://www.ti.com)). Both development platforms provide a bootable SD-card image and the AM335x and AM57xx Linux SDK Essentials required to operate the reference design.

### 3.2.1 Software Change Procedure

The following sections describe the software setup for the SD-card including the changes required in the device tree to support the display used in this reference design.

#### 3.2.1.1 Create a Bootable SD-Card

Starting from the processor SDK for [AM335x](#) or [AM572x](#) Web page, click *Get Software* for the latest PROCESSOR-SDK-LINUX-<AMxxxx> software package. Under the *AMxxxx Linux SDK SD Card Creation* section, download the <amxxxx>-evm-linux-<linux-sdk-version>.img.zip file. Unzip this bootable image and flash it to an SD-card.

#### 3.2.1.2 Linux SDK Essentials

Download the file *ti-processor-sdk-linux-<amxxxx>-evm-<linux-SDK-version>-Linux-x86-Install.bin* and install it on a Linux host machine.

In the following sections, the *SD root directory* is `~/ti-processor-sdk-linux-<amxxxx>-evm-<linux-SDK-version>`. The *device tree source directory* is `<SDK root directory>/board-support/linux.../arch/arm/boot/dts/`.

#### 3.2.1.3 Device Tree Changes

The *AM335x Starter Kit* is shipped with a WQVGA (480x273 pixel) LCD and the *AM572x Evaluation Module* with a WVGA (800x600 pixel) LCD. The display used in this reference design is a WSVGA (1024x600 pixel) LCD. The timing of the video interface must be changed to support the new resolution. This is accomplished by changing the device tree configuration of the Sitara microprocessor. The video bridge itself is transparent to the system and does not required any software support.

Open in the device tree source directory the file *am335x-evmsk.dts*(AM335x) or *am57xx-evm-common.dtsi* (AM572x) with a text editor and change the timings to run the WSVGA display:

```
1024x600 {
    clock-frequency = <51206400>;
    hactive = <1024>;
    vactive = <600>;
    hfront-porch = <160>;
    hback-porch = <160>;
    hsync-len = <10>;
    vfront-porch = <12>;
    vback-porch = <23>;
    vsync-len = <10>;
    hsync-active = <0>;
    vsync-active = <0>;
    de-active = <1>;          /* AM572x only */
    pixelclk-active=<1>;     /* AM572X only */
}
}
```

Go to the SDK root directory and run the command:

```
> make linux.dtb
```

This will recompile the device tree. As a result, the recompiled file *am335x-evmsk.dtb* (AM335x) or *am57xx-evm-reva3.dtb* (AM572x) is available in the device tree source directory including the new display timings. Copy and replace files on the SD-card (partition roots, directory boot) as follows:

- AM335x: *am335x-evmsk.dtb* -> *devicetree-zImage-am335x-evmsk.dtb*
- AM572x: *am572x-evm-reva3.dtb* -> *devicetree-ulmage-am572x-evm-reva3.dtb*

Insert the SD-card to the *AM335x Starter Kit*, or *AM572x Evaluation Module*. After power up, the display shows the *Matrix App Launcher* application.

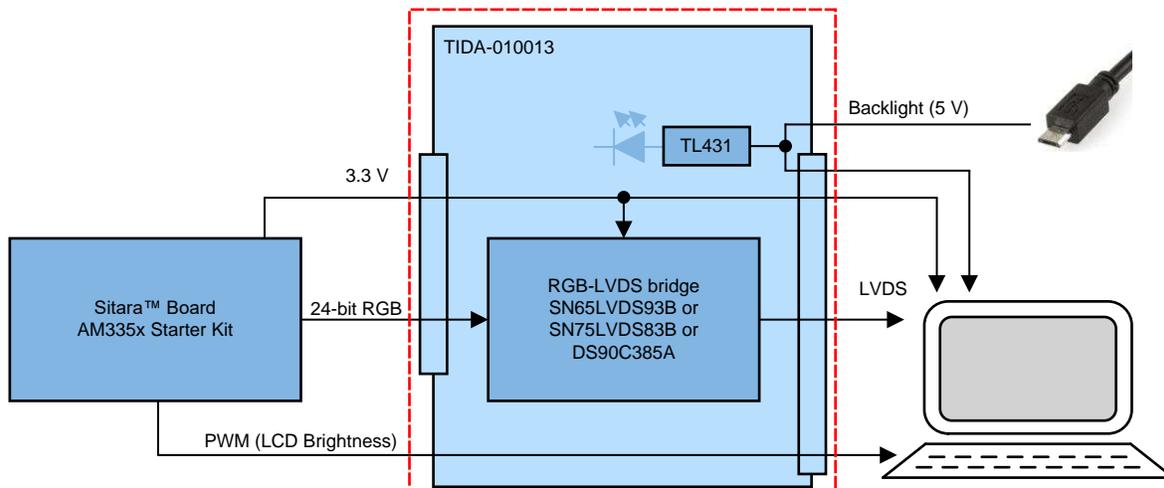
### 3.3 Testing and Results

#### 3.3.1 Test Setup

The hardware is inserted between the video source (Sitara platform) and video sink (display). The following sections describe the setup for both the *AM335x Starter Kit* and the *AM572x Evaluation Module*.

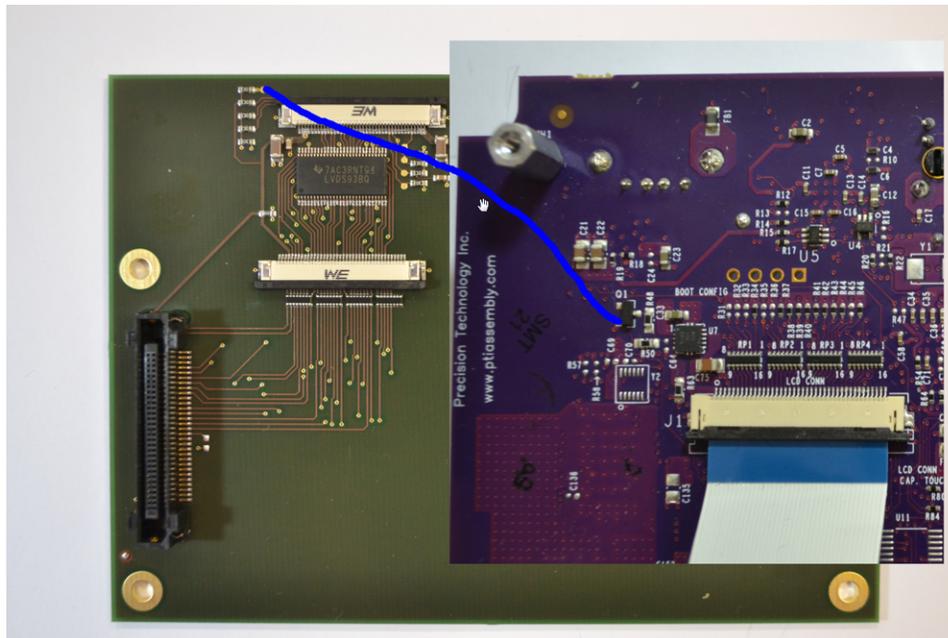
##### 3.3.1.1 AM335x Starter Kit

The *AM335x Starter Kit* includes a 40-pin FFC connector at the bottom, which connects to J1 of the reference design. The LVDS output video signal is available at J2 where the display connects seamlessly. See [Figure 4](#) for the complete setup.



**Figure 4. Hardware Setup With AM335x Starter Kit**

Full LCD brightness is selected by the pullup resistor R4. If brightness control is required, additional blue-wiring must be performed since the FFC video connector does not provide such a signal. Solder a wire between the gate of transistor Q1 of the *AM335x Starter Kit* and testpoint *PWM* close to R4 of the reference design (see [Figure 5](#)).



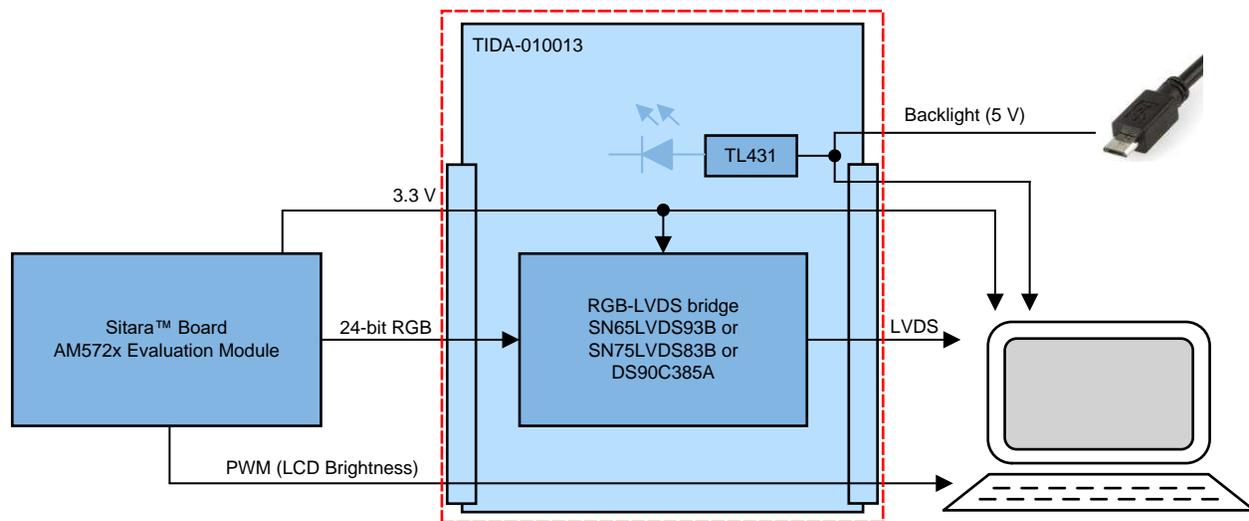
**Figure 5. Blue-Wiring for AM335x Brightness Control**

For the display used in this reference design, the backlight power is generated by the LCD module and controlled by an externally-provided PWM. For the original LCD, the (PWM controlled) backlight power is generated on the *AM335x Starter Kit* and connected to the LCD over the FFC. This means the PWM signal is available and already considered in the device tree and can be used just the same way as with the original LCD.

When the two boards and the LCD are connected, provide +5 V to the reference design via the micro-USB connector and power up the *AM335x Starter Kit* afterwards. The *Matrix App Launcher* application is displayed after around 1 minute.

### 3.3.1.2 AM572x Evaluation Module

The *AM572x Evaluation Module* consists of two boards: The processor board and the LCD board with a 7-inch wide video graphics array (WVGA) LCD with RGB interface. The LCD board is fully replaced by the reference design and the display. The processor board connectors P17 and P18 connect to J17 and J18 of the reference design. The LVDS output video signal is available at J2 where the display connects seamlessly. See [Figure 6](#) for the complete setup. The PWM signal for LCD backlight brightness can be provided by the AM572x high-resolution PWM output EHRPWM2. This peripheral is available from pin P18.44 of the AM572X processor board if R19 is populated (0  $\Omega$ ). For simplification reasons for the bringup-procedure, R19 remains unpopulated (full backlight brightness).



**Figure 6. Hardware Setup with AM572x Evaluation Module**

When the two boards and the LCD are connected, provide +5 V to the reference design via the micro-USB connector and power-up the *AM572x Evaluation Module* afterwards. The *Matrix App Launcher* application is displayed after around 1 minute.

### 3.3.2 Test Results

#### 3.3.2.1 Video Bridge Power Consumption

Table 3 shows the power consumption for the three video bridges with a 51.2-MHz pixel clock. During measurement, the Qt demo *Deform* was executed. This program is part of the standard SDK package for the Sitara platforms.

**Table 3. Current Consumption of LVDS Bridges**

VIDEO BRIDGE	CURRENT CONSUMPTION AT 3.3 V
SN65LVDS93B	39.5 mA
SN75LVDS83B	38.8 mA
DS90C385A	36.2 mA

The voltage drop over the 200-mΩ shunt resistor R12 was measured to obtain the current consumption data.

#### 3.3.2.2 LCD Backlight Power Consumption

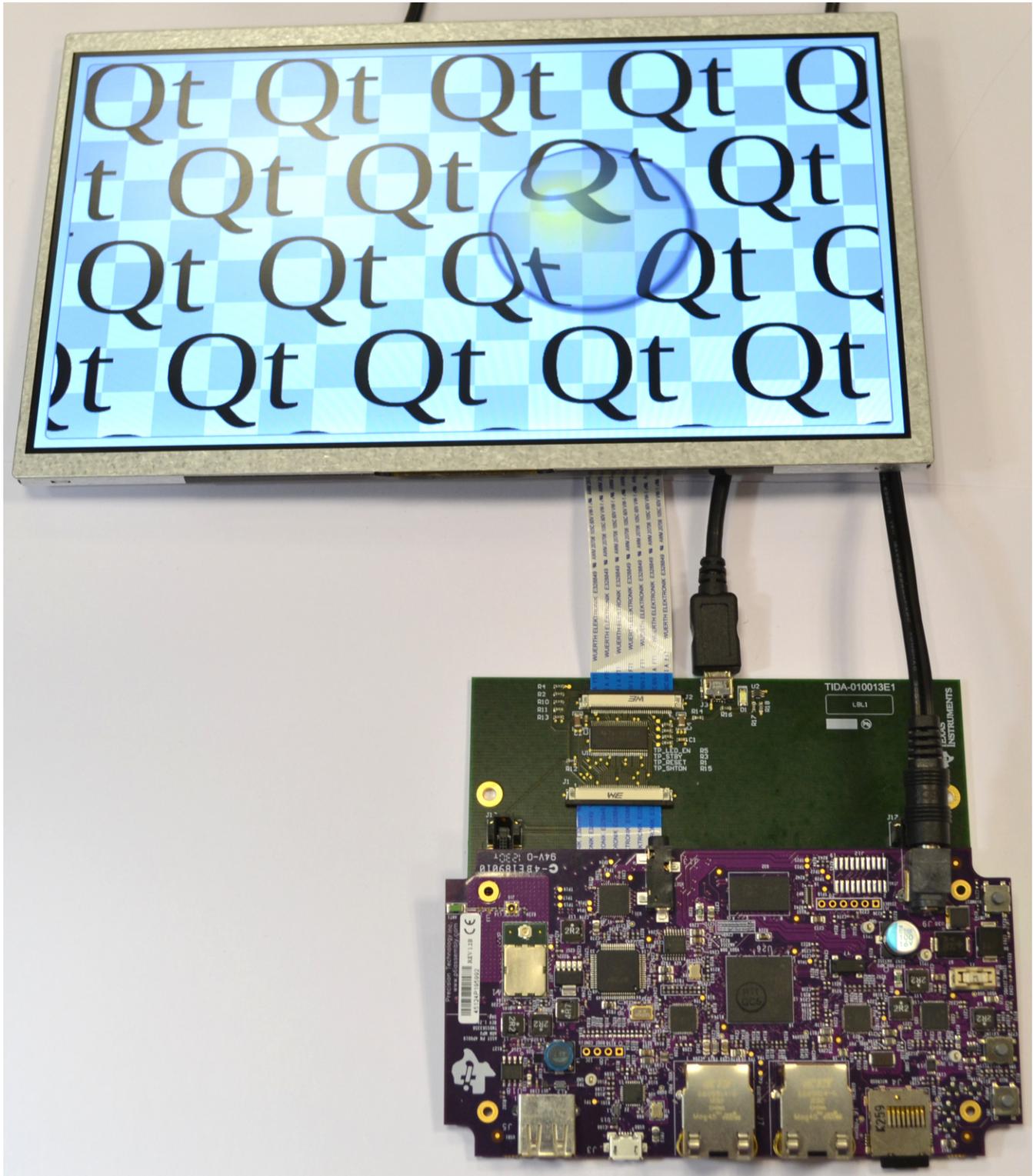
Shunt resistor R14 is used to measure the current consumption of the LCD backlight. At full brightness, a current of 980 mA is measured over the 200-mΩ shunt resistor R14. Standard USB ports may supply a current of up to 500 mA only. A wall plug power supply with more than 1 A is recommended. The nominal input voltage for the backlight is 7 V. The overall power consumption is 4.9 W at 5 V and 4.6 W at 7 V. TI recommends operating at the nominal voltage to keep the power consumption at an optimum. Higher voltages than 5 V can be supplied by a custom USB cable with an adjustable lab power supply as source.

#### CAUTION

The TIDA-010013 has no reverse polarity and overvoltage protection. A wrongly applied voltage via the USB connector may cause permanent damage to the LCD and reference design board.

**3.3.2.3 Lab Results**

Figure 7 shows the working setup with the AM335x Starter Kit with application *Deform* running on the processor.



**Figure 7. Running Setup With AM335x Starter Kit**

Figure 8 shows the setup with the AM572x Evaluation Module.

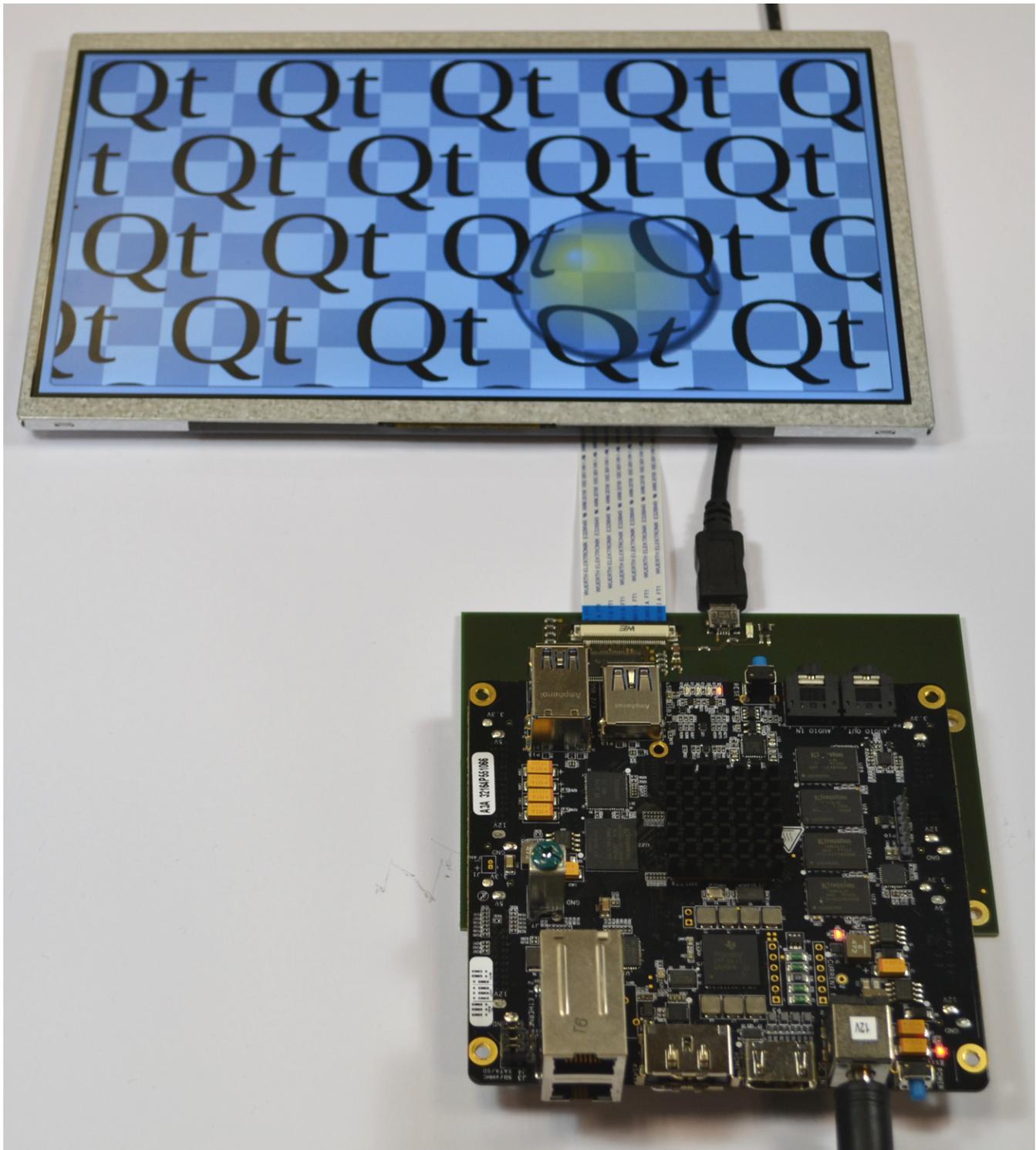


Figure 8. Running Setup With AM572x Evaluation Module

## 4 Design Files

### 4.1 Schematics

To download the schematics, see the design files at [TIDA-010013](#).

### 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-010013](#).

### 4.3 PCB Layout Recommendations

Refer to the data sheet of the particular video bridge for layout recommendations.

#### 4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-010013](#).

### 4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-010013](#).

### 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-010013](#).

### 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-010013](#).

## 5 Related Documentation

1. Texas Instruments, [SN65LVDS93B 10 MHz - 85 MHz 28-bit Flat Panel Display Link LVDS Serdes Transmitter Data Sheet](#)
2. Texas Instruments, [SN75LVDS83B FlatLink™ Transmitter](#)
3. Texas Instruments, [DS90C385A +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display Link-87.5 MHz Data Sheet](#)
4. Texas Instruments, [AM335x Starter Kit Product Folder](#)
5. Texas Instruments, [AM335x Sitara™ Processors Silicon Errata](#)
6. Texas Instruments, [AM572x Evaluation Module](#)
7. Texas Instruments, [AM572x Sitara™ Processors Technical Reference Manual](#)
8. New Haven Display Intl, [NHD-10.1-1024600AF-LSXV# TFT Color Liquid Crystal Display Module Product Specification](#)
9. Himax, [HX8282-A01 TXT LCD Source Driver with LVDS TCONF Data Sheet](#)

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## 6 About the Author

LARS LOTZENBURGER is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Lars brings to this role his extensive experience in analog and digital circuit development, PCB design, and embedded programming. Lars earned his diploma in electrical engineering from the University of Applied Science in Mittweida, Saxony, Germany. He currently focuses on functional safety and human machine interface (HMI) applications for Industrial.

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