TI Designs: TIDA-01579
High-Efficiency, Low-Output Ripple Power Supply Reference Design for Imaging Application

Description

The point-of-load power-tree on video surveillance systems is optimized with this reference design. This reference design has a high performance on key parameters such as output voltage accuracy, voltage ripple, and thermal dissipation. This high performance is possible with a small board area and low BOM cost. The design operates from a 5-V supply commonly found in video doorbells, IP network cameras, and wireless cameras.

Resources

TIDA-01579	Design Folder
TPS62821	Product Folder
TLV62568	Product Folder
TLV742P	Product Folder
TPS61169	Product Folder
TPS22976	Product Folder
TCA9535	Product Folder

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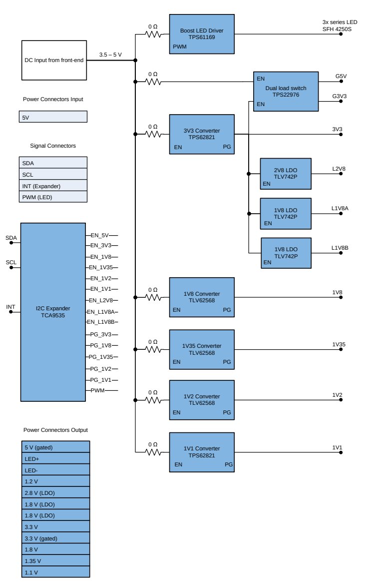
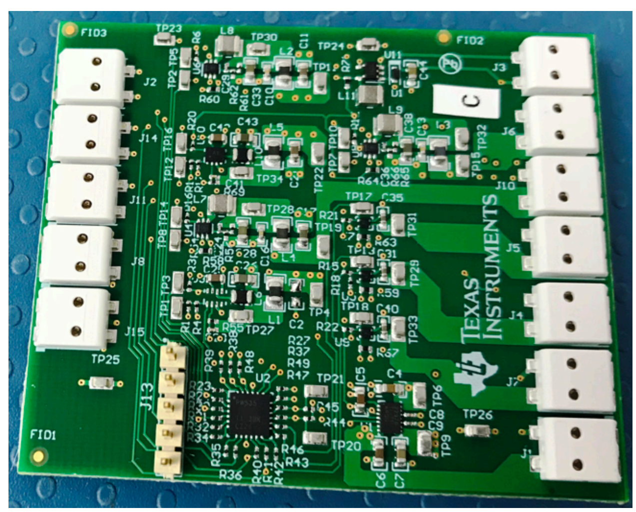
Features

- 1% Typical output voltage accuracy
- High system efficiency to 90% at full load
- Voltage ripple < 60-µV, useful for noise-critical peripherals
- Thermal hot spot is < 45°C at full load current
- Small PCB real estate
- Low BOM cost

Applications

- Video Doorbell
- IP Network Camera
- Wireless camera
- Thermal Imaging Camera
- Analog Security Camera





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1 System Description

Video doorbells provide a set of features common to many traditional video surveillance devices. This distinguishing feature demands a unique power design to ensure trouble-free operation from the ubiquitous, but widely-varying, AC doorbell supply. To fully utilize an AC source that presents a substantial bottleneck, the power design should be as efficient as possible. This design uses TI's new synchronous buck converters and LDOs providing a complete and customizable supply optimized for video doorbells. Our newest converters in QFN and SOT-563 packages allow for a supply design that requires minimal board space and has a low thermal impact—both of which are needed for smaller form factor electronics. For better compatibility, sequencing is possible for all rails.

IP network cameras have increasing image resolution, processing, and illumination requirements while still fitting in small enclosures. After stepping down from a mid- to high-voltage DC power source such as plug-in power or PoE, the system demands point-of-load conversion with high efficiency and a small footprint. Both efficiency and footprint are important to accommodate small enclosures with, typically, less-than-adequate ventilation. This design is optimized for both efficiency and footprint while also providing the flexibility to tailor to more advanced, power-demanding loads, such as a dedicated image recognition processor or 4K video processor.

Wireless or battery-powered cameras require high efficiency at both full loads and light loads. These cameras typically employ motion detection, human interface, or wireless communications monitoring, or any combination of the three, to minimize time spent in power-hungry states quiescent currents and shutdown currents of subsystems are very important as these standby currents can have significant impact on overall battery life. The TIDA-01579 reference design has been optimized for this application by utilizing TI's low-power converters featuring both light load efficiency and shutdown with low I_q. Converter shutdown and low-I_q load switches can be used to cut power to subsystems with less-than-desirable standby consumption—saving cost and extending battery life.

1.1 Key System Specifications

Table 1. Key System Specifications

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT	CONDITION
ELECTRICAL SPECIFICATION								
VIN	Input voltage			3.5	5	5.5	V	
Po	Output power	Full load		-	5	-	W	
		Light load		-	0.1	-		
η	System efficiency	Full load		-	90	-	%	
		Light load		-	84	-		
V3.3	General rail	Io		0.05	0.8	1.2	A	
		Ripple	PWM	-		25	mV	Pre-filter at PWM frequency
			PSM	-		50	mV	Pre-filter at PSM frequency
V1.35	DDR3 supply	Io		0.05	0.1	0.25	A	
		Ripple	PWM	-		10	mV	Pre-filter at PWM frequency
			PSM	-		25	mV	Pre-filter at PSM frequency
V1.1	Core Voltage	Io		0.05	1	1.2	A	
		Ripple	PWM	-		10	mV	Pre-filter at PWM frequency
			PSM	-		25	mV	Pre-filter at PSM frequency
V1.2	Sensor	Io		0.05	0.1	0.25	A	
		Ripple	PSM	-		5	mV	Pre-filter at PWM frequency
			PSM	-		25	mV	Pre-filter at PSM frequency
V1.8	Auxiliary General or Core supply	Io		0.05	0.1	0.25	A	
		Ripple	PWM	-	-	10	mV	Pre-filter at PWM frequency
			PSM	-	-	25	mV	Pre-filter at PSM frequency
V1.8	I/O voltage	Io		0.005	0.02	0.05	A	
		Ripple	PSM	-		5	mV	LDO O/P
			PSM	-		25	mV	
V2.8	Sensor voltage	Io		0.005	0.05	0.1	A	
		Ripple	PWM	-		5	mV	LDO O/P
			PSM	-		10	mV	
V1.8_ADD	Analog voltage for audio	Io		0.005	0.01	0.025	A	
		Ripple	PWM	-		5	mV	LDO O/P
			PSM	-		10	mV	
MECHANICAL SPECIFICATION								
L	Length			-	60	-	mm	
W	Width			-	50	-	mm	
ENVIRONMENTAL								
T	Operating temperature			–40	25	125	°C	

2 System Overview

2.1 Block Diagram

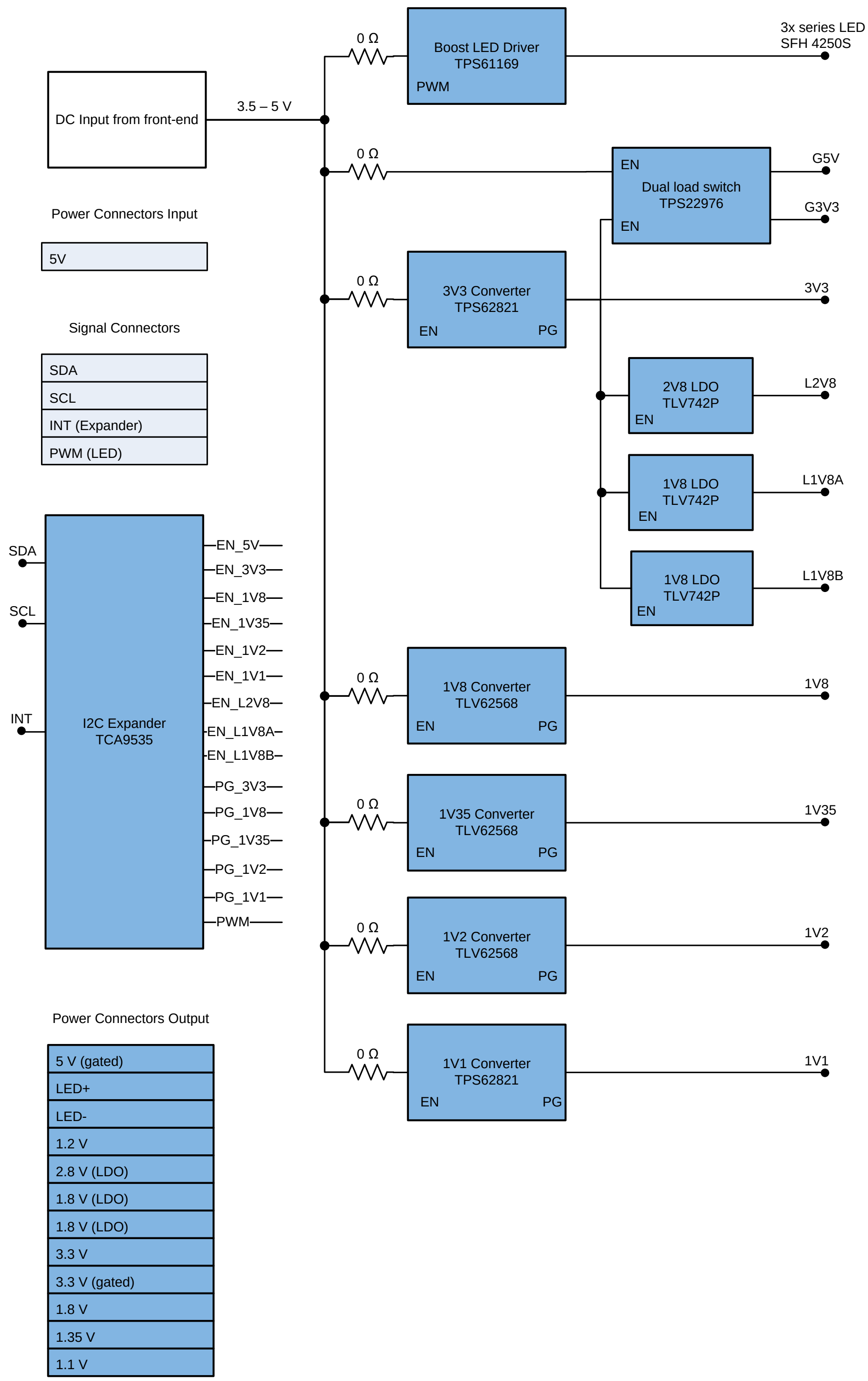


Figure 1. Block Diagram

3 Highlighted Products

With small footprint, and high efficiency DC/DC regulators from TI, it is possible to design compact, highly-efficient point of load power solutions.

3.1 TLV62568

The TLV62568 device is a synchronous step-down buck DC/DC converter optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 1 A. At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 1.5-MHz switching frequency. At light load, the device automatically enters power save mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is reduced to less than 2 μA. The device is available in a SOT23 and SOT563 package

3.2 TPS62821

The TPS6282x is an all-purpose and easy-to-use synchronous step-down DC/DC converter with a very-low quiescent current of only 4 µA. It supplies up to 3-A output current (TPS62823) from a 2.4-V to 5.5-V input voltage. Based on the DCS-Control™ topology it provides a fast transient response.

The internal reference allows regulating the output voltage down to 0.6 V with a high feedback voltage accuracy of 1% over the junction temperature range of –40°C to 125°C. The TPS6282x are packaged in a 2-mm × 1.5-mm QFN-8 package.

3.3 TLV742P

The TLV742P series of low-dropout (LDO) linear voltage regulators are optimized to providing excellent performance by supporting a wide output voltage range. The LDO regulators can directly regulate a single cell Li-ion battery input-to-output voltage as low as 0.85 V. If used to post-regulate a DC/DC converter output, the high PSRR of 55 dB at 1 MHz suppresses ripple to provide a stable low-noise, well-regulated output voltage. The TLV742P series of voltage regulators are available in a 1-mm × 1-mm X2SON package to minimize the PCB area.

3.4 TCA9535

The TCA9535 is a 24-pin device that provides 16 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I^2C bus or (SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V. The TCA9535 device consists of two 8-bit configuration (input or output selection), input port, output port, and polarity inversion (active-high or active-low operation) registers.

3.5 TPS61169

With a 40-V rated integrated switch FET, the TPS61169 is a boost converter that drives LEDs in series. The boost converter has a 40-V, 1.8-A internal MOSFET with minimum 1.2-A current limit; thus it can drive single or parallel LED strings for small- to large-size panel backlighting. The TPS61169 device is available in a space-saving 5-pin SC70 package.

3.6 TPS22976

The TPS22976 product family consists of two devices: TPS22976 and TPS22976N. Each device is a dual-channel load switch with controlled turn on. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.6 V to 5.7 V, and can support a maximum continuous current of 6 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. The TPS22976 device is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch off. The switch turns on again when the junction temperature stabilizes to a safe range. The TPS22976 device also offers an optional integrated 230-Ω on-chip load resistor for quick output discharge when the switch is turned off. The TPS22976 is available in a small, space-saving 3-mm × 2-mm 14-SON package (DPU) with integrated thermal pad allowing for high power dissipation.

4 System Design Theory

Video surveillance products such as a video doorbell or Wi-Fi® camera typically consist of power processor interfacing with high-speed image sensor and video encoder. The processor also interfaces with SD ram, audio codec supporting two-way audio communication, lens driver with IR cut filter sub circuitry. From power perspective many different supply rails are needed to be generated required to drive core voltage, I/O rail, and analog voltage for the previously-mentioned peripherals. Figure 1 shows a representation of typical power tree.

4.1 Buck DC/DC Regulator

For this application as fast transient response, low voltage ripple in a small form factor is required, selecting right control topology is the first step. Buck Converter has two sections that impact the performance, one is the power stage and other is the control topology. Power stage remains the same for all control topology. The inductor value is computed based on the preferred mode of switching operation. Whereas the control loop effects the loop response time, switching frequency, voltage ripple, full and light load efficiency.

The TI portfolio offers devices with 12 different types of control architectures. Most-commonly used are output voltage control, peak current control, hysteric or adaptive or fixed on time. Application requirements are driving factors for selecting the control topology. In this application a fast output response is needed, low voltage ripple, high DC voltage accuracy with minimum external components and seamless transition from PWM to power save mode, DCS-Control architecture is selected for high current demanding rail such as MPU Core voltage. This architecture offers benefits of both Voltage control loop for high DC accuracy and hysteric control loop for seamless transition, fast response with minimum external components with only trade off of wide variation of switching frequency as function of load current. Post damped PI filters have been implemented to counter impact of wide switching frequency ripple voltage variation on peripheral supply rail.

4.1.1 Power Stage Design Consideration

Before computing the Power stage Inductor & Capacitor values, the operating mode for maximum period of operation is considered. For rails that operate most of time in moderate to full load CCM mode is considered (Core Voltage and 3.3 V) were as for rails which operate most of time in light to moderate load DCM mode is considered (DDR3 and Sensor Voltage).

4.1.1.1 Inductor Ripple Current CCM Mode

In CCM mode the inductor ripple is a non-zero AC triangular ripple waveform with DC offset equal to output current as Figure 2 shows.

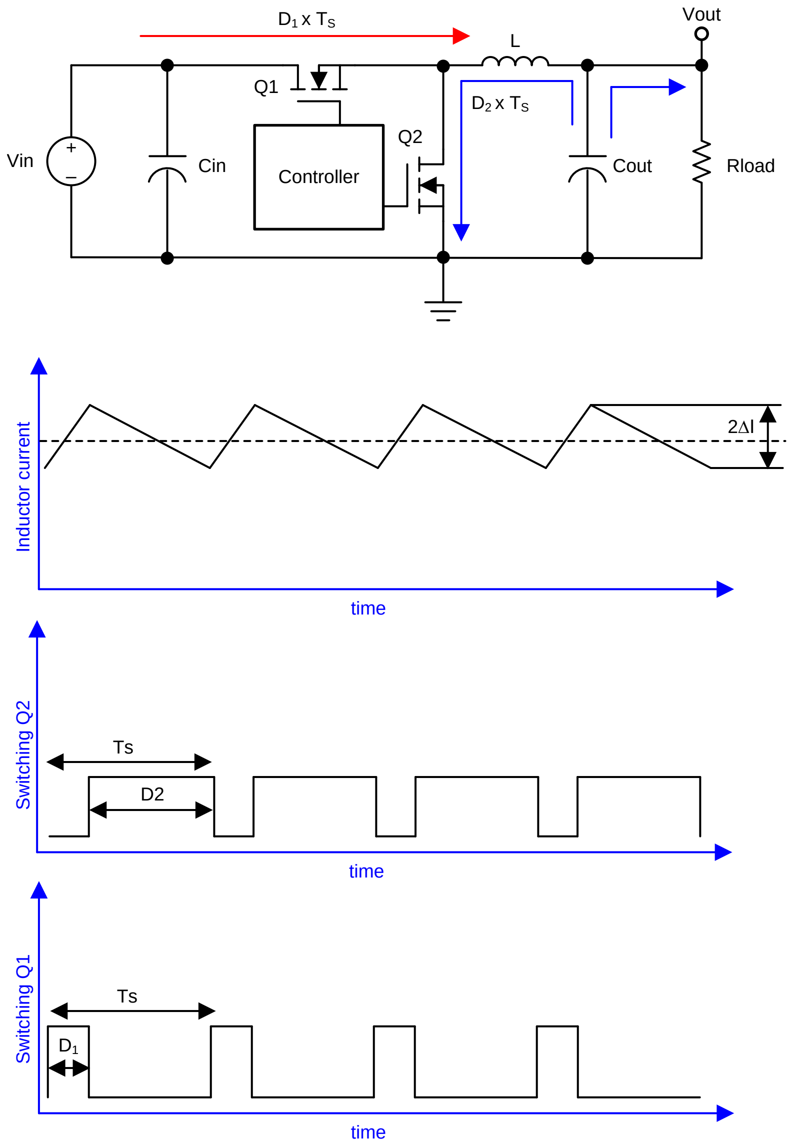


Figure 2. CCM Mode Operation

CCM Mode reduces AC core loss in inductor for moderate to full load. For making the flux swing in inductor core less than one half of maximum flux density, ripple current should be kept between 20%–40% of output DC current. In CCM mode there are two paths in one switching cycle. To reduce DC loss and reduce thermal hotspot for full load current, it is required that the DCR of inductor be as low as possible. To achieve very small DCR, lower no of turns is required which will result into smaller inductance value. Smaller inductor will result into higher ripple current dominating core and AC losses. Inductor has been selected keeping into consideration of both AC and DC losses in this design.

Compute the operating duty cycle and power stage inductor using Equation 1 and Equation 2:

$$D = \frac{V_{out}}{V_{in}} \tag{1}$$

$$L = \frac{(V_{in} - V_{out}) \times D}{(0.2 \text{ to } 0.4) \times I_{outmax} \times f_{sw}} \tag{2}$$

4.1.1.2 Inductor Ripple Current DCM Mode

In DCM mode, the inductor ripple is an AC triangular ripple waveform with zero crossing in each switching period as Figure 3 shows.

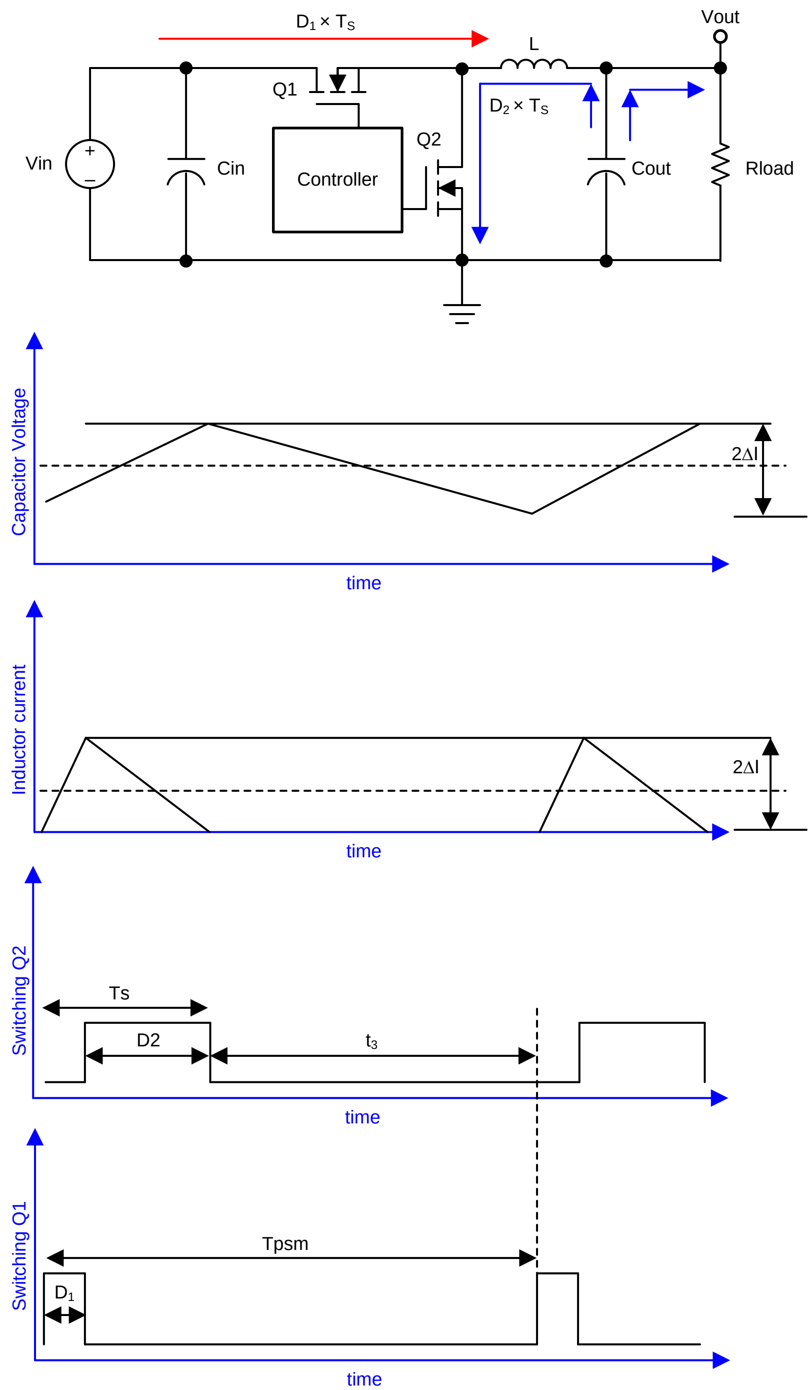


Figure 3. DCM Mode Operation

At light loads the ensure the flux swing in the inductor core still remains less than one half of maximum flux density. Using average equation of triangular waveform (1/2 x base x height) the ripple current needs to higher than twice of output current for one switching period as shown if fig. For ratio greater than 2 the inductance size can be further brought down thus increasing ripple current. In such scenarios the pause time t3 increases thus decreasing output voltage ripple frequency.

In this mode there are three states in one switching cycle described as on time (D1TS), off time (D2TS) and pause time (t3). Pause time is function of output load current and output capacitor value. At load conditions that satisfy condition as shown in equation Equation 3 results into DCM mode operation.

$$L < \frac{R_L}{2 \times f_{SW}} \tag{3}$$

4.1.1.3 Output Capacitor

An output capacitor with a power inductor forms the second-order low-pass filer attenuating the switching ripple voltage and also as energy storage for fast transient loads above a closed-loop bandwidth. At a higher switching frequency, the capacitance lead inductance also comes into the picture which is known as ESL and ESR of the capacitor as Figure 4 shows.

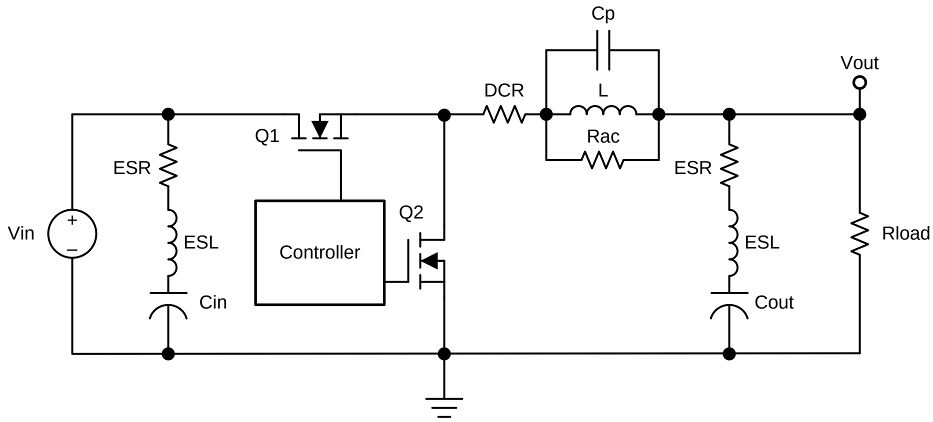


Figure 4. Non-Ideal Buck Converter

The expected ripple voltage in the CCM mode output capacitor can be computed using Equation 4. A capacitor with low ESR and low ESL reduces the output ripple voltage. For ESL values of picohenrys, the ESL factor can be ignored:

$$C_{out} = \frac{1}{8 \times f_{SW} \left(\left(\frac{\Delta V - \left(ESL \times \frac{V_{in} - V_{out}}{L} \right)}{di} \right) - ESR \right)} \tag{4}$$

In the case of DCM mode output, ripple voltage will be slightly higher based on pause time and output current which retriggers internal comparator of DC/DC converter when ripple voltage is lower than threshold. To derive output voltage ripple we can integrate capacitor current as shown in waveform during turn on and take twice of its value to get peak to peak ripple voltage. Capacitor current during turn on pulse can be put together as Equation 5 shows:

$$I_c = \frac{(V_{in} - V_{out}) \times t_{on}}{L} - I_{out} \tag{5}$$

Solving the integration during the turn on period for capacitor current and capacitor voltage is expressed as Equation 6 shows:

$$Vc = \int_0^{D \times T_S} \frac{(V_{in} - V_{out}) \times t_{on}}{L} - I_{out} = \frac{\left(\left(\frac{(V_{in} - V_{out}) \times t_{on}}{L} - I_{out} \right) \right)^2}{2 \times \frac{(V_{in} - V_{out})}{L}} = \frac{(D \times T_S \times (di - I_{out}))^2}{2 \times di} \tag{6}$$

The peak to peak ripple voltage considering an additional ESR voltage is expressed as Equation 7 shows:

$$\Delta V = \frac{\left[(D \times T_S \times (di - I_{out})^2) \right]}{di} + 2 \times R_{ESR} \times (di - I_{out}) \tag{7}$$

PSM mode switching frequency can be computed using device-specific equations as explained in the data sheet of device.

4.1.1.4 Input Capacitor

Due to the switching event, the ripple can be observed at the input side of the buck converter also. Using a capacitor at the input side the ripple voltage can be kept within expected limits. Use Equation 8 to compute the input capacitor using the expected ripple voltage as an input parameter:

$$C_{in} = \frac{V_{out}}{f_{sw} \times V_{in} \times \left(\frac{\Delta V_{in}}{I_{outmax}} - ESR \right)} \tag{8}$$

4.1.2 Power Stage Calculations

Using Equation 1, Equation 2, Equation 4, Equation 7, and Equation 8 the required power stage inductor, capacitor for DC/DC rail is calculated as shown in the following table.

PARAMETER, RAIL	UNIT	CORE VOLTAGE 1.1 V	GENERAL RAIL 3.3 V	IMAGE SENSOR CORE VOLTAGE 1.2 V	DDR3 SUPPLY VOLTAGE 1.35 V	DC/DC 1.8 V
Mode		CCM	CCM	CCM	CCM	CCM
Output Current	A	1.2	1.2	0.25	0.25	0.25
Inductor	µH	1	1	2.2	2.2	2.2
Output Capacitor	µF	10	10	4.7	4.7	4.7
Input Capacitor	µF	1	1	1	1	1
Ripple Voltage (PWM)	mV	8	10	3	3.5	3.7
Ripple Voltage (PSM)	mV	14	30	11	11	18.9
Feedback Resistor R1	kΩ	82.5	453	100	124	200
Feedback Resistor R2	kΩ	100	100	100	100	100

4.1.3 LDO

In this design image sensor analog voltage, audio CODEC analog voltage and MPU I/O voltage is powered using post LDO. TI's TLV742P device offers excellent high PSRR up to –45 dB at 1 MHz and very low noise output voltage noise to meet the critical specification of analog peripherals. The TLV742P device requires input and output capacitor bare minimum external components with internal feedback and a compensation circuit.

A post-PI filter can be added on each LDO output rail to increase PSRR even further.

4.1.4 PI Filter

Switching regulators generates undesired output artifacts that are harmful to noise critical rails. LDO do offer best rejection for post filtering but result into higher thermal losses at high load currents. An effective method to filter high frequency components is to use ferrite bead in PI configuration with capacitor to introduce low pass filter. Figure 5 shows most common filtering scheme implemented in power circuits.

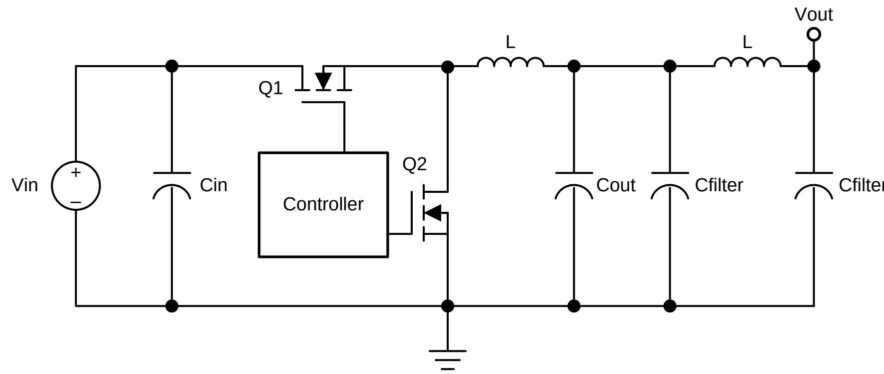


Figure 5. PI Filter

Ferrite bead detailed equivalent circuit analysis is considered to understand effects of self-resonance and LC resonance on gain plot to design effective filtering network. Ferrite bead has three operation regions: inductive, resistive and capacitive. These regions can be located from ZXR plot of ferrite bead as shown in Figure 6. The Ferrite bead can be modeled using an inductor, capacitor and resistor as Figure 6 shows, were RDC is DC resistance; Cpar, Lpar and Rac are bead inductance, capacitance and AC core loss resistance

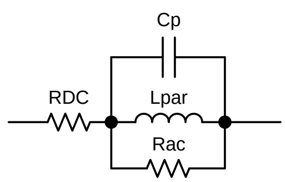


Figure 6. Bead Equivalent Model

Using an impedance curve for zero DC bias above values can be computed as per Equation 9, Equation 10, and Equation 11.

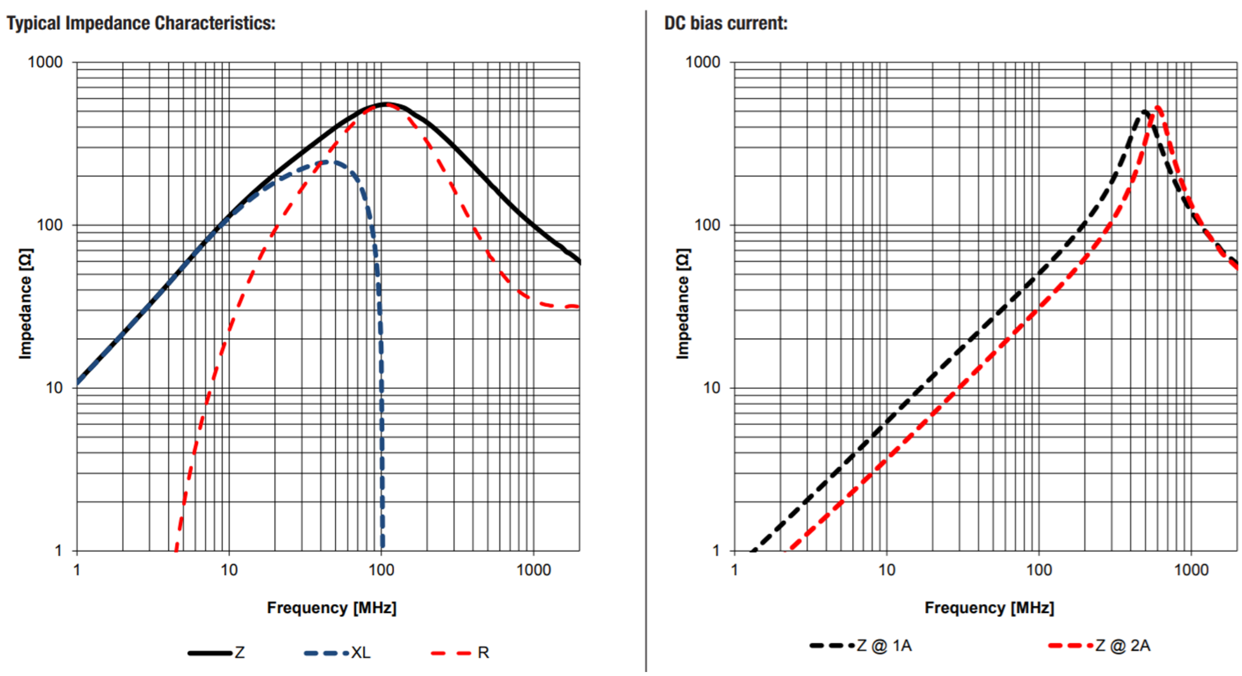


Figure 7. Impedance Curve

$$L_{par} = \frac{Z_L}{2 \times \pi \times f_L} \tag{9}$$

$$C_{par} = \frac{1}{2 \times \pi \times Z_C \times f_C} \tag{10}$$

$$R_{AC} = Z_{resonance} = \frac{1}{2 \times \pi \times C_{par} \times f_{resonance}} = 2 \times \pi \times L_{par} \times f_{resonance} \tag{11}$$

The data sheet also gives characteristics curve of impedance vs frequency for various DC Bias current. For maximum output current there will be shift in DC Inductance which needs to be calculated as it impacts into shift of corner frequency towards right side.

Assuming a ripple voltage of 25 mV at 2.2 MHz and required ripple voltage of 25 µV the required attenuation is –54 dB. Using ideal LC second order equation, resonant frequency of LC and filter capacitor can be calculated using Equation 12 and Equation 13.

$$f_{LC} = \frac{f_a(2.2\ \text{MHz})}{\sqrt{\left(\frac{1}{10^{\frac{-54}{20}}}\right)^2 - 1}} \tag{12}$$

$$C_{filter} = \frac{1}{2(4 \times \pi^2 \times f_{LC}{}^2 \times L_{par})} \tag{13}$$

A ferrite bead with a self-resonant frequency of at least 20, to approximately 50 times greater than switching frequency needs to be selected to operate in inductive region. Using a true bead model with output decoupling capacitor we see peaking occurring which results in gain at resonant frequency component as shown in Figure 8.

So LC filter needs to damped to reduce the peaking. Using series resistor damping can be achieved but will result into increased DC loss and voltage drop, Adding damp resistor in parallel to ferrite bead is another technique but results in bypass path at higher switching frequency.

One of the best techniques to avoid issue is to add bulk capacitor with series resistor which not only damps the peak but also does not degrade the effectiveness of filtering. Damp capacitor needs to higher than DC/DC output capacitor, at least 5 times will reduce value of series damp resistor.

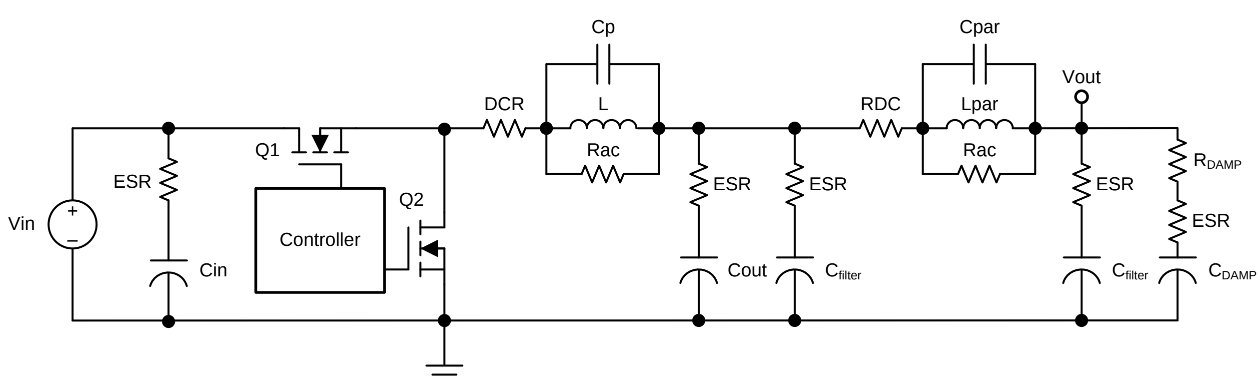


Figure 8. Non-Ideal PI Filter

Using Equation 14 damp resistor can be computed.

$$R_{damp} \le 0.5 \times \sqrt{\frac{L_{par}}{C_{filter}}} \tag{14}$$

Comparing simulation data as shown in Figure 9 and Figure 10 for damping circuit we see attenuation for desired frequency region with damping of LC resonance.

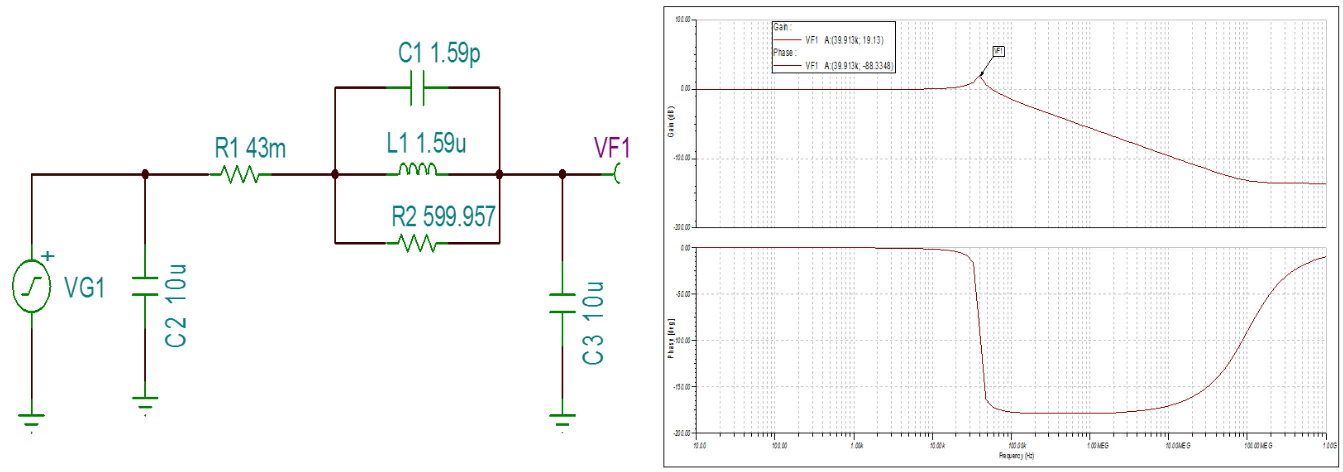


Figure 9. Undamped Filter Response

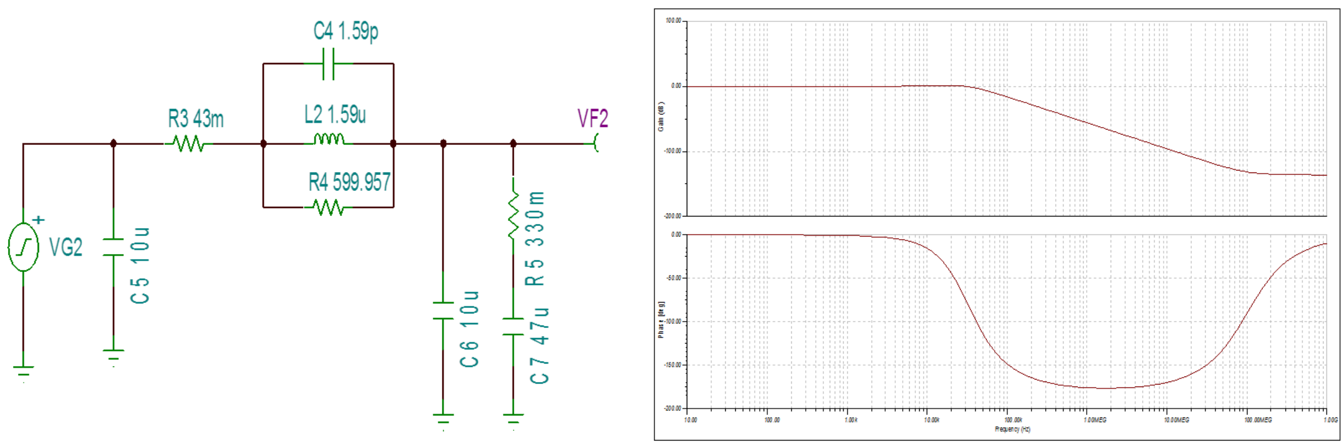


Figure 10. Damped Filter Response

4.1.5 Boost LED Driver

TIDA-01579 board has provision of Boost LED Driver to test IR LED illumination typically required in Video Imaging application. For more details refer to the TIDA-01586 design.

4.2 PCB Layout Consideration

PCB Layout determines Ground bounce, Electromagnetic Interference (EMI), and Thermal Behavior of switching regulator circuit. In switching regulator circuits there are fast switching node currents due to operation of synchronous FET. This gives rise to fast di/dt currents.

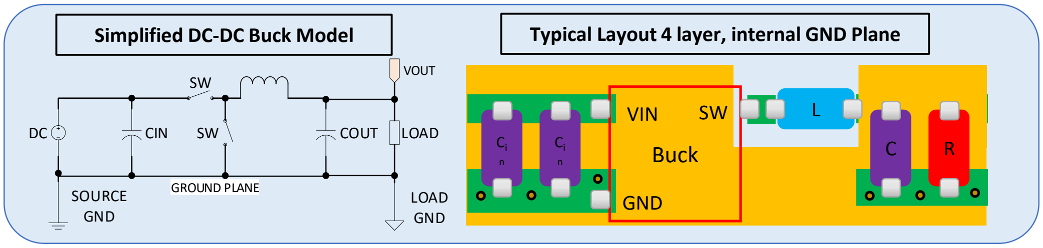


Figure 11. Typical Buck Converter Layout

Switching current flowing through return trace will result into change of flux which is function of loop area and magnetic flux density linked to it. In case of poor layout techniques having large ground loop, the fast switching current will results in rise of transient voltage, EMI interference and changing potential between actual ground and load ground. This impacts accuracy of output voltage.

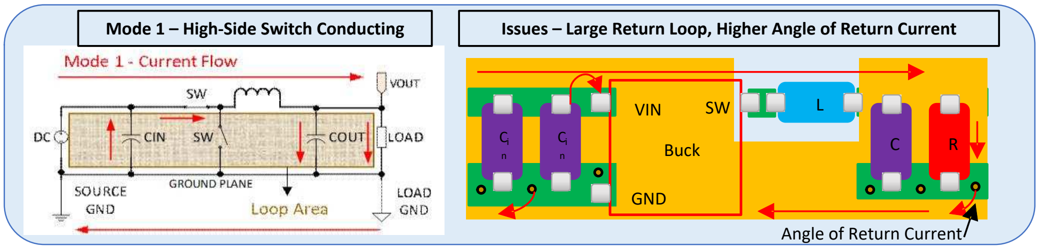


Figure 12. Mode 1 Switching Current

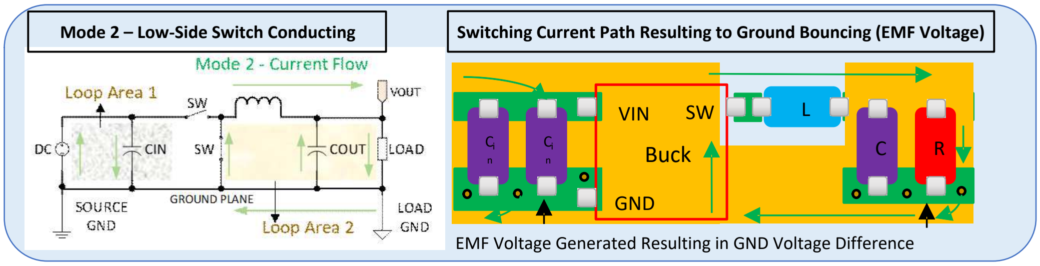


Figure 13. Mode 2 Switching Current

Placement of input capacitor, output capacitor, and power inductor with respect to switching point of device determines loop area of switching node. Adding even ground plane in inner layer does not minimize ground bounce issue.

To mitigate the previously-discussed issues, ground loop between switching node needs to be minimized. The placement of input and output capacitors must have a very short return ground plane as Figure 14 shows. To avoid operating issues due to PCB layout errors, see the *TI Layout* guidelines mentioned in the data sheet.

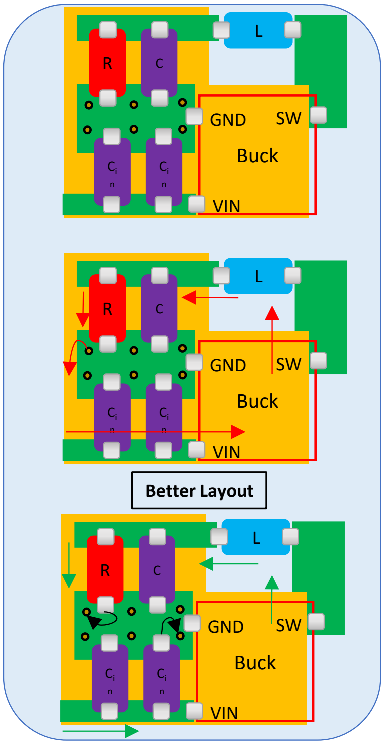


Figure 14. Recommended Layout

For example, in the layout for IC, U3 the input capacitor C25, output capacitor C26, power inductor L6 and are placed with lowest return path.

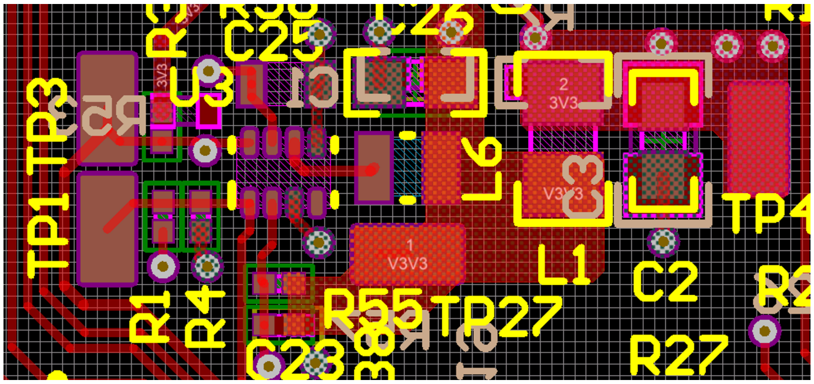


Figure 15. DC/DC Layout Example

5 Getting Started With the Hardware

The TIDA-01579 board supports external connector for independent testing and two boards interconnect connectors for interfacing with TI's Wi-Fi 1080p reference design board.

Before powering up the board, check for input and output connectors, and test points as described in the following. Verify for components that needs to be depopulated in the case of testing with digital sequencing. See Table 2 for more details on connectors provided on the board

Table 2. Board Connectors

CONNECTOR NUMBER	DESCRIPTION
J1	3.3-V DC/DC Output
J2	1.8-V DC/DC Output
J6	1.35-V DC/DC Output
J10	1.2-V DC/DC Output
J14	1.1-V DC/DC Output
J3	IR LED Output
J4	2.8-V LDO Output
J5	1.8-V LDO Output
J7	1.8 V LDO Output
J8	Gated 5V Output
J11	Gated 3.3-V Output
J9	20 pin Board Interface Connector
J12	20 pin Board Interface Connector
J15	DC Input Connector

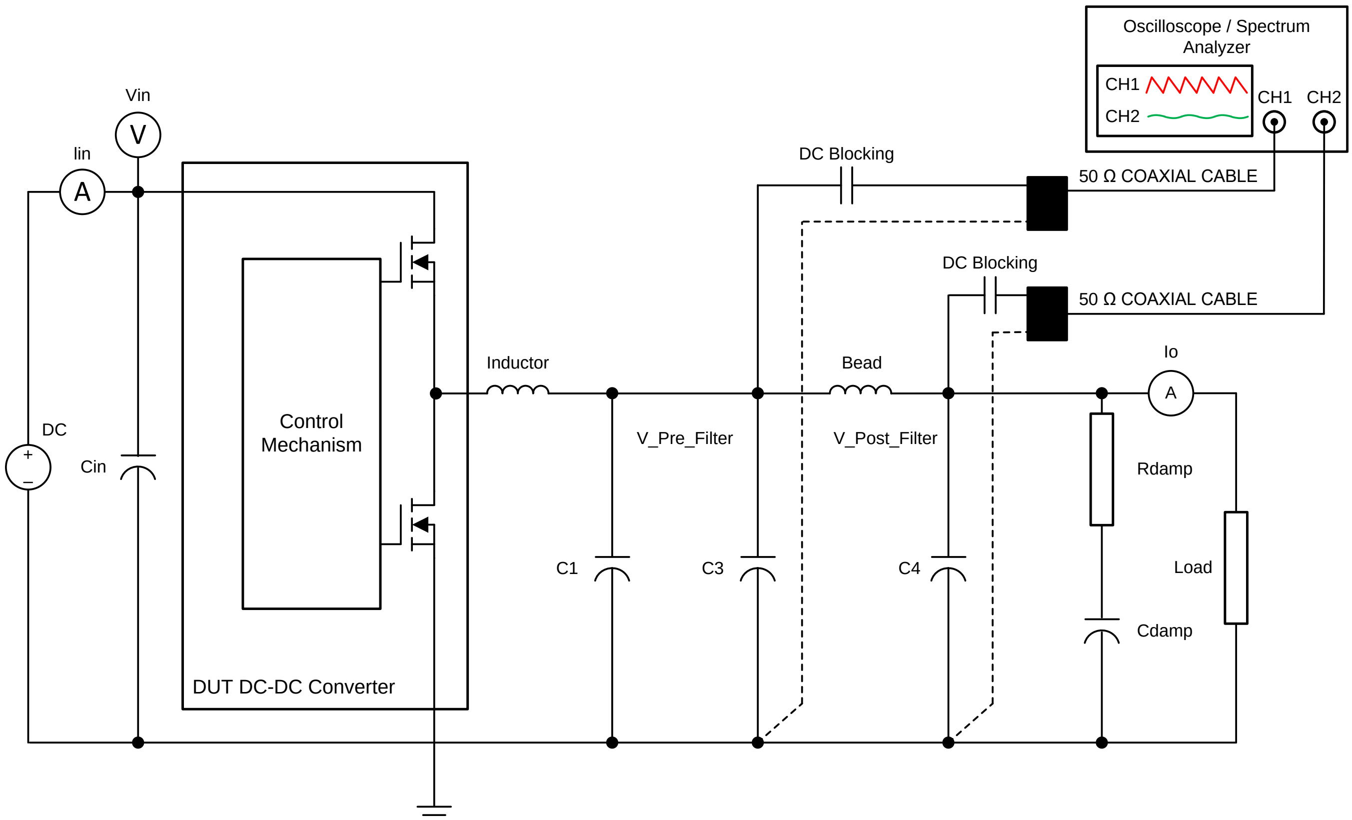
Required test point has been populated for measuring signals at each interface point of the design. For more details, see Table 3.

Table 3. Test Points

TEST POINT NUMBER	DESCRIPTION	VOLTAGE
TP4	3.3-V DC/DC post filter output	3.3 V
TP11	1.8-V DC/DC post filter output	1.8 V
TP15	1.35-V DC/DC post filter output	1.35 V
TP19	1.1-V DC/DC post filter output	1.1 V
TP22	1.2-V DC/DC post filter output	1.2 V
TP27	3.3-V DC/DC pre-filter output	3.3 V
TP30	1.8-V DC/DC pre filter output	1.8 V
TP32	1.35-V DC/DC pre-filter output	1.35 V
TP34	1.1-V DC/DC pre-filter output	1.1 V
TP28	1.2-V DC/DC pre-filter output	1.2 V
TP29	2.8-V LDO Output	2.8 V
TP31	1.8-V LDO Output	1.8 V
TP33	1.8-V LDO Output (Audio)	1.8 V
TP3	Power Good for 3.3 V	0 V - 3.3 V
TP5	Power Good for 1.8 V	0 V - 3.3 V
TP10	Power Good for 1.35 V	0 V - 3.3 V
TP14	Power Good for 1.2 V	0 V - 3.3 V
TP16	Power Good for 1.1 V	0 V - 3.3 V
TP23,TP24,TP25,TP26	GND	0 V

6 Test Setup

The test setup consists of TIDA-00753 Board, Keithley DC Supply, Agilent DMM, Decade Box, Current Probe as Figure 16 shows.



DUT: device under test

The oscilloscope analog signal bandwidth must be greater than 400 times the switching frequency

The oscilloscope should have a higher memory depth and sampling rate to capture the ripple waveform accurately (at least 4 GSPS, memory depth > 1 Mpts)

Oscilloscope probe terminated to 50 Ω

Set the spectrum analyzer with a frequency resolution less than 100 times the switching frequency to capture a better noise floor and SPUR

Figure 16. TIDA-01579 Test Setup

The tests to be conducted for this design are:

1. Device Efficiency and System Efficiency at various load and input voltage range
2. Ripple Voltage, Ripple Frequency at Full and light load conditions, Output Voltage Accuracy, Standard Deviation, Min and Max for various light and full load current's
3. Line and Load Transient Response
4. Light and Full Load Thermal Capture

To test the previous condition, the Agilent 61/2 DMM is set with the following settings to average the source and instrument error

1. Slow Filter – 7 seconds/ Reading
2. No of Samples – 50 (Approximately 6 min)

7 Test Results

7.1 Point of Load Characterization and Efficiency

7.1.1 Output 3.3 V

Table 4. Characterization 3.3 V

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)	Io (A)	Po (W)	Pin (W)	EFFICIENCY (%)	Pre_Filter_Output VOLTAGE RIPPLE (V)	Pre_Filter OUTPUT VOLTAGE RIPPLE FREQUENCY (Hz)
Full Load - 1 A											
3.5	1.01E+00	3.248	3.00E-03	3.245	-1.67	1.00E+00	3.258E+00	3.52E+00	92.62	4.00E-03	-
5	7.12E-01	3.312	3.00E-03	3.309	0.27	1.00E+00	3.322E+00	3.56E+00	93.32	9.20E-03	1.98E+06
5.5	6.48E-01	3.311	3.00E-03	3.308	0.24	1.00E+00	3.321E+00	3.56E+00	93.18	1.04E-02	2.05E+06
Light Load - 50 mA											
3.5	5.00E-02	3.37	3.00E-03	3.367	2.03	5.00E-02	1.684E-01	1.75E-01	96.2	8.00E-03	8.00E+05
5	3.60E-02	3.369	3.00E-03	3.366	2	5.00E-02	1.683E-01	1.80E-01	93.5	2.96E-02	3.87E+05
5.5	3.30E-02	3.374	3.00E-03	3.371	2.15	5.00E-02	1.686E-01	1.82E-01	92.86	3.52E-02	3.13E+05

7.1.2 Output 1.1 V

Table 5. Characterization 1.1 V

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)	Io (A)	Po (W)	Pin (W)	EFFICIENCY (%)	Pre_Filter_Output VOLTAGE RIPPLE (V)	Pre_Filter OUTPUT VOLTAGE RIPPLE FREQUENCY (Hz)
Full Load 1 A											
3.5	3.64E-01	1.062	3.00E-03	1.059	-3.72	1.00E+00	1.06E+00	1.27E+00	83.45	2.00E-03	1.90E+06
5	2.54E-01	1.067	3.00E-03	1.064	-3.27	1.00E+00	1.07E+00	1.27E+00	84.11	7.60E-03	1.60E+06
5.5	2.31E-01	1.061	3.00E-03	1.058	-3.81	1.00E+00	1.06E+00	1.27E+00	83.60	8.60E-03	1.50E+06
Light Load 50 mA											
3.5	1.80E-02	1.12	3.00E-03	1.117	1.54	5.00E-02	5.59E-02	6.30E-02	88.65	9.60E-03	6.25E+05
5	1.40E-02	1.121	3.00E-03	1.118	1.63	5.00E-02	5.59E-02	7.00E-02	79.85	1.40E-02	4.25E+05
5.5	1.30E-02	1.126	3.00E-03	1.123	2.09	5.00E-02	5.62E-02	7.15E-02	78.53	1.64E-02	3.75E+05

7.1.3 Output 1.35 V

Table 6. Characterization 1.35 V

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)	Io (A)	Po (W)	Pin (W)	EFFICIENCY (%)	Pre_Filter_Output VOLTAGE RIPPLE (V)	Pre_Filter OUTPUT VOLTAGE RIPPLE FREQUENCY (Hz)
Full Load 250 mA											
3.5	1.04E-01	1.355	3.00E-03	1.352	0.37	2.50E-01	3.38E-01	3.64E-01	92.85	2.80E-03	1.54E+06
5	7.60E-02	1.362	3.00E-03	1.359	0.88	2.50E-01	3.40E-01	3.80E-01	89.40	3.20E-03	1.61E+06
5.5	7.20E-02	1.363	3.00E-03	1.360	0.96	2.50E-01	3.40E-01	3.96E-01	85.85	3.28E-03	1.64E+06
Light Load 50 mA											
3.5	2.20E-02	1.373	3.00E-03	1.370	1.70	5.03E-02	6.90E-02	7.70E-02	89.56	9.60E-03	5.50E+05
5	1.60E-02	1.37	3.00E-03	1.367	1.48	5.05E-02	6.91E-02	8.00E-02	86.34	1.08E-02	5.12E+05
5.5	1.50E-02	1.372	3.00E-03	1.369	1.62	5.06E-02	6.92E-02	8.25E-02	83.91	1.16E-02	5.00E+05

7.1.4 Output 1.2 V

Table 7. Characterization 1.2 V

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)	Io (A)	Po (W)	Pin (W)	EFFICIENCY (%)	Pre_Filter_Output VOLTAGE RIPPLE (V)	Pre_Filter OUTPUT VOLTAGE RIPPLE FREQUENCY (Hz)
Full Load 250 mA											
3.5	9.30E-02	1.223	3.00E-03	1.220	1.91	2.50E-01	3.05E-01	3.26E-01	93.70	2.64E-03	1.53E+06
5	6.90E-02	1.223	3.00E-03	1.220	1.91	2.57E-01	3.14E-01	3.45E-01	90.91	3.04E-03	1.58E+06
5.5	6.50E-02	1.225	3.00E-03	1.222	2.08	2.50E-01	3.06E-01	3.58E-01	85.45	3.12E-03	1.60E+06
Light Load 50 mA											
3.5	1.90E-02	1.24	3.00E-03	1.237	3.33	5.00E-02	6.19E-02	6.65E-02	93.00	1.00E-02	5.25E+05
5	1.50E-02	1.241	3.00E-03	1.238	3.41	5.00E-02	6.19E-02	7.50E-02	82.53	1.08E-02	5.25E+05
5.5	1.40E-02	1.247	3.00E-03	1.244	3.91	5.00E-02	6.22E-02	7.70E-02	80.77	1.16E-02	4.75E+05

7.1.5 Output 1.8 V

Table 8. Characterization 1.8 V

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)	Io (A)	Po (W)	Pin (W)	EFFICIENCY (%)	Pre_Filter_Output VOLTAGE RIPPLE (V)	Pre_Filter OUTPUT VOLTAGE RIPPLE FREQUENCY (Hz)
Full Load 250 mA											
3.5	1.38E-01	1.841	3.00E-03	1.838	2.11	2.50E-01	4.60E-01	4.83E-01	95.13	3.28E-03	1.49E+06
5	1.00E-01	1.832	3.00E-03	1.829	1.61	2.50E-01	4.57E-01	5.00E-01	91.45	3.76E-03	1.60E+06
5.5	9.40E-02	1.837	3.00E-03	1.834	1.88	2.50E-01	4.59E-01	5.17E-01	88.68	3.76E-03	1.63E+06
Light Load - 50 mA											
3.5	2.80E-02	1.846	3.00E-03	1.843	2.38	5.00E-02	9.22E-02	9.80E-02	94.03	1.08E-02	5.62E+05
5	2.10E-02	1.852	3.00E-03	1.849	2.72	5.00E-02	9.25E-02	1.05E-01	88.04	1.90E-02	3.68E+05
5.5	2.00E-02	1.852	3.00E-03	1.849	2.72	5.00E-02	9.25E-02	1.10E-01	84.04	1.88E-02	3.65E+05

7.1.6 LDO Output 2.8 V

Table 9. Characterization 2.8 V

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)
Full Load 50 mA					
3.5	5.00E-02	2.857	3.00E-03	2.854	2.035
5	3.60E-02	2.853	3.00E-03	2.850	1.89
5.5	3.40E-02	2.851	3.00E-03	2.848	1.82
Light Load 5 mA					
3.5	6.00E-03	2.855	3.00E-03	2.852	1.96
5	4.00E-03	2.853	3.00E-03	2.850	1.89
5.5	4.00E-03	2.862	3.00E-03	2.859	2.21

7.1.7 LDO Output 1.8 V (I/O)

Table 10. Characterization 1.8 V_I/O

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)
Full Load 50 mA					
3.5	5.00E-02	1.814	3.00E-03	1.811	0.77
5	3.60E-02	1.811	3.00E-03	1.808	0.61
5.5	3.30E-02	1.812	3.00E-03	1.809	0.66
Light Load 5 mA					
3.5	6.00E-03	1.816	3.00E-03	1.813	0.88
5	4.00E-03	1.814	3.00E-03	1.811	0.77
5.5	4.00E-03	1.814	3.00E-03	1.811	0.77

7.1.8 LDO Output 1.8 V (Audio)

Table 11. Characterization 1.8 V_Audio

Vin (V)	Iin (A)	Vo (V)	PROBE ERROR (V)	FINAL OUTPUT (V)	ERROR (%)
Full Load 25 mA					
3.5	2.60E-02	1.805	3.00E-03	1.802	0.27
5	1.90E-02	1.81	3.00E-03	1.807	0.55
5.5	1.70E-02	1.809	3.00E-03	1.806	0.5
Light Load 5 mA					
3.5	6.00E-03	1.812	3.00E-03	1.809	0.66
5	4.00E-03	1.812	3.00E-03	1.809	0.66
5.5	4.00E-03	1.811	3.00E-03	1.808	0.61

7.2 Point of Load Pre and Post Output Voltage Ripple and FFT Plots

Using the *Spectrum Analyzer* function, 1× AC probe as shown in the Test Setup Image, Spectrum plot have been captured for all DC/DC rail to validate very low ripple output and Harmonic free Spectrum to achieve Higher ENOB with respect to Power supply Spur and Noise Floor.

7.2.1 3.3-V Output

Table 12. 3.3-V Ripple and FFT Plot

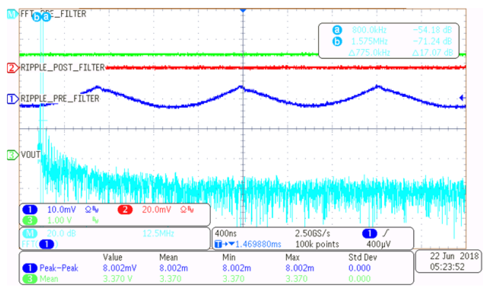
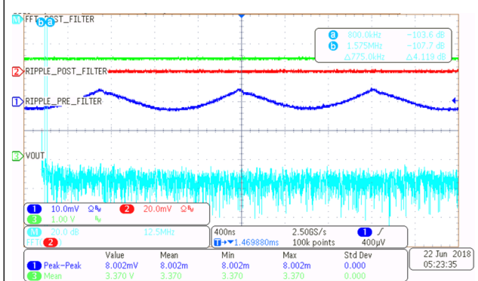
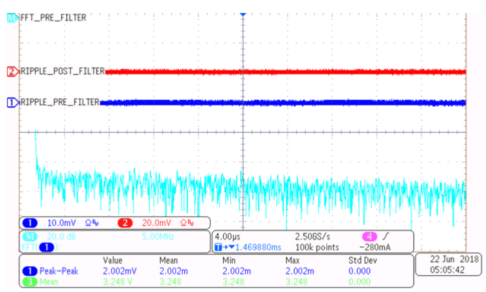
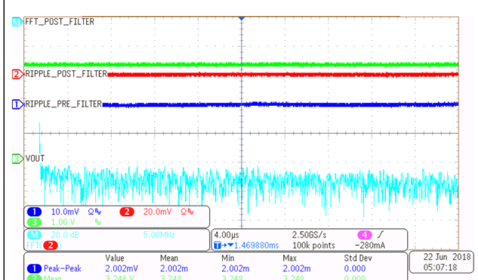
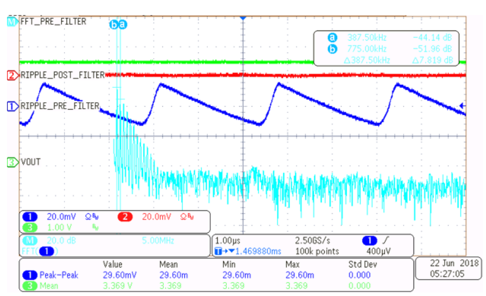
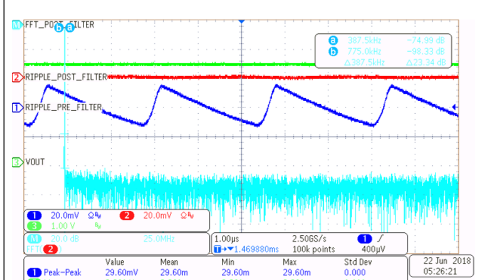
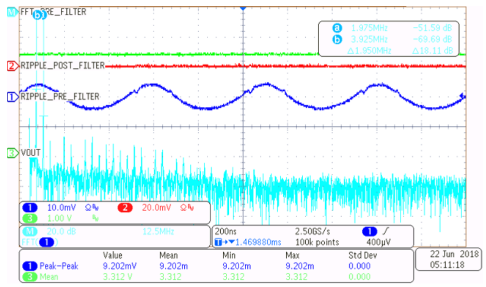
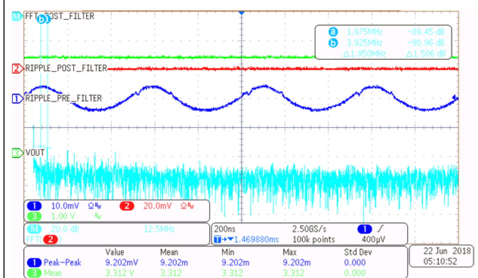
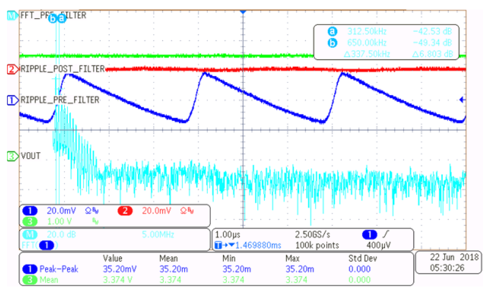
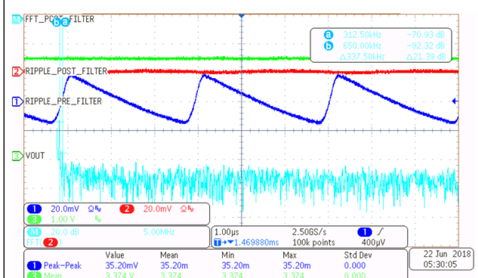
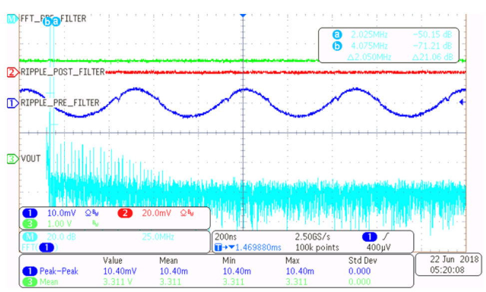
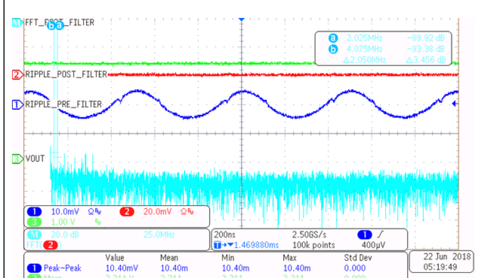
INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
3.5	Light Load	 Figure 17. DC/DC FFT and Ripple Under Light Load	 Figure 18. Post Filter FFT and Ripple Under Light Load
3.5	Full Load	 Figure 19. DC/DC FFT and Ripple Under Full Load	 Figure 20. Post Filter FFT and Ripple Under Full Load
5	Light Load	 Figure 21. DC/DC FFT and Ripple Under Light Load	 Figure 22. Post Filter FFT and Ripple Under Light Load

Table 12. 3.3-V Ripple and FFT Plot (continued)

INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
5	Full Load	 **Figure 23. DC/DC FFT and Ripple Under Full Load**	 **Figure 24. Post Filter FFT and Ripple Under Full Load**
5.5	Light Load	 **Figure 25. DC/DC FFT and Ripple Under Light Load**	 **Figure 26. Post Filter FFT and Ripple Under Light Load**
5.5	Full Load	 **Figure 27. DC/DC FFT and Ripple Under Full Load**	 **Figure 28. Post Filter FFT and Ripple Under Full Load**

7.2.2 1.1-V Output

Table 13. 1.1-V Ripple and FFT Plot

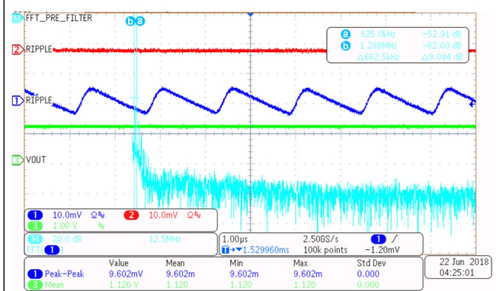
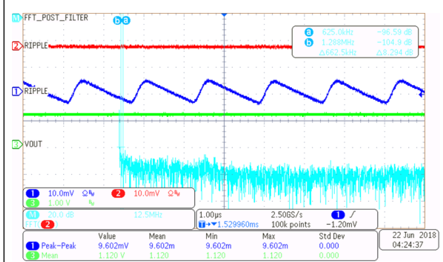
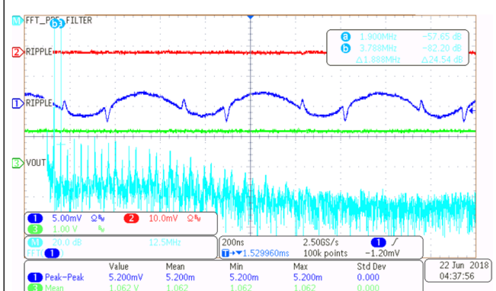
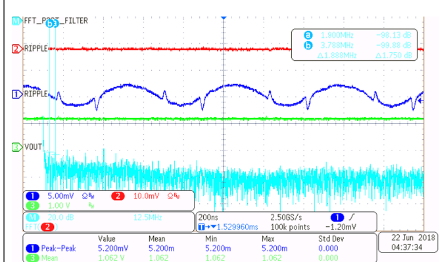
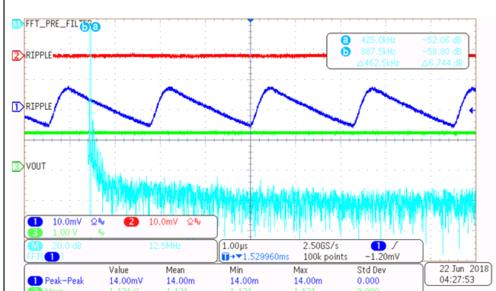
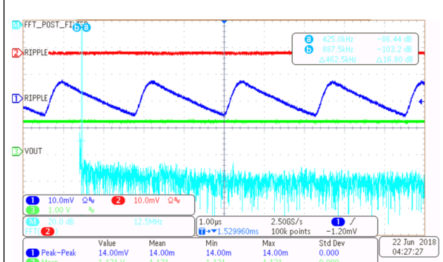
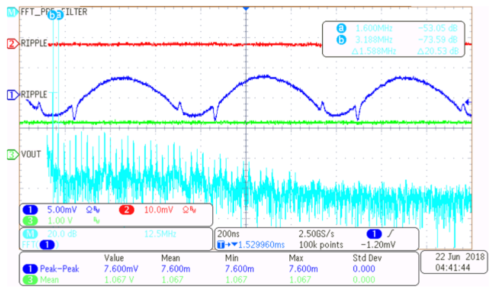
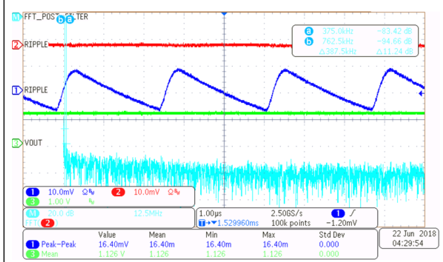
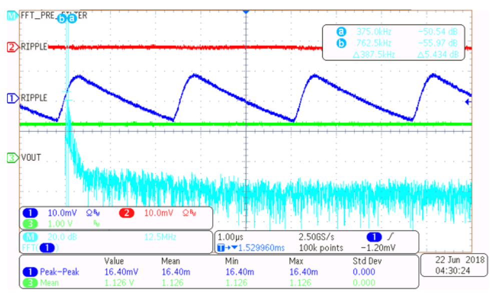
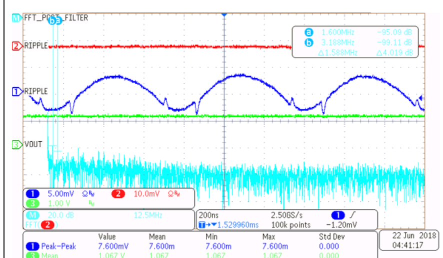
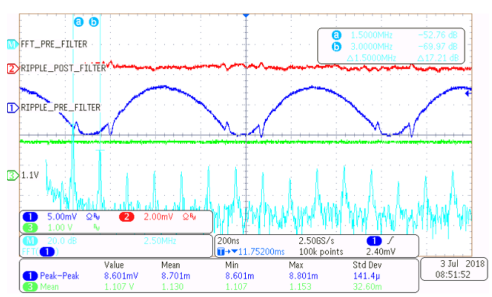
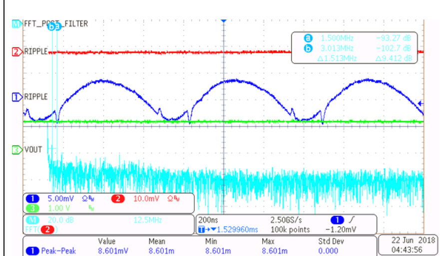
INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
3.5	Light Load	 Figure 29. DC/DC FFT and Ripple Under Light Load	 Figure 30. Post Filter FFT and Ripple Under Light Load
3.5	Full Load	 Figure 31. DC/DC FFT and Ripple Under Full Load	 Figure 32. Post Filter FFT and Ripple Under Full Load
5	Light Load	 Figure 33. DC/DC FFT and Ripple Under Light Load	 Figure 34. Post Filter FFT and Ripple Under Light Load

Table 13. 1.1-V Ripple and FFT Plot (continued)

INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
5	Full Load	 **Figure 35. DC/DC FFT and Ripple Under Full Load**	 **Figure 36. Post Filter FFT and Ripple Under Full Load**
5.5	Light Load	 **Figure 37. DC/DC FFT and Ripple Under Light Load**	 **Figure 38. Post Filter FFT and Ripple Under Light Load**
5.5	Full Load	 **Figure 39. DC/DC FFT and Ripple Under Full Load**	 **Figure 40. Post Filter FFT and Ripple Under Full Load**

7.2.3 1.35-V Output

Table 14. 1.35-V Ripple and FFT Plot

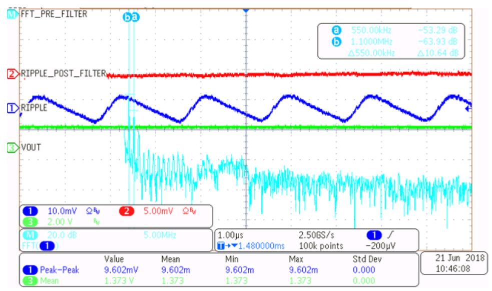
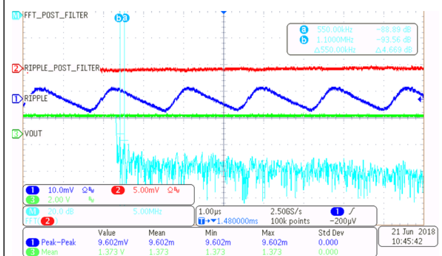
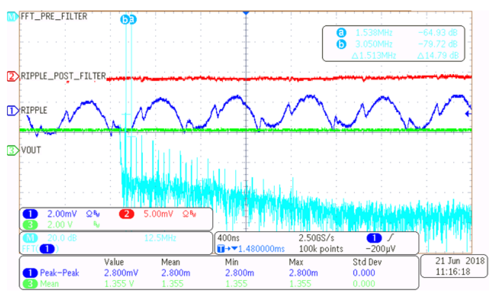
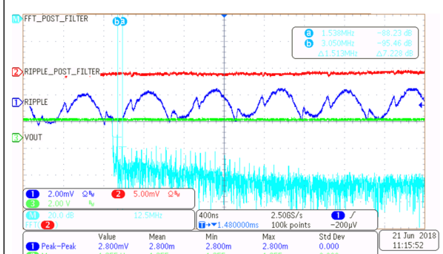
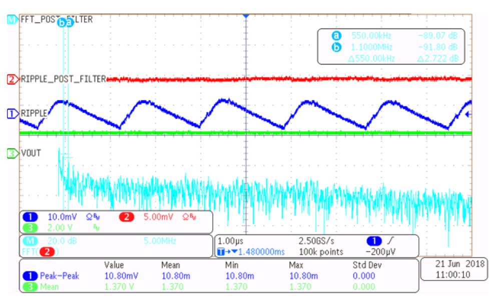
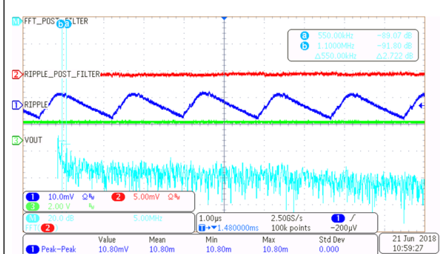
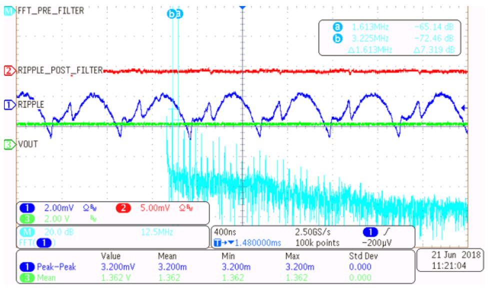
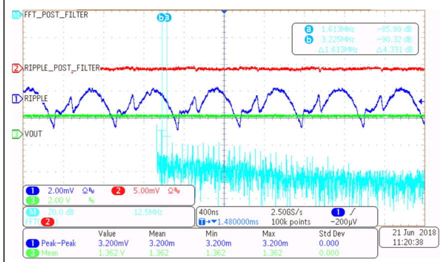
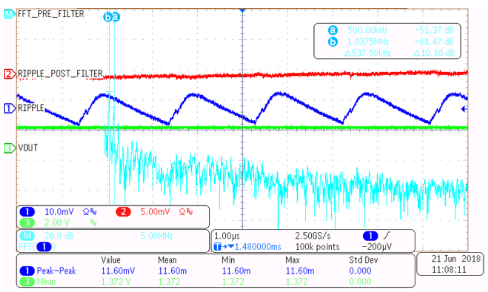
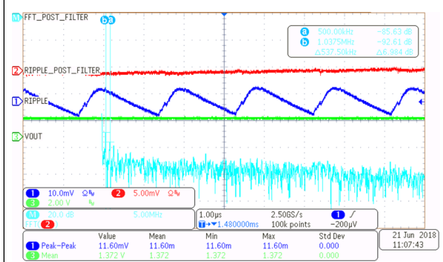
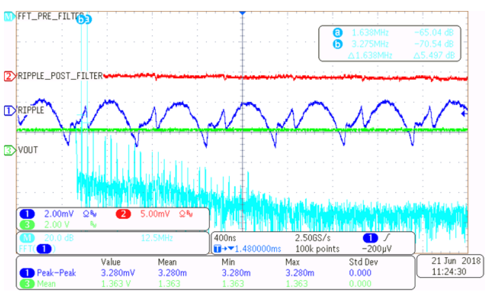
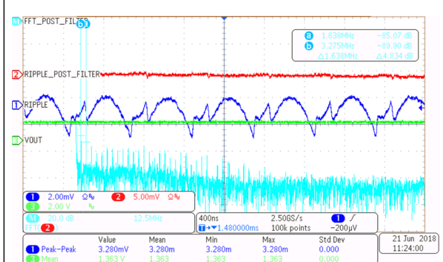
INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
3.5	Light Load	 **Figure 41. DC/DC FFT and Ripple Under Light Load**	 **Figure 42. Post Filter FFT and Ripple Under Light Load**
3.5	Full Load	 **Figure 43. DC/DC FFT and Ripple Under Full Load**	 **Figure 44. Post Filter FFT and Ripple Under Full Load**
5	Light Load	 **Figure 45. DC/DC FFT and Ripple Under Light Load**	 **Figure 46. Post Filter FFT and Ripple Under Light Load**

Table 14. 1.35-V Ripple and FFT Plot (continued)

INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
5	Full Load	 **Figure 47. DC/DC FFT and Ripple Under Full Load**	 **Figure 48. Post Filter FFT and Ripple Under Full Load**
5.5	Light Load	 **Figure 49. DC/DC FFT and Ripple Under Light Load**	 **Figure 50. Post Filter FFT and Ripple Under Light Load**
5.5	Full Load	 **Figure 51. DC/DC FFT and Ripple Under Full Load**	 **Figure 52. Post Filter FFT and Ripple Under Full Load**

7.2.4 1.2-V Output

Table 15. 1.2-V Ripple and FFT Plot

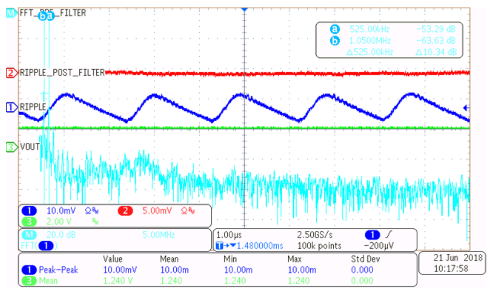
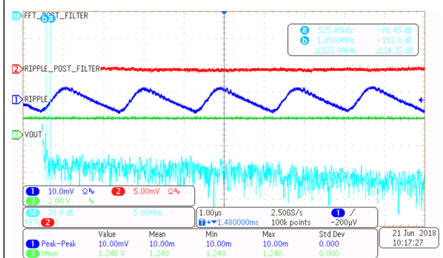
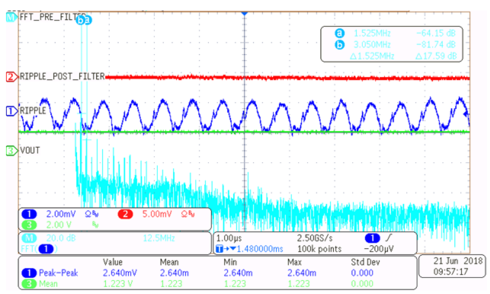
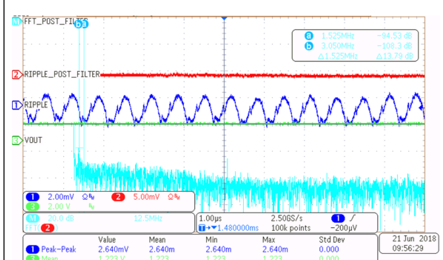
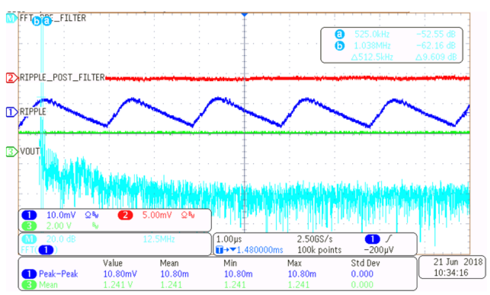
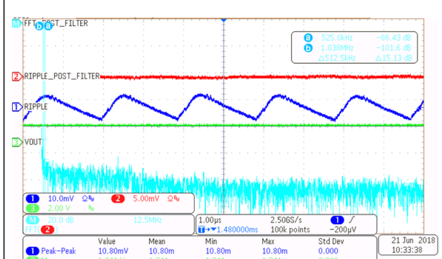
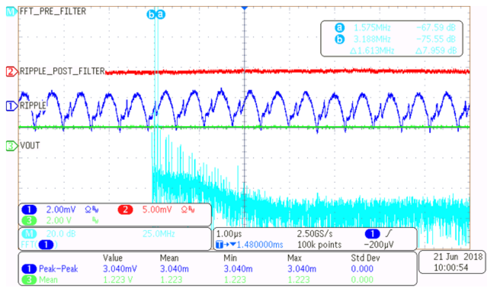
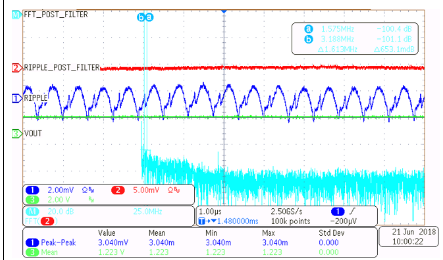
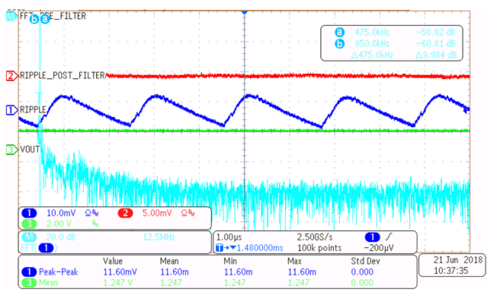
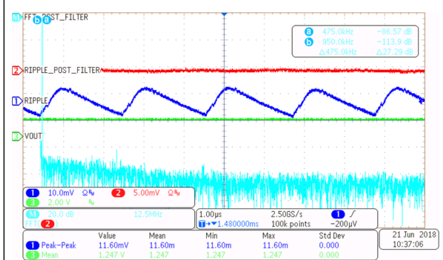
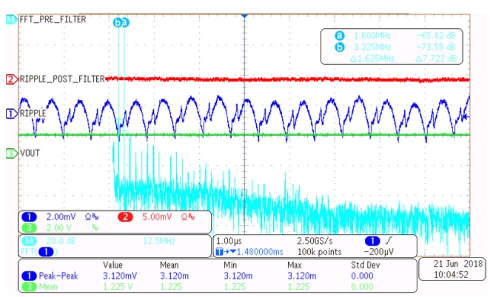
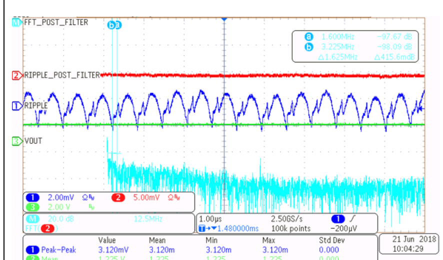
INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
3.5	Light Load	 **Figure 53. DC/DC FFT and Ripple Under Light Load**	 **Figure 54. Post Filter FFT and Ripple Under Light Load**
3.5	Full Load	 **Figure 55. DC/DC FFT and Ripple Under Full Load**	 **Figure 56. Post Filter FFT and Ripple Under Full Load**
5	Light Load	 **Figure 57. DC/DC FFT and Ripple Under Light Load**	 **Figure 58. Post Filter FFT and Ripple Under Light Load**

Table 15. 1.2-V Ripple and FFT Plot (continued)

INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
5	Full Load	 **Figure 59. DC/DC FFT and Ripple Under Full Load**	 **Figure 60. Post Filter FFT and Ripple Under Full Load**
5.5	Light Load	 **Figure 61. DC/DC FFT and Ripple Under Light Load**	 **Figure 62. Post Filter FFT and Ripple Under Light Load**
5.5	Full Load	 **Figure 63. DC/DC FFT and Ripple Under Full Load**	 **Figure 64. Post Filter FFT and Ripple Under Full Load**

7.2.5 1.8-V Output

Table 16. 1.8-V Ripple and FFT Plot

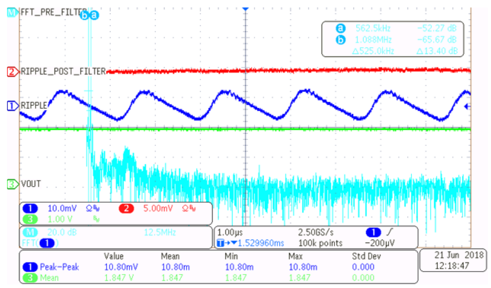
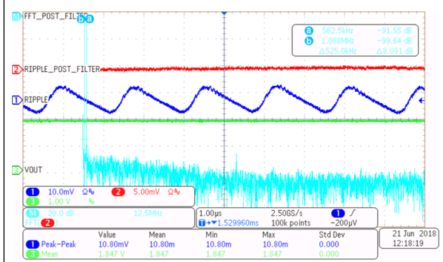
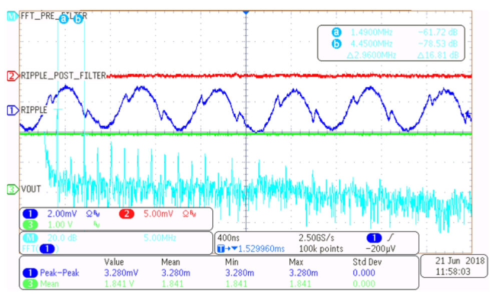
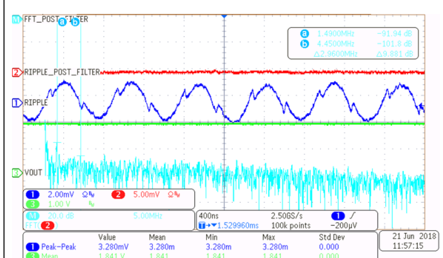
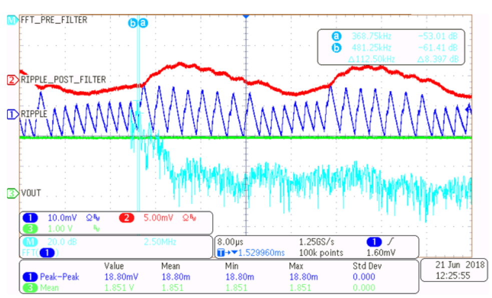
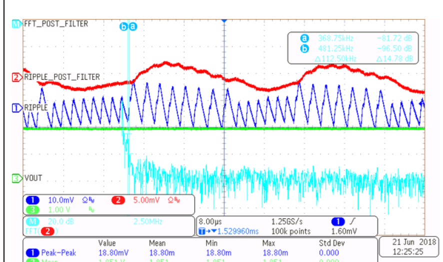
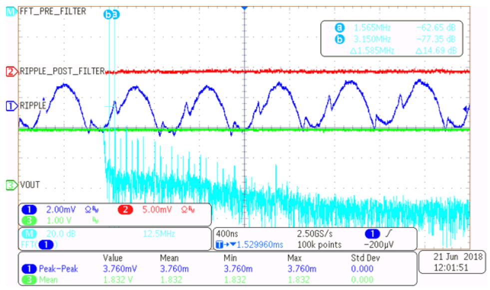
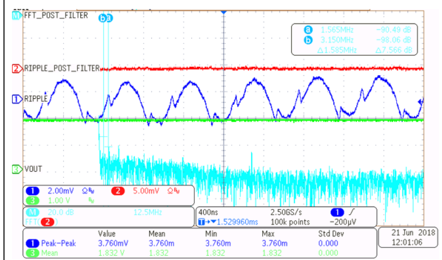
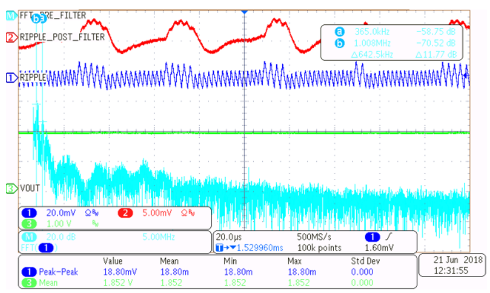
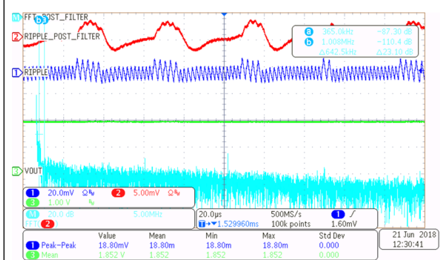
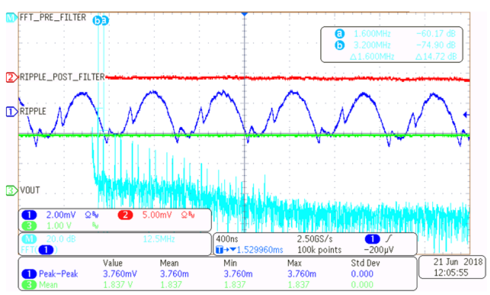
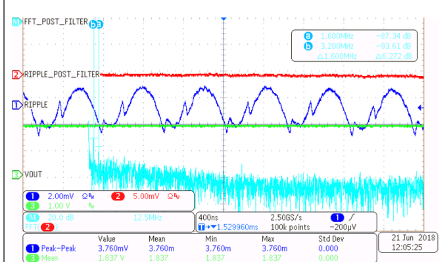
INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
3.5	Light Load	 Figure 65. DC/DC FFT and Ripple Under Light Load	 Figure 66. Post Filter FFT and Ripple Under Light Load
3.5	Full Load	 Figure 67. DC/DC FFT and Ripple Under Full Load	 Figure 68. Post Filter FFT and Ripple Under Full Load
5	Light Load	 Figure 69. DC/DC FFT and Ripple Under Light Load	 Figure 70. Post Filter FFT and Ripple Under Light Load

Table 16. 1.8-V Ripple and FFT Plot (continued)

INPUT VOLTAGE (V)	LOAD CONDITION	PRE FILTER	POST FILTER
5	Full Load	 **Figure 71. DC/DC FFT and Ripple Under Full Load**	 **Figure 72. Post Filter FFT and Ripple Under Full Load**
5.5	Light Load	 **Figure 73. DC/DC FFT and Ripple Under Light Load**	 **Figure 74. Post Filter FFT and Ripple Under Light Load**
5.5	Full Load	 **Figure 75. DC/DC FFT and Ripple Under Full Load**	 **Figure 76. Post Filter FFT and Ripple Under Full Load**

7.3 Point of Load Transient Response

Each DC/DC rail has been tested for Transient load condition ranging from (50 mA to 1 A/250 mA) using DC electronic load with 10-kHz switching frequency, 50% duty cycle and 250 mA/µs slew rate to capture and compare FFT spectrum of DC/DC output rail with Post Filter Response. Also overshoot, undershoot is observed to validate fast transient response. From test result we clearly see ripple voltage changing under load condition and having low and high frequency switching components. Using external filter we can achieve clean DC output immune to switching harmonics across wide load conditions

Table 17. Transient Response

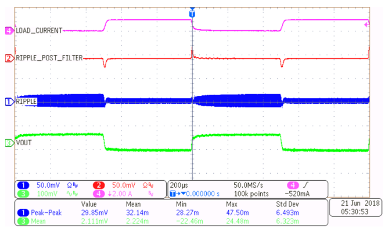
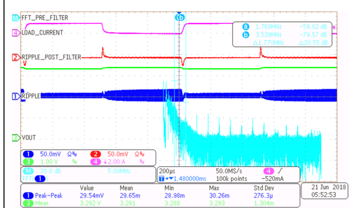
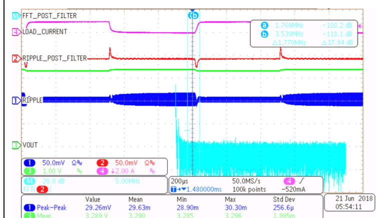
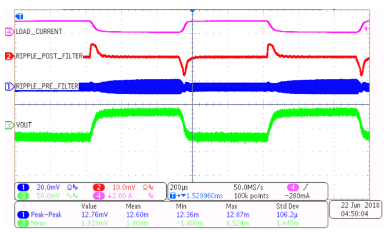
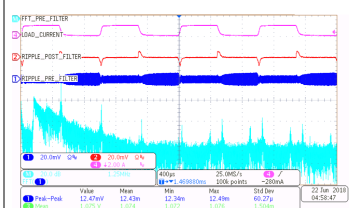
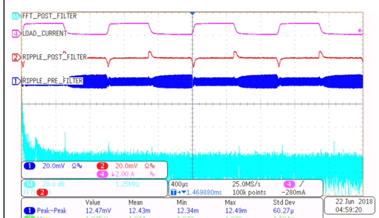
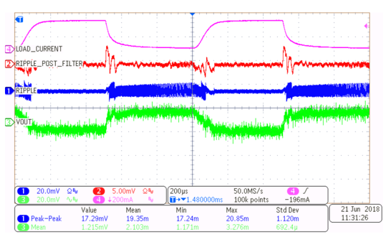
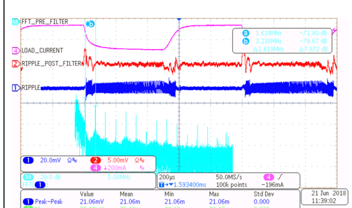
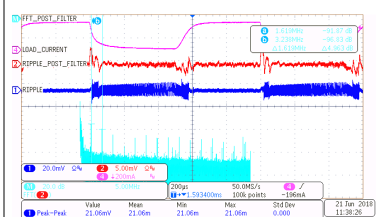
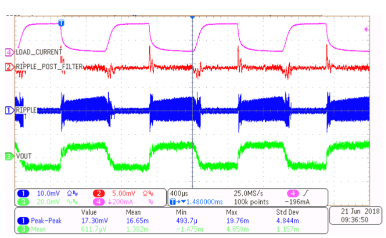
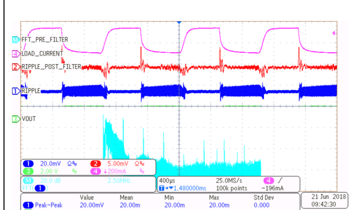
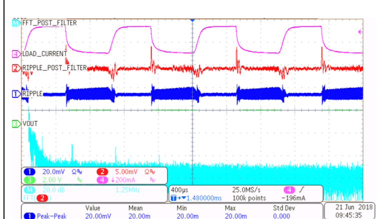
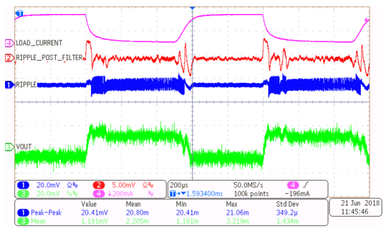
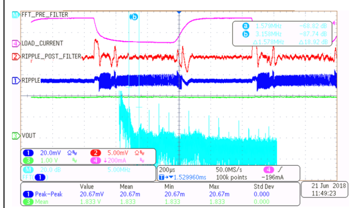
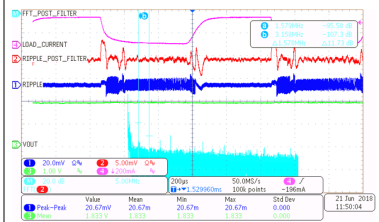
OUTPUT RAIL	TRANSIENT LOAD (AC COUPLED)	PRE FILTER	POST FILTER
3.3 V	 Figure 77. Transient AC Coupled	 Figure 78. Transient Pre-Filter FFT	 Figure 79. Transient Post-Filter FFT
1.1 V	 Figure 80. Transient AC Coupled	 Figure 81. Transient Pre-Filter FFT	 Figure 82. Transient Post-Filter FFT
1.35 V	 Figure 83. Transient AC Coupled	 Figure 84. Transient Pre-Filter FFT	 Figure 85. Transient Post-Filter FFT
1.2 V	 Figure 86. Transient AC Coupled	 Figure 87. Transient Pre-Filter FFT	 Figure 88. Transient Post-Filter FFT

Table 17. Transient Response (continued)

OUTPUT RAIL	TRANSIENT LOAD (AC COUPLED)	PRE FILTER	POST FILTER
1.8 V	 Figure 89. Transient AC Coupled	 Figure 90. Transient Pre-Filter FFT	 Figure 91. Transient Post-Filter FFT

7.4 Sequencing

TIDA-01579 Board supports both passive and active sequencing. Resistor divider as shown in schematic can be modified to passive RC circuit to design passive sequencing. Generic passive sequencing has been implemented and tested to meet most common sequencing for Core Voltage (1.1 V), DDR3L Voltage (1.35 V) and 3.3-V rail. Using Port expander and Power Good output of DC/DC digital sequencing is also possible

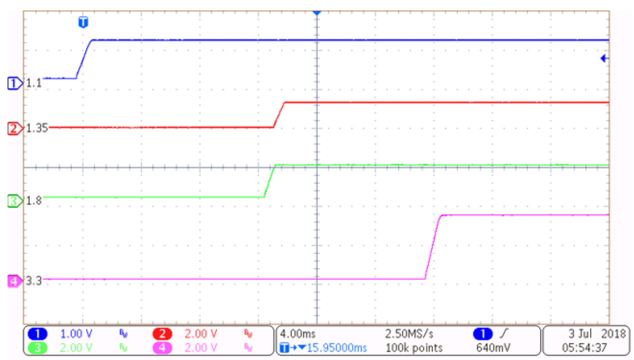


Figure 92. Passive Sequencing 0.1 V, 1.35 V, 3.3 V, and 1.8 V

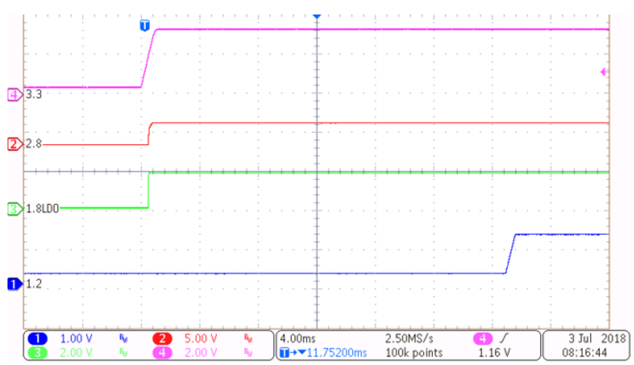


Figure 93. Passive Sequencing 2.8 V, 1.8 V, and 1.2 V

7.5 Thermal Performance

TIDA-01579 has been targeted to achieve very low thermal dissipation in small form factor. Using IR Thermal Gun at full load condition we see the overall board temperature is below 45°C at room temperature

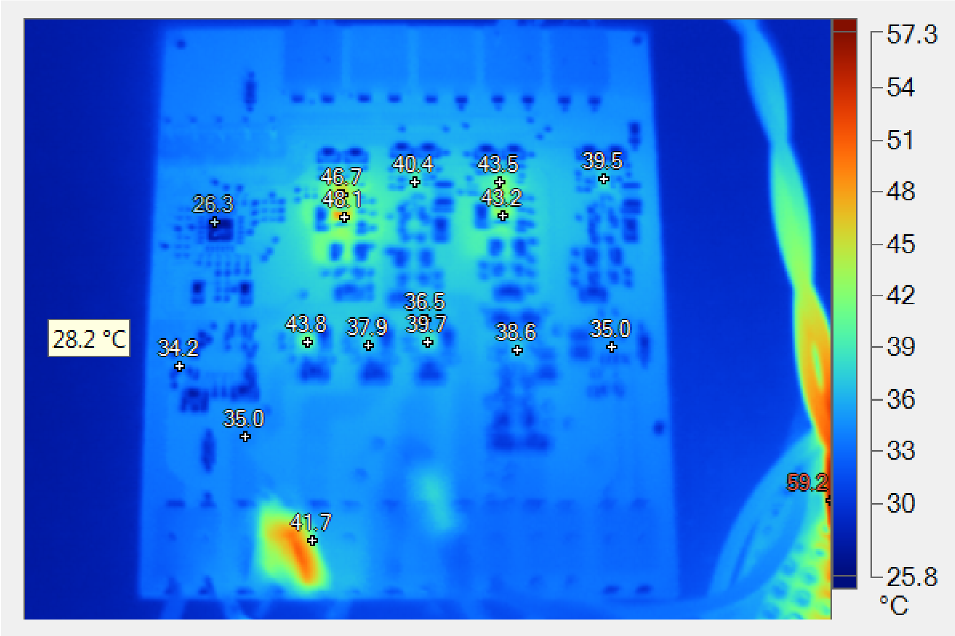


Figure 94. Thermal Performance

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-01579.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01579.

8.3 PCB Layout Recommendations

8.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01579.

8.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01579.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01579.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01579.

9 Related Documentation

1. Texas Instruments, *TLV62568 1-A High Efficiency Step-down Converter in SOT23 Package Data Sheet*
2. Texas Instruments, *TPS6282x 6-V, 1-,2-,3-A Step-Down Converter with DCS-Control™ Data Sheet*
3. Texas Instruments, *TLV742P 200mA, Small-Size, Low-Droput Linear Voltage Regulator Data Sheet*
4. Texas Instruments, *TCA9535 Low Voltage 16-Bit I2C and SMBus Low-Power I/O Expander Data Sheet*
5. Texas Instruments, *TPS61169 38-V High Current-Boost WLED Driver with PWM Control Data Sheet*
6. Texas Instruments, *TPS22976 5.7-V, 6-A, 14-mΩ On-Resistance Dual-Channel Load Switch Data Sheet*

9.1 Trademarks

10 About the Author

SRINIVASAN IYER is a Systems Architect at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Srinivasan has expertise in power supply and analog circuit for Imaging , Video Processing, High Speed and Motor Control Systems.

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