TI Designs: TIDEP-0100
AM570x Six-Layer Reference Design

Description

This reference design focuses on system-level cost-saving tactics. Key areas affecting fabrication costs are the number of PCB layers and via drill size. The AM570x features a package with *via channel arrays*. These channels make it possible to build the PCB in only six layers while still achieving 100% signal breakout. The added room helps with signal breakout and routing while avoiding the need for smaller, costlier drill bits for the vias. Another added benefit of larger vias is improved via reliability and electrical performance.

This reference design is based on the Texas Instruments Sitara™ AM570x System on Chip (SoC). The source documents provided represent a board design that is tested for stability and compliance in certain key areas. Those areas are DDR stability, HDMI performance, oscilloscope captures of the power sequencing, and a power design network (PDN) integrity analysis.

Resources

TIDEP-0100	Design Folder
AM570x	Product Folder
TPS65916	Product Folder

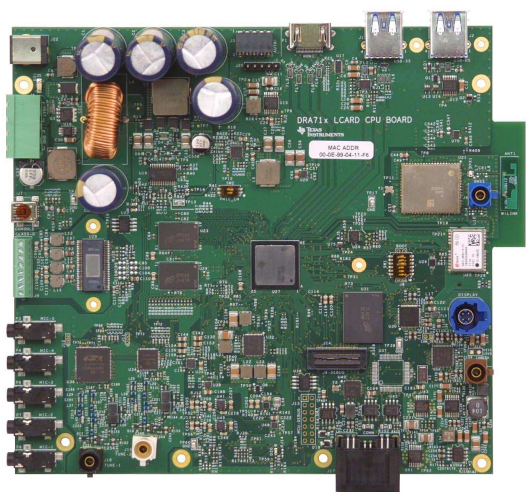
TI E2E™ Community — ASK Our E2E™ Experts

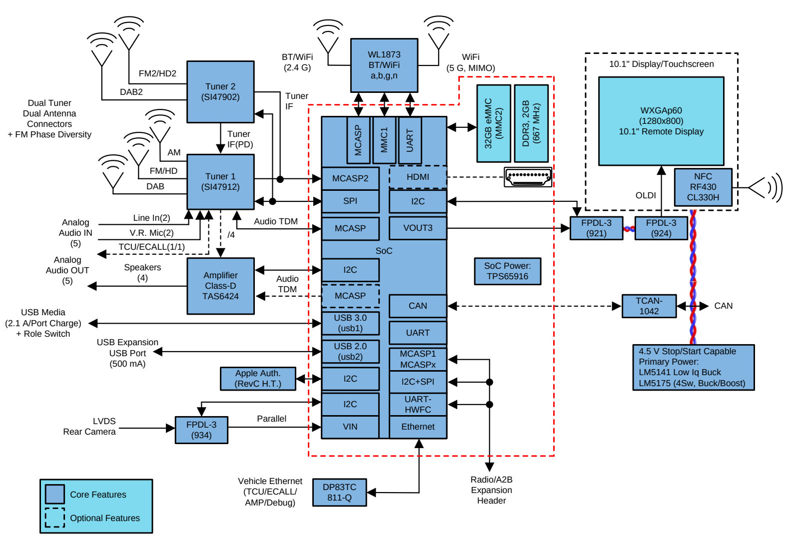
Features

- Sitara AM570x System on Chip (17 × 17 mm)
- Reference Design Files for Six-Layer Board
- 100% Signal Breakout and Routing for All Signals
- SerDes Routing for DDR, HDMI, USB3, and CSI-2
- Reference Power Design With TPS65916 PMIC

Applications

- Industrial Communication
- Factory Automation
- Grid Infrastructure
- Voice and Audio Processing





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1 System Description

This reference system is built to meet the key specifications listed in Table 1. This automotive design is compatible with the AM570x family of processors. The targeted application for this board is in entry-level infotainment systems and vehicle head units. Figure 1 shows the block diagram. The reference design files provided are intended to assist in the design of a custom board focused on the portion selected by the red dotted line. The needs of user applications can vary, so features are intended to be added or removed. Software support in the Processor SDK is not officially available. However, useful software references for U-Boot and the Linux kernel are available at the TIDEP-0097 tool page.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input power	Variable power supply, 12 V nominal	Section 2.2.2
Power brownout	System can run as low as 6 V	Section 2.2.3
Power blackout	System has 50 ms of backup energy	Section 2.2.4
Power sequencing	TPS65916 PMIC, all-in-one SoC power solution	Section 2.3.2
Low-cost design	Low PCB layer count, via channels	Section 2.4

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2 System Overview

2.1 Block Diagram

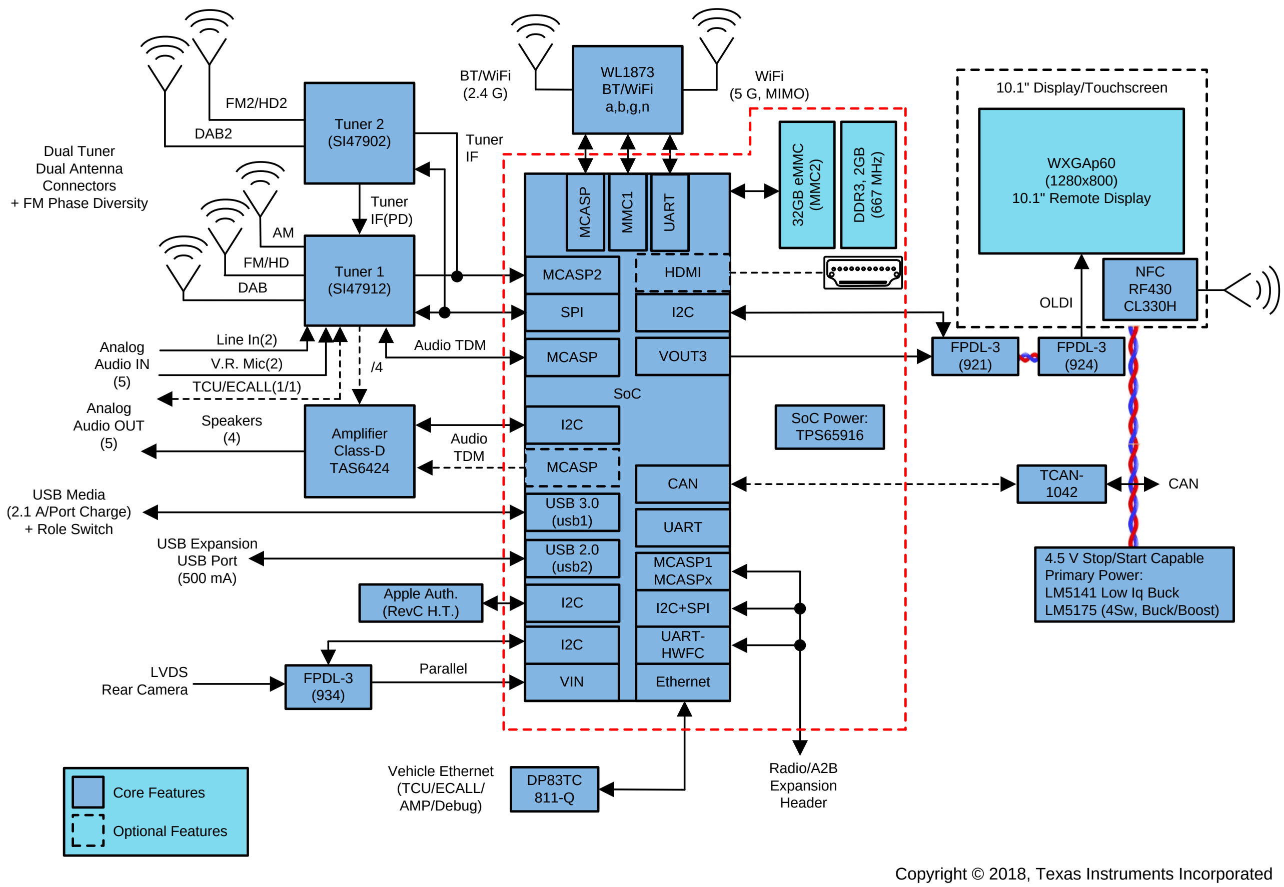

Figure 1. TIDEP-0100 Block Diagram

2.2 Design Considerations

2.2.1 AM570x System on Chip

For overall design considerations, see the *AM57xx Schematic Checklist* [3] when designing for the AM57xx family of SoCs. Compared to the AM572x and the AM571x, this device features a simplified power supply rail mapping to enable lower cost power management IC (PMIC) solutions. The AM570x device also adds the MIPI CSI-2 interface not found in the AM572x.

2.2.2 Power Architecture

The TPS65916 PMIC is designed to provide all the power rails needed for the AM570x SoC using mainly the 3.3-V supply and the 5.0-V supply as needed for USB. Depending on the application requirements, a first-stage power supply can be used if 3.3-V and 5.0-V rails are not already available.

This reference design has optimized the power architecture to be used with a 12-V power source similar to a car battery. The input source can be variable from 6 V to 16 V, so the first stage supplies are a boost converter to 16 V and a buck converter to 3.3 V. The 16 V is used for the media hub, display module, and 5.0-V USB power. The 16 V is also bucked down to 10.5 V to be used for sensor ports and modules. The 3.3 V is the input to the TPS65916.

A good design reference is the *TPS65916 User's Guide to Power AM570x* [1].

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2.2.3 Power Brownout

When the input supply dips for a short time, this is called a power brownout. Brownouts can occur when a load is activated (for example, a motor starting, turning on Wi-Fi®, or processor transient). Use a first-stage boost converter before generating the 10.5-V and 5.0-V supplies to guarantee their reliable operation. The input supply can operate anywhere between 6 V to 16 V.

2.2.4 Power Blackout

A sudden power loss causes an uncontrolled power-down sequence that can permanently damage the SoC. Therefore, the design includes a TPS3808 voltage supervisor to monitor the input line for any drops below 4.6 V. The supervisor output is wired to initiate the PMIC ACT2OFF shutdown sequence by pulling PMIC_EN low. To make sure the PMIC stays on long enough to complete a graceful shutdown sequence (about 1.5 ms), there must be enough capacitance at the PMIC input to serve as reserve energy.

In this reference design, four parallel 2200-µF capacitors act as a small energy reserve to keep the PMIC operational for as long as 50 ms while the source power input is lost before initiating shutdown. This protection keeps the system operational while providing immunity to repeated voltage dropouts that can occur.

2.2.5 High-Definition Multimedia Interface (HDMI)

The design includes an integrated HDMI, which is supported on a type-A HDMI connector. The interface supports up to 1080p60 with 24-bit color. A communication channel (DDC/CEC) is supported to the HDMI connector for communication with the HDMI panel. A 5.0-V supply is needed for the TPD12S016 HDMI companion chip which provides level translation for the DDC/CEC and hot-plug detect signals between the SoC and HDMI connector.

2.2.6 Universal Serial Bus (USB)

The design includes two integrated USB transceivers. USB3.0 super-speed bus (USB-SS) is supported using port USB-SS to a USB3.0 type-A connector. This interface supports up to 5 Gbps and can operate in host or device mode. Also included is a USB2.0 high-speed interface HUB (USB-HS) and can support rates up to 480 Mbps. All USB interfaces can supply VBUS to peripheral when in host mode by enabling VBUS switch; however, the design cannot be powered from VBUS when in device mode.

2.2.7 Dual-Voltage SD/MMC UHS-I Cards

LDO1 on the TPS65916 PMIC is configured to meet the power supply requirements of newer dual-voltage SD cards. At start-up, the BOOT pin is held high for load-switch mode. The 3.3-V LDO1 input is delivered to the LDO1 output directly. During UHS-1 speed negotiations a GPIO pin from the SoC drives the BOOT pin low causing the PMIC to regulate LDO1 to 1.8 V. Connect the LDO1 output to the VDDSHV8 input of the AM570x SoC as well.

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2.3 Highlighted Products

This reference design features the following TI devices:

- AM570x SoC
- TPS65916 PMIC

For more information, see their corresponding data sheets.

2.3.1 AM570x System on Chip

The Sitara AM570x SoC is purpose built to meet the processing needs of modern embedded systems. The Sitara family provides flexible processor solutions by delivering a tight integration of mixed processing cores with a rich peripheral set. Target applications can be industrial or multimedia centric. Examples include home and factory automation, industrial Ethernet, human machine interfaces, 2D and 3D accelerated graphics, voice and multichannel audio processing, video encode and decode, and digital signage solutions.

Key features of this device include:

- Arm® Cortex®-A15 MPU
- C66x floating-point DSP
- Video, image, and graphics processing support:
  – Full-HD video (1920 × 1080 p, 60 fps)
  – Parallel CMOS and MIPI CSI-2 camera inputs
  – 2D and 3D graphics cores
  – HD image and video accelerator core
- Two Arm Cortex-M4 cores
- DDR3/DDR3L memory interface
- HDMI 1.4a compliant encoder
- SuperSpeed USB3.0 dual-role interface

2.3.2 TPS65916 Power Management IC

The TPS65916 PMIC integrates four configurable step-down converters with up to 3.5 A of output current to power the processor core, memory, I/O, and pre-regulation of low-dropout (LDO) regulators. The power-sequence controller uses one-time programmable (OTP) memory to control the power sequences as well as default configurations such as output voltage and GPIO configurations. The OTP is factory programmed to allow start-up without any required software.

Key features of this device include:

- Four switching regulators with integrated FETs
- Four LDO linear regulators
- Power sequencing for the AM570x SoC
- System voltage range from 3.135 V to 5.25 V
- Support for dual-voltage SD/MMC UHS-I cards
- 7×7-mm QFN package, 0.5-mm pitch

For more information, see *TPS65916 User's Guide to Power AM570x* [1].

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2.4 System Design Theory

This section discusses the critical design elements from a hardware standpoint, which includes the AM570x SoC, PMIC, DDR3L, and high-speed interfaces included in this design. This reference design has 100% breakout of all the signals from the SoC.

2.4.1 Six-Layer PCB Design

The theory behind a six-layer PCB is to summarize the low-cost aspect of this design. A PCB with fewer layers lowers the cost of manufacturing because there are fewer layers to be fabricated. When reducing the number of layers on a PCB, the power distribution and signal integrity must be taken into account to ensure there is not a quality decline. When PCB designing, focus on both the high-speed, differential SerDes signaling breakout and routing as well as matching DDR3L routing—both of which must be routed first when designing. A few key parameters to define for each PCB design are the PCB stack-up and routing plan, controlled impedance plan, and SoC breakout scheme.

2.4.2 VCA versus BGA

A full ball grid array (BGA) for the AM570x is 625 balls. If unused or voided balls are removed from the package, a via channel array (VCA) is created. Eighty-seven balls are voided on the SoC to create a VCA, which leaves 538 balls to be supported. Creating a VCA package enables routing channels to escape inner most BGA positions and reduce the number of routing layers for 100% signal breakout. A big advantage of VCA is the allowance of larger breakout via land and drill diameters. Smaller via diameters require smaller drill bits that cost more money and more precise manufacturing. Larger via diameters lowers PCB manufacturing costs and also improves PCB reliability and performance. The power integrity of power and ground planes improves, the impedance versus frequency response lowers, and the current density or carrying capacity to the inner most ball positions is maintained.

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2.4.3 Via Breakout Scheme

The reference board is *Class 2*, as classified by IPC, and "includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical." By following the Class 2 guidelines, there are unique aspects of the design scheme:

- Package solder mask opening (SMO) to PCB land diameters aspect ratio = 0.350 / 0.300 mil, which yields the same board level reliability (BLR) performance as the initial aspect ratio of 0.350 / 0.350 mil
- 16/8 breakout via: via pad/land diameter = 16 mil, via drill diameter = 8 mil
- Centering via between balls

Because the BLR performance is the same as a 1:1 aspect ratio, the smaller land diameter enhances the via centering scheme. With an IPC Class 2 classification, there is a specification that allows *90° partial via breakout*, which means the via drill edge can extend beyond via land by approximately 1.2 mil. Figure 2 shows the breakout scheme.

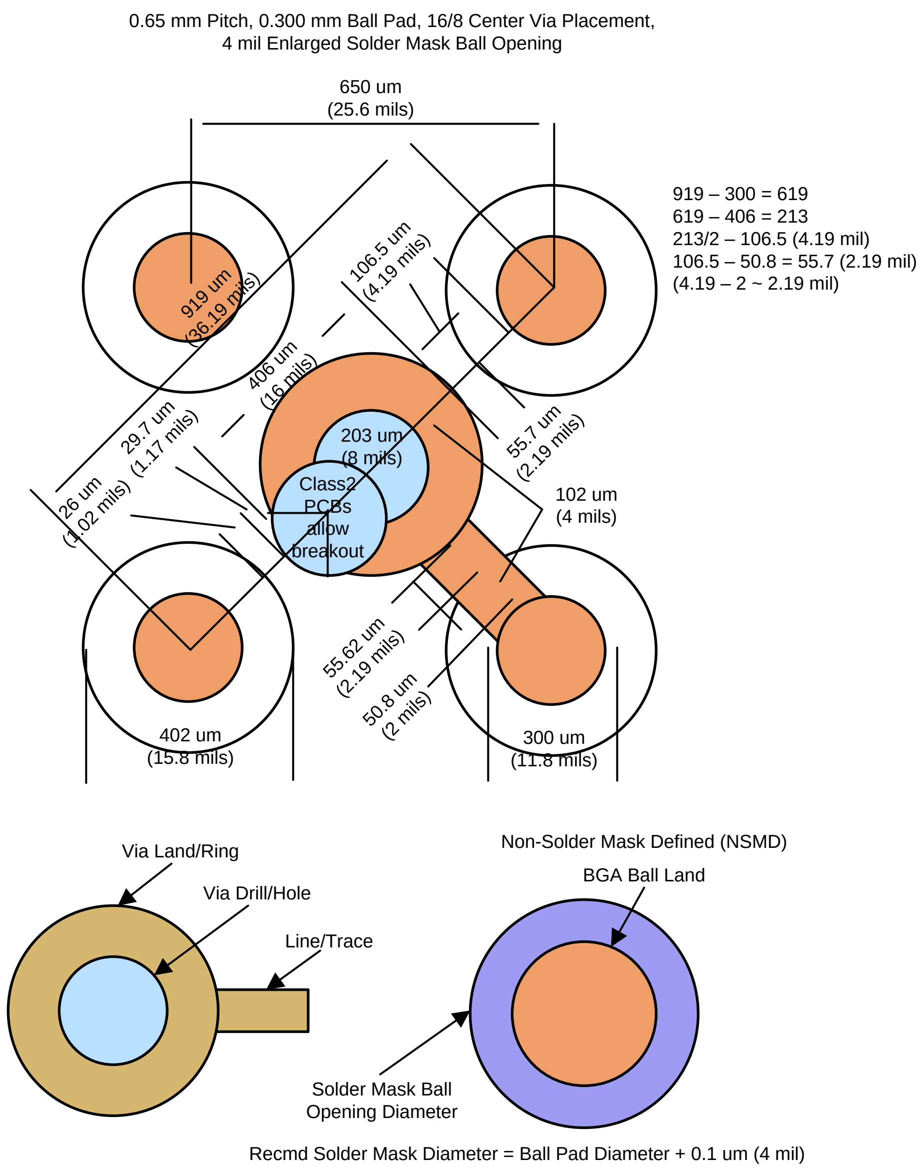

Figure 2. 16/8 Center Via Placement Breakout Scheme

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A key advantage of this breakout is reduced PCB costs from 9% to 18% by center locating vias under the SoC and eliminating the *non-conductive via fill* step. During the *via fill* step, the via is placed between the balls with a larger land diameter and risks wicking solder into the via from the balls during the soldering process. Another advantage of center locating the via is impedance versus frequency response improves because the power and ground routing is closer to the balls in this scheme. A modified via land shape must be implemented, which is called *filleting*. The shape looks similar to a tear drop and prevents the via breaking out onto the etch and potentially causing an open at that point.

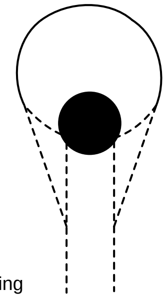

Figure 3. Modified Via Land Shape

2.4.4 Power Distribution Network (PDN)

For the block diagram of the PMIC-to-SoC connections, see Figure 1 in the *TPS65916 User's Guide to Power AM570x* [1].

2.4.4.1 Power-Up Sequence

For the verified SoC power-up sequence, see Appendix A. This sequence has been verified to meet the power-up sequence requirements.

2.4.4.2 Power-Down Sequence

For the verified SoC power-down sequence, see Appendix B. This sequence has been verified to meet the power-down sequence requirements.

2.4.4.3 Power Distribution Network (PDN)

Key device processor high-current power domains must be evaluated for power rail IR drop, decoupling capacitor loop-inductance, and power rail target impedance. The PDN performance of a PCB can only be truly accessed by comparing these model PI parameters versus TI's recommended values. Table 2 shows the recommended values to achieve when conducting a PDN test. These supplies are tested in the included results. For more detailed content, see the *AM570x Sitara Processor Data Sheet* [2].

Table 2. Processor Recommended PDN and Decoupling Characteristics

PDN ANALYSIS	STATUS	DYNAMIC			NUMBER OF RECOMMENDED DECOUPLING CAPACITORS							
SUPPLY	MAXIMUM R_{eff} (mΩ)	DECOUPLING CAPACITORS MAXIMUM LL (nH)	MAXIMUM IMPEDANCE (mΩ)	FREQUENCY RANGE OF INTEREST (MHz)	100 nF	220 nF	470 nF	1 µF	2.2 µF	4.7 µF	10 µF	22 µF
vdd_dsp	22	2.5	54	≤20	6	1	1	1	1	1		1
vdd	18	2	57	≤20	6	1	1	1	1		1	
vdds_ddr1	33	2.5	200	≤50	8	3		2		2		1

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2.4.4.4 PDN Simulation Results

For simulation results regarding the main SoC power rails, see Appendix C. The simulation results for each rail includes effective resistance, loop inductance, static voltage drop, and target impedance.

2.4.5 High-Speed Differential (HSD), DDR3L Routing

Differential pairs must be etched properly to have matching length and coupling. With high-speed interfaces, such as DDR memory, USB3.0, and HDMI, proper etching is crucial especially because a six-layer design has fewer layers, which leaves less space for all components to be etched on the PCB. When designing the PCB, the differential pairs must be laid out first to have all the matching lengths and isolation before populating with other etches. Figure 4 shows some of the etching of differential signals on the reference design.

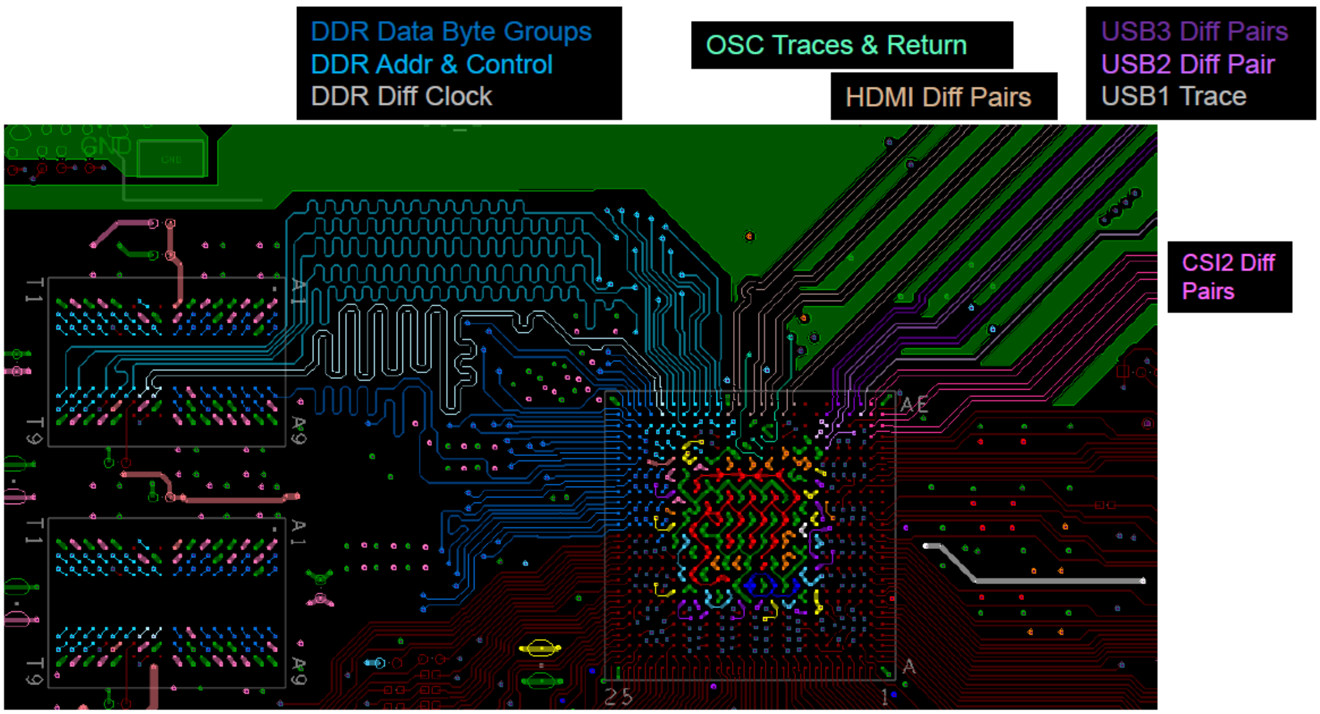

Figure 4. High-Speed Signaling Breakout Overview (Top Layer)

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3 Testing and Results

3.1 DDR3L-1333 Memory Testing

The following output shows the memory testing results. Follow the memory routing on the PCB closely to ensure that similar results can be achieved.

```
root@jacinto6evm:/ # memtester-4.3.0 1G 1
memtester version 4.3.0 (32-bit)
Copyright (C) 2001-2012 Charles Cazabon.
Licensed under the GNU General Public License version 2 (only).

pagesize is 4096
pagesizemask is 0xfffff000
want 1024MB (1073741824 bytes)
got  1024MB (1073741824 bytes), trying mlock ...locked.
Loop 1/1:
  Stuck Address       : ok
  Random Value        : ok
  Compare XOR         : ok
  Compare SUB         : ok
  Compare MUL         : ok
  Compare DIV         : ok
  Compare OR          : ok
  Compare AND         : ok
  Sequential Increment: ok
  Solid Bits          : ok
  Block Sequential    : ok
  Checkerboard        : ok
  Bit Spread          : ok
  Bit Flip            : ok
  Walking Ones        : ok
  Walking Zeroes      : ok
  8-bit Writes        : ok
  16-bit Writes       : ok

Done.
```


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3.2 HDMI Test Results

HDMI testing is performed with the device configured for a pixel clock frequency of 148.50 MHz. The bandwidth provided yields a resolution of 1080p60, also known as 1920×1080 at 60 Hz. Table 3 shows the results of the HDMI testing. Figure 5 captures the HDMI eye diagram.

Table 3. HDMI Test Results at 148.50 MHz

INDEX	TEST NAME	LANES	SPEC RANGE	MEAS VALUE	RESULT
1	7-9: Source clock jitter	CK	Clock jitter < 0.25*Tbit	0.075*Tbit	Pass
2	7-10: Source eye diagram	CK - D0	Data jitter < 0.3*Tbit	0.12*Tbit	Pass
3	7-10: Source eye diagram	CK - D1	Data jitter < 0.3*Tbit	0.1*Tbit	Pass
4	7-10: Source eye diagram	CK - D2	Data jitter < 0.3*Tbit	0.1*Tbit	Pass
5	7-6: Source inter-pair skew	D0 - D1	Skew < 0.2*TPixel	0.001*TPixel	Pass
6	7-6: Source inter-pair skew	D1 - D2	Skew < 0.2*TPixel	0.006*TPixel	Pass
7	7-6: Source inter-pair skew	D2 - D0	Skew < 0.2*TPixel	0.005*TPixel	Pass
8	7-4: Source rise time	CK	75.00 ps < TRISE	239.07 ps	Pass
9	7-4: Source rise time	D0	75.00 ps < TRISE	219.56 ps	Pass
10	7-4: Source rise time	D1	75.00 ps < TRISE	222.28 ps	Pass
11	7-4: Source rise time	D2	75.00 ps < TRISE	232.10 ps	Pass
12	7-4: Source fall time	CK	75.00 ps < TFALL	243.51 ps	Pass
13	7-4: Source fall time	D0	75.00 ps < TFALL	207.81 ps	Pass
14	7-4: Source fall time	D1	75.00 ps < TFALL	217.58 ps	Pass
15	7-4: Source fall time	D2	75.00 ps < TFALL	226.33 ps	Pass
16	7-8: Maximum duty cycle	CK	Maximum duty cycle < 60.0%	50.19%	Pass
17	7-8: Minimum duty cycle	CK	40.0% < Minimum duty cycle	49.3%	Pass

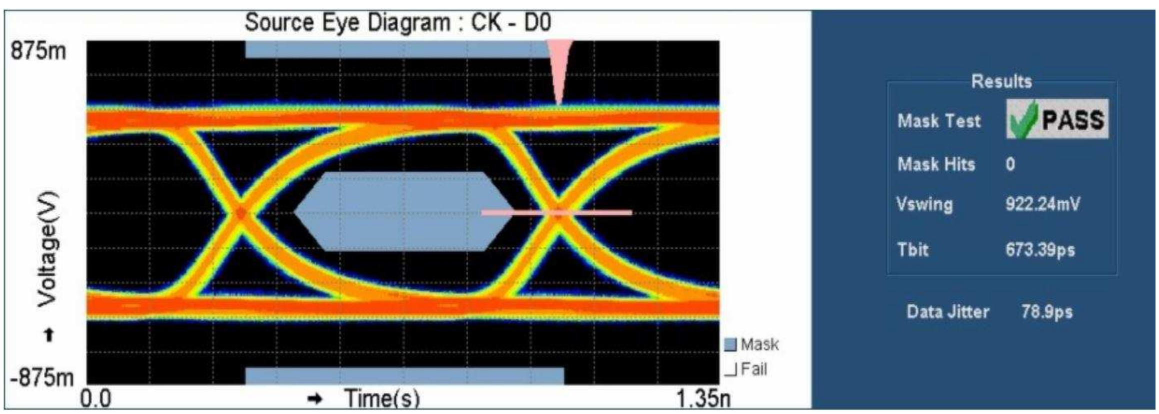

Figure 5. HDMI Eye Diagram Waveform

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDEP-0100.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP-0100.

4.3 PCB Layout

To download the layer plots, see the design files at TIDEP-0100.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDEP-0100.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP-0100.

5 Related Documentation

1. Texas Instruments, *TPS65916 User's Guide to Power AM570x*
2. Texas Instruments, *AM570x Sitara Processor Data Sheet*
3. Texas Instruments, *AM57xx Schematic Checklist Wiki*
4. Texas Instruments, *High-Speed Interface Layout Guidelines Application Report*
5. Texas Instruments, *AM572x GP EVM Power Simulations Application Report*
6. Texas Instruments, *AM57xx BGA PDB Design Application Report*

5.1 Trademarks

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6 About the Authors

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Appendix A Power-up Sequencing

This appendix shows oscilloscope images of the initial power-up sequence of the TPS65916 PMIC.

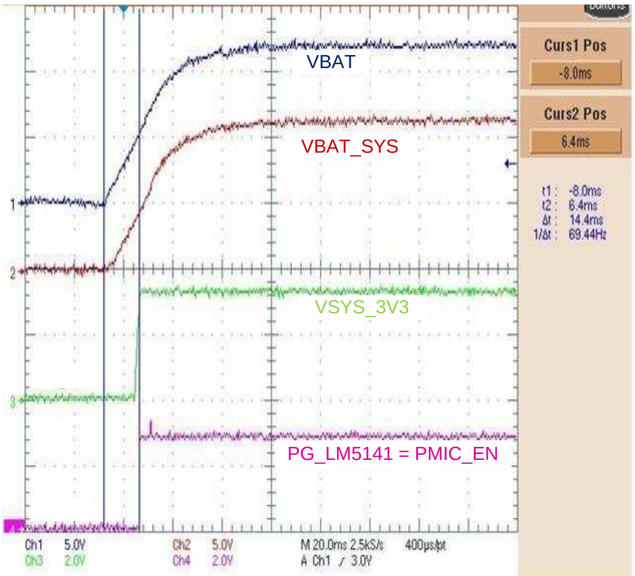

Figure 6. Initial Front-End Power-up Stage of Design

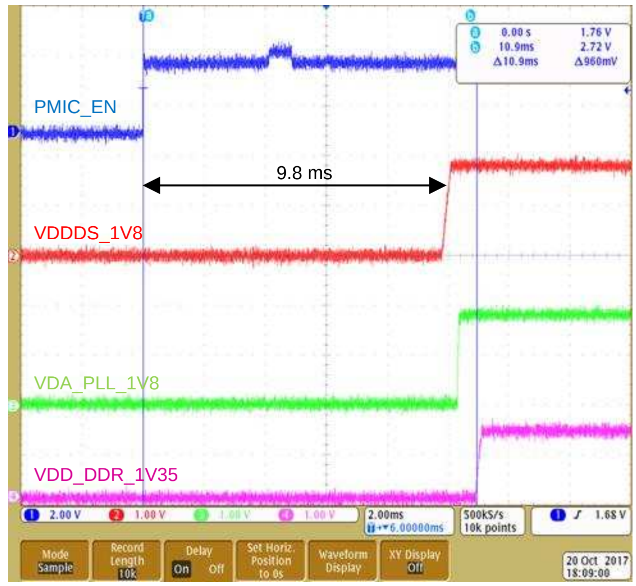

Figure 7. TPS65916 Stages 1 to 3 Power-up

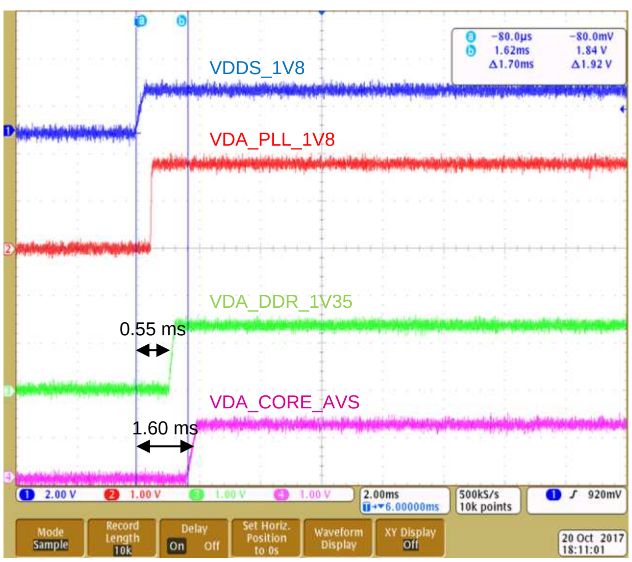

Figure 8. TPS65916 Stage 4 and 5 Power-up

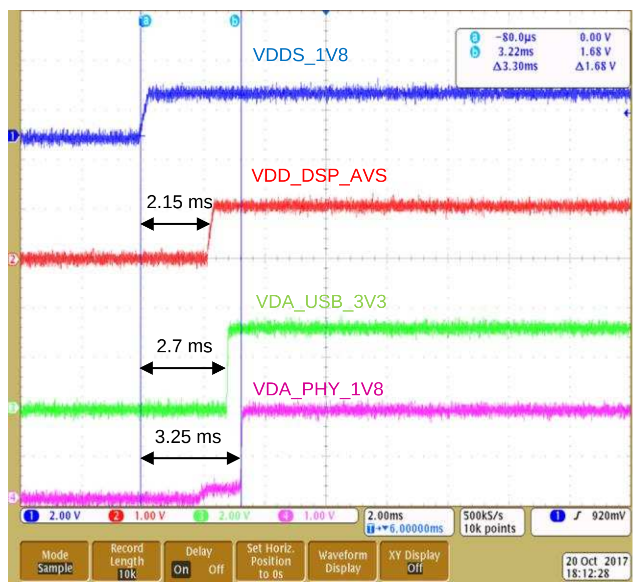

Figure 9. TPS65916 Stages 6 to 8 Power-up

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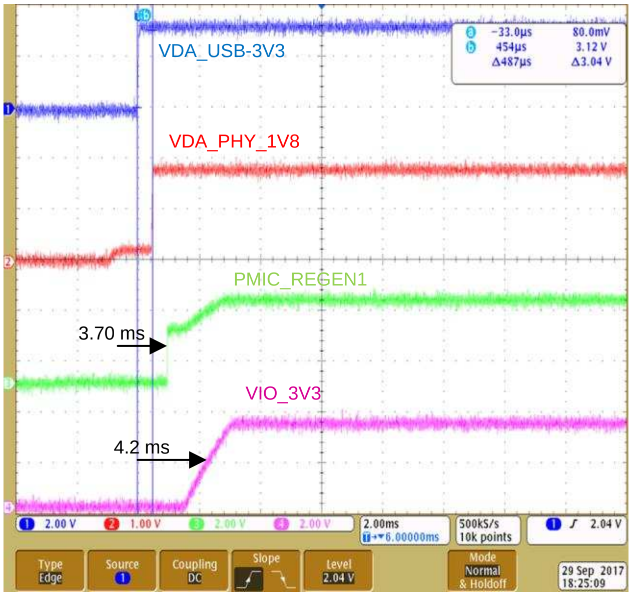

Figure 10. TPS65916 Stages 7 to 10 Power-up

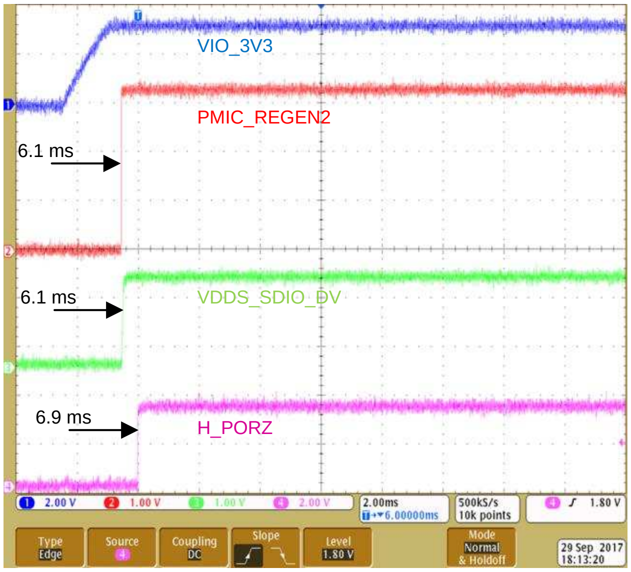

Figure 11. TPS65916 Stages 10 to 13 Power-up

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Appendix B Controlled Power-Down Sequence

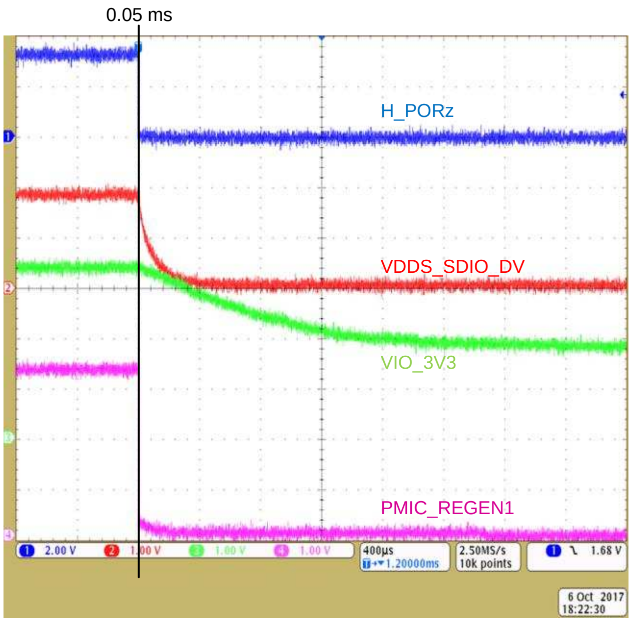

Figure 12. TPS65916 Stage 1 Power Down

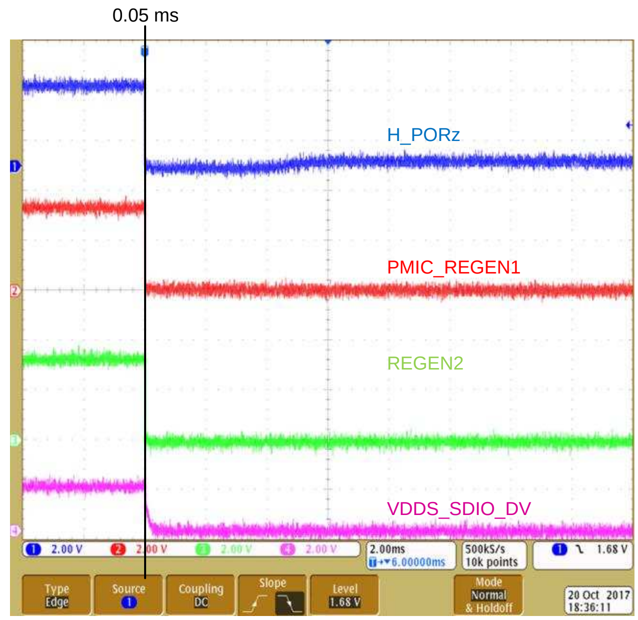

Figure 13. TPS65916 Stage 1 Power Down (Cont.)

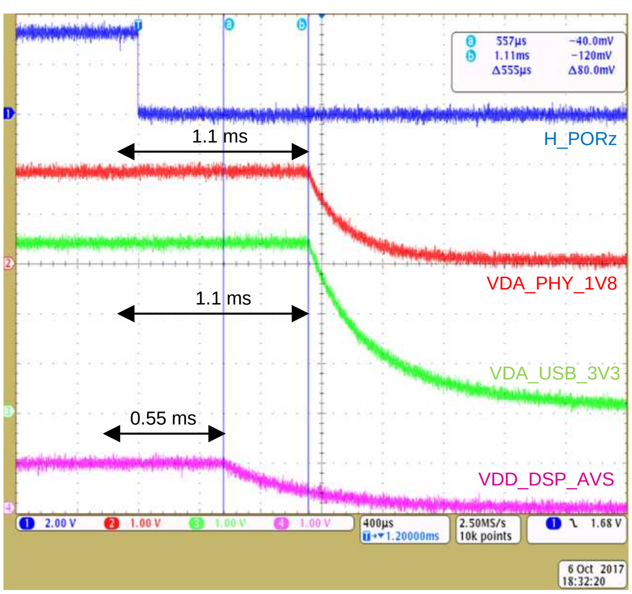

Figure 14. TPS65916 Stage 2 and 3 Power Down

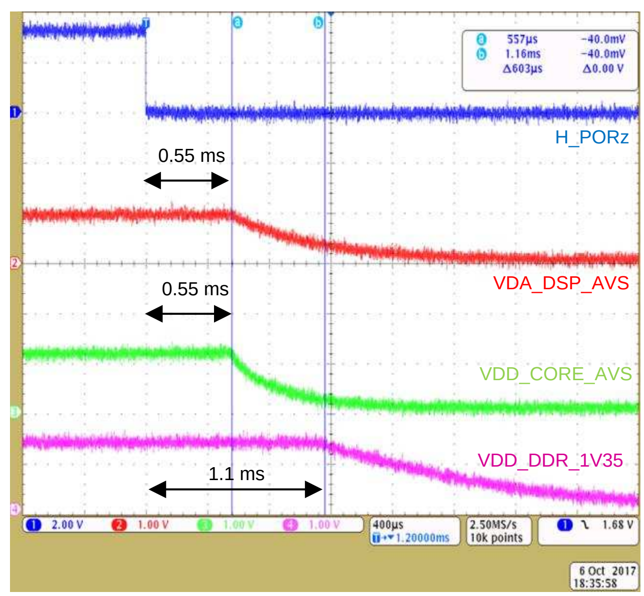

Figure 15. TPS65916 Stage 2 and 3 Power Down (Cont.)

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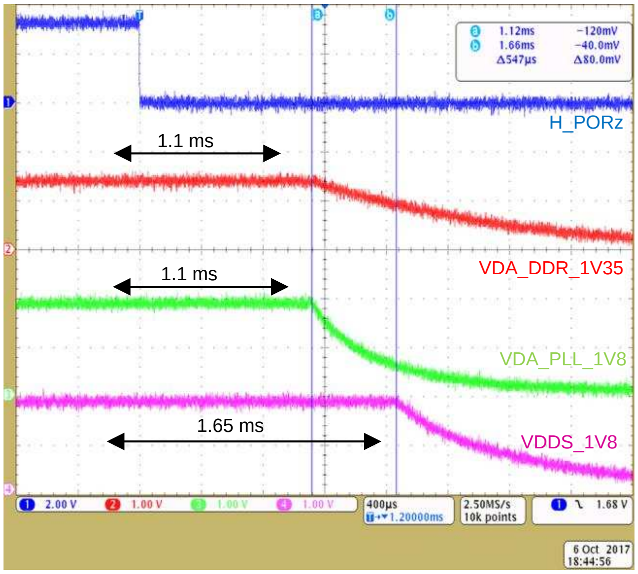

Figure 16. TPS65916 Stage 3 and 4 Power Down

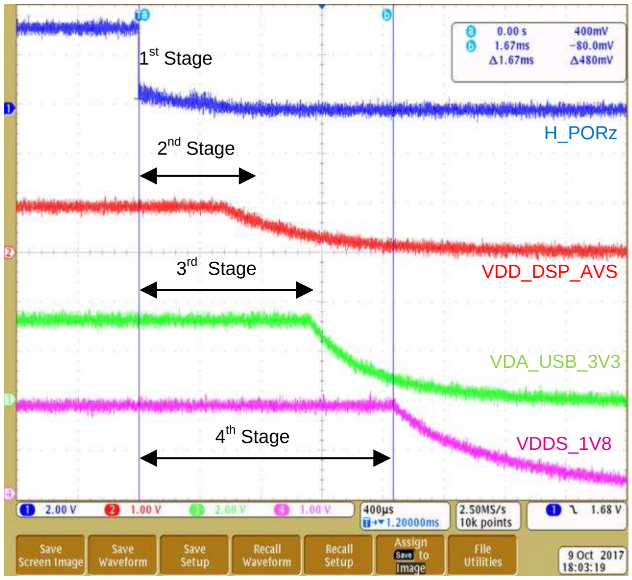

Figure 17. TPS65916 All Four Stages of Power Down

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Appendix C Reference Board Power Integrity Analysis (PIA)

This appendix analyzes the PDN and provides the effective resistance, loop inductance, and target impedance of the three main power rails to the SoC. The effective resistance (static impedance) is the measurement of a rail's static voltage drop divided by a test current. Loop inductance (LL) measures trace inductance of the power and ground loop to each capacitor. Distance is measured from the center of the BGA ball to the center of the capacitor pad. The frequency response of a power rail (dynamic impedance) measured at a frequency of interest is the target impedance (T_z)

Table 4. Reference Design PIA Summary

DOMAIN NAME AND PRIORITY	LIMIT	EFFECTIVE RESISTANCE (R_{eff}) (mΩ) PMIC to SoC	LOOP INDUCTANCE (LL) (nH) at 50 MHz AVERAGE	TARGET IMPEDANCE (T_z) (mΩ) at (MHz)
1 - VDD_DSP_AVS	Measured	3.3	1.72	46
*VDD_DSP	Max	< 22	< 2.5	< 54 at 20 MHz
2 - VDD_CORE_AVS	Measured	6.1	1.56	25
*VDD	Max	< 18	< 2	< 57 at 20 MHz
3 - VDD_DDR_1V35	Measured	6.6	2.38	208
*VDDS_DDR1	Max	< 33	< 2.5	< 200 at 50 MHz
4 - CAP_VDDRAM_x	Measured		3.58 - 5.78 (min - max)	
*CAP_VDDRAM_x	Max		< 6	

C.1 VDD_DSP_AVS

Table 5. Effective Resistance of VDD_DSP_AVS

DERIVED FROM: V_{DROP} ANALYSIS						
NAME	V_{IN} (V)	V_{OUT} (V)	V_{DROP} (V)	CURRENT (A)	R_{eff} (Ω)	TARGET (mΩ)
VPO_S1_AVS	1.0000	0.9967	0.0033	1	0.0033	22.000

DERIVED FROM: DC ANALYSIS							
NET (FROM)	COMPONENT (FROM)	GROUP/PIN (FROM)	NET (TO)	COMPONENT (TO)	GROUP/PIN (TO)	R_{eff} (Ω)	SEGMENT WEIGHT
VDD_DSP_AVS	L18	Group4	VDD_DSP_AVS	U27	Group1	0.001842	51%
VDD_DSP_SW	L18	Group5	VDD_DSP_SW	U32	Group2	0.001773	49%
					TOTAL	0.003615	

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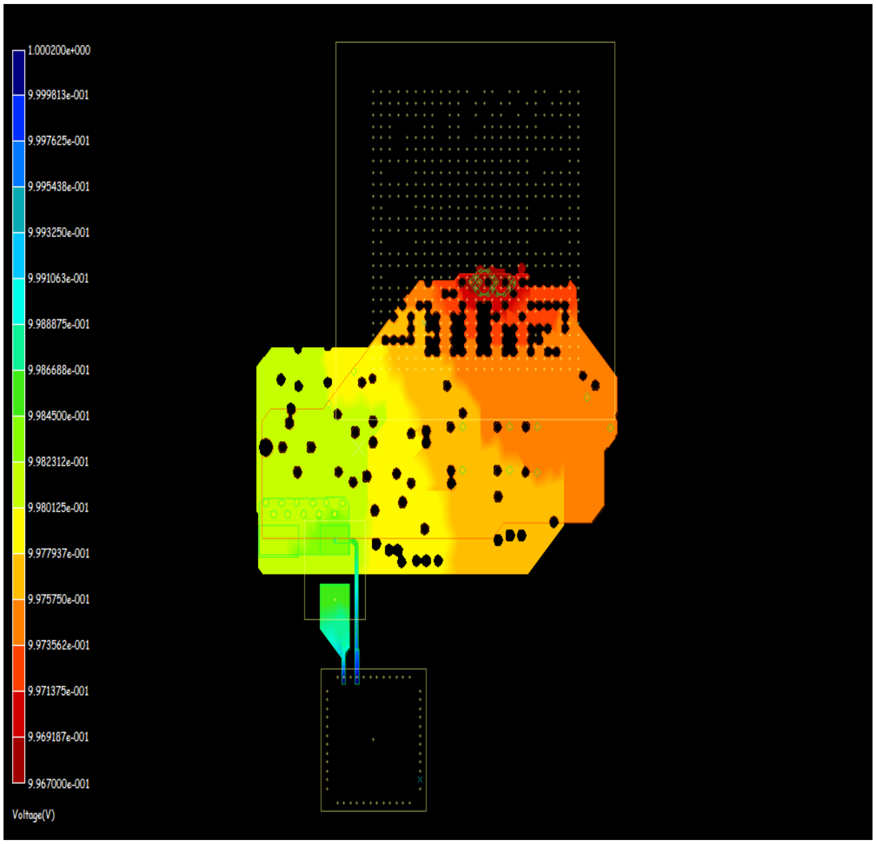

Figure 18. VDD_DSP_AVS IR Drop Analysis

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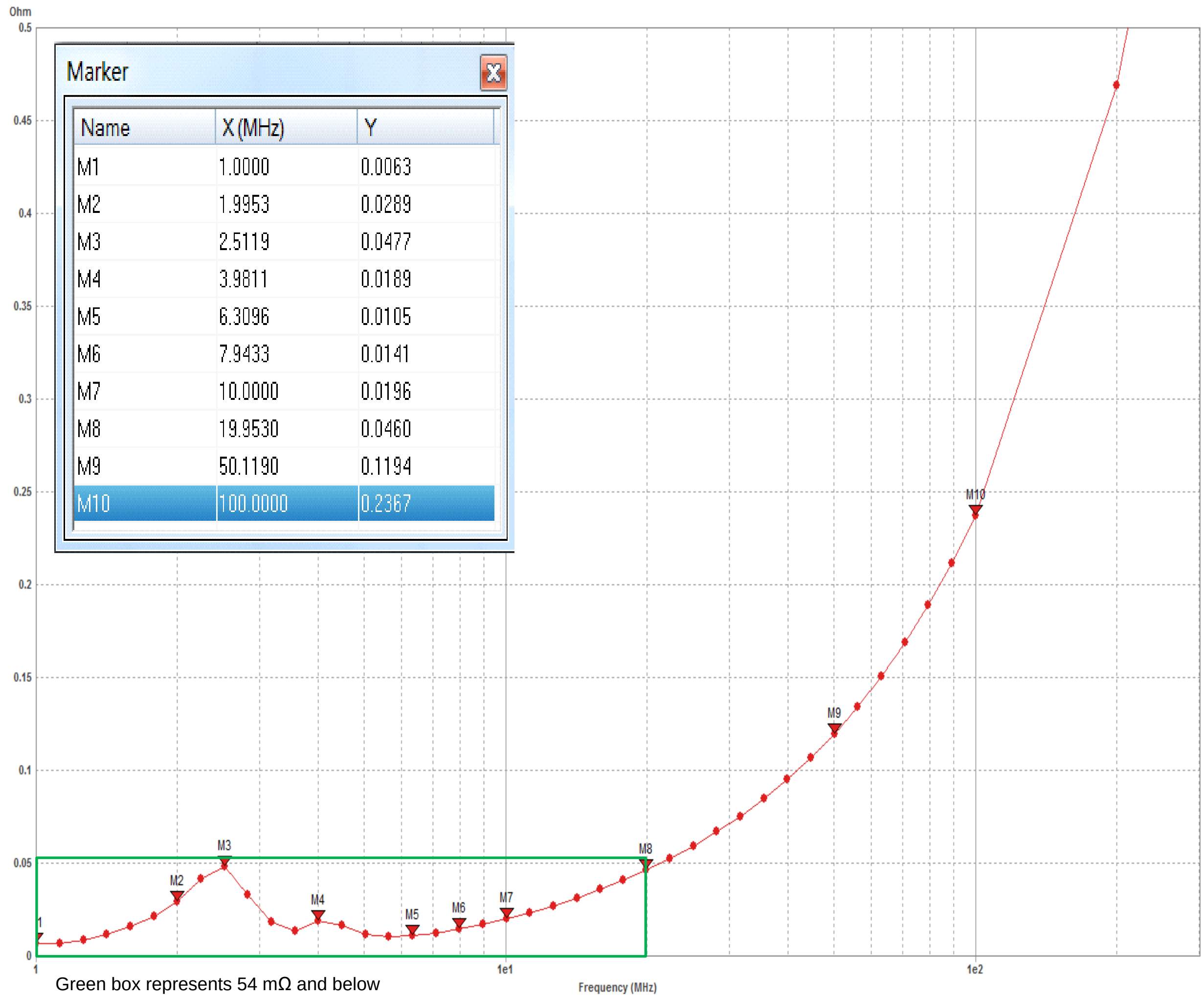

Figure 19. Target Impedance: VDD_DSP_AVS

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Table 6. Loop Inductance: VDD_DSP_AVS

TARGET CAP	LL at 50 MHz (nH)	FOOTPRINT TYPE	PCB SIDE	DISTANCE TO PIN (mils)	VALUE (µF)	SIZE
C357	1.605	2vWSE	Bottom—under BGA	81	0.47	0402
C361	0.998	2vWSE	Bottom—under BGA	58	0.47	0402
C362	1.3352	2vWSE	Bottom—under BGA	29	0.47	0402
C367	1.264	2vWSE	Bottom—under BGA	64	0.47	0402
C368	1.722	2vWSE	Bottom—under BGA	102	0.47	0402
C370	1.470	2vWSE	Bottom—under BGA	57	0.47	0402
C385	2.266	4vWSE	Bottom	518	1	0508
C393	2.062	4vWSE	Bottom	420	1	0508
C401	2.056	4vWSE	Bottom	381	1	0508
C402	1.924	4vWSE	Bottom	370	1	0508
C403	1.759	4vWSE	Bottom	389	1	0508
C536	1.947	Segmented	Bottom	432	10	1210
C537	1.968	Segmented	Bottom	385	10	1210
MINIMUM	0.998					
MAXIMUM	2.266					
AVERAGE	1.721					

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C.2 VDD_CORE_AVS

Table 7. Effective Resistance: VDD_CORE_AVS

DERIVED FROM: V_{DROP} ANALYSIS						
NAME	V_{IN} (V)	V_{OUT} (V)	V_{DROP} (V)	CURRENT (A)	R_{eff} (Ω)	TARGET (mΩ)
VDD_CORE	1.0000	0.9939	0.0061	1	0.0061	18.000

DERIVED FROM: DC ANALYSIS							
NET (FROM)	COMPONENT (FROM)	GROUP/PIN (FROM)	NET (TO)	COMPONENT (TO)	GROUP/PIN (TO)	R_{eff} (Ω)	SEGMENT WEIGHT
VDD_CORE_AVS	L23	Group167	VDD_CORE_AVS	U27	Group131	0.003899	64%
VDD_CORE_SW	L23	Group168	VDD_CORE_SW	U32	Group73	0.002182	36%
					TOTAL	0.006081	

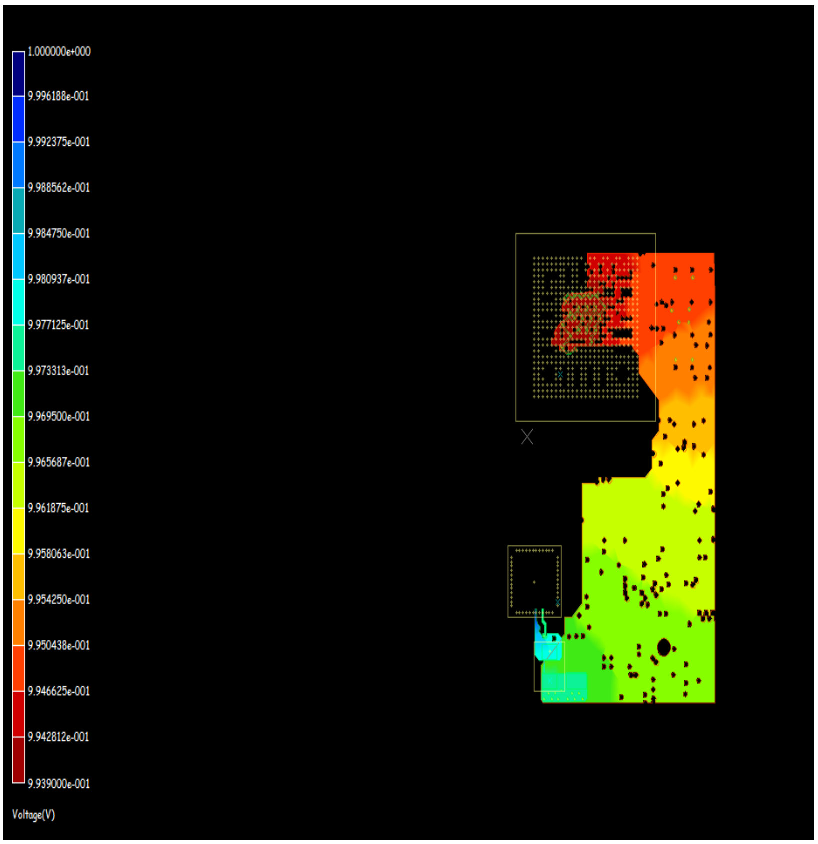

Figure 20. VDD_CORE_AVS IR Drop Analysis

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Table 8. Loop Inductance: VDD_CORE_AVS

TARGET CAP	LL AT 50 MHz (nH)	FOOTPRINT TYPE	PCB SIDE	DISTANCE TO PIN (mils)	VALUE (µF)	SIZE
C303	2.39	4vWSE	Bottom—under BGA	627	1	0508
C321	0.492	2vWSE	Bottom—under BGA	77	0.47	0402
C323	2.28	4vWSE	Bottom—under BGA	582	1	0508
C332	0.555	2vWSE	Bottom—under BGA	35	0.47	0402
C341	0.528	2vWSE	Bottom—under BGA	55	0.47	0402
C344	2.4	4vWSE	Bottom—under BGA	600	1	0508
C347	0.468	2vWSE	Bottom—under BGA	99	0.47	0402
C348	0.571	2vWSE	Bottom—under BGA	81	0.47	0402
C373	2.7	4vWSE	Bottom	626	1	0508
C551	3.13	4vWSE	Bottom	534	10	0805
MINIMUM	0.468					
MAXIMUM	3.130					
AVERAGE	1.555					

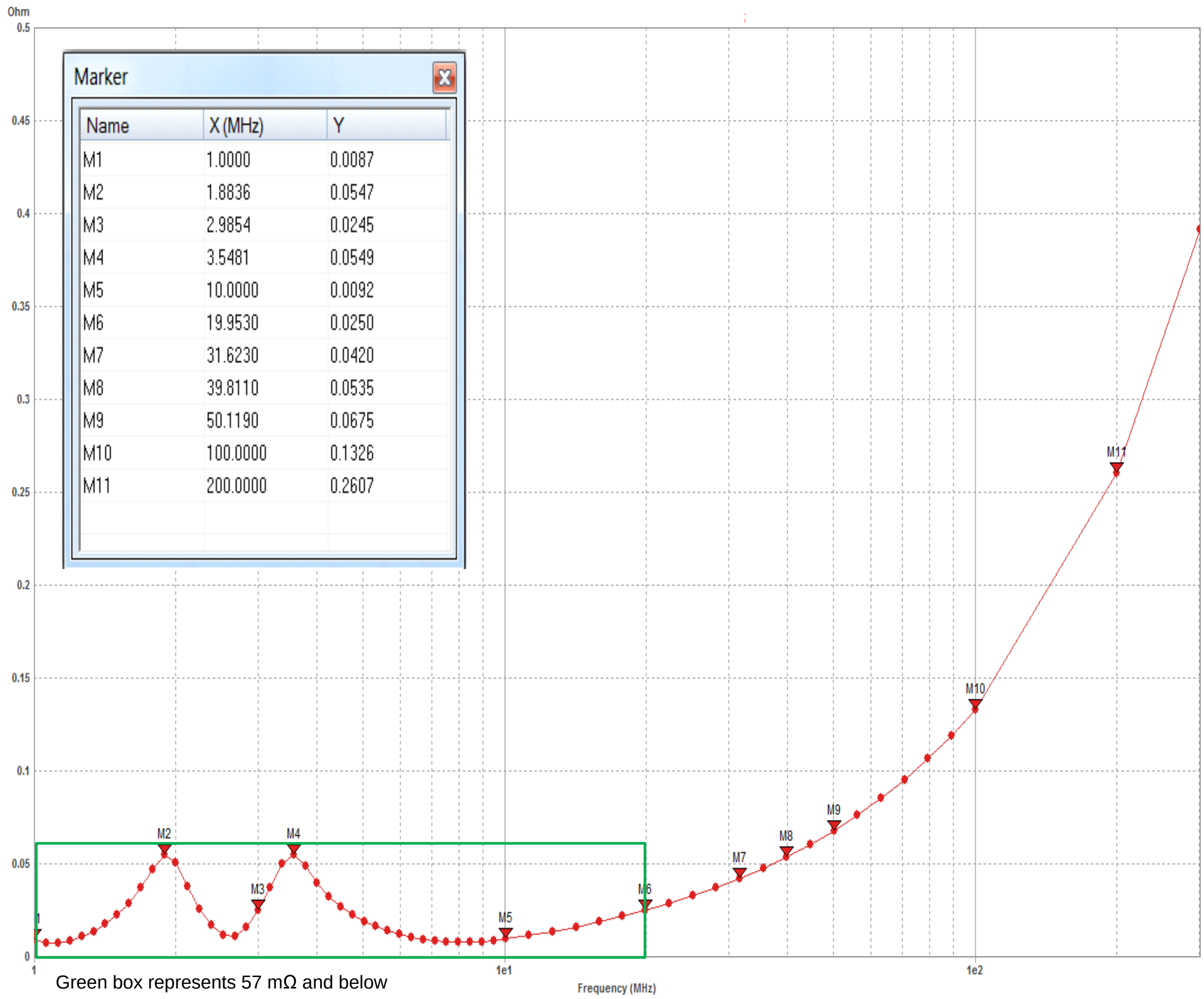

Figure 21. Target Impedance: VDD_CORE_AVS

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C.3 VDD_DDR_1V35

Table 9. Effective Resistance: VDD_DDR_1V35

DERIVED FROM: V_{DROP} ANALYSIS						
NAME	V_{IN} (V)	V_{OUT} (V)	V_{DROP} (V)	CURRENT (A)	R_{eff} (Ω)	TARGET (mΩ)
VDD_S1_AVS	1.0000	0.9934	0.0066	1	0.0066	33.000

DERIVED FROM: DC ANALYSIS							
NET (FROM)	COMPONENT (FROM)	GROUP/PIN (FROM)	NET (TO)	COMPONENT (TO)	GROUP/PIN (TO)	R_{eff} (Ω)	SEGMENT WEIGHT
VDD_DDR_1V35	L22	Group4	VDD_DDR_1V35	U27	Group1	0.004403	65%
VDD_DDR_SW	L22	Group5	VDD_DDR_SW	U32	Group2	0.002365	35%
					TOTAL	0.006768	

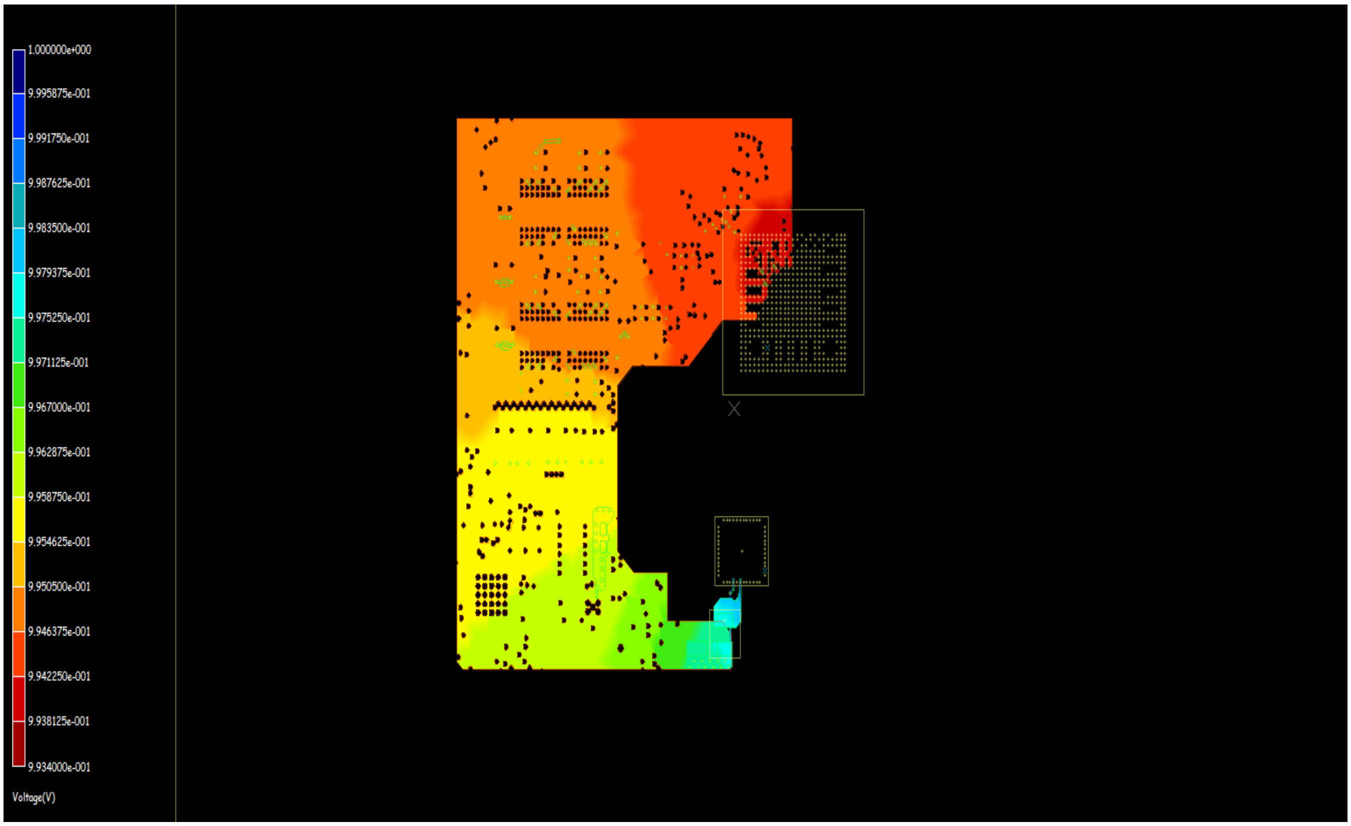

Figure 22. VDD_DDR_1V35 IR Drop Analysis

Table 10. Loop Inductance: VDD_DDR_1V35

TARGET CAP	LL AT 50 MHz (nH)	FOOTPRINT TYPE	PCB SIDE	DISTANCE TO PIN (mils)	VALUE (µF)	SIZE
C289	2.148	4vWSE	Bottom	373	1	0508
C293	2.26	4vWSE	Bottom	329	0.47	0402
C294	2.43	4vWSE	Bottom	349	0.47	0402
C295	2.41	4vWSE	Bottom	381	0.47	0402
C297	2.247	4vWSE	Bottom	265	0.47	0402
C307	2.937	4vWSE	Bottom	612	10	0805
C311	2.51	4vWSE	Bottom	425	0.47	0402
C312	2.62	4vWSE	Bottom	488	0.47	0402
C315	2.168	2vWSE	Bottom—under BGA	33	0.47	0402
C319	1.53	2vWSE	Bottom—under BGA	118	0.47	0402

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Table 10. Loop Inductance: VDD_DDR_1V35 (continued)

TARGET CAP	LL AT 50 MHz (nH)	FOOTPRINT TYPE	PCB SIDE	DISTANCE TO PIN (mils)	VALUE (µF)	SIZE
C325	1.18	2vWSE	Bottom—under BGA	88	0.47	0402
C351	2.96	4vWSE	Bottom	683	0.47	0402
C352	3.04	4vWSE	Bottom	746	0.47	0402
C354	2.89	4vWSE	Bottom	616	0.47	0402
MINIMUM	1.180					
MAXIMUM	3.040					
AVERAGE	2.381					

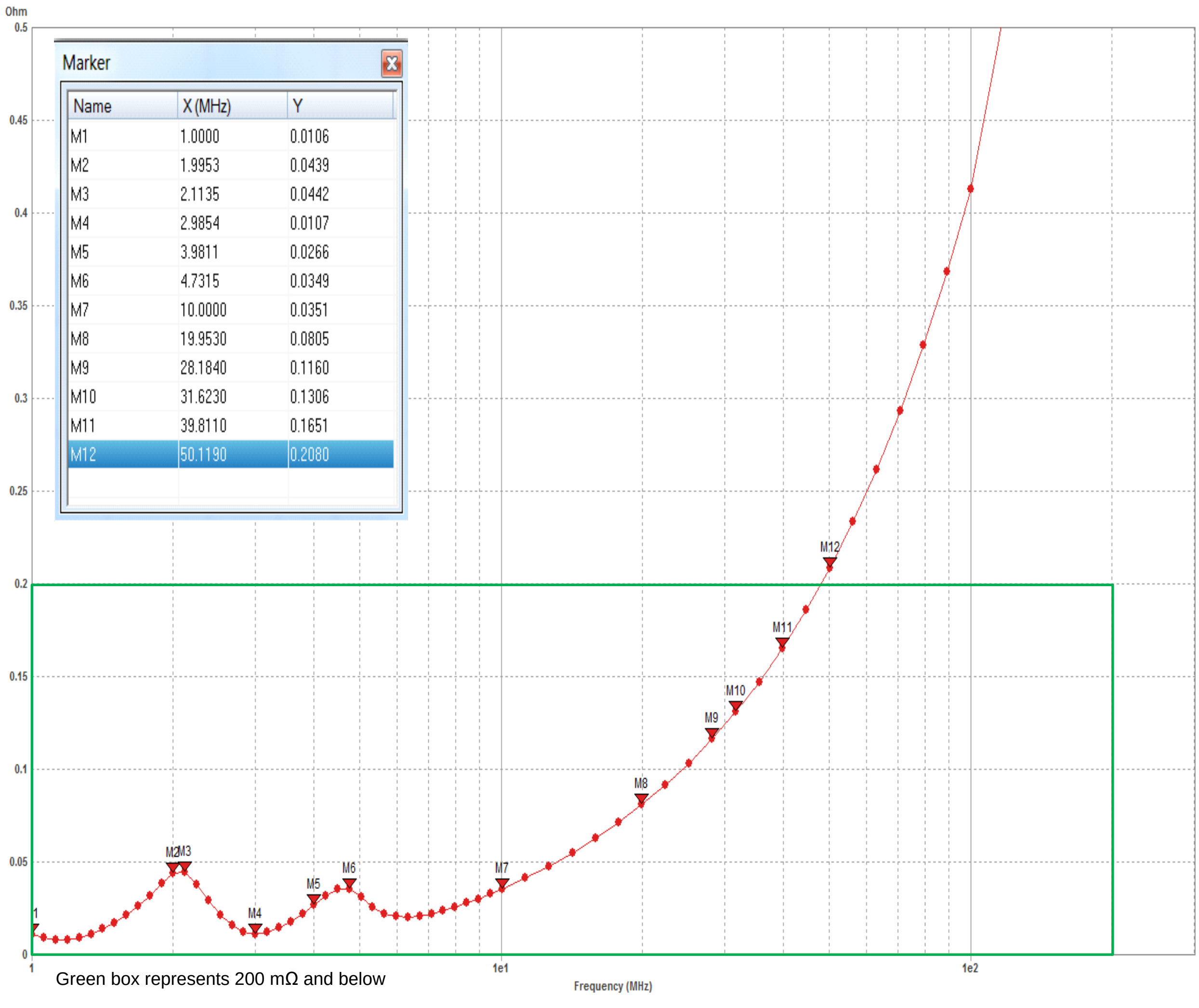

Figure 23. Target Impedance: VDD_DDR_1V35

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