TI Designs: TIDA-01621
Smart Holding-Brake Control and Diagnostics Reference Design for Servo Drives and Robotics

Description

This reference design implements a smart, holding-brake control functionality for variable speed drives. The holding brake is latched when power to the braking coil is removed, de-energized, or otherwise cut off, and the brake is released when voltage is applied to the brake coil, allowing the shaft of the motor to spin. This process is accomplished by enabling and disabling the smart electronic-load switch and solenoid-current controller, which supply power to the brake coil. This reference design also implements robust protection at the power supply input as well as at the brake coil output, thereby increasing the reliability of the system. The TIDA-01621 uses the C2000™ LaunchPad™ development kit to generate the brake-control signals and to perform the diagnostics functionality.

Resources

TIDA-01621	Design Folder
TPS2660	Product Folder
DRV110	Product Folder
ISO7142CC	Product Folder
TPS7B69-Q1	Product Folder
LMR23610	Product Folder
TVS3300	Product Folder

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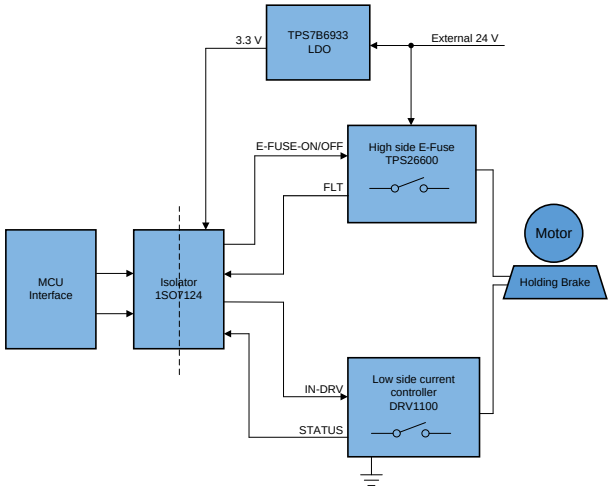
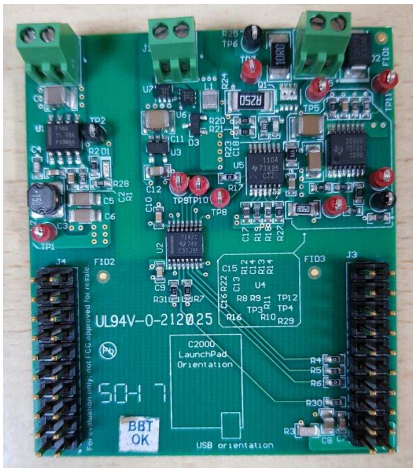
Features

- Compact, Smart, Holding-Brake Controller Solution Uses Integrated Chips to Implement Brake-Control Function, as Defined in IEC / EN 61800-5-2
- Can Control 24-V Rated Holding Brake With Current up to 2 A
- Dual-Switch Control Provides Redundancy to Open Brake-Coil Circuit
- Galvanic Isolation up to 2500-VRMS Between Holding-Brake Circuit and Microcontroller
- Hardware-Based, Pulse Width Modulation (PWM), Current-Control Loops Help to Maintain Constant Hold Current, Irrespective of Variation at Input Voltage
- Protection Against Overvoltage, Undervoltage, Reverse Polarity, and Overcurrent
- Continuous Monitoring of System Health Using Status and Fault Signals, to Enable Diagnostics

Applications

- Servo Drives
- Robotics
- Computer Numeric Control (CNC)
- Holding-Brake Controller





1 System Description

Variable-speed drives are used in a wide range of applications, including elevators, robotics, and CNC machines used in automated production. However, there are dangers in automated production, particularly from gravitational forces, in the case of gravity-loaded (vertical) axes, during power failures. This danger is because suspended loads represent substantial risk potential in machines and systems – in particular if people are standing under them. If inadvertent lowering or drops occur, the load must be brought to a standstill within the shortest possible time, to protect people and material against damage.

The recent development of drives with built-in safety-related features eliminates conventional methods of using standstill and speed monitors, limit switches, position cameras, contactors, and so on, which highly improves the reliability of the system. Recently, many drives started incorporating the safe brake control (SBC) function, as defined in EN 61800-5-2: 2007 functional safety for speed variable drives (see Figure 1). The SBC function provides a safe output signal to control an external brake, thereby preventing suspended loads from falling. In the horizontal axis of CNC machines, the SBC prevents movement of work due to external force. The brakes used must be safety brakes in which a quiescent current operates against a spring. If the current flow is interrupted, the brake engages and holds the motor shaft.

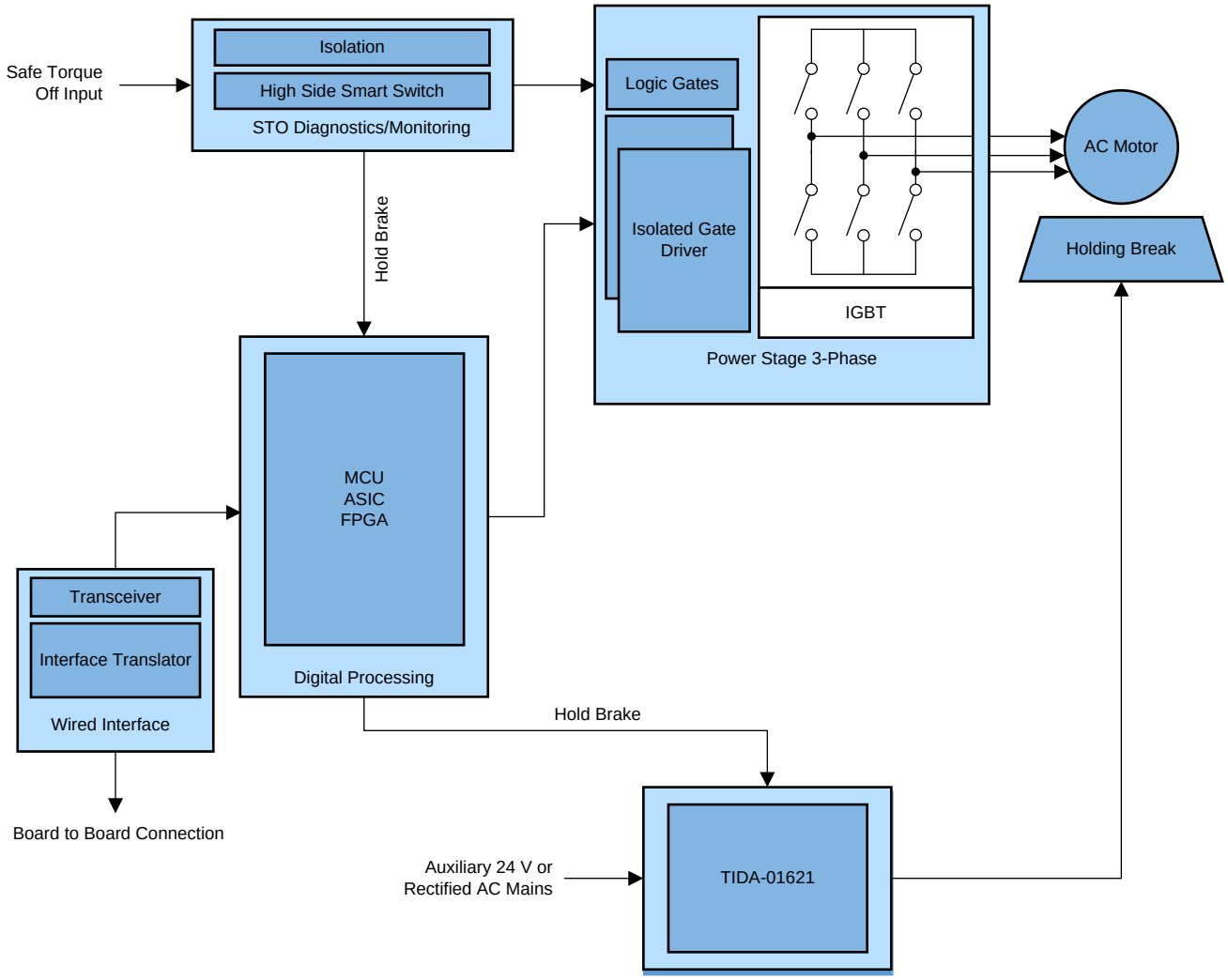


Figure 1. Implementation of Smart-Brake Control in Servo Drives

The holding-brake control module frequently includes a power-reduction feature for when the brake is released, to reduce energy consumption or brake-coil heating. This reference design demonstrates implementing a smart-holding brake controller for holding brakes rated up to 2 A of current.

This design uses the TPS26600PWPR, which is an e-fuse on the high-side power line, and the DRV110APWR, which is a current controller for solenoids on the low-side power line. Dual-switch control on both the high side and low side is implemented to provide redundancy in interrupting the current into the brake coil, to ensure highly-reliable brake operation. The brake-control signals are isolated from the controller through the digital isolator, ISO7142. The TPS26600 enables the design to detect and protect against overload and short-circuit conditions at the brake output, enhancing the safety of the system. Output voltage from the brake coil is reduced through the PWM on the low-side switch, reducing power consumption while the brake is energized. The load switch eliminates the discrete elements, which improves system reliability. Figure 1 shows the implementation of the smart-brake control in servo drives.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Nominal input voltage	24 V (±20%)
Output voltage without voltage reduction	Input – 1 V (nominal)
Output voltage with voltage reduction	10 V to (Vin – 1) V
Brake current	2 A
Switching frequency	20 KHz
Hardware redundancy	1
Protection features	Reverse-polarity, overload, and short-circuit protection
Undervoltage rating	17 V
Overvoltage rating	30 V
Release time	< 100 ms
Applying time	< 200 ms
Time to voltage reduction	Programmable through external capacitor
Isolation	2500 VRMS for 1 minute per UL and 4242-VPK per VDE.

2 System Overview

2.1 Block Diagram

Figure 2 shows the system-level block diagram for this reference design.

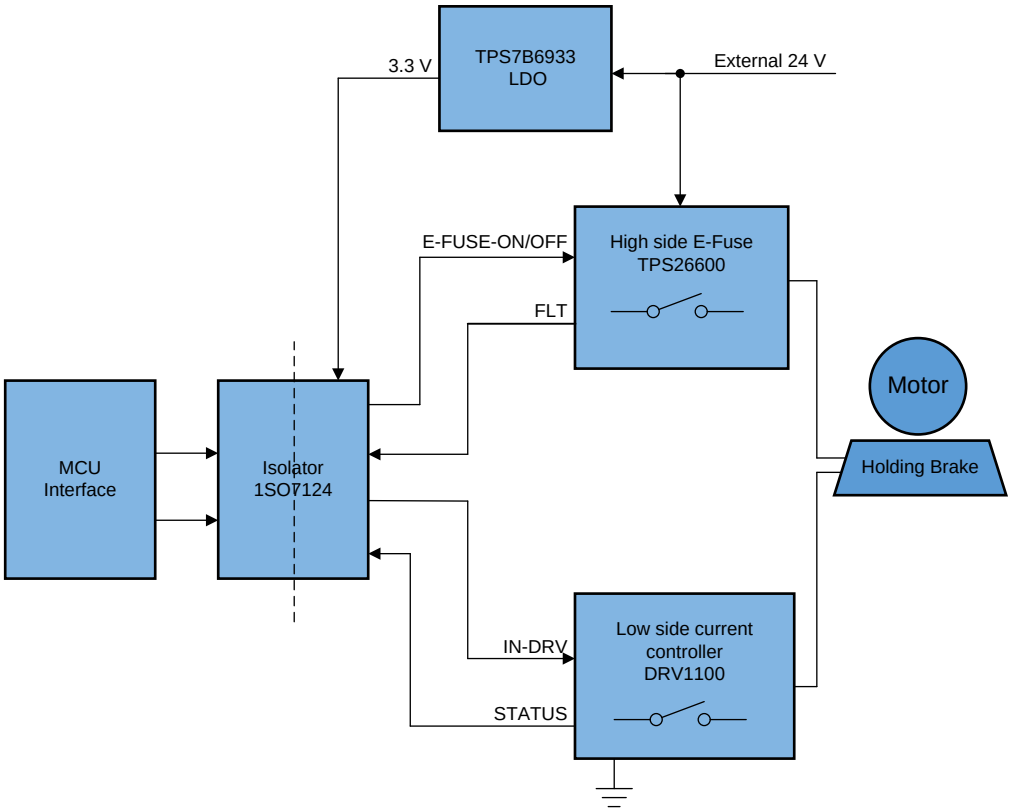


Figure 2. Block Diagram of TIDA-01621

This design provides a reference solution for implementing a smart-current regulated, holding-brake controller in servo drives. This reference design provides a safe output signal to control the external brake. Holding brakes specified for 24 VDC, with a current rating of up to 2 A, can be controlled. The main parts of the design include the ISO7142 digital isolator, the high-side e-fuse TPS26600, and the low-side current controller DRV110. The brake coil is connected between the output of the TPS26600 (high-side switch) and DRV110 (low-side switch). The switches are enabled and disabled by the digital signal generated by the MCU through the digital isolator. The board is powered with two, external, 24-V power supplies – one each for the primary and secondary sides. The MCU and VCC1 of the digital isolator, which comes on the primary side, are powered using the 3.3 V generated from the 24-V supply using a simple switcher, LMR23610. The high-side switch and VCC2 of the digital isolator, which are present on the secondary side, are powered using the 3.3 V generated from the 24-V supply using the LDO, TPS7B6933.

The system is designed to be protected against overload, short-circuit, overtemperature, and reverse-polarity. The $\overline{\text{FAULT}}$ (FLT) of the TPS26600 open-drain output asserts under the following conditions: undervoltage, overvoltage, overload, reverse current, and thermal shutdown. This fault signal is fed to the MCU through the digital isolator. The device can also withstand and protect the loads from positive and negative supply voltages up to ±60 V.

The DRV110 device is a PWM current controller for solenoids. The device is designed to regulate the current with a well-controlled waveform, to reduce power dissipation. The solenoid current is ramped up fast, to ensure opening of the brake.

After the initial ramping, the brake-coil current is kept at a peak value, to ensure correct operation, after which the current is reduced to a lower-hold level, to avoid thermal problems and reduce power dissipation. The open-drain pull-down path at the STATUS pin of the DRV1100 is deactivated if the undervoltage lockout (UVLO) or thermal shutdown blocks have triggered, or if the EN pin is low.

2.2 Highlighted Products

2.2.1 ISO7142

The ISO7142CC provides galvanic isolation up to 2500 VRMS for 1 minute per UL and 4242-VPK per VDE. The ISO7142CC is a quad-channel isolator with two forward- and two reverse-direction channels. This device is capable of a maximum data rate of 50 Mbps with 5-V supplies and 40 Mbps with 3.3-V or 2.7-V supplies. The ISO7142CC has integrated filters on the inputs to support noise-prone applications. Figure 3 shows the pin diagram of the device.

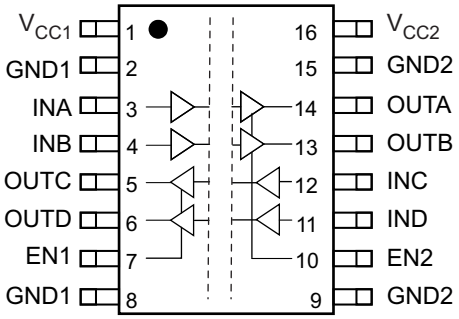


Figure 3. Pin Diagram of ISO7142

2.2.2 TPS26600

The TPS2660x devices are compact, feature-rich, high-voltage eFuses with a full suite of protection features. The wide supply-input range of 4.2 to 55 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±60 V. Integrated back-to-back FETs provide a reverse-current blocking feature, making the device suitable for systems with output-voltage holdup requirements during power fail and brownout conditions. Load, source, and device protection are provided with many adjustable features, including overcurrent and output-slew rate as well as overvoltage and undervoltage thresholds. The internal, robust, protection-control blocks, combined with the high-voltage rating of the TPS26600, helps to simplify the system designs for surge protection. Figure 4 shows the functional block diagram of the device.

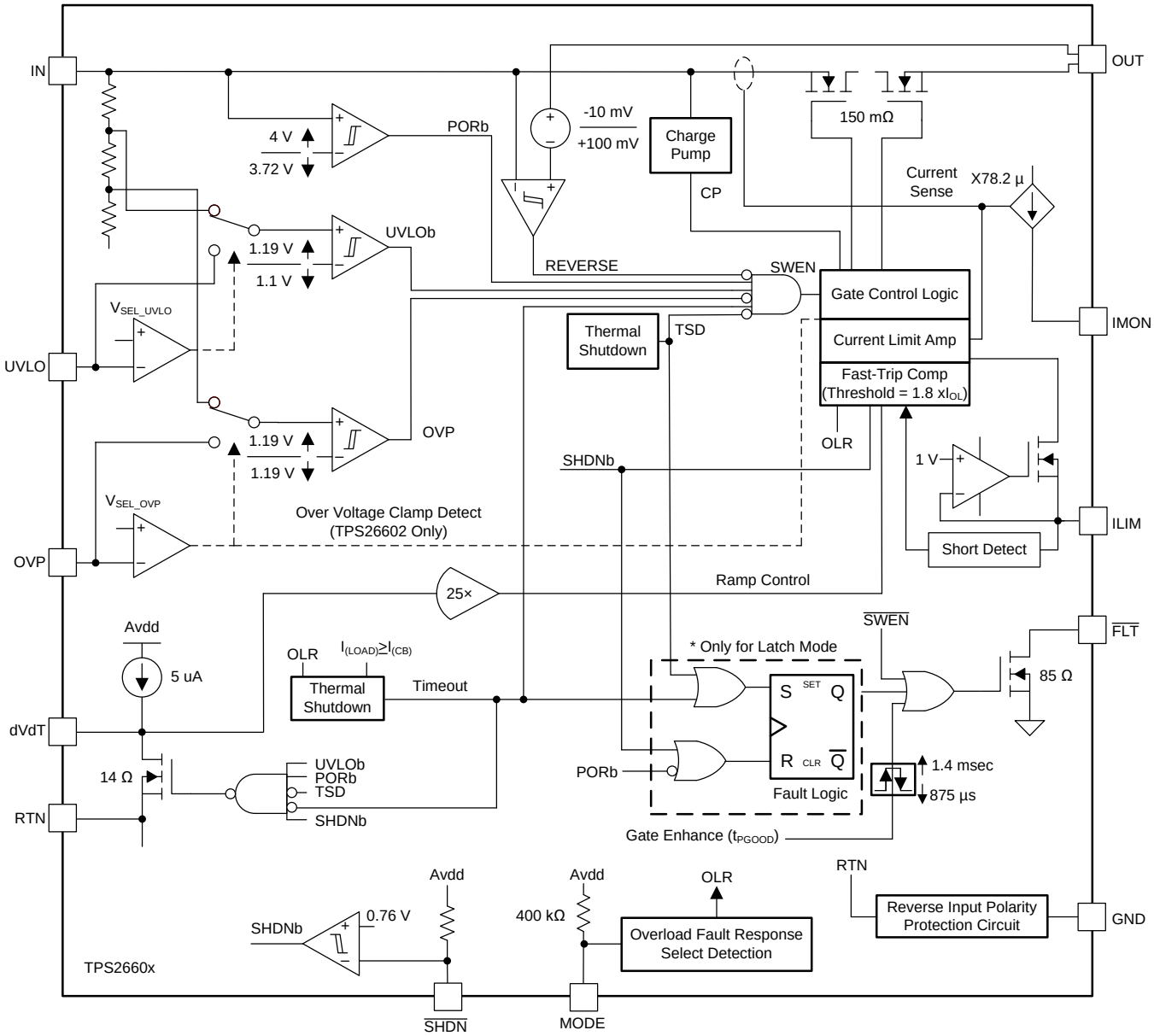


Figure 4. Functional Diagram of TPS26600

2.2.3 DRV110

The DRV110 device is a PWM-current controller for solenoids. The device is designed to regulate the current with a well-controlled waveform, to reduce power dissipation. The solenoid current is ramped up fast to ensure opening of the valve or relay. After the initial ramping, the solenoid current is kept at a peak value, to ensure correct operation, after which the current is reduced to a lower hold level, to avoid thermal problems and reduce power dissipation. Figure 5 shows the functional block diagram of the device.

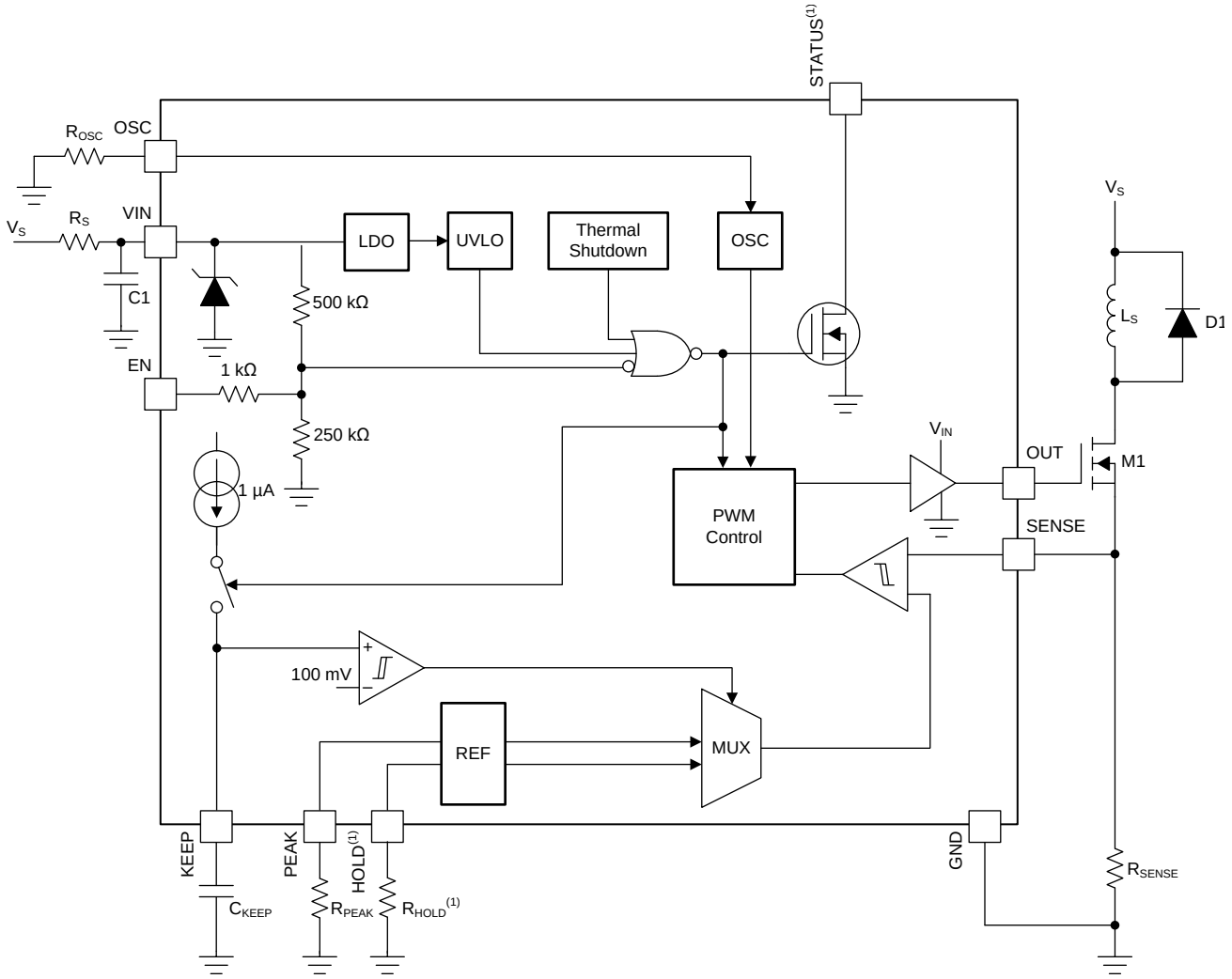


Figure 5. Functional Block Diagram DRV110

2.2.4 LMR23610ADDAR

The LMR23610 simple switcher is an easy-to-use, 36-V, 1-A, synchronous step-down regulator. Peak-current mode control is employed to achieve simple control loop compensation and cycle-by-cycle current limiting. A quiescent current of 75 µA makes the device suitable for battery-powered systems. An ultra-low, 2-µA shutdown current can further prolong battery life. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This feature also minimizes the external components. A precision-enable input allows simplification of regulator-control and system-power sequencing. Protection features include cycle-by-cycle current limit, hiccup mode, short-circuit protection, and thermal shutdown due to excessive power dissipation.

2.2.5 TPS7B6933

The TPS7B6933-Q1 is a high-voltage linear regulator that operates over a 4-V to 40-V input-voltage range. The device has an output-current capability of 150 mA and offers a fixed-output voltage of 3.3 V. The device features thermal shutdown and short-circuit protection, to prevent damage during overtemperature and overcurrent conditions.

2.2.6 TVS3300

The TVS3300 is a unidirectional, precision, surge-protection clamp, with a 33-V working voltage, designed specifically to protect systems with mid-voltage rails in industrial, communication, and factory automation applications. The TVS3300 has a fast response time when the surge current is applied, so there is no overshoot voltage during clamping, which makes it ideal for replacing traditional TVS and Zener diodes.

2.3 System Design Theory

2.3.1 DC Voltage Input

This reference design is designed to operate for a DC voltage of 24 V (±20 %). The board has two separate connectors to supply 24 V to the primary and secondary sides. J1 is the input connector for supplying the 24-V DC to the primary side. The DC voltage can be applied to the reference design at connector J2. The TVS3300 is a 33-V precision clamp that is connected in a bidirectional configuration, for protection against high-voltage transients. The Inductor L1 and capacitor C11 form the power filter.

2.3.2 Low-Power, Quad-Channel Digital Isolator

The MCU sends the control signals through the ISO7142 digital isolator to independently drive the high-side and the low-side switches (see Figure 6). The EFUSE_FLT signal from the high-side switch provides the diagnostic coverage against fault conditions. The FLT open-drain output asserts (active low) under the following conditions:

- Fault events, such as undervoltage, overvoltage, overload, reverse current, and thermal shutdown
- When device enters low-current shutdown mode when SHDN is pulled low
- During start-up, when the internal FET GATE is not fully enhanced

Figure 6 shows the circuit for the ISO7142.

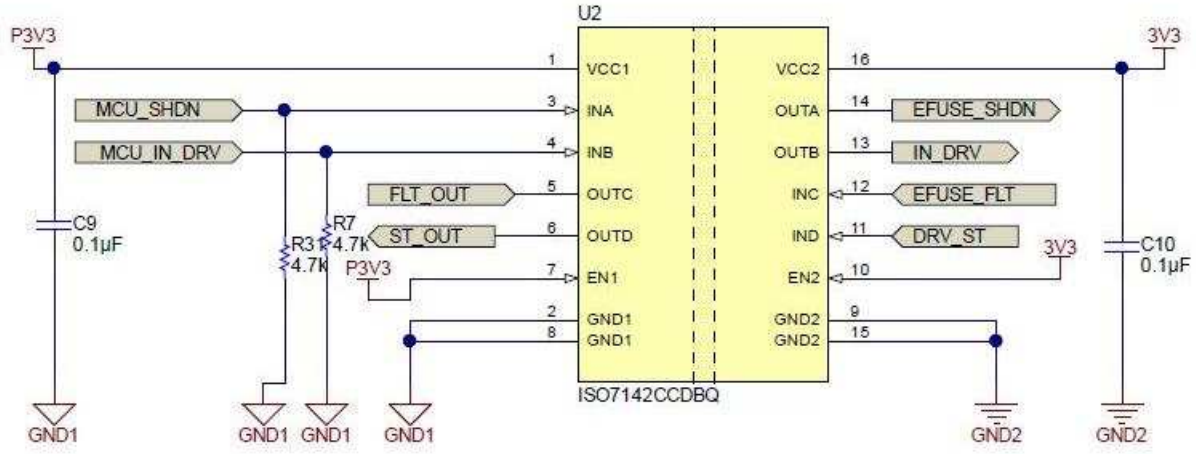


Figure 6. Schematic of ISO7142

The DRV_ST signal from the low-side switch provides the diagnostic coverage against UVLO and thermal shutdown.

The VCCI pin is supplied with the 3.3 V generated using the LMR23610 simple switcher. C9 (0.1 µF) is used as a local decoupling capacitor for the VCCI pin. The EN1 pin of the isolator is tied high, to enable the output channels on the primary side. The VCC2 pin is supplied with the 3.3 V generated using the TPS7B6933 LDO. C10 (0.1 µF) is used as a local decoupling capacitor for the VCC2 pin. The EN2 pin of the isolator is tied high, to enable the output channels on the secondary side.

2.3.3 High-Side E-fuse

Figure 7 shows the schematic of the high-side e-fuse.

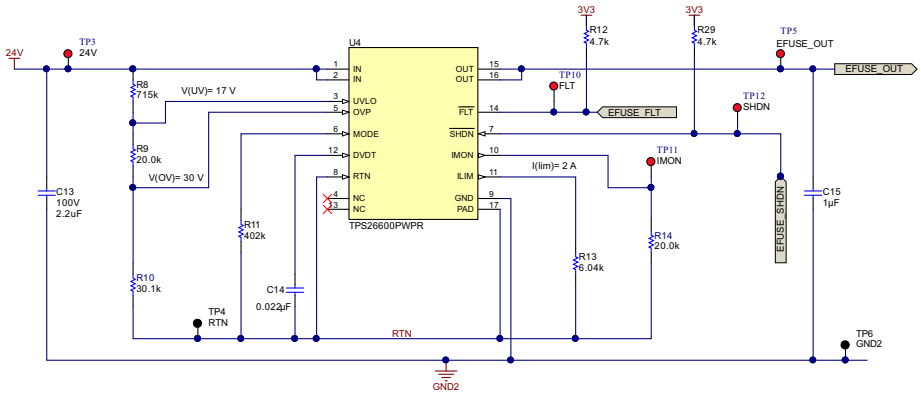


Figure 7. Schematic of High-Side E-fuse

2.3.3.1 Undervoltage Lockout and Overvoltage Set Point

The UVLO and overvoltage trip point are adjusted using an external voltage-divider network, R1, R2, and R3, connected between the IN, UVLO, OVP, and RTN pins of the device. The values required for setting the undervoltage and overvoltage thresholds are calculated by solving Equation 1 and Equation 2.

$$V_{OVPR} = \frac{R3}{R1 + R2 + R3} \times V_{OV} \quad (1)$$

$$V_{UVLOR} = \frac{R2 + R3}{R1 + R2\,R3} \times V_{UV} \quad (2)$$

To minimize the input current drawn from the power supply, a higher value resistance for R8, R9, and R3 is used.

From the device electrical specifications, V_{OVPR} = 1.19 V and V_{UVLOR} = 1.19 V. From the design requirements, V_{OV} is 30 V and V_{UV} is 17 V. After solving Equation 1 and Equation 2 for the overvoltage threshold of 30 V and undervoltage threshold of 17 V, the values of the resistors are as follows:

- R8 = 708.6 kΩ
- R9 = 20.05 kΩ
- R10 = 30.1 kΩ

The closest, standard, 1% resistor values were chosen for this design: R8 = 715 kΩ, R9 = 20 kΩ, and R10 = 30.1 kΩ.

2.3.3.2 Programming Current Monitoring Resistor: R_{IMON}

R_{IMON} must be configured based on the maximum input-voltage range of the ADC used.

For I_{LIM} = 2 A (considering the maximum input-operating voltage, V_{IMON_MAX}, to be 3.3 V), R_{IMON} is calculated as 20 kΩ using Equation 3.

$$R_{IMON} = \frac{V_{IMON\_MAX}}{I_{LIM} \times 75 \times 10^{-6}} \quad (3)$$

2.3.3.3 Programming Current-Limit Threshold: R_{ILIM} Selection

The R($_{ILIM}$) resistor at the I_{LIM} pin sets the overload current limit, which can be set using Equation 4.

$$R_{ILIM} = \frac{12}{I_{LIM}} \quad (4)$$

The current limit is set to 2 A. The closest standard resistor value for the current limit of 2 A is 6.04 kΩ.

2.3.3.4 MODE Pin Configuration

The MODE pin allows the flexibility to configure the device between the three current-limiting fault responses (circuit breaker, latch off, and auto-retry modes). This design is configured for active-current limiting with latch-off mode. A 402-kΩ resistor across the MODE pin to the RTN pin is connected for configuring in this mode.

2.3.3.5 Setting Output Voltage Ramp Time: $t_{dV/dT}$

A capacitor from the dV/dt pin to the RTN sets the output-voltage slew rate. The total ramp time $t_{dV/dt}$ of V_{OUT} for 0 to V_{IN} can be calculated using Equation 5.

To obtain dV/dt of 4.5 ms, the value of the capacitor is found to be 0.022 µF.

$$t_{\frac{dV}{dt}} = C_{\frac{dV}{dt}} \times 8 \times 10^{3} \times V_{IN} \quad (5)$$

2.3.4 Motor Brake

The electromechanical brake consists of an electromagnetically-inductive coil wound around a movable steel or iron slug, called the armature or plunger. The brake coil needs more current only during actuation, called the pull-in current, to pull the plunger into the solenoid. However, when the brake coil is actuated, it needs approximately 30% of its nominal current, called the hold current, to keep the plunger in the same position. The brake coil operating with nominal current consistently raises the temperature in the coil due to higher power dissipation. When plunger movement is detected, the steady-state current can be reduced to the hold current value, to minimize the power dissipation in the coil.

2.3.5 Low-Side, Solenoid Current Controller

Figure 8 shows the low-side, solenoid current controller.

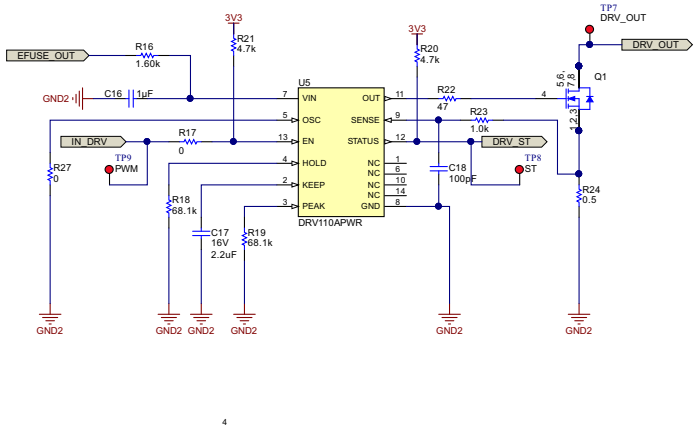


Figure 8. Schematic of Low-Side Current Controller

Keep time, t_{KEEP}, is set externally by connecting a capacitor to the KEEP pin. A constant current sourced from the KEEP pin is driven into an external capacitor, resulting in a linear-voltage ramp. When the KEEP-pin voltage reaches 100 mV, the current-regulation reference voltage, V_{REF}, is switched from V_{PEAK} to V_{HOLD}. The internal current source is switched off, and the capacitor is grounded for discharge. The dependency of t_{KEEP}, from the external capacitor size, can be calculated with Equation 6.

$$t_{KEEP}[s] = C_{KEEP}[F] \times 10^5 \left[\frac{S}{F}\right] \quad (6)$$

V_{PEAK} and V_{HOLD} depend on fixed resistance values, R_{PEAK} (R19) and R_{HOLD} (R18) . The currents and resistor values must be chosen such that the voltage across the sense resistor is more than 30 mV. I_{PEAK} and I_{HOLD} values can be calculated by using Equation 7 and Equation 8.

The peak current and hold current are set to 1.8 A and 300 mA, respectively. The values of R_{SENSE}, R_{HOLD}, and R_{PEAK}, calculated using Equation 7 and Equation 8, are 0.5 A, 68k, and 68k, respectively.

The frequency of the internal-PWM clock signal, PWMCLK, which triggers each OUT-pin ON-cycle, can be adjusted using the external resistor, R_{OSC} (R27), connected between OSC and GND.

$$I_{PEAK} = \frac{V_{REF}}{R_{SENSE}} = \frac{1\,\Omega \times 900\text{ mA} \times 66.67\text{ k}\Omega}{R_{PEAK}} \times \frac{1}{R_{SENSE}} \quad (7)$$

where

- 66.7 kΩ < R_{PEAK}< 2 MΩ

$$I_{HOLD} = \frac{V_{REF}}{R_{SENSE}} = \frac{1\,\Omega \times 150\text{ mA} \times 66.67\text{ k}\Omega}{R_{HOLD}} \times \frac{1}{R_{SENSE}} \quad (8)$$

where

- 66.7kΩ < R_{HOLD} < 333 kΩ

Figure 9 shows the frequency as a function of the resistor value.

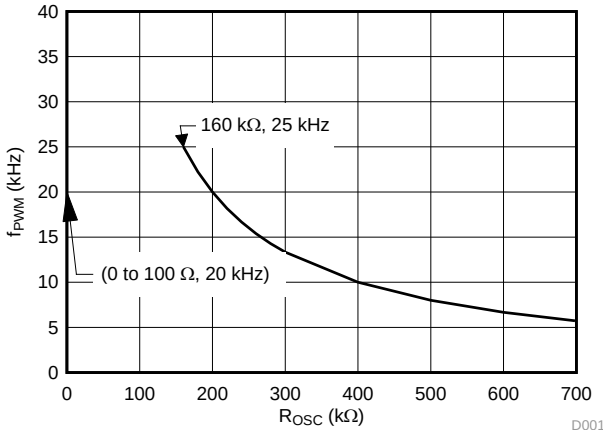


Figure 9. Oscillation Frequency as Function of Resistor Value

Equation 9 can be used to calculate the PWM frequency, as a function of the external fixed adjustment resistor value (greater than 160 kΩ).

$$f_{PWM} = \frac{60\ kHz}{R_{OSC}} \times 66.67\ k\Omega$$

where

- $160\ k\Omega < R_{OSC} < 2\ M\Omega$ (9)

In this design, R27 is connected directly to ground for a PWM-oscillation frequency of 20 KHz.

The DRV110 can regulate the VIN voltage to 15 V from a higher external supply voltage, 30 V in this design, using an internal-bypass regulator that replicates the function of an ideal Zener diode. This occurrence requires that the supply current is sufficiently limited by an external resistor between the VS and the VIN pin. An external capacitor connected to the VIN pin is used to store enough energy to charge the external switch-gate capacitance at the OUT pin. A current-limiting resistor size to keep quiescent current less than 1 mA can be calculated with Equation 10.

$$R_{S\_MAX} = \frac{V_{S\_MIN\_DC} - V_{ZENER}}{1\,mA + I_{GATE\_AVG}} \quad (10)$$

The value of R_S, calculated from Equation 10, for I_{GATE_AVG} of 7.5 mA, is 1.6 kΩ in this design.

2.3.6 Snubber Circuit

Figure 10 shows the snubber circuit connected across the brake coil. When the switch is opened, the inductance of the coil responds to the decrease in current by inducing a voltage of reverse polarity, which damages the switch. R25 is placed in series with the commutating diode, D2, connected in parallel to the brake coil, to demagnetize the brake coil faster, thus protecting the switch from a high-reverse voltage transient.

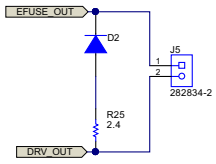


Figure 10. Schematic of Snubber Circuit

2.3.7 Power Supplies

2.3.7.1 3.3-V Generation Using LMR23610ADDAR

The LMR23610 is a step-down, DC-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage, with a maximum output current of 1 A. The WEBENCH® software from TI can be used to generate complete designs. Figure 11 shows the schematic of the device.

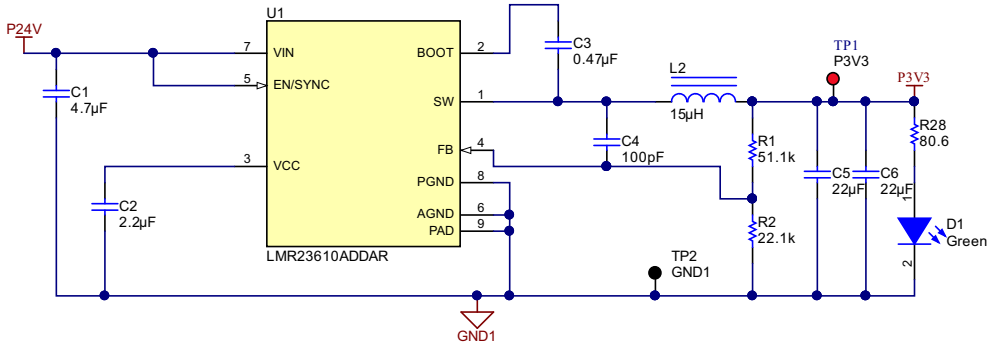


Figure 11. Schematic of LMR23610

2.3.7.2 3.3-V Generation Using TPS7B6933

A 3.3-V supply is needed to power the digital isolator on the secondary side. Here, the TPS7B6933 is used to convert 24 V to 3.3 V, to supply power to the secondary side of the isolator and the high-side switch. Figure 12 shows the schematic of the TPS7B6933.

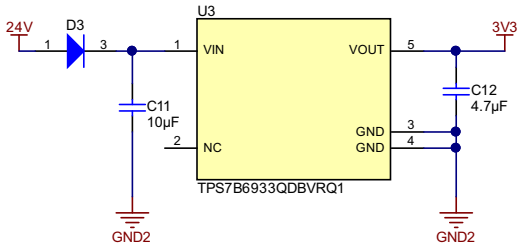


Figure 12. Schematic of TPS7B6933

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

This section explains the top and bottom views of the PCB for this reference design. This section also details the power-supply requirements and connectors used to connect to the external world.

3.1.1 PCB Overview

Figure 13 shows the top view of the PCB. The high-side and low-side switches are also highlighted.

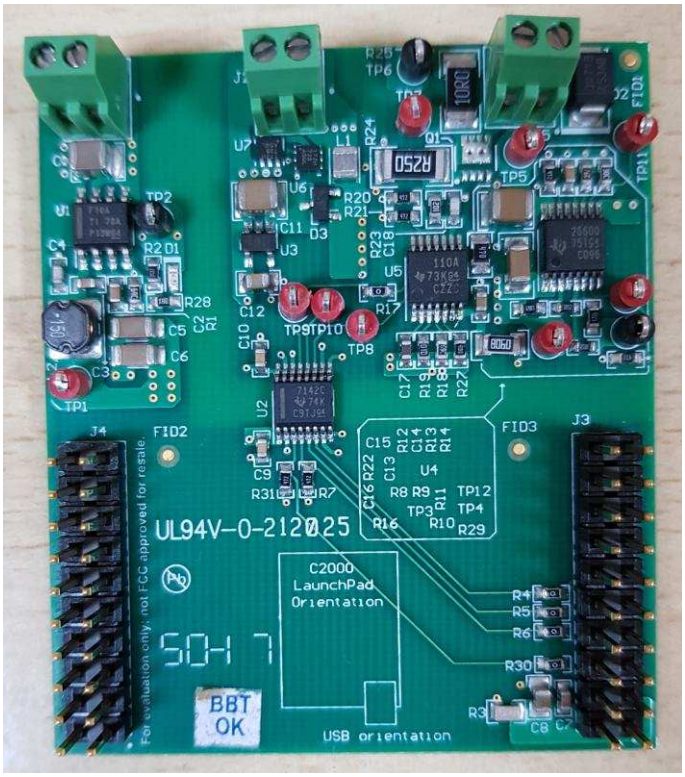


Figure 13. Top View of PCB

Table 2 lists the connectors.

Table 2. Connectors of TIDA-01621

CONNECTORS	FUNCTION OF CONNECTOR
J1	24 V_VIN power supply to power the primary side of the board
J2	24 V_VIN power supply to power the secondary side of the board
J3	20-pin connector to connect to the C2000 LaunchPad
J4	20-pin connector to connect to the C2000 LaunchPad
J5	Output connector for connecting the brake coil

3.2 Testing and Results

This section describes the test results, which evaluate the functionality and the performance specified in the design. This reference design uses a 1-kW servo motor with a brake coil for testing. The brake coil is powered by a 24-V DC, and the current rating of the coil is about 0.81 A. The inductance of the coil is measured to be about 65.35 mH and the resistance is about 30.8 Ω.

3.2.1 Test Results

3.2.1.1 Operation of DRV110

The hold current in the DRV110 is set to 300 mA and peak current is set to 1.8 A, as explained in Section 2.3.5. Figure 14 shows the hold and peak currents passing through the switch. The hold current is 300 mA, as was set in the calculations. The peak current is limited by the internal resistance of the coil and is measured to be 740 mA.

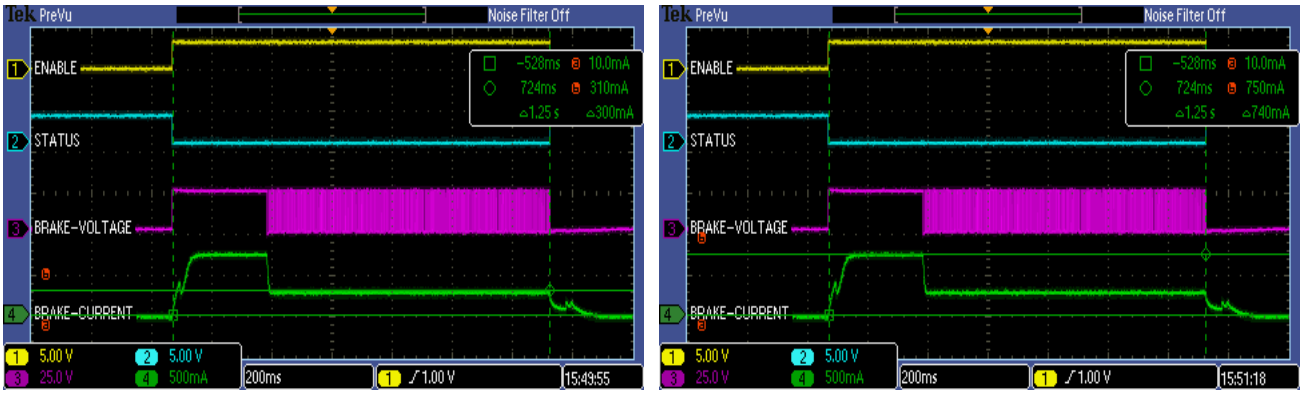


Figure 14. Hold and Peak Currents of Brake Coil

Figure 15 shows the zoomed-in version of the brake current and voltage for the rising and falling edge of the enable signal.

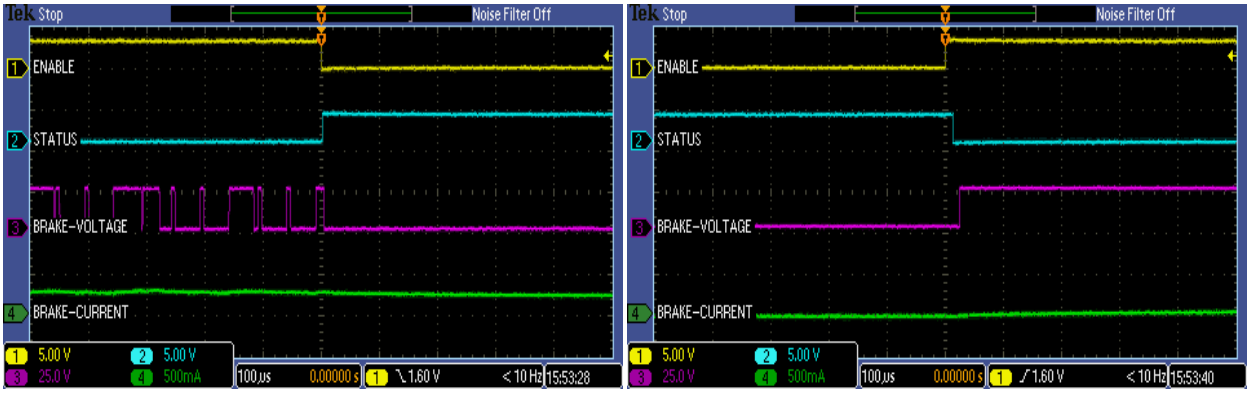


Figure 15. Zoomed-In View of Rising and Falling Edge of Brake Voltage and Brake Current

3.2.1.2 Current Regulation With DRV110 at Different Voltages

The brake current must remain constant, as set by the designer irrespective of the variations in the input supply voltages. This setting can be validated by capturing the brake current for different sets of operating voltages. Figure 16 shows the brake-hold currents for an input voltage of 19-V and 28-V.

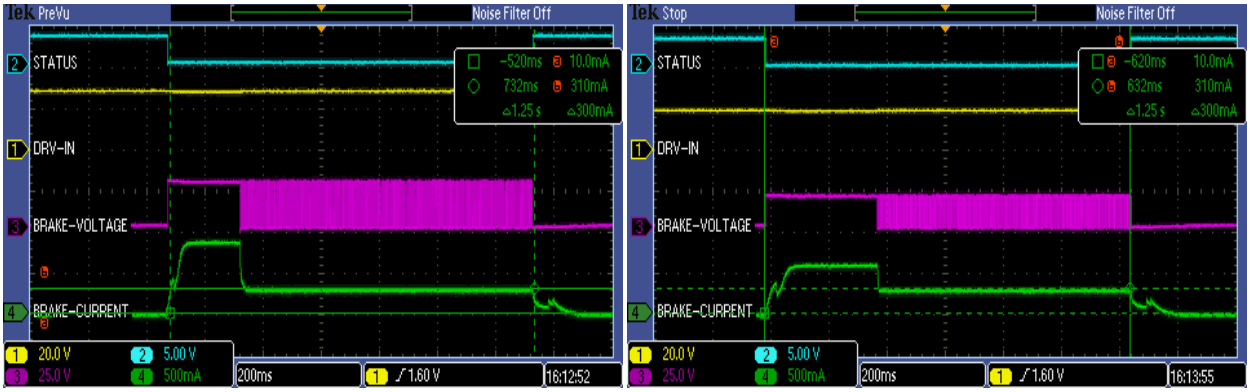


Figure 16. Hold Current of Brake Fixed to 300 mA at 19-V and 28-V Input Voltage

The value of the peak current is set to 1.8 A in this design. However, the maximum current that can pass through the coil is limited by the internal resistance of the coil. Because the resistance of the coil is 30.8 Ω, the maximum current at 19 V and 28 V is 616 mA and 909 mA, respectively, which is less than the current limit set in the design. So, the peak current is flexibly allowed to vary according to supply voltage, as shown in Figure 17.

Figure 17. Relative Increase in Peak Current at 19-V and 28-V Input Supply Voltages

3.2.1.3 Normal Operation of TPS26600

Figure 18 shows the functionality of the TPS26600. The e-fuse input voltage is set to 24-V. FLT is as active low signal, so it remains high under normal conditions. The brake coil current is hereby limited to 300 mA by the DRV110.

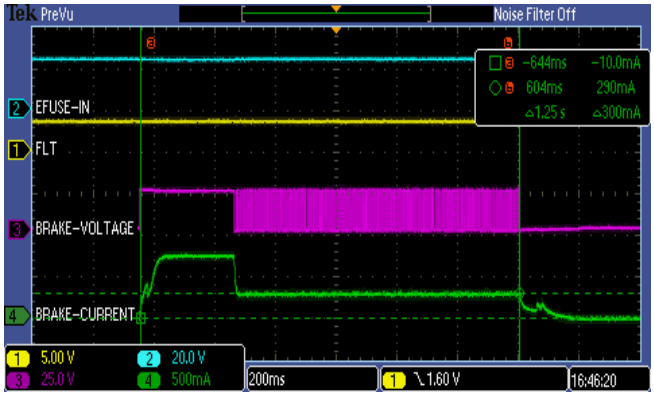


Figure 18. Functionality of E-Fuse, TPS26600

3.2.1.4 UVLO and Overvoltage of TPS26600

The UVLO and overvoltage of this design are set to 17 V and 30 V, respectively, as described in Section 2.3.3.1. For detection of the UVLO, the system is triggered at the falling edge of the input voltage. The voltage measured at the fall of the FLT signal is measured to be 16.8 V, as shown in Figure 19.

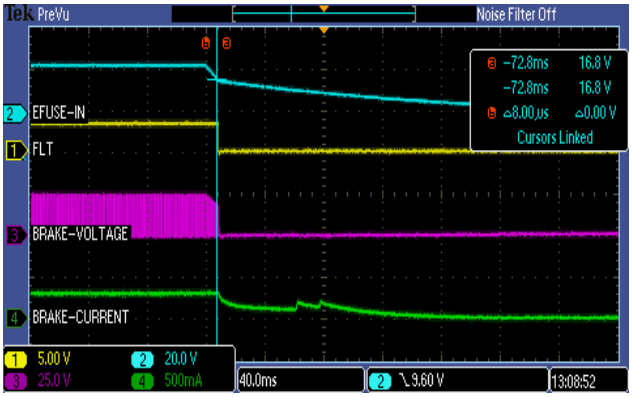


Figure 19. UVLO Threshold for TPS26600

Similarly, for the detection of overvoltage, the system is triggered at the rising edge of the input voltage. The voltage measured at the fall of the FLT signal is measured to be 29.2 V, as shown in Figure 20.

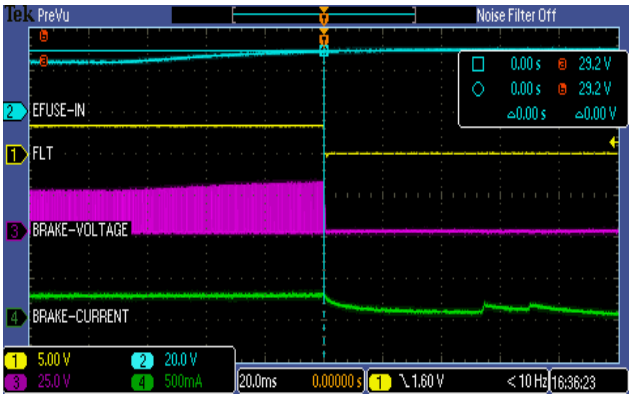


Figure 20. Overvoltage Threshold for TPS26600

3.2.1.5 Reverse-Polarity Protection of TPS26600

The TPS26600 provides reverse-input polarity protection down to –60 V. Figure 21 shows the test result for the input voltage of –30 V. The output to the e-fuse remains off and the brake current is also zero.

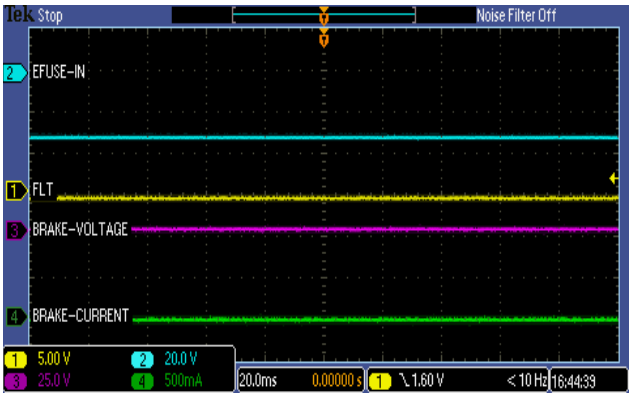


Figure 21. Reverse-Input Polarity Protection at –30 V

3.2.1.6 Short-Circuit Protection of TPS26600

During a transient-output short-circuit event, the current through the device increases very rapidly. Because the current-limit amplifier cannot respond quickly to this event, due to its limited bandwidth, the device incorporates a fast-trip comparator, I(FASTRIP), with a threshold. The fast-trip comparator turns off the internal FET within 250 ns (typical), when the current through the FET exceeds I(FASTRIP) (I(OUT) > I(FASTRIP)), and terminates the rapid short-circuit peak current. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to I(OL). Then, the device behaves similar to during the overload condition. Figure 22 and Figure 23 show the behavior of the system when the current exceeds the fast-trip threshold.

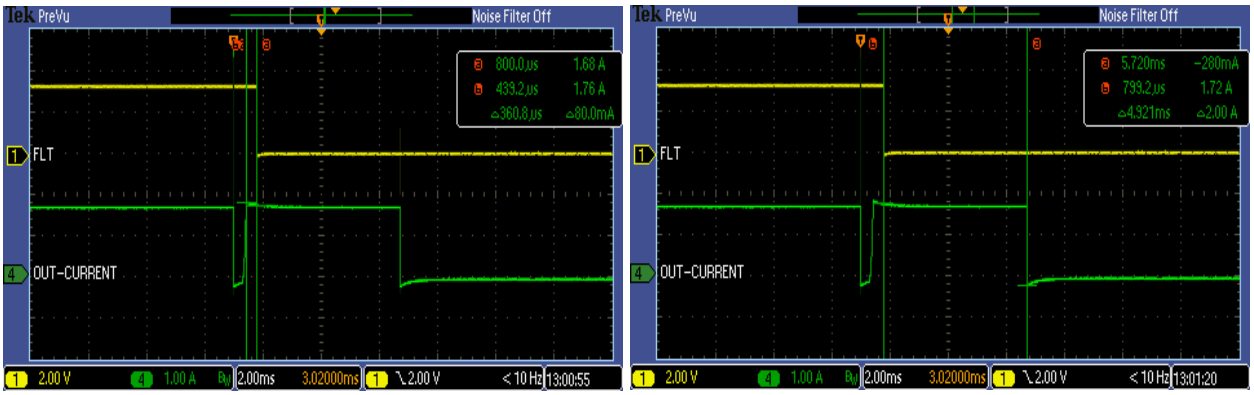


Figure 22. Short-Circuit Event Under Normal Operation of TPS26600

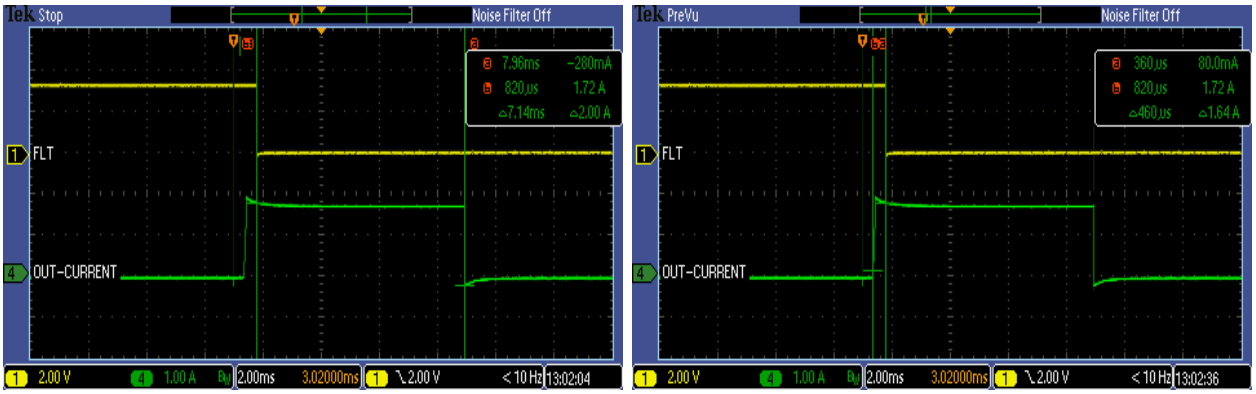


Figure 23. Short-Circuit Event When Circuit Was Originally Open Circuited

3.2.1.7 Board Thermal

Figure 24 shows a thermal image of the board at 24 V and 28 V, respectively.

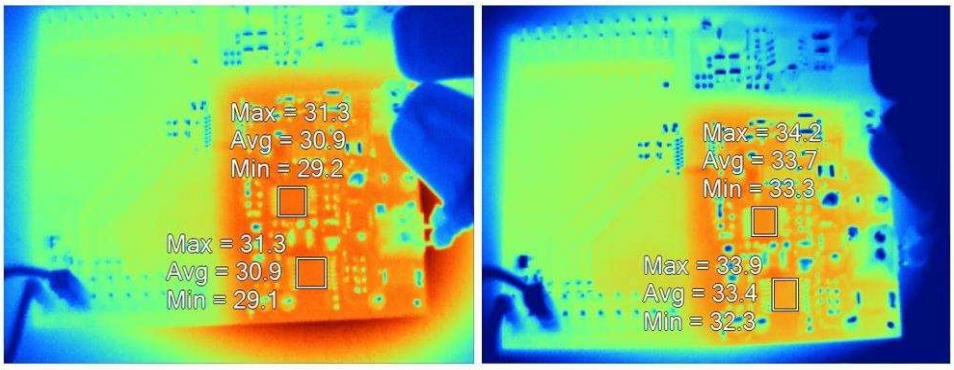


Figure 24. Thermal Image of TIDA-01621 Board

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01621.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01621.

4.3 PCB Layout Recommendations

Figure 25 and Figure 26 show the isolation barrier and the ground split, respectively. The primary and secondary copper tracks are separated from each other by the isolation barrier. A copper-to-copper creepage spacing of 4 mm is maintained between the primary and the secondary sides. The two, 20-pin connectors, J3 and J4, are placed 20 mm apart for interfacing to the C2000 LaunchPad. The power plane is divided into 3.3-V and 24-V planes.

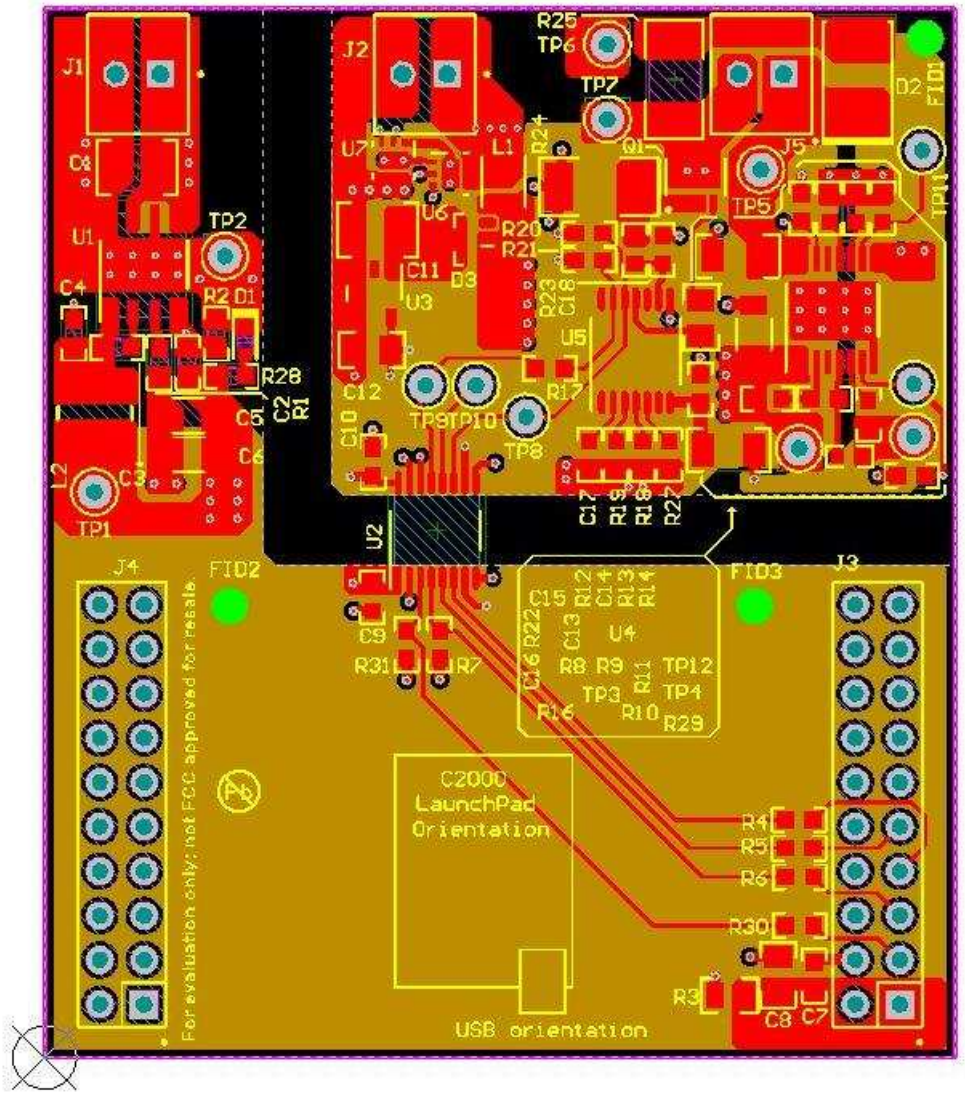


Figure 25. Isolation Barrier and Power Plane of Layout

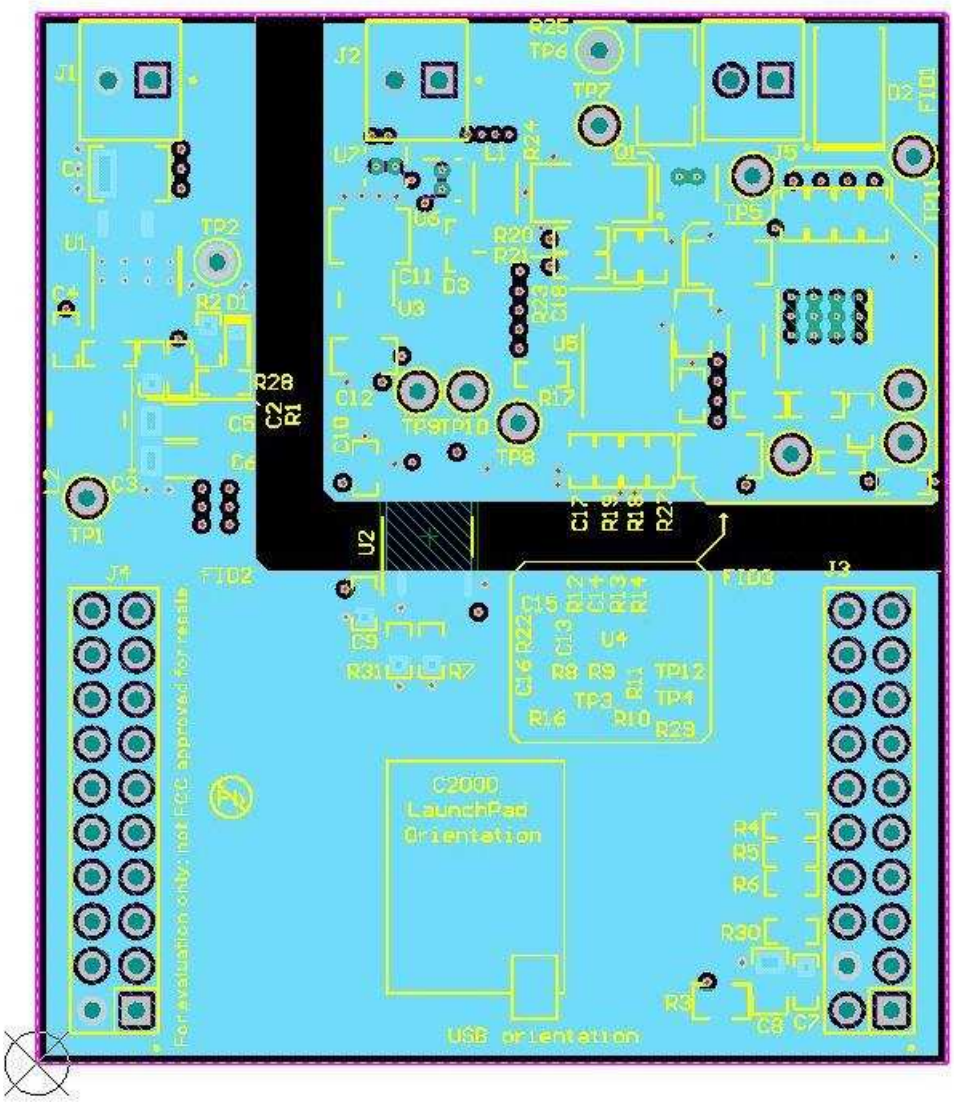


Figure 26. Split in Ground Plane of Layout

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01621.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01621.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01621.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01621.

5 Related Documentation

1. International Electrotechnical Commission (IEC), IEC 61800-5-2:2016 RLV: Adjustable speed electrical power drive systems - Part 5-2: Safety requirements - Functional , 18 April 2016

6 Trademarks

6.1 Trademarks

7 About the Authors

AISHWARYA BHATNAGAR is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems. Aishwarya earned her bachelor of technology in electronics and communication engineering from MNNIT, Allahabad.

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Recognition: The authors would like to recognize the excellent contributions of **MANU BALAKRISHNAN** during the test phase of the TIDA-01621 design.

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