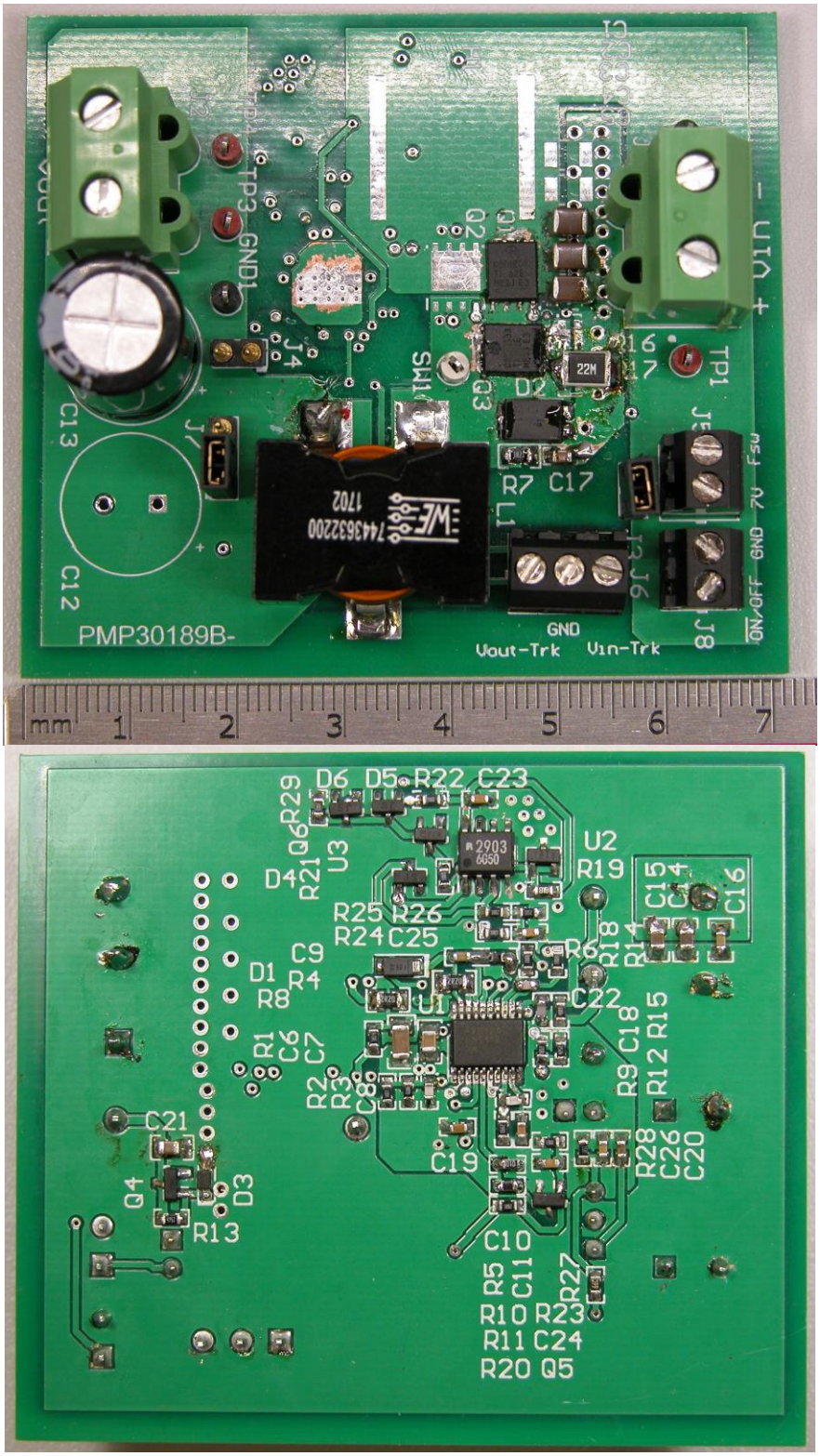
1. Photo of the prototype (71.12mm x 62.23mm).

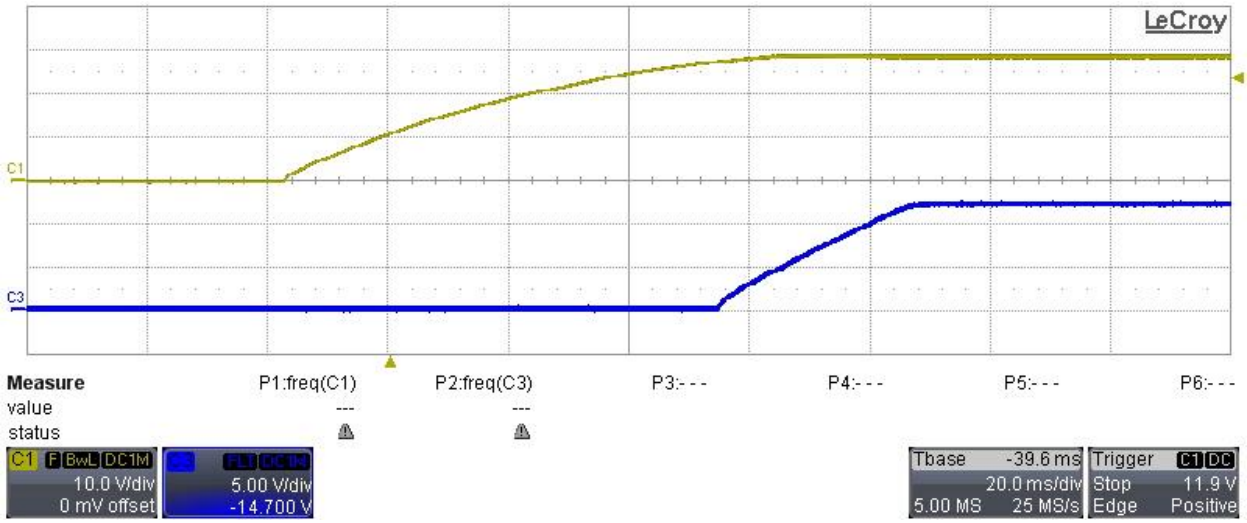
The reference design PMP30301 Rev_A has been built on PMP30189 Rev_B PCB



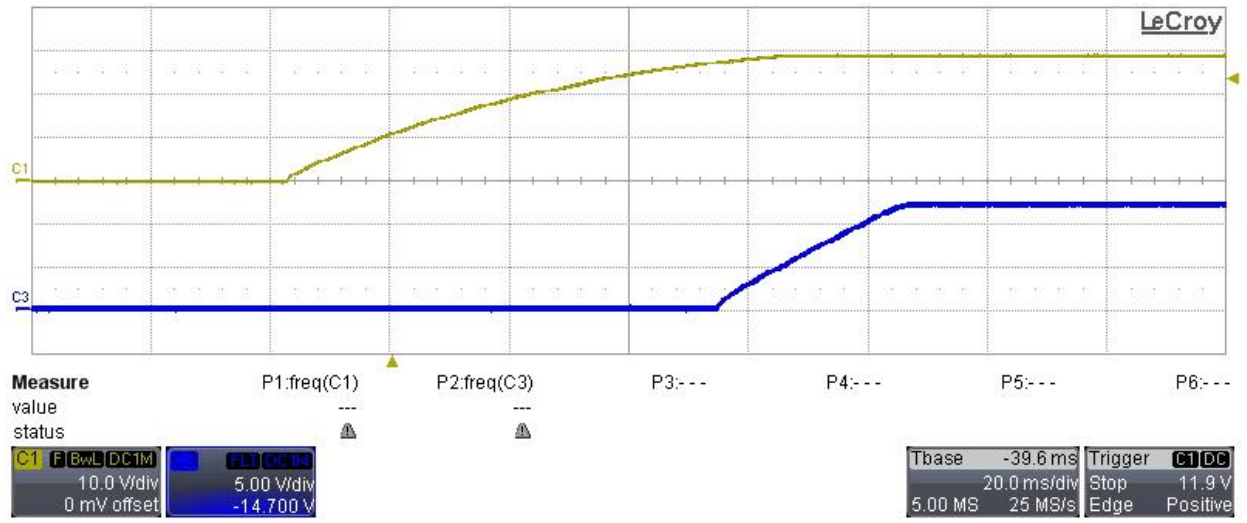
2. Startup

The input and output voltage behavior at full and no-load conditions is shown in the images below.

Ch.1: Input voltage (10V/div, 20ms/div, 20MHz BWL)
Ch.3: Output voltage (5V/div, 20MHz BWL)
Load = 6.5A (full load), Vin = 29V



Same condition as above but with zero load:



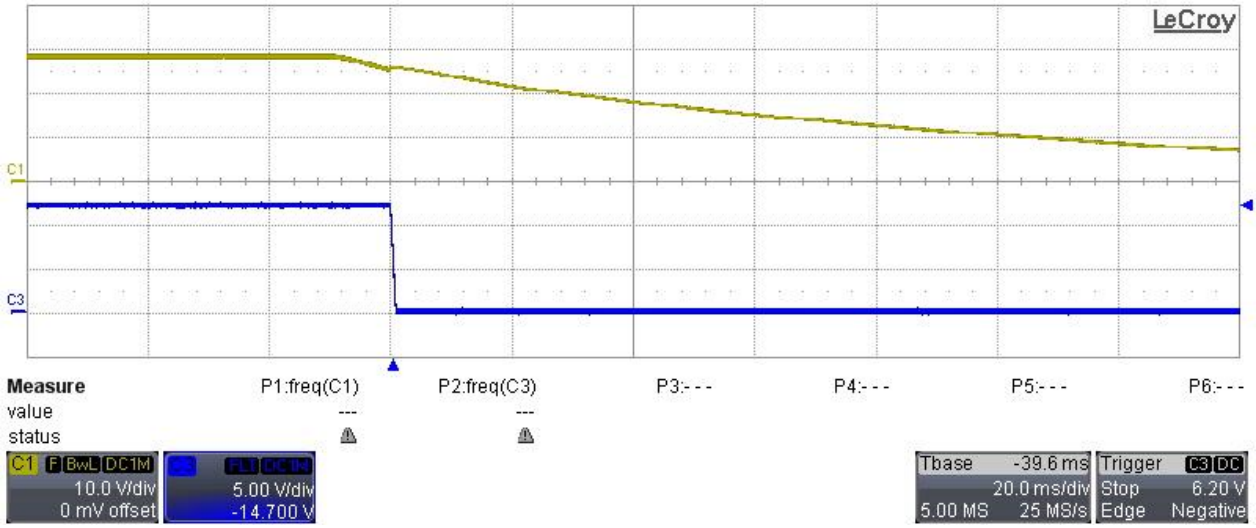
3. Shut down

The input and output voltage behavior during shut-down at full is shown below.

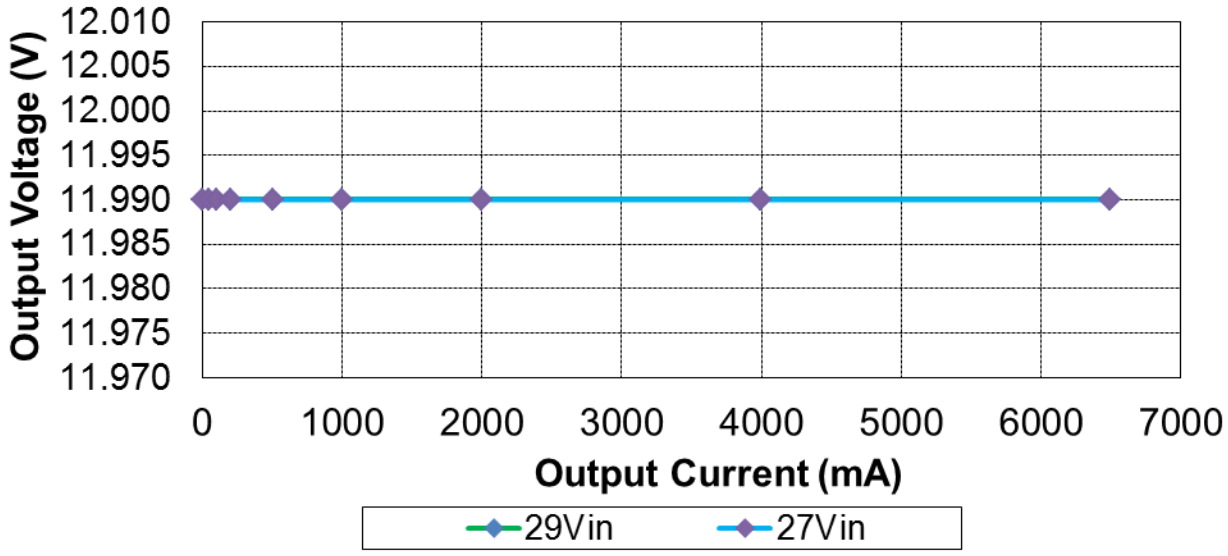
Ch.1: Input voltage (10V/div, 20ms/div, 20MHz BWL)

Ch.3: Output voltage (5V/div, 20MHz BWL)

Load = 6.5A, Vin = 29V



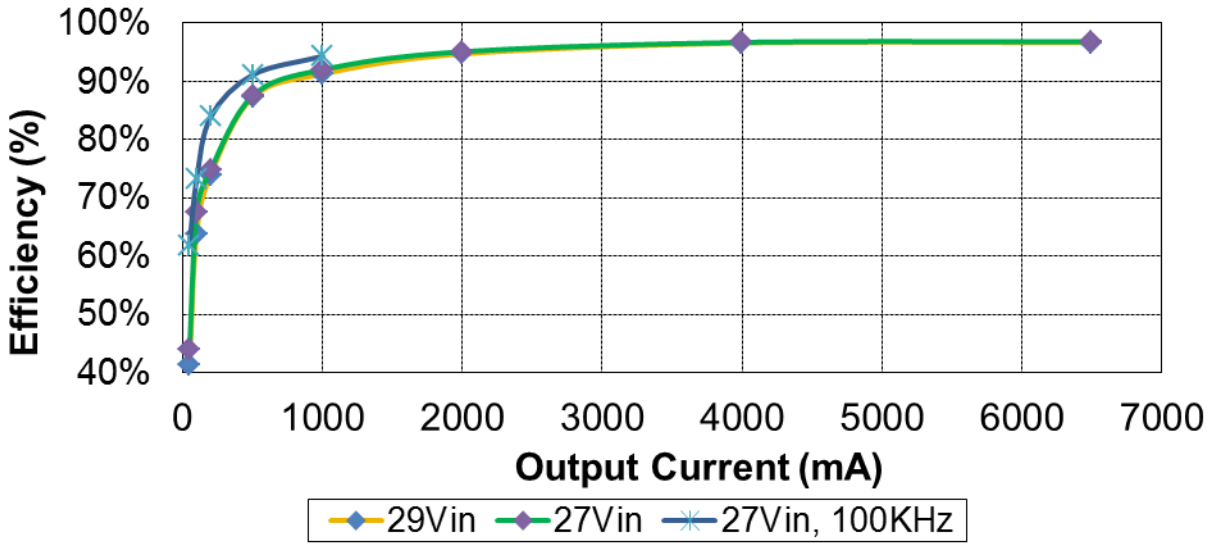
4. Output voltage regulation



5. Efficiency

The efficiency data, versus input and output voltage are shown in the tables and graphs below. The load (constant-current electronic load) has been varied from 0 to 6.5A. The input voltage has been set to 27V and 29V. Switching frequency setup:

a) 100KHz: pin 1-2 of J5 left open
b) 250KHz pin 1-2 of J5 shorted

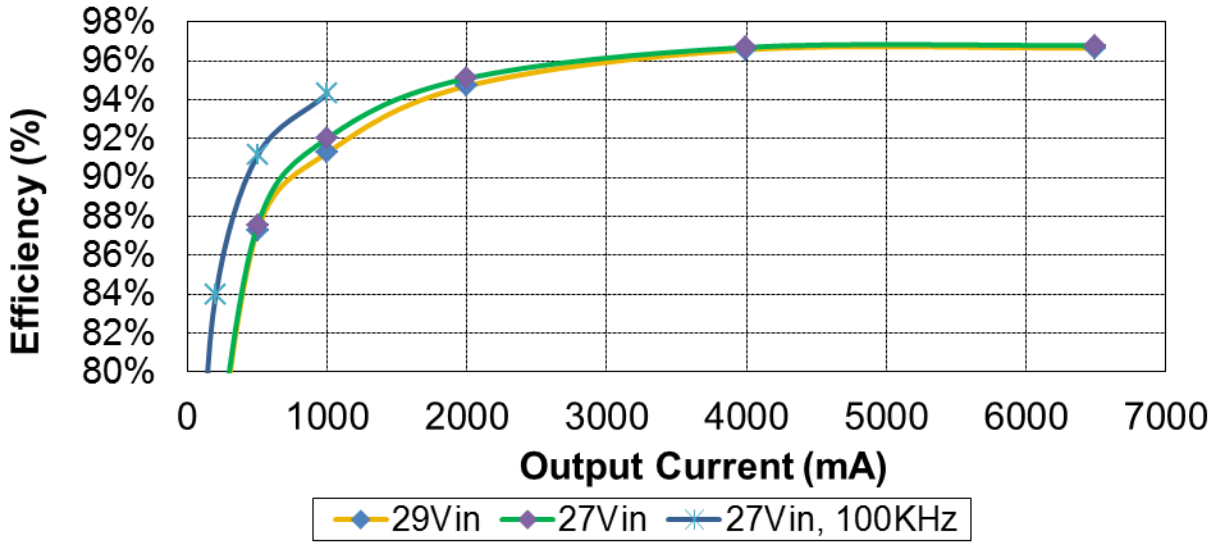


29Vin, Fsw = 250 KHz						
Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
29.03	27.9	0.8099	11.99	0	0.00	0%
29.03	50.7	1.472	11.99	50.7	0.61	41.3%
29.03	65.7	1.907	11.99	101.5	1.22	63.8%
29.02	112.1	3.25	11.99	200.3	2.40	73.8%
29.01	238.1	6.91	11.99	502.8	6.03	87.3%
29.06	453.3	13.17	11.99	1002.8	12.02	91.3%
29.00	873	25.32	11.99	2000	23.98	94.7%
29.00	1712	49.65	11.99	3999	47.95	96.6%
29.01	2777	80.56	11.99	6495	77.88	96.7%

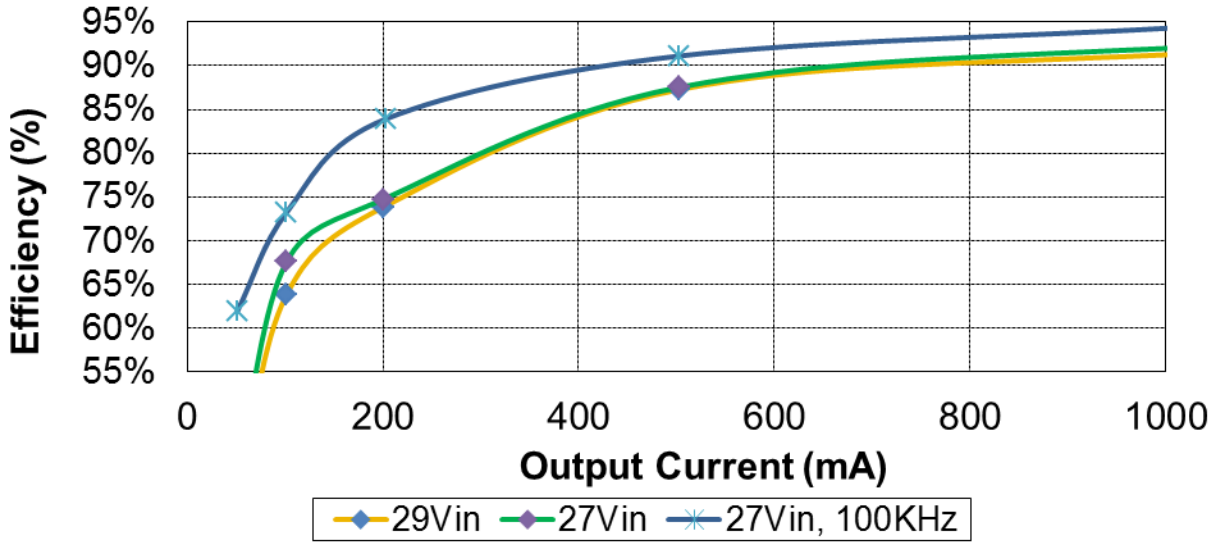
27Vin, Fsw = 250 KHz						
Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
27.00	28.6	0.7722	11.99	0	0.00	0%
27.00	51.5	1.391	11.99	50.9	0.61	43.9%
27.00	66.8	1.804	11.99	101.7	1.22	67.6%
27.04	118.9	3.22	11.99	200.4	2.40	74.7%
27.02	254.9	6.89	11.99	502.9	6.03	87.5%
27.00	484.0	13.07	11.99	1002.9	12.02	92.0%
27.05	932	25.22	11.99	2000	23.98	95.1%
27.00	1836	49.57	11.99	3998	47.94	96.7%
27.00	2979	80.43	11.99	6494	77.86	96.8%

27Vin, Fsw = 100 KHz						
Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
27.00	9.4	0.2538	11.99	0	0	0%
27.00	36.6	0.988	11.99	51.0	0.61	61.9%
27.00	61.7	1.666	11.99	101.8	1.22	73.3%
27.00	107.5	2.90	11.99	203.2	2.44	83.9%
27.00	245.1	6.62	11.99	503.0	6.03	91.1%
27.00	472.2	12.75	11.99	1002.9	12.02	94.3%

More details about efficiency:



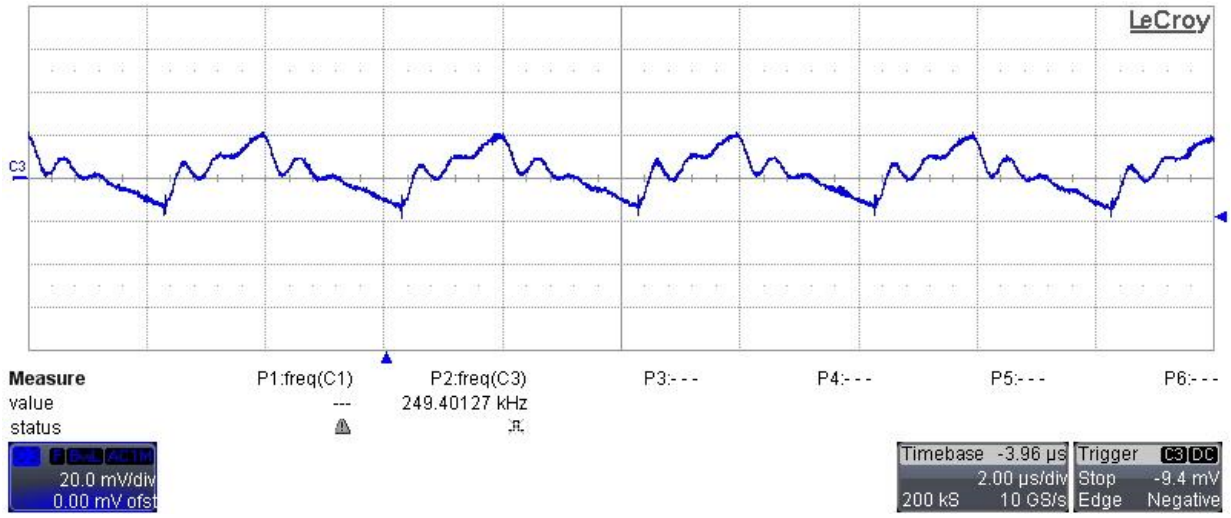
Light load details:



6. Output Ripple Voltage

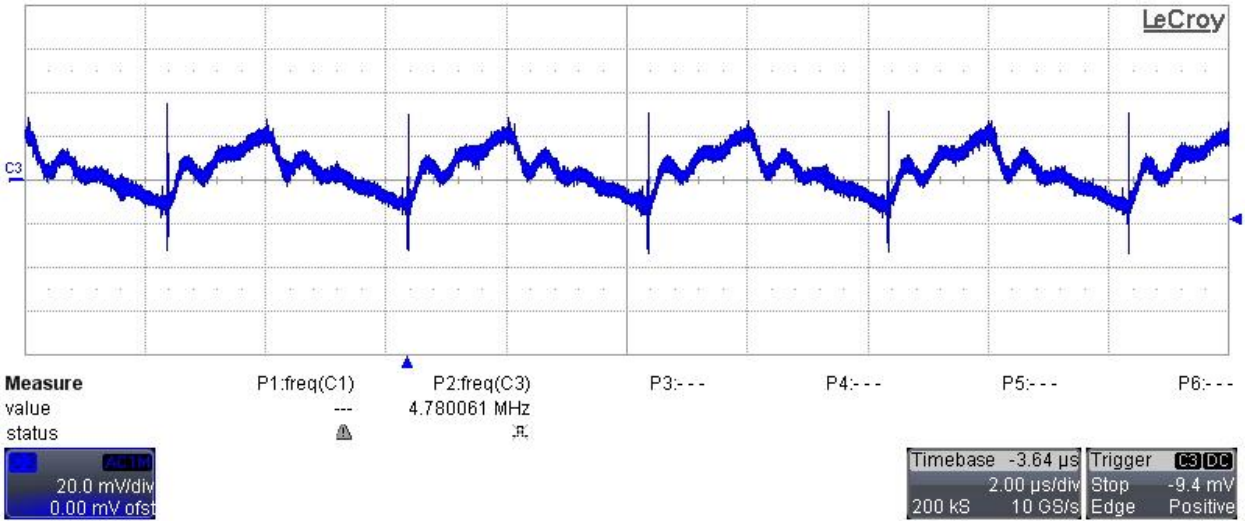
The output ripple voltage has been measured by supplying the converter at 29V while running at full load.

Ch.3: Output ripple voltage (20mV/div, AC coupling, 2usec/div, 20MHz BWL)



The following shows the measurement taken at the same conditions but without any bandwidth limit.

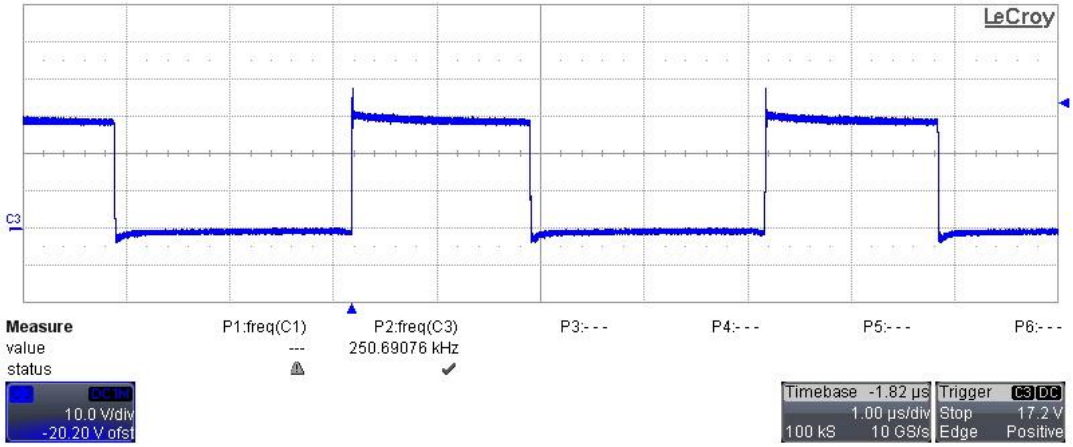
Ch.3: Output ripple voltage (20mV/div, AC coupling, 2usec/div, no BWL)



7. Switch Node

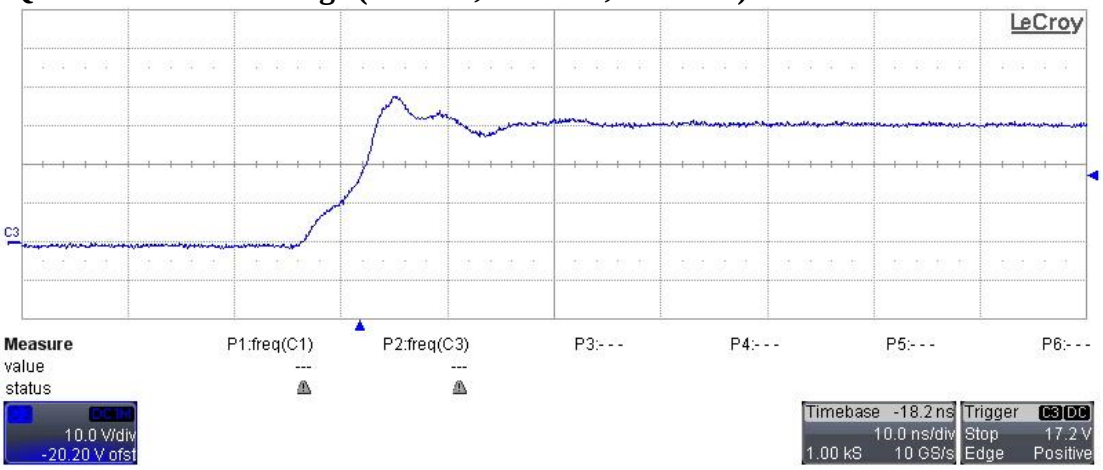
The images below show the drain of Q3 taken at Vin = 29V and full load.

Ch.3: Q3 Drain-Source voltage (10V/div, 1us/div, no BWL)

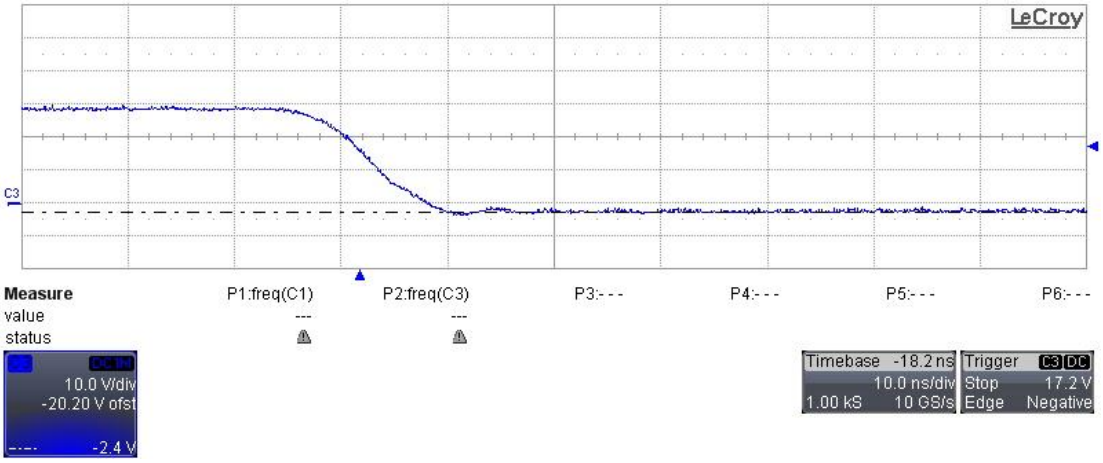


Rise time:

Ch.3: Q3 Drain-Source voltage (10V/div, 10ns/div, no BWL)



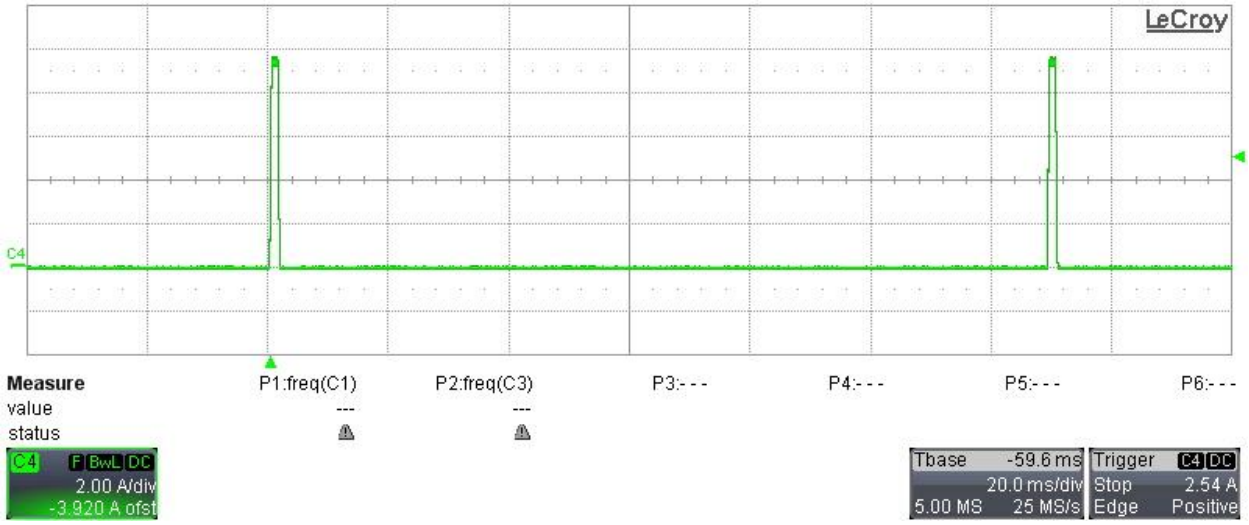
Fall time:



8. Behavior in short circuit

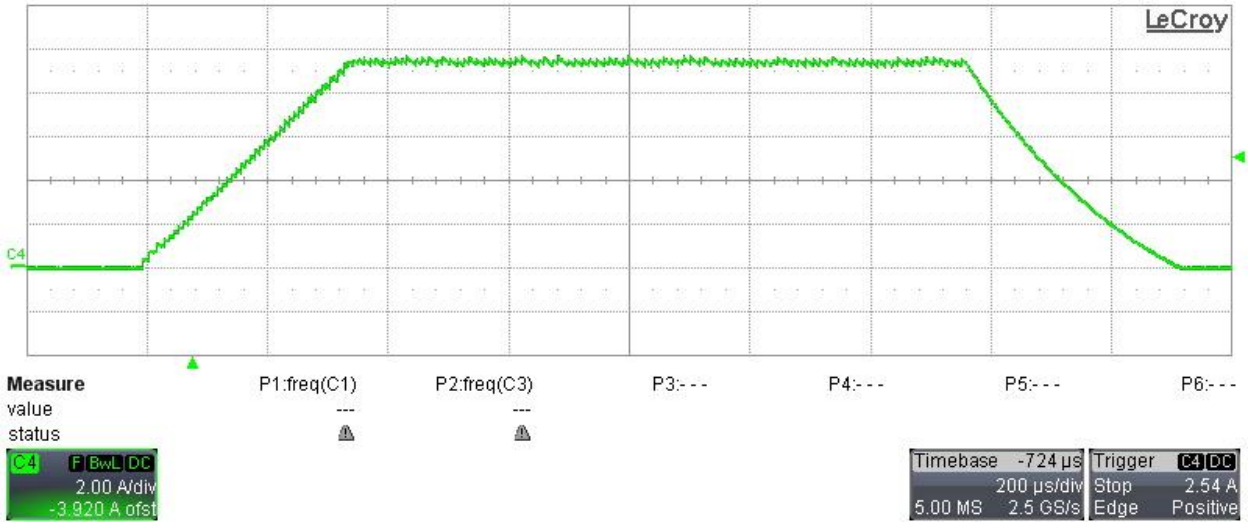
The images below show the behavior of inductor current during short circuit condition at Vin = 29V.

Ch.4: L1 inductor current (2A/div, 20ms/div, 20MHz BWL)



Same measurement but with smaller time base:

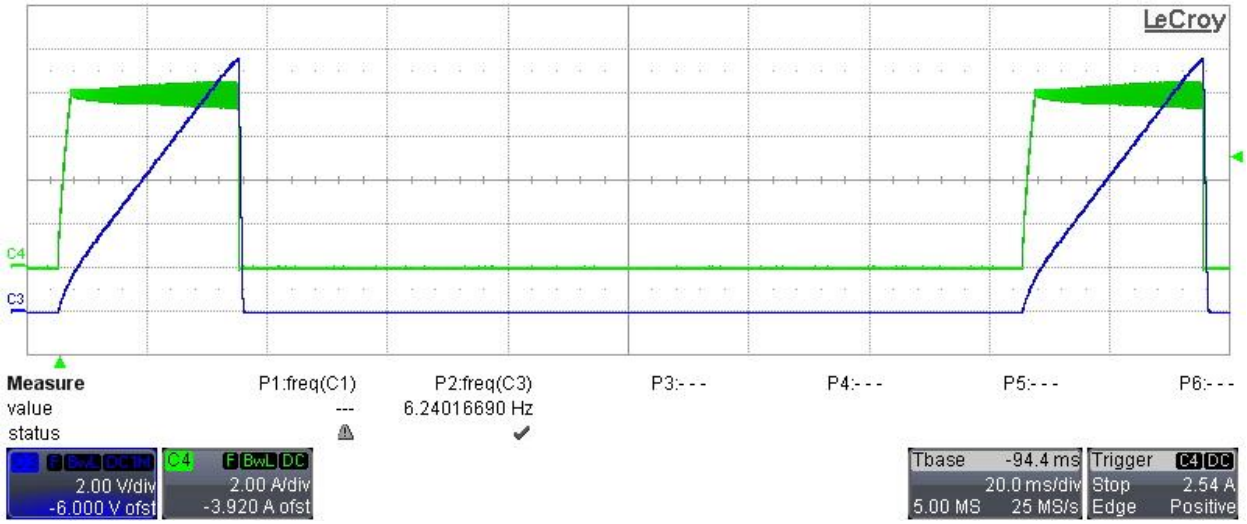
Ch.4: L1 inductor current (2A/div, 200us/div, 20MHz BWL)



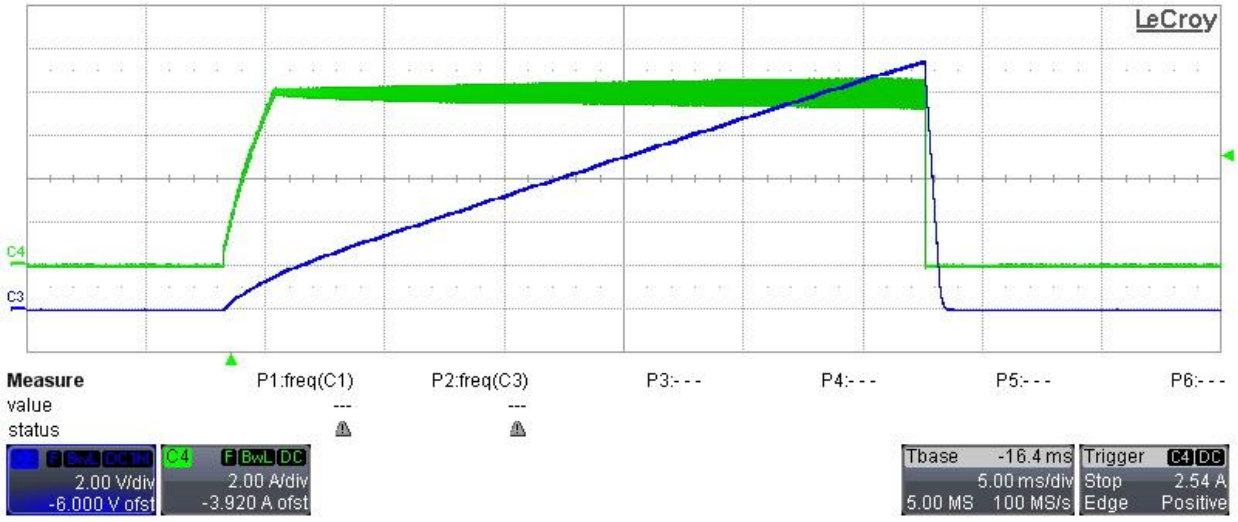
9. Current limit protection

The images below show the behavior of the converter during current limit protection (without latch). Vin has been set to 29V and the current increased until switch-off.

Ch.4: L1 inductor current (2A/div, 20ms/div, 20MHz BWL)
Ch.3: Output voltage (2V/div, 20MHz BWL)
Load = 7.6A



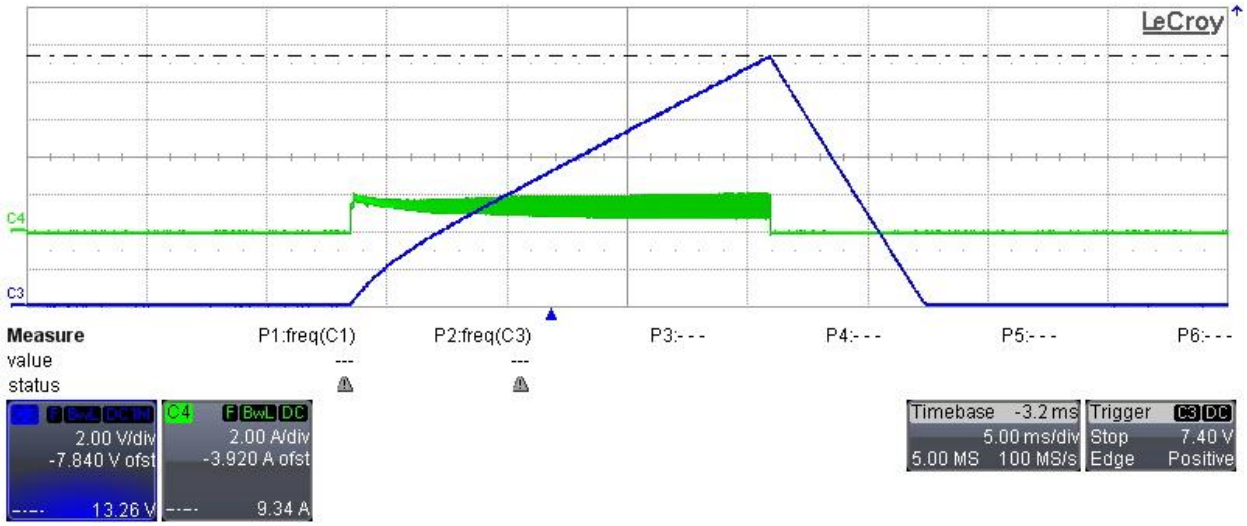
Same measurement as above, but with smaller time base:
Ch.4: L1 inductor current (2A/div, 5ms/div, 20MHz BWL)
Ch.3: Output voltage (2V/div, 20MHz BWL)
Load = 7.6A



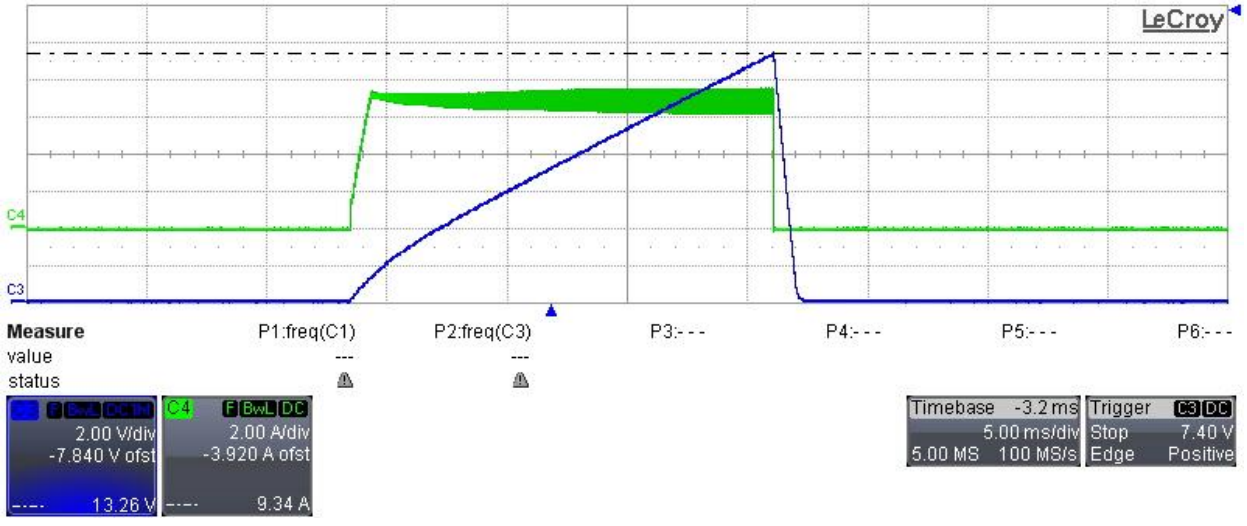
10. Behavior during over voltage protection

The images below show the behavior of the converter during over-voltage protection (with latch), performed by decreasing R9 to a value equivalent to Vout = 15V. Vin has been set to 29V and the load set to 1A for the first screenshot, 6.5A for the second one and unloaded for the third one.

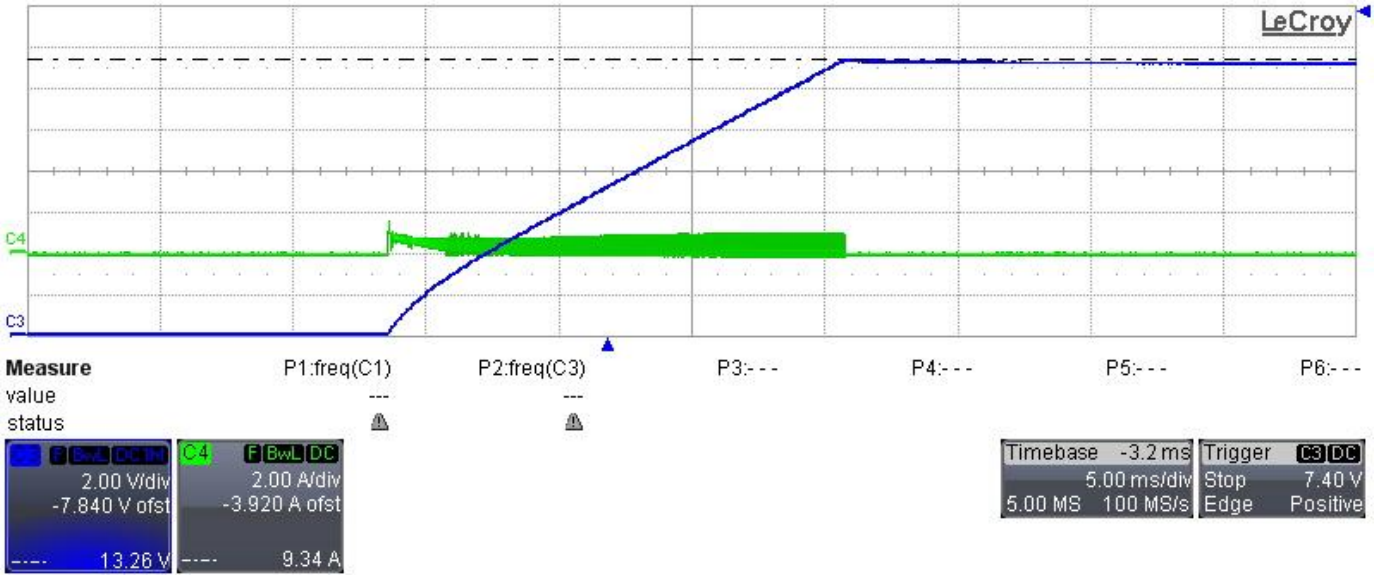
Ch.3: Output voltage (2V/div, 5ms/div, 20MHz BWL)
Ch.4: L1 inductor current (2A/div, 20MHz BWL)
Load = 1A



Ch.3: Output voltage (2V/div, 5ms/div, 20MHz BWL)
Ch.4: L1 inductor current (2A/div, 20MHz BWL)
Load = 6.5A



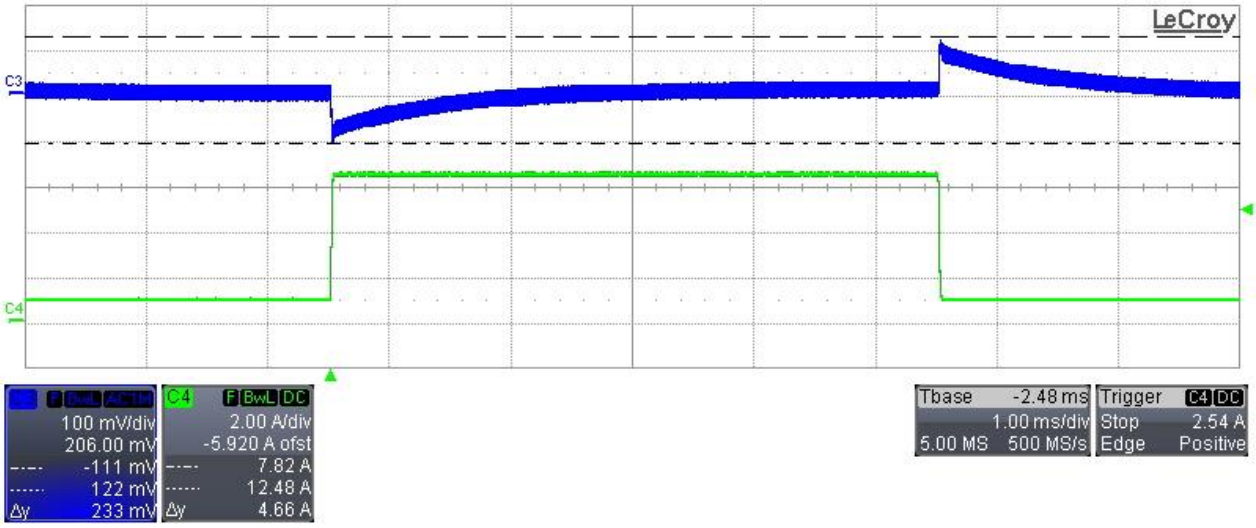
Ch.1: Output voltage (2V/div, 5ms/div, 20MHz BWL)
Ch.4: L1 inductor current (2A/div, 20MHz BWL)
Load = 0



11. Load transient response

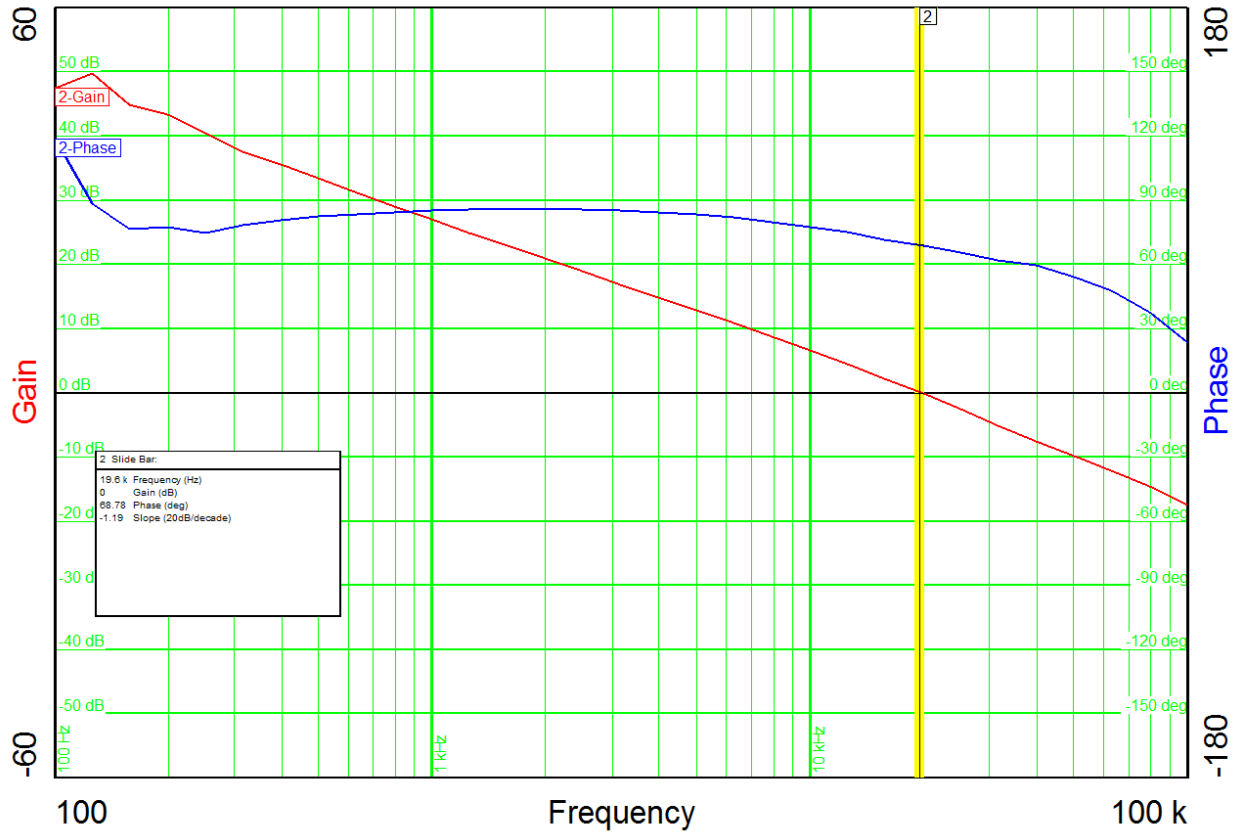
The converter has been loaded by switching the output current between 2A and 10A while supplied at 29V. The image below shows the output voltage deviation from nominal value.

Ch.3: Output voltage (100mV/div, 1ms/div, AC coupling, 20MHz BWL)
Ch.4: Output current (2A/div, 20MHz BWL)



12. Feedback Loop Analysis

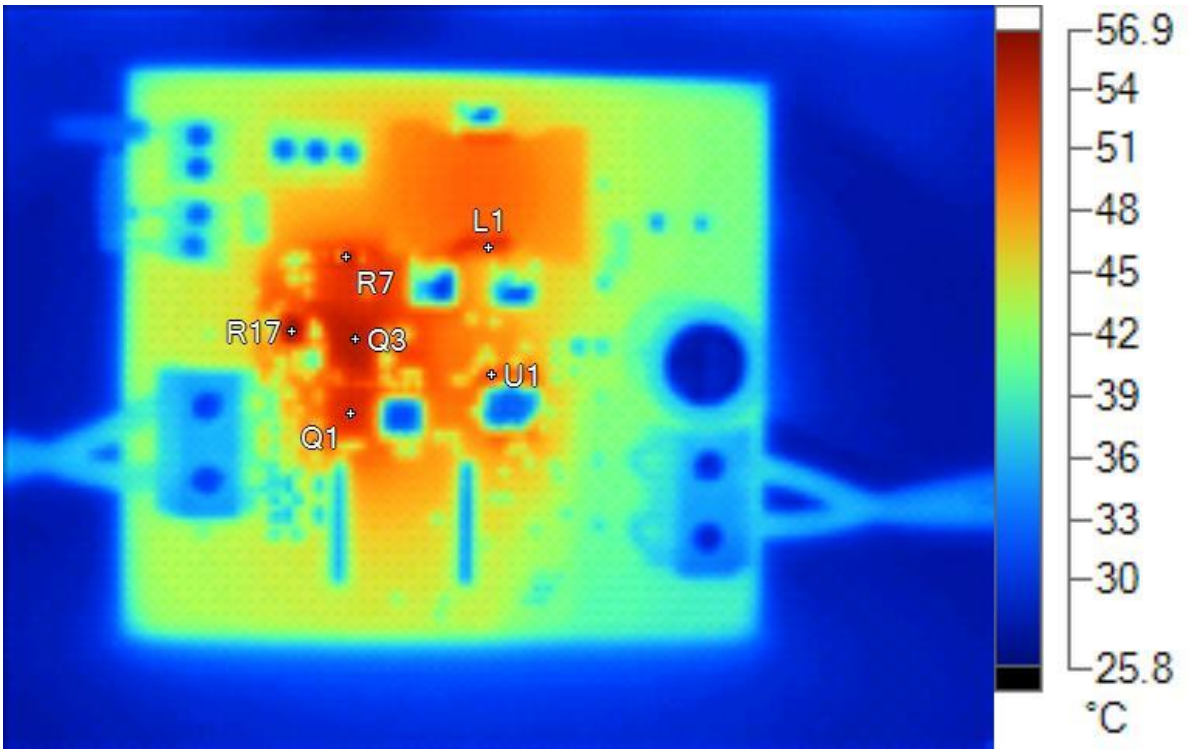
The image below shows the open loop gain and phase bode plot of the converter. The board has been supplied at Vin = 29V and the load was a constant-current electronic load, set to 6.5A.
Crossover frequency: 19.6 KHz
Phase margin: 68.78 deg.
Gain margin: > 20 dB



13. Thermal Analysis

During the thermal analysis, the converter has been placed vertical on the bench in still air conditions, while supplied at 29V and fully loaded.

The thermal image has been taken after 30 minutes @ Ta = 25C.



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Main Image Markers

Name	Temperature	Emissivity	Background
Q1	53.8°C	0.95	25.0°C
Q3	54.7°C	0.95	25.0°C
R17	55.7°C	0.95	25.0°C
R7	51.3°C	0.95	25.0°C
L1	52.1°C	0.95	25.0°C
U1	50.5°C	0.95	25.0°C

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