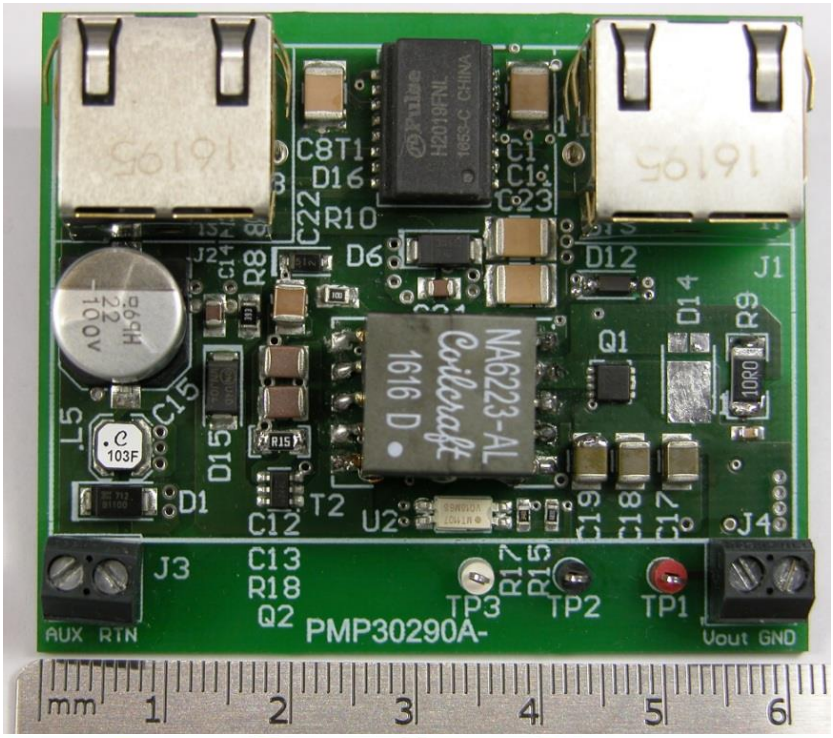
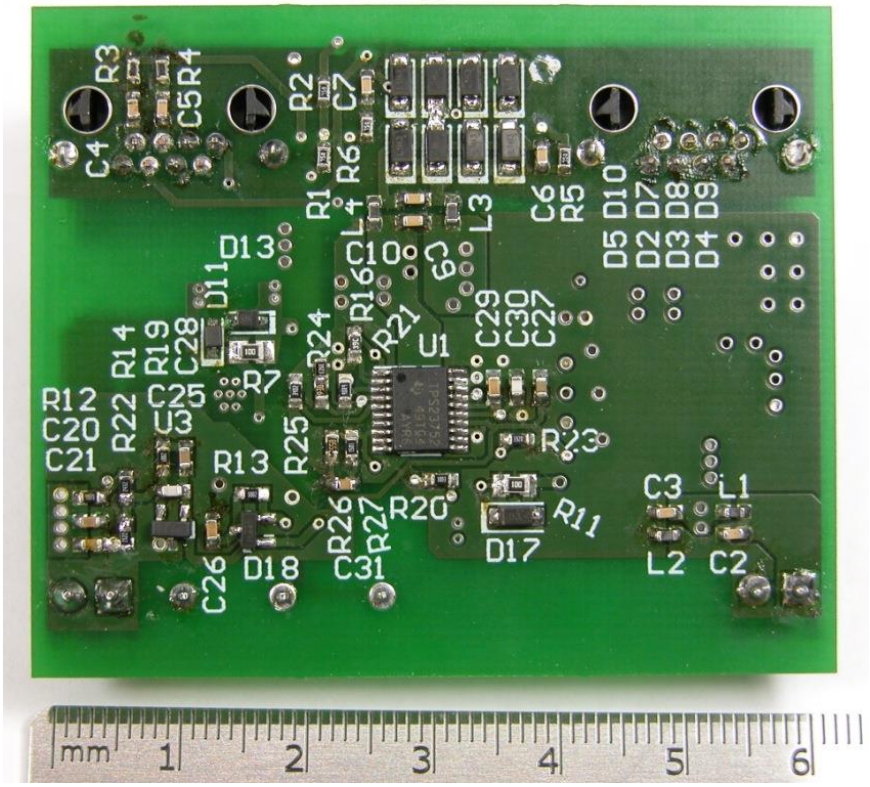
1 Photo of the prototype

The reference design PMP30290 Rev_B has been built on PMP30290 Rev_A PCB

Board: 52mm x 62mm, effective dimensions (white rectangle): 40mm x 60mm

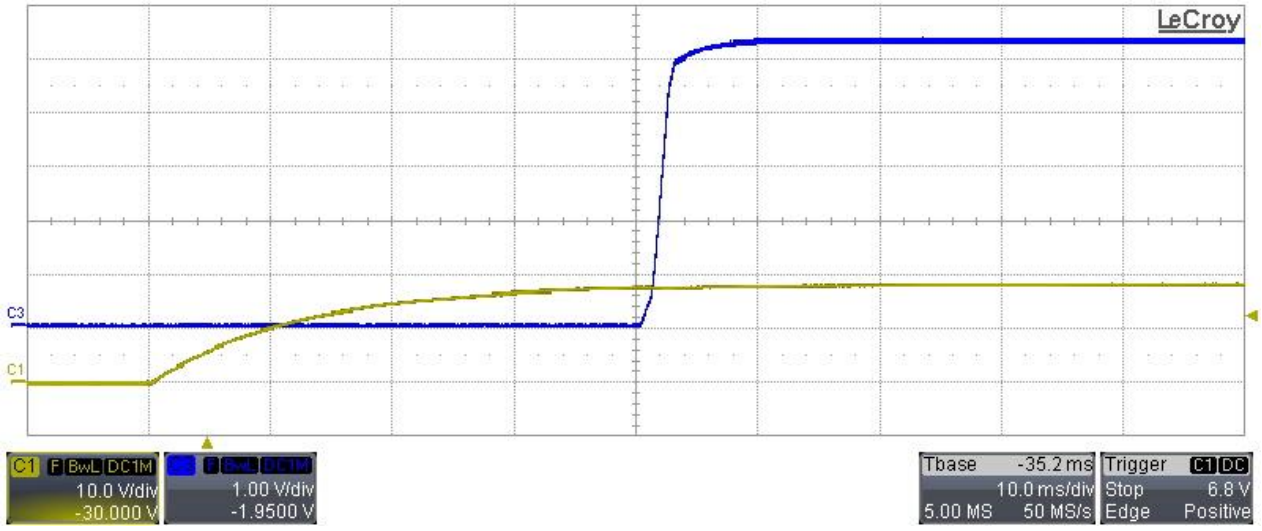




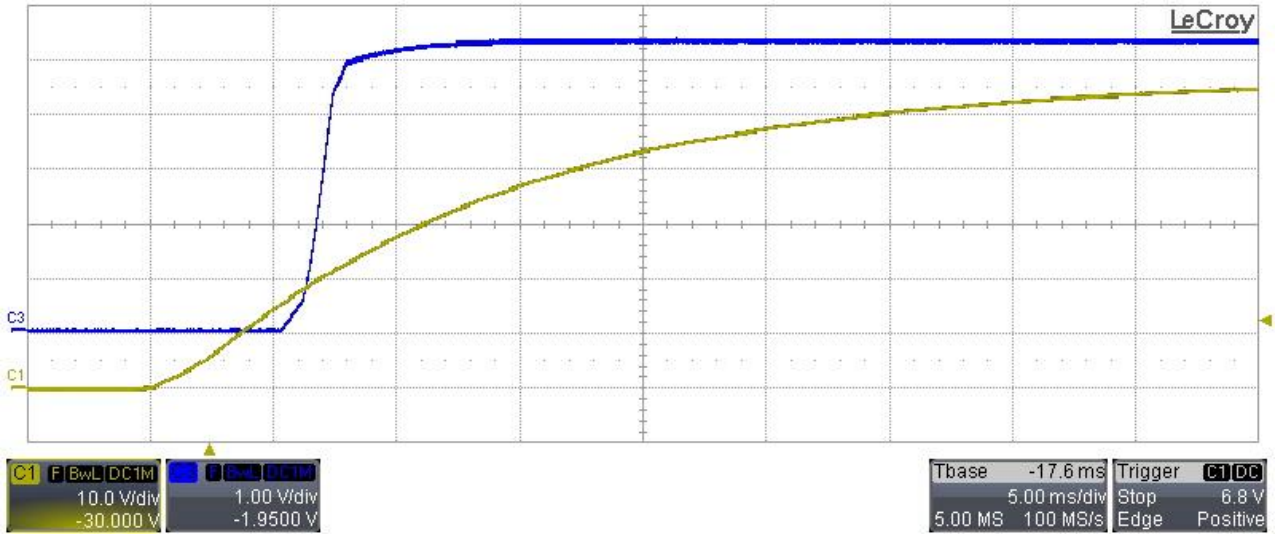
2 Startup

The input and output voltage ramp-up behavior is shown in the images below.
Vin has been set to 18.5V and 57V, using the auxiliary input J3.
The output was unloaded and fully loaded.

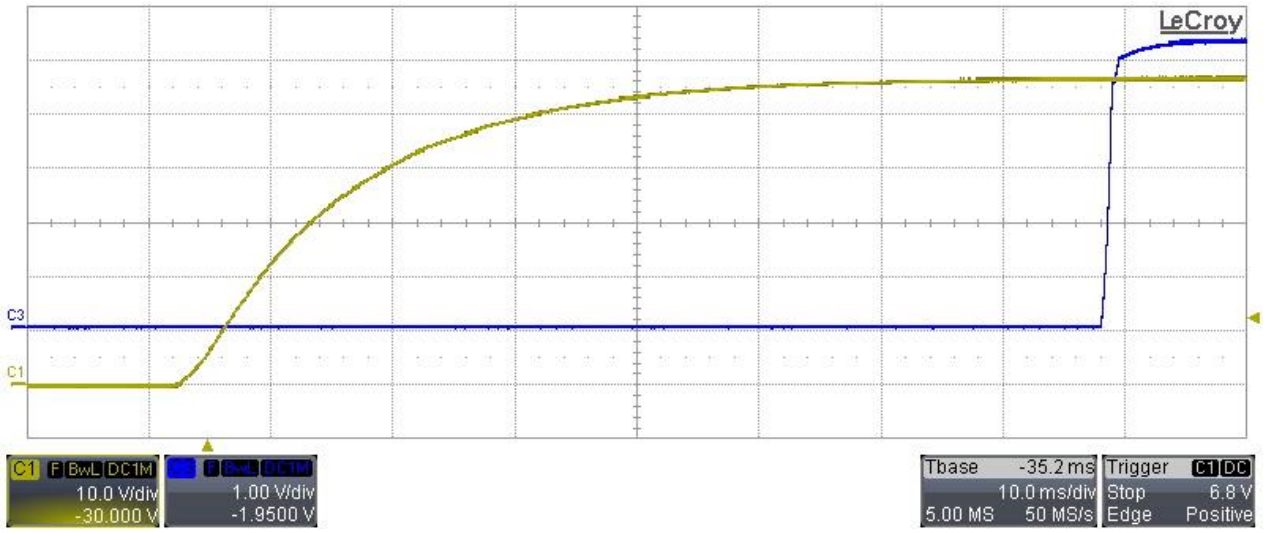
Ch.1: Input voltage (10V/div, 10ms/div, 20MHz BWL)
Ch.3: Output voltage (1V/div, 20MHz BWL)
Vin = 18.5V, Full load.



Ch.1: Input voltage (10V/div, 5ms/div, 20MHz BWL)
Ch.3: Output voltage (1V/div, 20MHz BWL)
Vin = 57V, Full load.



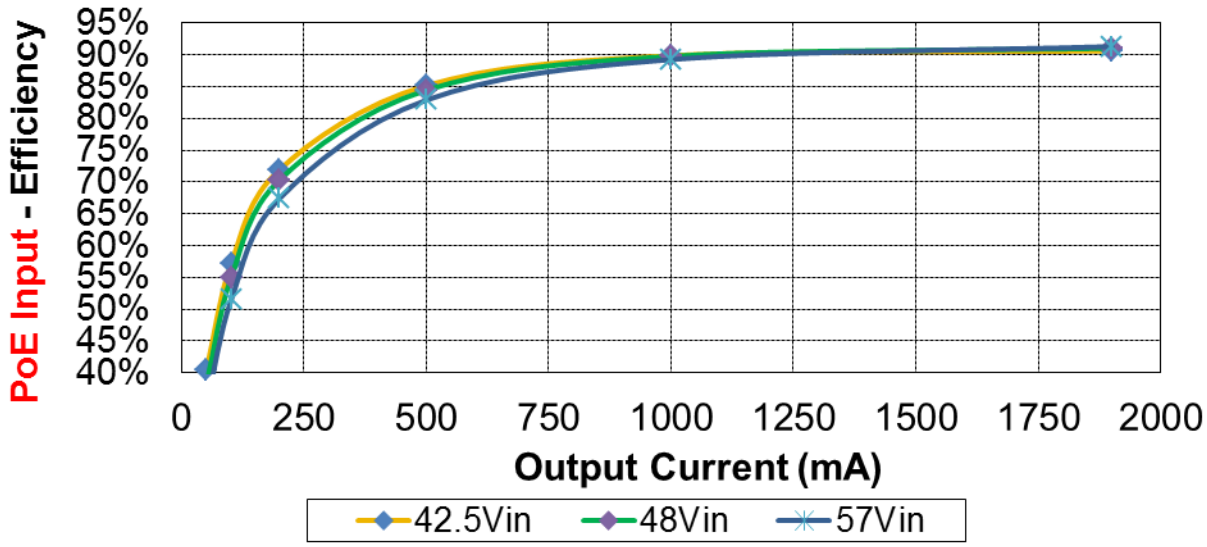
Ch.1: Input voltage (10V/div, 10ms/div, 20MHz BWL)
Ch.3: Output voltage (1V/div, 20MHz BWL)
Vin = 57V, Zero load.



3 Efficiency

The efficiency data, versus input voltage and output current are shown in the tables and graph below. The load has been varied from zero to 1.9A, Vin from 18.5V to 57V and both inputs (Auxiliary J3 and PoE J1) have been used.

PoE Input (J1):

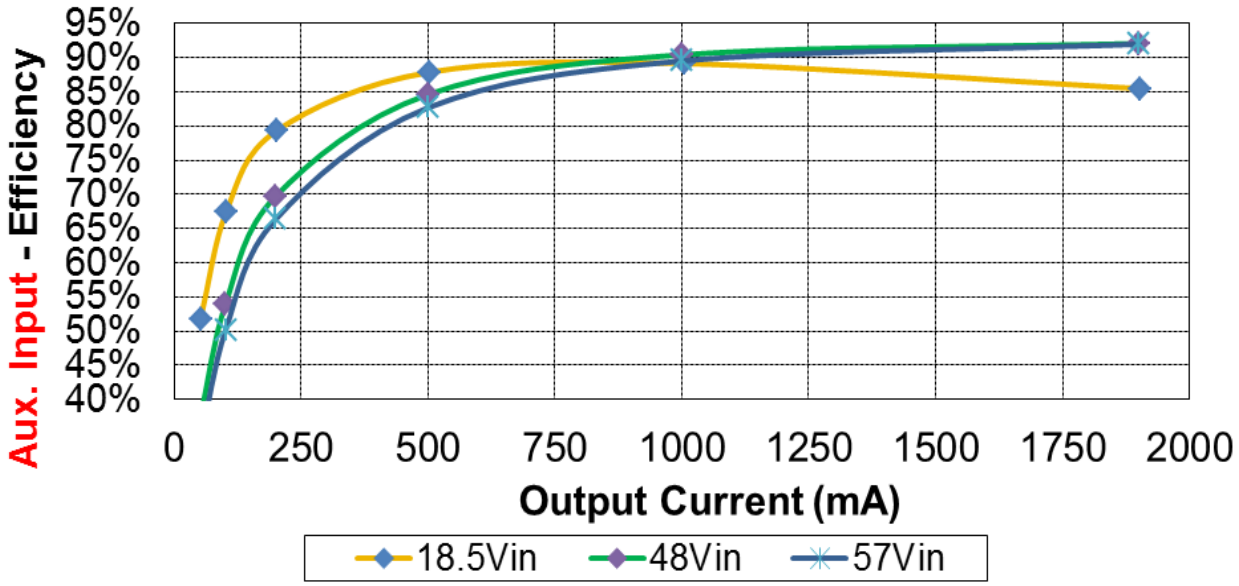


Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
42.52	9.41	0.4001	5.349	0.0	0	0%
42.51	15.90	0.676	5.349	51.0	0.273	40.4%
42.53	22.39	0.952	5.349	101.8	0.545	57.2%
42.53	35.06	1.49	5.349	200.6	1.07	72.0%
42.56	73.83	3.14	5.347	500.6	2.68	85.2%
42.53	139.88	5.95	5.344	1000.7	5.35	89.9%
42.54	263.19	11.20	5.339	1901.0	10.15	90.7%

Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
48.12	9.12	0.4389	5.350	0.0	0	0%
48.10	14.85	0.714	5.350	51.0	0.273	38.2%
48.09	20.59	0.990	5.350	101.8	0.545	55.0%
48.07	31.74	1.53	5.350	200.6	1.07	70.3%
48.00	66.03	3.17	5.348	500.6	2.68	84.5%
48.04	124.00	5.96	5.345	1000.7	5.35	89.8%
48.03	232.13	11.15	5.341	1901.0	10.15	91.1%

Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
57.03	8.91	0.5081	5.351	0.0	0	0%
57.02	13.73	0.783	5.351	51.0	0.273	34.9%
57.01	18.57	1.059	5.351	101.8	0.545	51.5%
57.00	27.93	1.59	5.351	200.6	1.07	67.4%
57.04	56.62	3.23	5.349	500.6	2.68	82.9%
57.05	105.06	5.99	5.347	1000.7	5.35	89.3%
57.03	195.00	11.12	5.342	1901.0	10.16	91.3%

Auxiliary Input (J3):



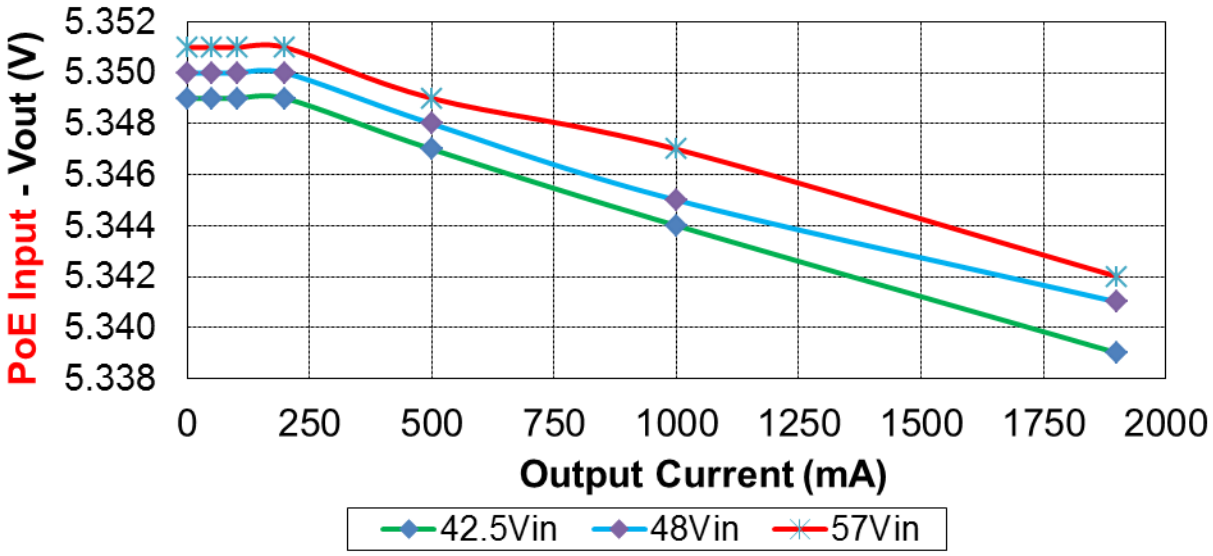
Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
18.52	13.71	0.2539	5.348	0.0	0	0%
18.49	29.07	0.538	5.348	52.0	0.278	51.7%
18.52	44.03	0.815	5.348	102.9	0.550	67.5%
18.50	73.48	1.36	5.348	201.6	1.08	79.3%
18.54	165.39	3.07	5.345	504.3	2.70	87.9%
18.53	324.77	6.02	5.341	1004.5	5.37	89.1%
18.51	641.00	11.86	5.333	1902.0	10.14	85.5%

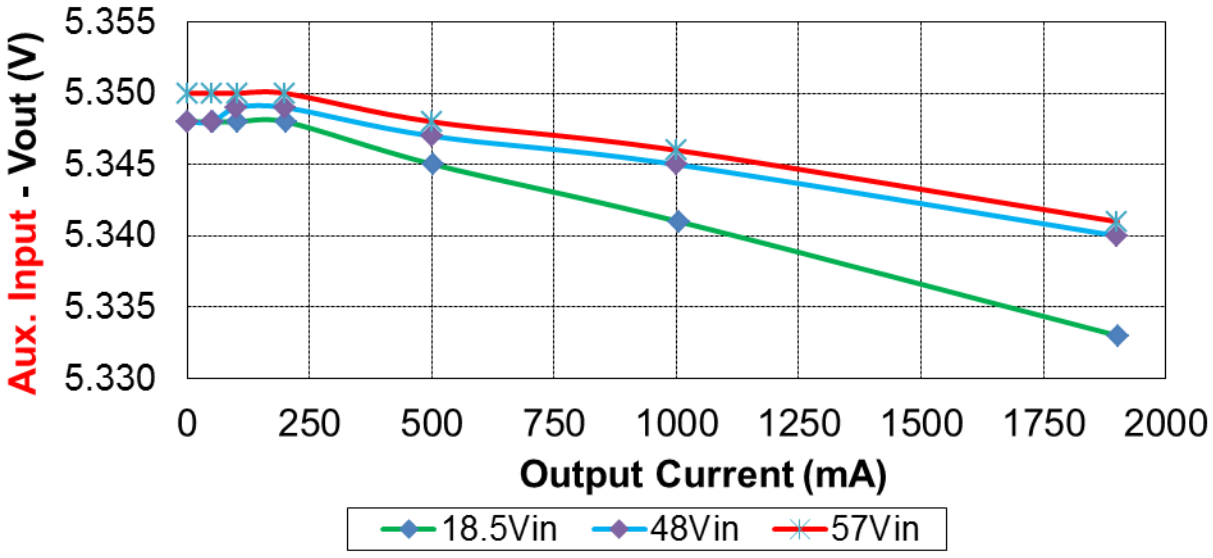
Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
48.00	9.62	0.4618	5.348	0.0	0	0%
47.99	15.29	0.734	5.348	50.8	0.272	37.0%
48.03	20.94	1.006	5.349	101.6	0.543	54.0%
48.01	32.02	1.54	5.349	200.5	1.07	69.8%
48.09	65.75	3.16	5.347	500.5	2.68	84.6%
48.04	123.11	5.91	5.345	1000.7	5.35	90.4%
48.04	229.46	11.02	5.340	1901.0	10.15	92.1%

Vin (V)	Iin(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)
57.03	9.49	0.5412	5.350	0.0	0	0%
57.02	14.27	0.814	5.350	51.0	0.273	33.5%
57.01	19.03	1.085	5.350	101.8	0.545	50.2%
57.05	28.33	1.62	5.350	200.6	1.07	66.4%
57.00	56.79	3.24	5.348	500.6	2.68	82.7%
57.05	104.74	5.98	5.346	1000.8	5.35	89.5%
57.03	193.51	11.04	5.341	1901.0	10.15	92.0%

4 Output Voltage Regulation

The output voltage variation graphs versus output current, for three different input voltages, and by using both inputs J1 and J3, are plotted below.

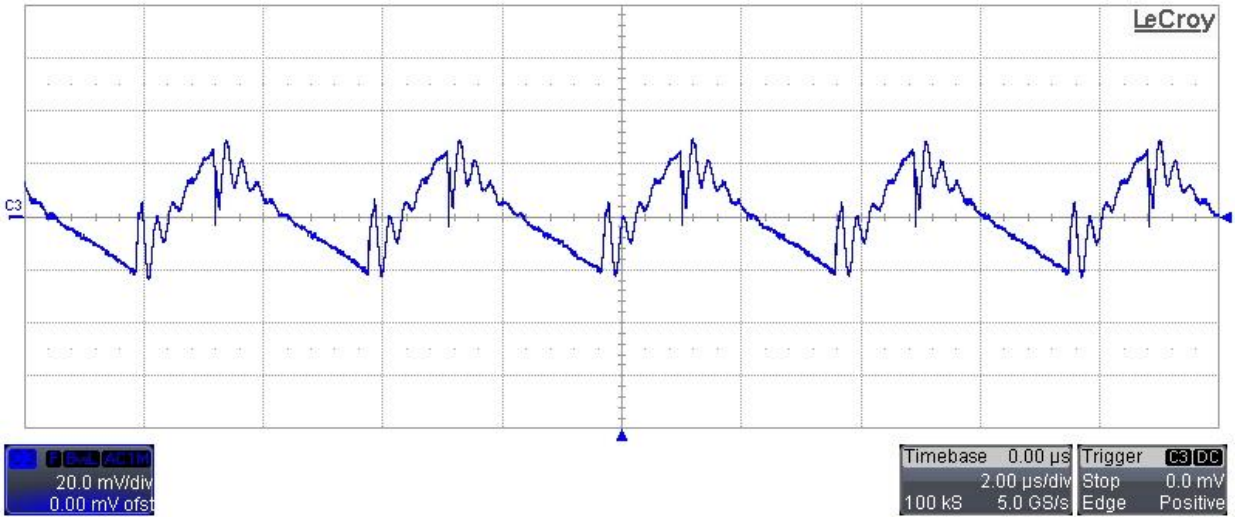




5 Output Ripple Voltage

The output ripple voltage has been measured by supplying the converter at 18.5V on J3 (worst case) while running at full load.

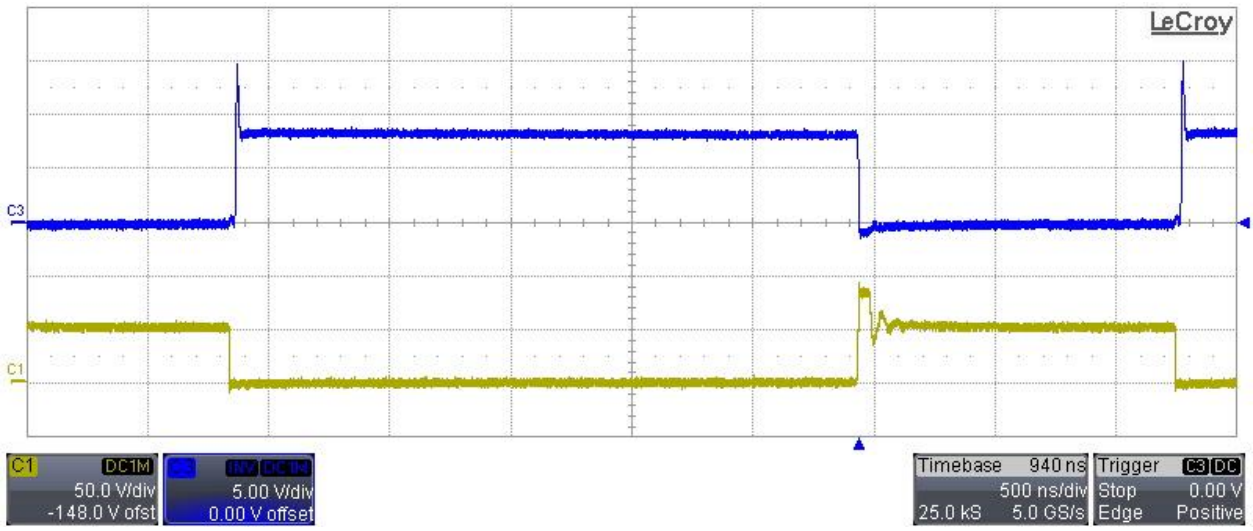
Ch.3: Output voltage (20mV/div, 2usec/div, AC coupling, 20MHz BWL)



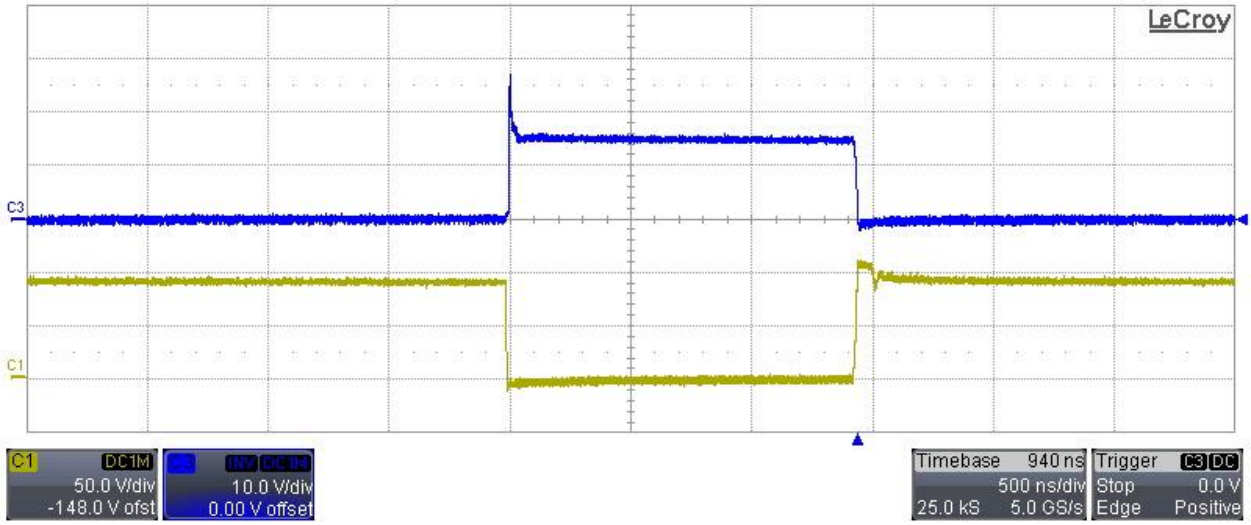
6 Switch Nodes (Q1, Q2 V_{DS})

The Drain-Source voltages of both FETs (Q1 and Q2) are shown in the picture below. Vin has been set to 18.5V and 57V, by using J3 input, while running at full load.

Ch.1: Q2 V_{DS} voltage (50V/div, 500ns/div, no BWL)
Ch.3: Q1 V_{DS} voltage (5V/div, no BWL)
Vin = 18.5V



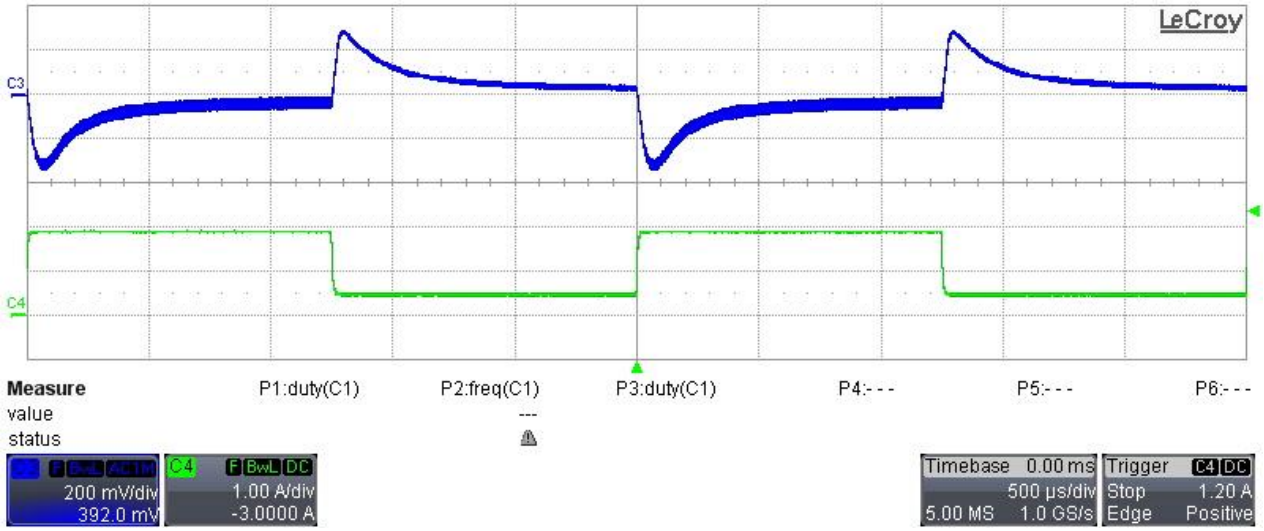
Ch.1: Q2 V_{DS} voltage (50V/div, 500ns/div, no BWL)
Ch.3: Q1 V_{DS} voltage (10V/div, no BWL)
Vin = 57V



7 Transient Response

The image below shows the response during output current variation between 0.5A and 1.9A. Vin has been set to 18.5V (worst case condition).

Ch.4: Output current (1A/div, DC coupling, 500usec/div, 20MHz BWL)
Ch.3: Output voltage (200mV/div, AC coupling, 20MHz BWL)
Vin = 18.5V

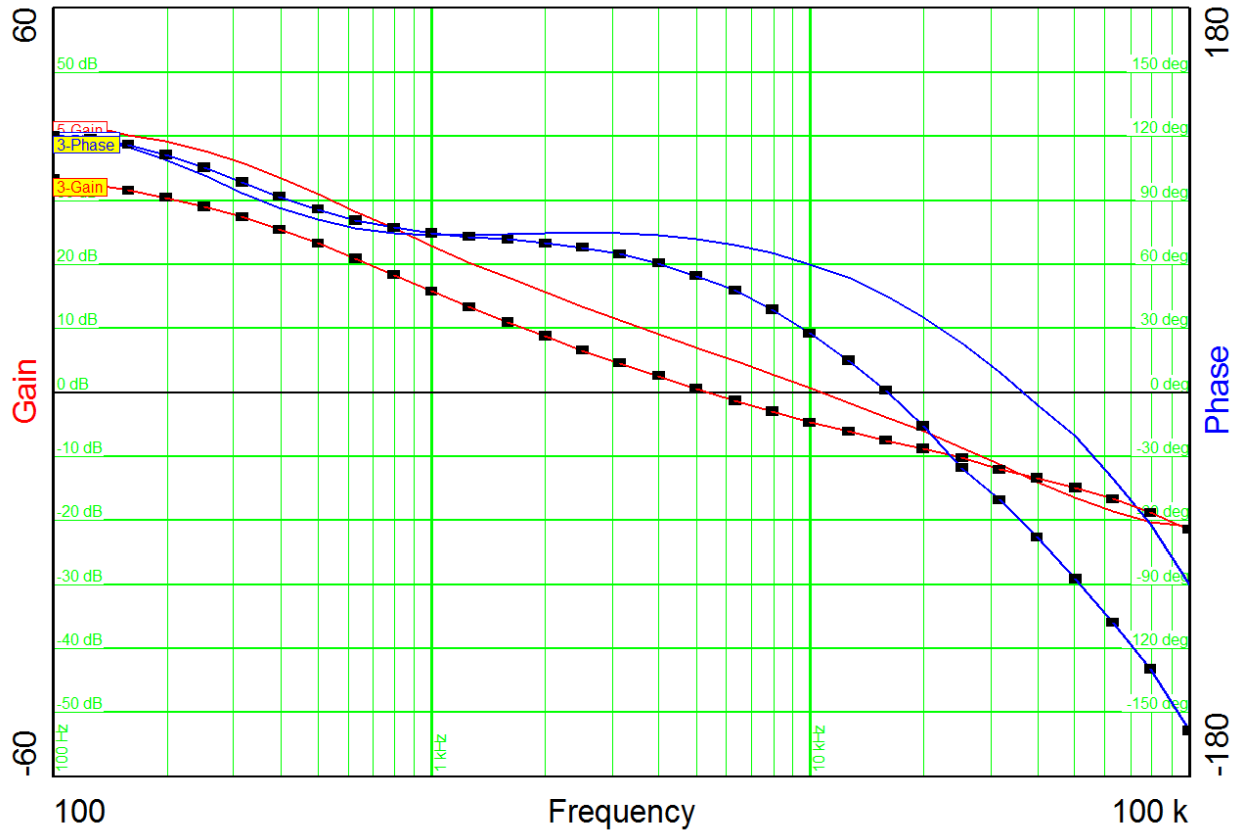


8 Feedback Loop Analysis

The image below shows the open loop gain and phase margin. The curves with lower crossover frequency refers to 18.5Vin (dotted line), while the solid line refers to 57Vin, both measured at full load.

Vin = 18.5V
Crossover frequency: 5.335 KHz
Phase margin: 52.62 deg.

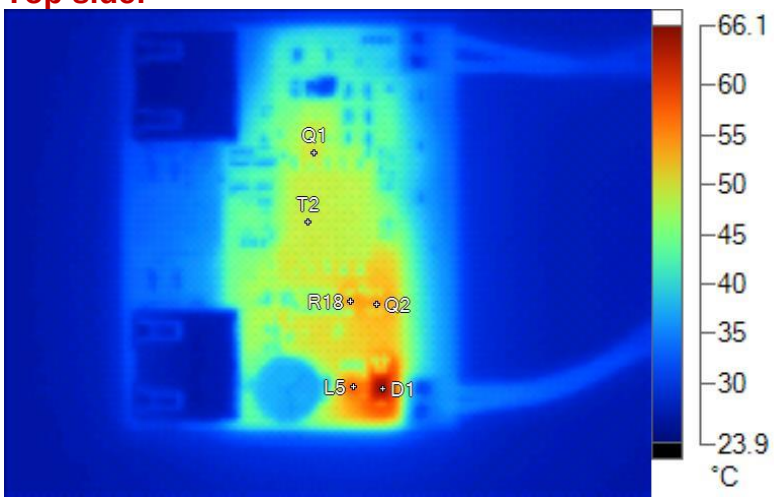
Vin = 57V
Crossover frequency: 10.66 KHz
Phase margin: 58.18 deg.



9 Thermal Analysis

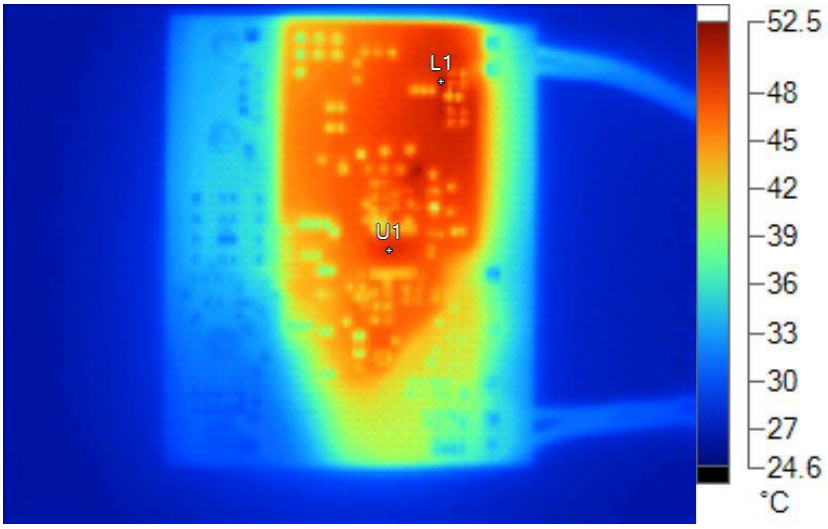
During the thermal analysis, the converter has been placed horizontally on the bench in still air conditions, while delivering 1.9A from 18.5V source.

Top side:



Name	Temperature	Emissivity	Background
D1	65.1°C	0.95	23.0°C
Q2	54.1°C	0.95	23.0°C
R18	54.0°C	0.95	23.0°C
L5	56.6°C	0.95	23.0°C
T2	48.9°C	0.95	23.0°C
Q1	49.5°C	0.95	23.0°C

Bottom side:



Name	Temperature	Emissivity	Background
L1	50.3°C	0.95	23.0°C
U1	49.3°C	0.95	23.0°C

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