

TI Designs: TIDA-01023

High-Channel-Count JESD204B Clock Generation Reference Design for RADAR and 5G Wireless Testers



Description

High-speed multichannel applications require low noise and scalable clocking solutions capable of precise channel-to-channel skew adjustment to achieve the optimal system signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), and effective number of bits (ENOB). This reference design supports high-channel-count, JESD204B-synchronized clocks using one master and multiple slave clocking devices. This design provides multichannel JESD204B clocks using TI's LMK04828 clock jitter cleaner and LMX2594 wideband phase-locked loop (PLL) with integrated VCOs to achieve a clock-to-clock skew of less than 10 ps. This design has been tested with TI's ADC12DJ3200 EVMs at 3 GSPS and a channel-to-channel skew of less than 50 ps is achieved with the improved SNR performance. All key design theories are described to guide users through the part selection process and design optimization.

Resources

TIDA-01023	Design Folder
ADC12DJ3200EVM	Tool Folder
ADC12DJ3200	Product Folder
LMX2594	Product Folder
LMK04828	Product Folder
LMK04828EVM	Tool Folder
TSW14J56EVM	Tool Folder

Features

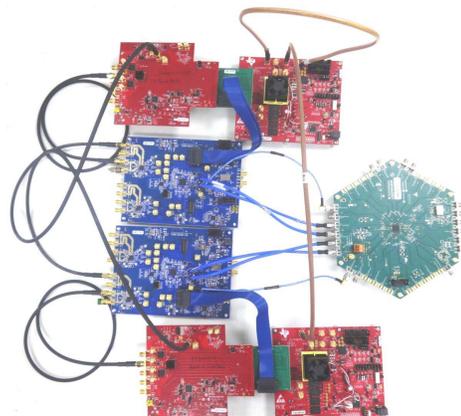
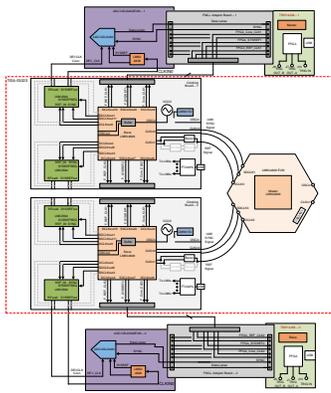
- High-Frequency (GSPS) Sample Clock Generation
- High Channel Count and Scalable JESD204B Compliant Clock Solution
- Low Phase Noise Clocking for RF Sampling ADC and DAC
- Configurable Phase Synchronization to Achieve Low Skew in Multichannel System
- Supports TI's High-Speed Converter and Capture Cards (ADC12DJ3200EVM, TSW14J56, or TSW14J57)

Applications

- [Wireless Communication Testers](#)
- [Phased Array Radars](#)



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1 System Description

Clocking solutions for high-speed GPS direct RF sampling signal chains are critical to achieve a high signal-to-noise ratio (SNR), low channel-to-channel skew, and to scale up the synchronized clocks for several pieces of end equipment. The tool folder for the TIDA-01021 shows the multichannel phase-synchronized JESD204B clock generation: [The Multichannel JESD204B 15-GHz Clocking Reference Design for DSO, Radar, and 5G Wireless Testers](#). This reference design is an enhancement of the TIDA-01021 reference design to scale up the synchronized clocks (multiboard synchronization) that can be used in applications such as a 5G wireless tester, phased array radars, and so forth.

Various topologies are available for synchronizing the multiple devices or boards, such as the tree topology and daisy chain topology. This design uses a tree topology to synchronize the multiple clocking boards. In this configuration, one master board (LMK04828 EVM) receives a high-frequency reference signal from an external clock source, which is distributed to the slave boards (clocking boards) along with the sync signals for synchronizing the slave devices. In this solution, master and slave LMK04828s are in distribution mode and do not add PLL noise. LMX2594 frequency synthesizers receive a reference signal through the slave LMK04828s and generate high-performance phase synchronized device clocks (sampling clocks) and SYSREF for multichannel high-speed signal chains. The slave LMK04828 also generates the field programmable gate array (FPGA) device clocks and SYSREFs to each channel.

Wireless tester equipment uses multichannel receivers for testing cellular and multiple-input and multiple-output (MIMO) devices. Wireless testers require multiple synchronized analog channels, high dynamic range, and wideband receivers to test 3G and later wireless standards compliant equipment. The ADC12DJ3200 is well suited for the multichannel receiver requirements of the wireless testers. The clocking solution that this reference design describes supplements a high-performance signal chain solution based on multiple ADC12DJ3200 analog-to-digital converters (ADCs) to achieve a low time skew between channels that provide both high dynamic range and a wide receiver.

Phased-array radar applications require multiple synchronized channels, high dynamic range, wide receiver bandwidth, and low latency. The signal chain solution based on the LMX2594, ADC12DJ3200, and LMK04828 devices are able to achieve optimum performance and high channel counts for phased-array radar applications.

1.1 Key System Specifications

The objective of the reference design is to demonstrate a scaling up of the high-speed clocking solution for multichannel signal chains. This design focuses on measuring the configurable phase delay to align board-to-board multichannel clocks, the SNR at ADC12DJ3200 multiple signal chains, and the time skew between them. The TSW14J56 devices performs the data capture, which is interfaced with the ADC12DJ3200EVM using an FMC adapter card. [Table 1](#) lists the key system level specifications for the signal chain from the clocking solution perspective.

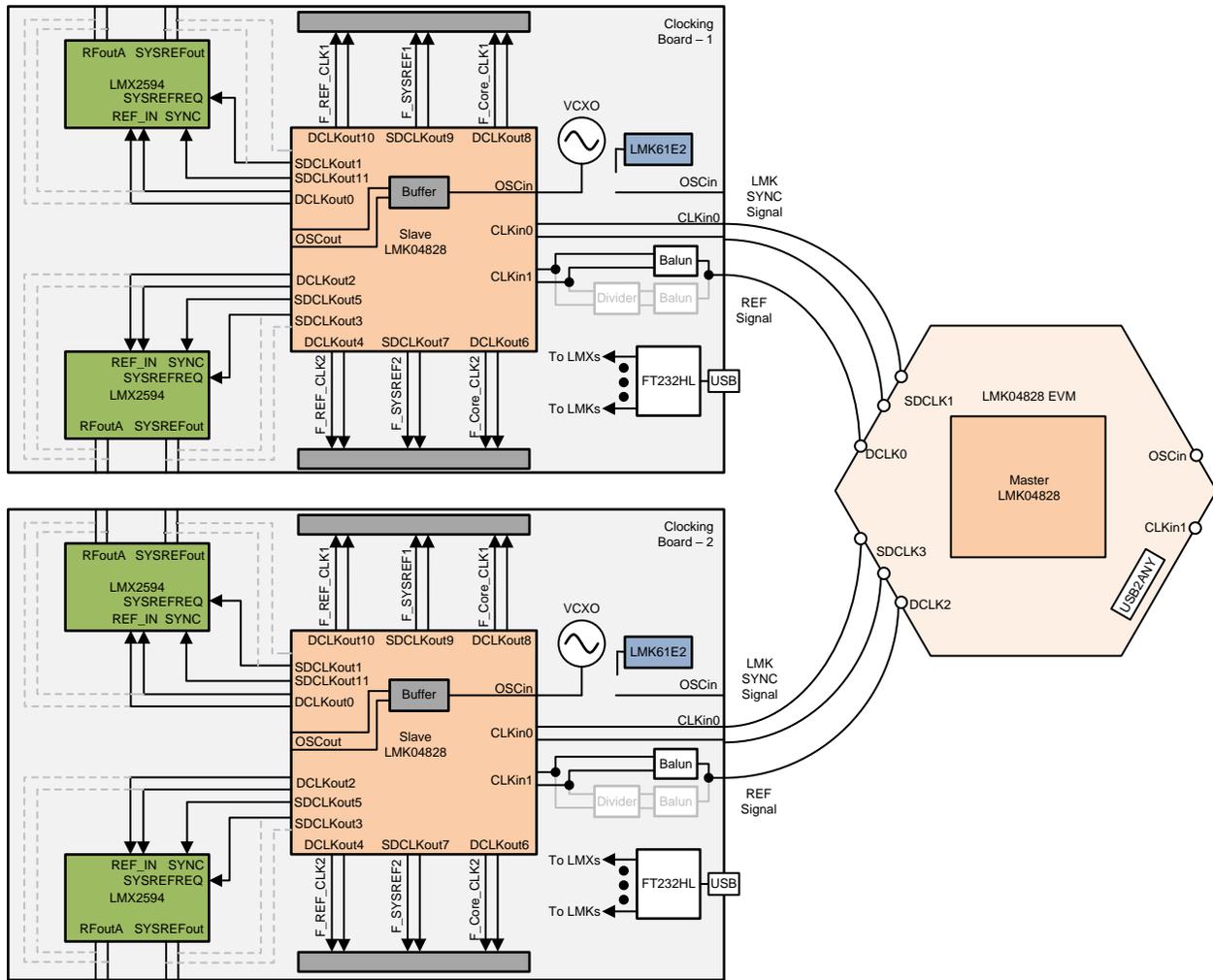
Table 1. Key Specifications

PARAMETER	SPECIFICATIONS	CONDITIONS
SNR (dBFS) (dual-channel mode)	55.2	997-MHz ADC input signal
	52.7	2482-MHz ADC input signal
Board-to-board clock time skew	< 10 ps	3-GHz clock output
Analog channel-to-channel time skew	< 50 ps	997-MHz ADC input signal
		2482-MHz ADC input signal

2 System Overview

2.1 Block Diagram

Figure 1 shows the block diagram of the proposed, scalable, multichannel phase-synchronized clock solution. Each slave clocking board has two, high-speed synchronized JESD204B clocks. These boards synchronize to each other using the tree configuration, which uses a master clocking board to provide the same reference input signals and sync signals to slave clocking boards. The master clocking board uses length-matched cables to provide the reference and sync signals.



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Figure 1. Tree Configuration for Synchronizing Multiple Slave Clocking Boards

2.2 Highlighted Products

2.2.1 LMX2594

The LMX2594 is a high-performance, wideband RF PLL with integrated VCO that supports a frequency range from 10 MHz to 15 GHz without using an internal doubler. The device supports both fractional-N and integer-N modes with a 32-bit fractional divider that allows fine-frequency selection. The high-performance PLL with figure of merit of -236 dBc/Hz and high-phase detector frequency can attain very-low in-band noise and integrated jitter. The integrated noise of 45 fs for a 7.5-GHz output makes the LMX2594 an ideal low-noise source. The device accepts input reference frequency up to 1.4 GHz, which combined with frequency dividers and programmable low-noise multiplier allows flexible frequency planning. The high-speed N-divider has no pre-divider and significantly reduces the amplitude and number of spurs. The additional, programmable low-noise multiplier allows users to mitigate the impact of integer boundary spurs. In fractional-N mode, the device can adjust the output phase by a 32-bit resolution. For applications that require fast-frequency changes, the device supports a fast calibration option, which takes less than 20 μ s. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard), which makes this device an ideal low-noise clock source for high-speed data converters. This configuration provides fine delay adjustment (9-ps resolution) to account for delay differences of board traces. This device uses a single 3.3-V supply and has integrated low-dropout linear regulators (LDOs) that eliminate the necessity for onboard low-noise LDOs.

2.2.2 ADC12DJ3200

The ADC12DJ3200 is an RF-sampling GSPS ADC with a -3 -dB input bandwidth up to 8 GHz. The 12-bit ADC12DJ3200 can sample up to 3200-MSPS in dual-channel mode and up to 6400-MSPS in single-channel mode. The ADC12DJ3200 can be used to sample signals in the first, second, and higher Nyquist zones. The ADC12DJ3200 uses a high-speed JESD204B output interface with up to 16 serialized lanes and supports subclass-1 for deterministic latency and multi-device synchronization. The serial output lanes support up to 12.8 Gbps and can be configured to trade off bit rate versus the number of lanes. In dual-channel mode, optional digital down converters can tune and decimate a band from RF to a complex baseband signal to reduce the interface data rate in bandwidth-limited applications.

2.2.3 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator for JESD204B systems. LMK04828 has 14 clock outputs from PLL2 that the user can configure to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. The LMK04828 supports two ranges of VCOs: 2370 MHz to 2630 MHz and 2920 MHz to 3080 MHz. The LMK04828 also supports a distribution mode where the device accepts the high-frequency reference signal and distributes the signal to all 14 clock outputs without adding a PLL noise.

2.3 System Design Theory

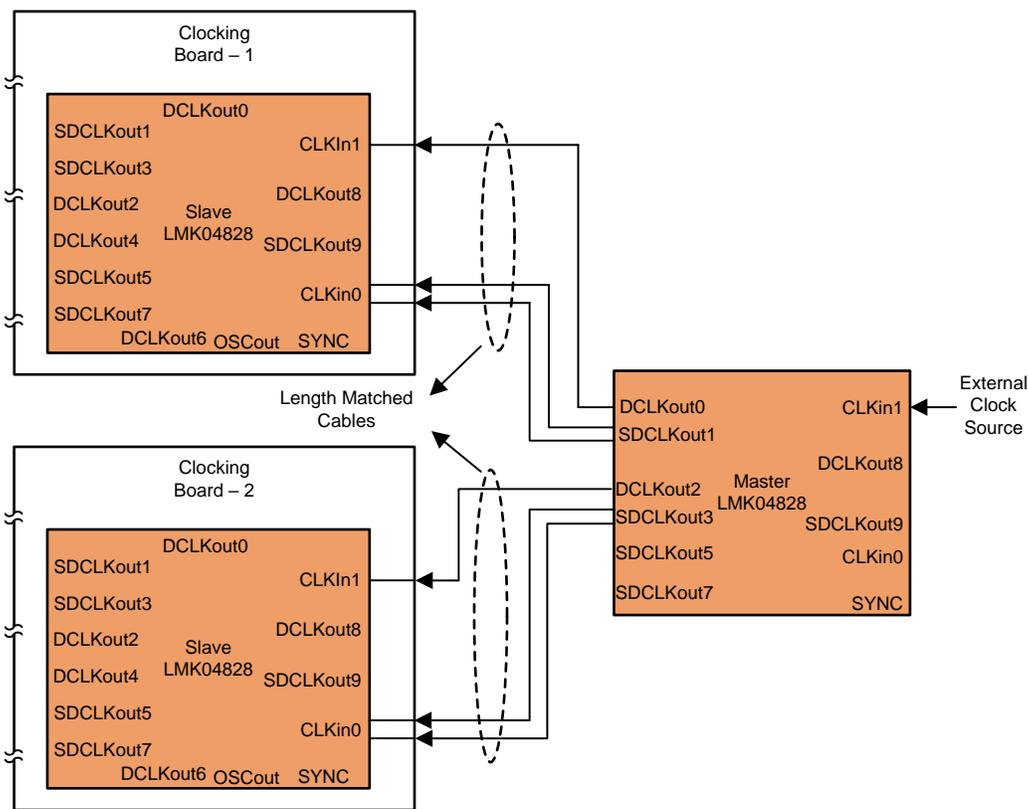
The high-channel-count JESD204B clock generation is based on the synchronization of board-to-board clocks with a provision for phase alignment trimming and high-performance clock generation using the external clock source. This section describes the design details of a multiboard synchronization approach to achieve synchronized, high-frequency, JESD204B-compliant clocks.

2.3.1 Board-to-Board Clock Synchronization

To demonstrate the board-to-board synchronization, multiple boards are connected in a configuration that requires a master clock source to provide the reference and sync signals to slave devices. The master device (LMK04828) can work in PLL mode or in distribution mode.

PLL mode requires a low-frequency reference signal and uses the internal VCO of the device to generate the clock signals. In PLL mode, the device adds the PLL noise, which can affect the overall performance of the generated clock signals. Whereas, in distribution mode, the master device receives a high-frequency reference signal from an external clock source and distributes the signal to the other clocks. This mode is good for fanning out reference clocks and high performance external clocks at high frequency because no PLL noise is added. However, this mode increases the noise floor at each level of the tree. Typically, in large systems, a tree topology is used to distribute clocks.

Figure 2 shows the tree configuration of multiple LMK04828 devices. In this design, the master clock board (LMK04828 EVM) receives the high-frequency external clock at CLKIn1 port and is configured in distribution mode. The slave LMK04828 is part of the clocking board, which is synchronized with the master LMK04828 using the reference signal at CLKIn1 and sync signal at CLKIn0. Initially, the master device synchronizes its own internal dividers after receiving the external reference signal, so the master device has all the in-phase DCLKout and SDCLKout signals. The slave devices receive the same reference signal at CLKIn1 from the master and then the slave devices are synchronized using the SYNC signals at CLKIn0 from the master. The end result is a design with synchronized slave LMK04828 outputs.

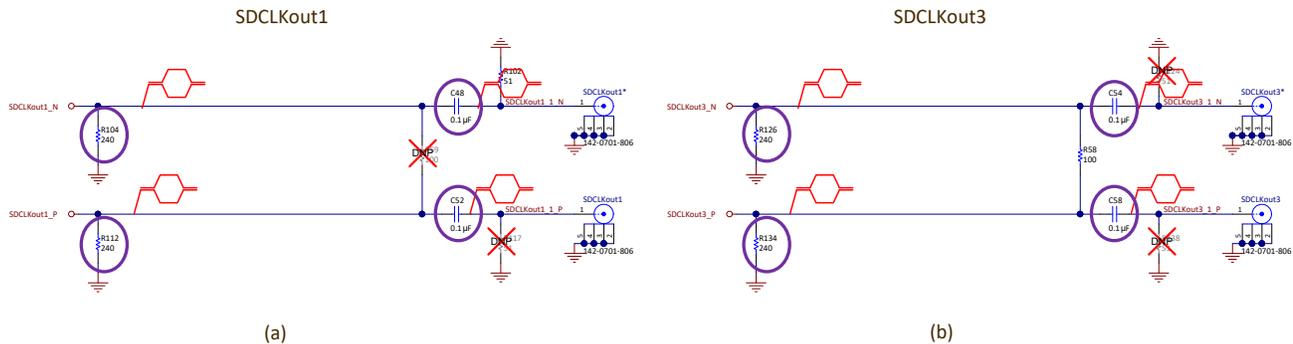


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Figure 2. Tree Configuration of Multiple LMK04828 Devices

In this design, the master LMK04828 receives the 3-GHz reference signal from an external source and divides the signal into 300-MHz DCLK and 37.5-MHz SYSREF/SYNC signals after divider synchronization. The DCLKout0 and DCLKout2 output signals of the master are fed to the slave LMK04828s at CLKIn1. The master then sends the DC-coupled sync pulses through SDCLKout1 and SDCLKout3 to the slaves for synchronization. Later, the LMK devices of the slaves generate the synchronized reference, SysRefReq, and SYNC signals to LMX2594 of the clocking boards and FPGA clocks to capture cards. After synchronizing the multiple boards, measure the clock skew, for which the results are available in [Section 3.2](#).

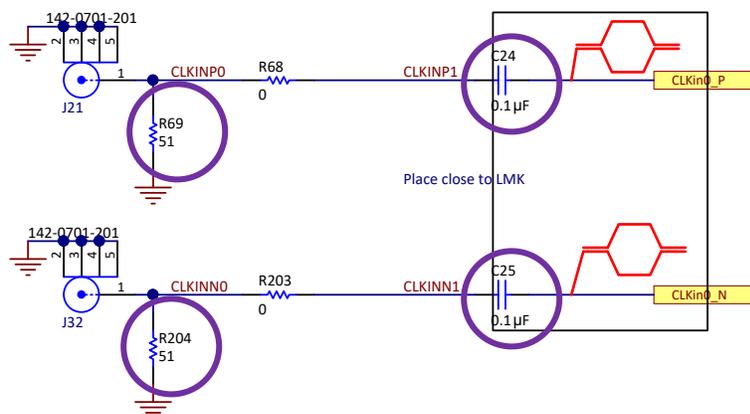
In the master LMK04828 EVM board, the SDCLKout1 and SDCLKout3 outputs must be modified for DC-coupled sync output signals. Remove the circled resistors R104, R112, R126, and R134 and replace capacitors C48, C52, C54, and C58 with 0603 0-Ω resistors (see Figure 3).



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Figure 3. Master LMK04828: EVM Modification for DC-Coupled SYNC Outputs

The CLKIn0 path of the slave LMK04828 in the clocking boards must be modified for DC-coupled sync input signals. Remove the circled resistors R69 and R204 and replace capacitors C24 and C25 with 0201 0-Ω resistors (see Figure 4).

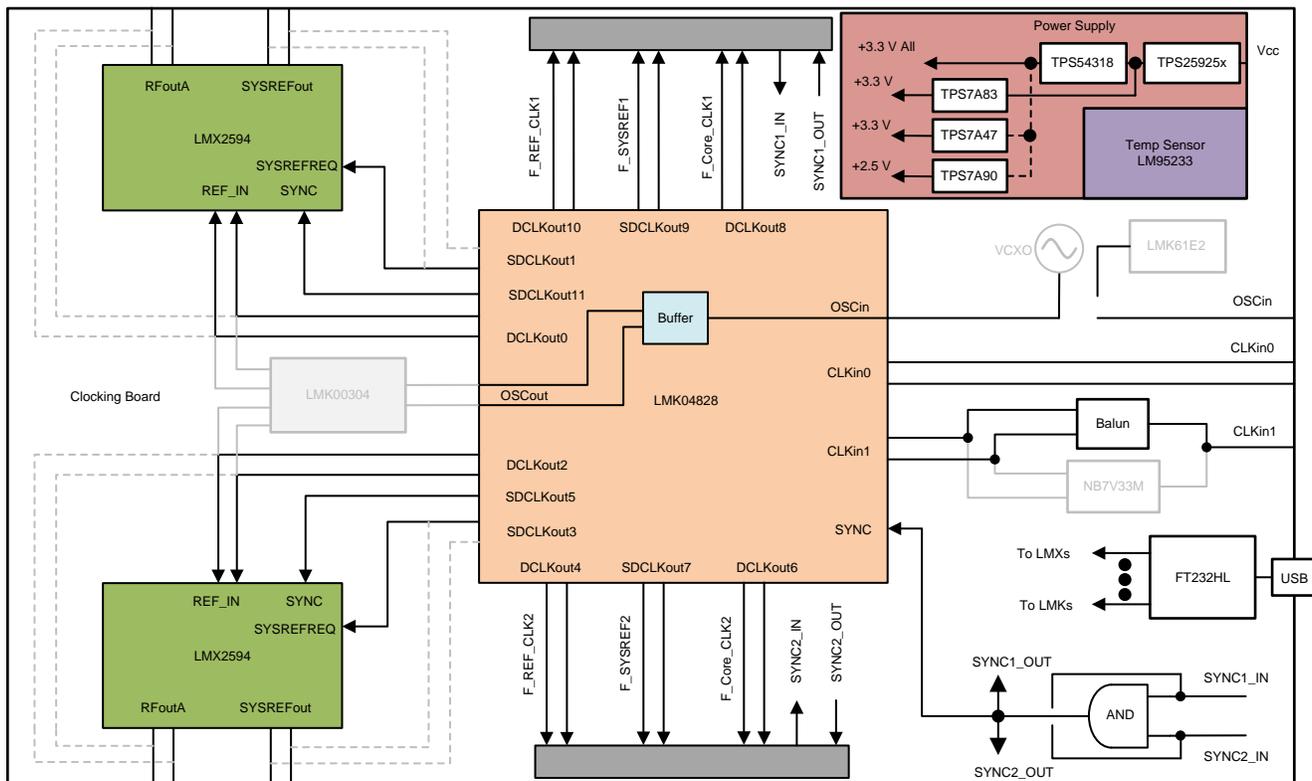


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Figure 4. Clocking Board LMK04828: CLKIn0 Path Modification for DC-Coupled SYNC Inputs

2.3.2 LMX2594 Synchronized Clocks Output

Figure 5 shows the block diagram of the multichannel clocking board. In this design, the slave LMK04828 operates in distribution mode, which receives the 300-MHz reference clocks at the CLKin1 input and distributes 37.5 MHz at DCLKout1 and DCLKout2 as the reference input to both LMX2594 devices, 300 MHz as the FPGA clocks, and 37.5 MHz as the SYSREF output. To achieve phase synchronization, assign a common frequency input to the two LMX2594 synthesizers, the SYNC and SYSREFREQ signals from the LMK04828. To adjust slight mismatches in the phase of the generated clocks, the LMX2594 provides a clock phase programming feature to program the clock phase using the MASH_SEED value. Each LMX2594 device may require tuning for the MASH_SEED and SYSREF delays to achieve in-phase generated clocks and the setup and hold time of the SYSREFs when interfaced with data converters. The operation and performance of both LMX2594s devices is equivalent to the device performance in the TIDA-01021 reference design; however, in this design, the devices receive the reference signal through the DCLKout of the LMK04828 to maintain the synchronized reference signals in multiple boards.



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Figure 5. Block Diagram of Multichannel Clocking Board

In this design, the reference input path of the LMX2594 on the clocking boards must be modified. Remove the 0-Ω resistors R103, R165, R137, and R168 and mount 0402 0-Ω resistors at R274, R275, R108, R110, R278, R279, R141, and R143.

An input reference frequency of 37.5 MHz is provided to the clocking board LMX2594 devices by the slave LMK04828. The phase detector frequency is also changed to 37.5 MHz and [Table 2](#) lists the new loop filter configuration.

Table 2. LMX2594 Loop Filter Components

COMPONENTS	VALUES
C62, C95	1.5 nF
C60, C93	56 nF
C59, C92	Open
C58, C91	1.8 nF
R96, R129	120 Ω
R95, R128	0 Ω
R94, R127	270 Ω

2.3.3 ADC12DJ3200 EVM Configuration

The design is validated with two channels of the ADC12DJ3200 EVMs in a setup that uses two sets of ADC12DJ3200 EVMs to measure the impact of the scalable multichannel clocking solution. The ADC12DJ3200 can reach up to a 3.2-GHz clock frequency, but the TSW14J56 capture card is limited at a 12-Gsps data rate, which limits the clocking frequency of the ADC. For these reasons, the ADC clock frequency is set to 3 GHz. The ADC12DJ3200 operates in dual-channel mode (JMODE2) where the input for only one channel is provided and the output from the corresponding ADC core is captured.

The slave LMK04828 of the clocking board on this design is used to provide the reference signals to the LMX2594s devices, FPGA reference clock, a core clock, and the SYSREF to the TSW14J56 capture card through the FMC+ adapter board. The reference and core clock frequency of the FPGA are 300 MHz and the SYSREF frequency is 37.5 MHz. The adapter board also provides the interface between the ADC EVM and the capture card because the board connects the ADC lanes to the FPGA. Various input signals are provided at the ADC input for SNR measurement. [Section 3.2](#) shows these results.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Slave Clocking Boards Setup

Figure 6 shows an image of the multichannel clocking board with the hardware configuration for each clocking board.

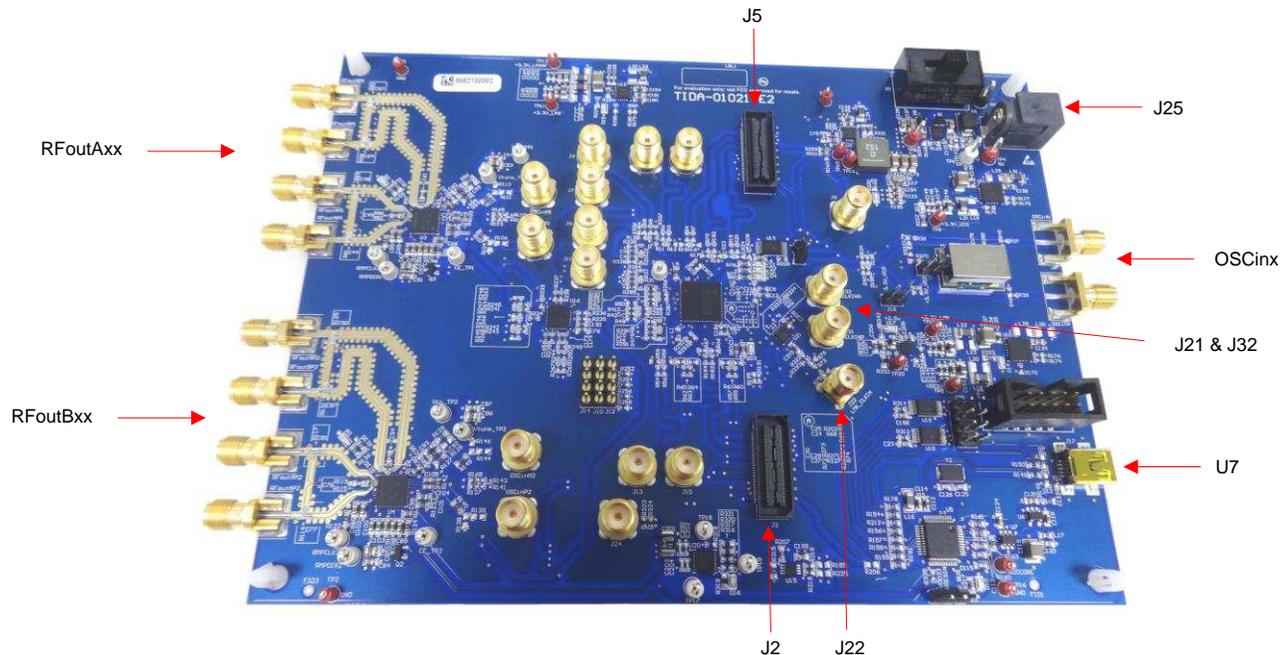


Figure 6. Multichannel Clocking Board Hardware

Power:

- Power supply connector J25: This connector is used to connect the power supply. Set the power supply to 5 V with a 2-A current limit.

Input reference signals:

- Option 1: The onboard VCXO Y1 is powered on using the jumper J8 and outputs a 100-MHz signal to the LMK04828 OSCin* pin input. While using Y1, disconnect the clock inputs from LMK61E2 (U2) and external reference by removing R36 and R38. At the same time, isolate the power supply to U2 by removing the jumper J16.
- Option 2: The onboard reference LMK61E2 (U2) is powered on using the jumper J16 and factory programmed to generate a 156-MHz LVDS output. U2 can be programmed to generate different clock frequencies using the I²C interface. While using U2, disconnect the clock inputs from Y1 and the external reference by removing C179, R37, and R39 then place R36 and R38. Isolate the power supply to Y1 by removing jumper J8.
- Option 3: Connect the external reference to external OSCinP and OSCinN connectors. While connecting the external reference, disconnect the Y1 and U2 connection by removing C179, R45, and R46 and place R36 and R38. Disconnect the power supply of Y1 and U2 by removing jumpers J8 and J16.
- Option 4: One of the previous options are used when LMK04828 works in PLL mode. When LMK04828 is operating in distribution mode, connect the external reference to external connector J22. While operating in distribution mode, power down Y1 and Y2 by removing jumpers J8 and J16.

Input sync signal:

- Connect the external sync signal at external J21 and J32 connectors to reset the LMK04828 dividers.

Output signals:

- RFoutAP1, RFoutAM1, RFoutAP2, and RFoutAM2 connectors generate the DCLK and are connected to ADC EVMs to measure the SNR.
- RFoutBP1, RFoutBM1, RFoutBP2, and RFoutBM2 connectors generate the low-frequency SYSREF signals.
- Connectors J2 and J5 generate the FPGA CLKs and SYSREFs for two channels.

Programming interface:

- Connect the USB mini cable to the onboard USB connector U7 and test PC to program the clocking board devices using the High Speed Data Converter (HSDC) TID GUI.

3.1.1.2 FMC+ to FMC Adapter Board Setup

The FMC+ to FMC adapter board has connections to take the FPGA clocks from the slave clocking or ADC12DJ3200 EVM. Follow the schematic in [Schematics](#) to connect the FPGA clocks and SYSREFs from the clocking board.

3.1.1.3 Master LMK04828 EVM Setup

See [LMK04826/28 User's Guide](#) for the LMK04828 EVM hardware setup procedure.

3.1.1.4 ADC12DJ3200 EVM Setup

See [ADC12DJ3200 Evaluation Module User's Guide](#) for the ADC12DJ3200 EVM hardware setup procedure. The ADC12DJ3200 EVM has both internal and external options for clocking the ADC. Select the DEVCLK based on the placement of capacitors on the shared pads. Connect C49 and C50 for the external DEVCLK. Connect the external SYSREF for the ADC at connector J38 from the slave clocking board.

3.1.1.5 TSW14J56 Setup

See [TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide](#) for the TSW14J56 EVM hardware setup procedure.

3.1.2 Software

After connecting and modifying the boards, configure all the devices in multiple boards.

3.1.2.1 Board-to-Board Synchronization Programming Sequence

1. Download the [TICSPRO-SW](#) tool from [TI.com](#) to program the master LMK04828 EVM. [Figure 7](#) shows the TICSPRO-SW GUI.
2. Download the [HSDC TID GUI](#) software from [TI.com](#) and install the program on two different test PCs to program the slave clocking board devices. [Figure 8](#) shows the HSDC TID GUI.
3. To synchronize the multiple board clocks:
 - Master LMK04828 EVM
 1. Feed the external reference signal at CLKin1.
 2. Load the `1023_LMK04828EVM_Master_3GREF_300MOut_37.5MSync_Output_Distribution.tcs` file in TICSPRO to program the LMK04828 in distribution mode.
 3. Click the *SYNC Dividers* button to synchronize all dividers of the master as (see [Figure 7](#)).

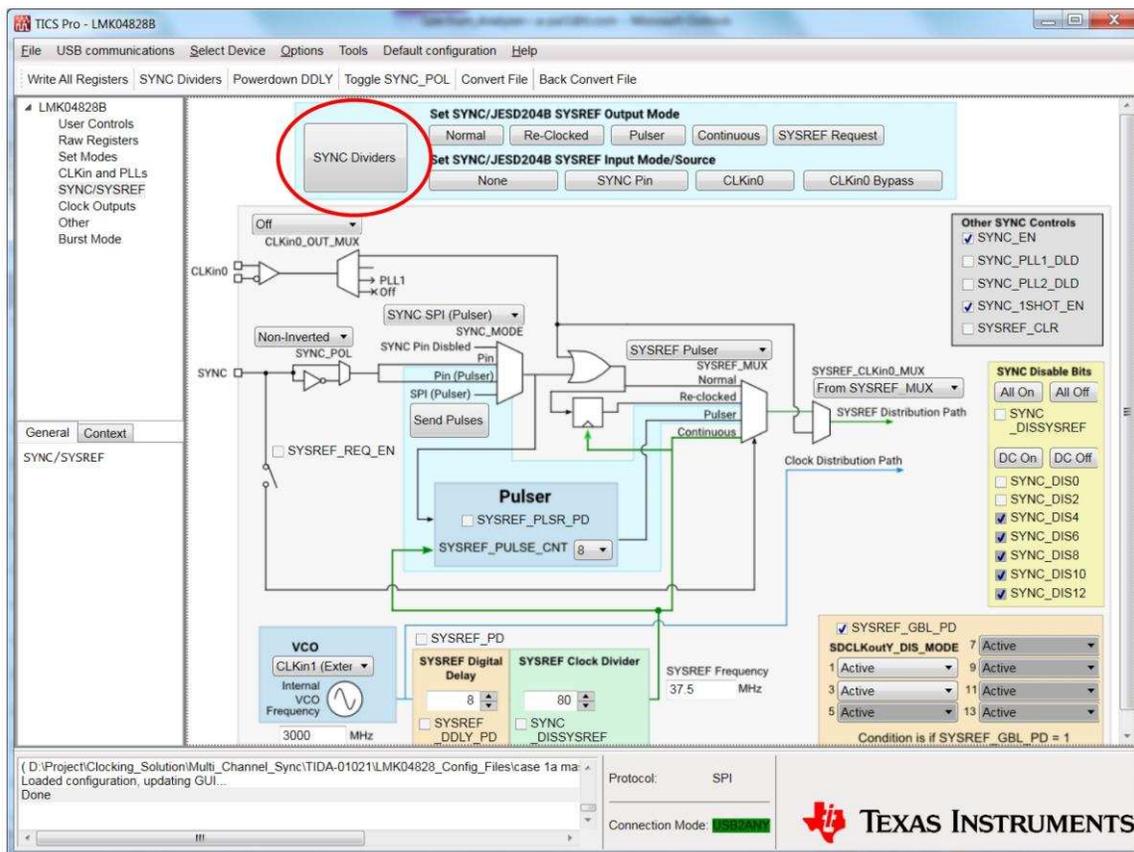


Figure 7. TICSPRO-SW GUI

- Slave Cloning Boards
 1. Load the `1023_BRDx_LMK04828_300MREF_300MFCLK_37.5MSYSREF.cfg` file in the respective HSDC TID GUI to program the LMK04828 device in distribution mode.

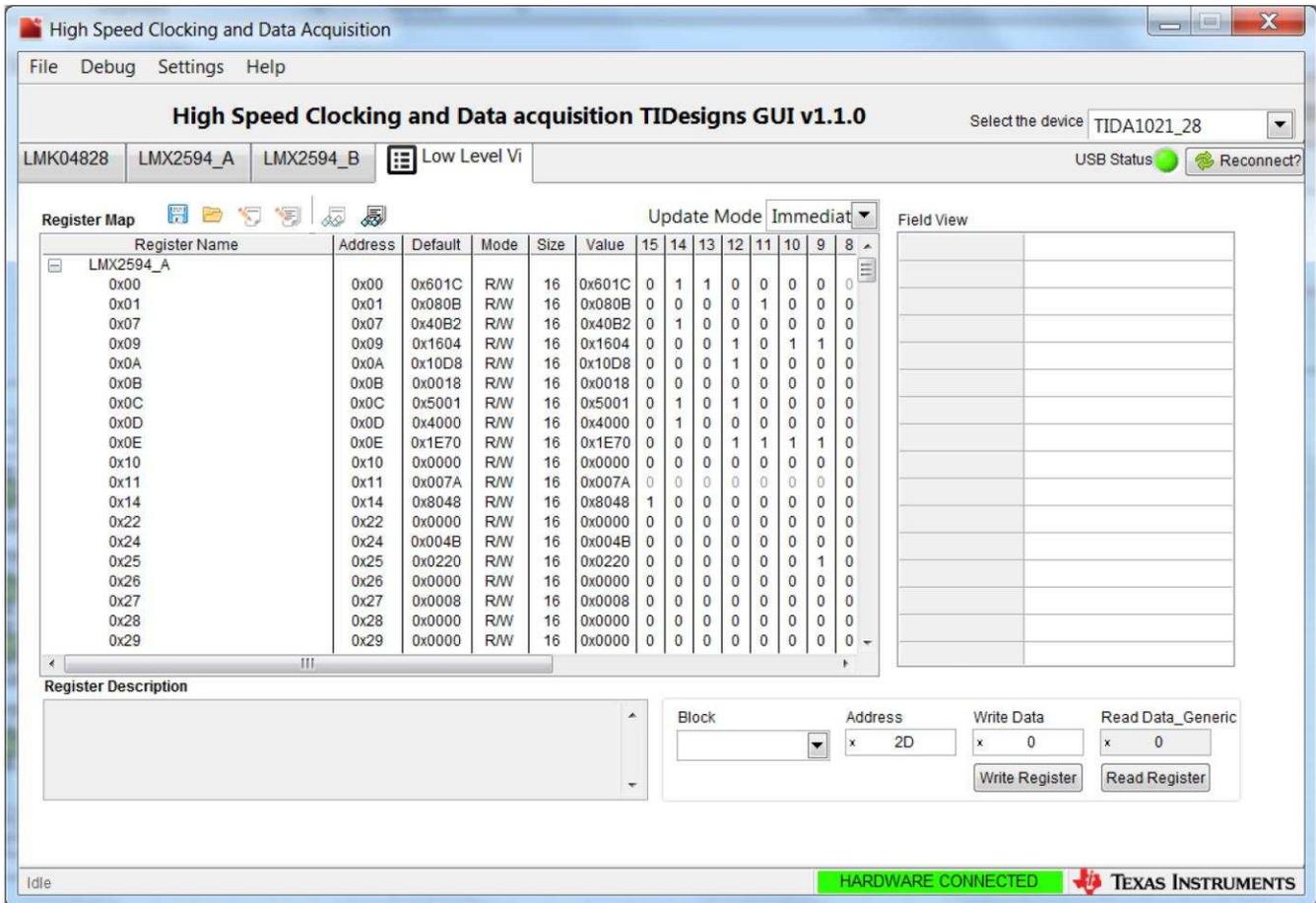


Figure 8. HSDC TID GUI Programming

- Master LMK04828
 1. Click the *Send Pulses* button to send a sync pulse to the slave LMK04828 devices to reset the dividers (see [Figure 9](#)).

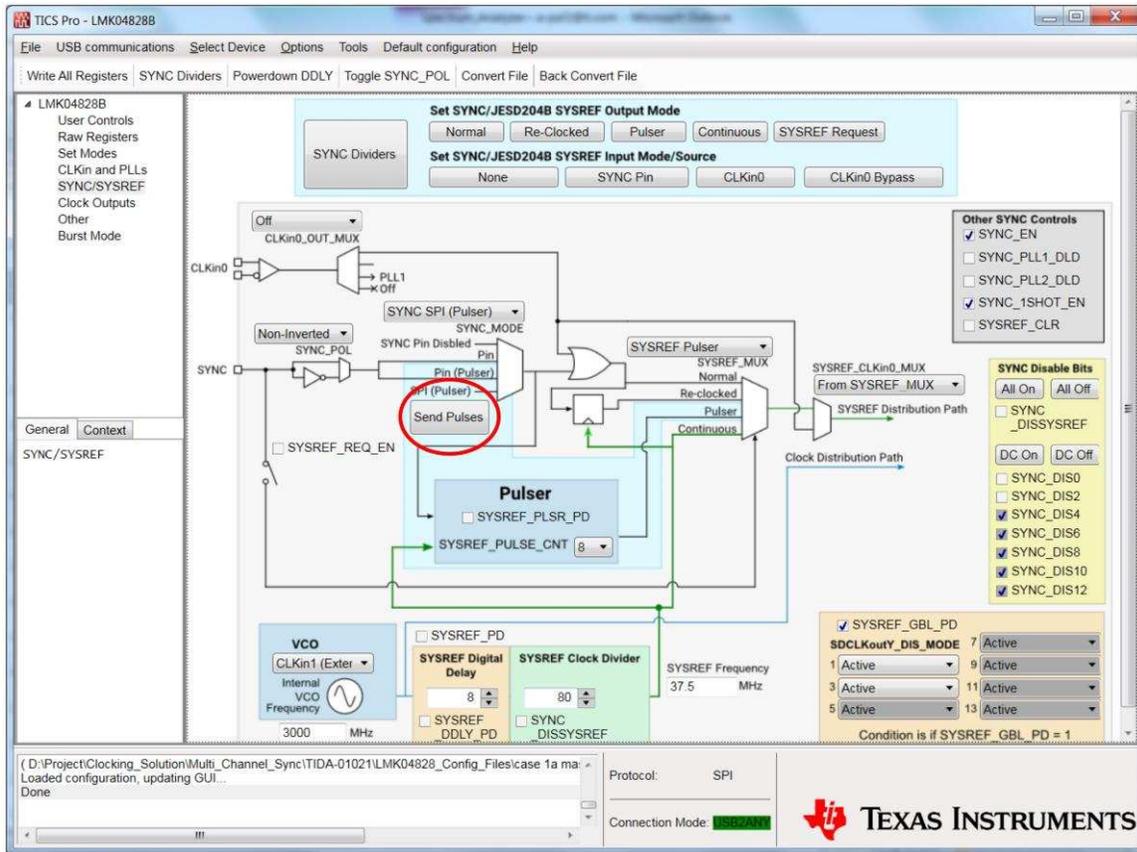


Figure 9. TICSPRO-SW GUI for Send Pulses

- Slave Clocking Boards
 1. Load the *1023_BRDx_LMX2594_A_B_3GCLK_37.5MREF_37.5MPFD.cfg* file in the respective HSDC TID GUI to *Disable SYNC on all Dividers* of the slave LMK04828 and configure the LMX2594 devices.
 2. After configuring the ADC EVMs, load the *1023_LMX2594_A_B_SYSREF_OFF.cfg* file in both HSDC TID GUI for SYSREF section OFF of all LMX2594 devices.

3.1.2.2 ADC12DJ3200 EVM Programming

Download the [ADC12DJxx00 GUI](#) from [TI.com](#) to program the ADC12DJ3200 EVM. The ADC12DJ3200 and LMK04828 devices are configured for SNR measurement in the ADC12DJ3200 EVM, as [Figure 10](#) shows. The LMK04828 is programmed in distribution mode for the CLKin0 drive to configure SYSREF directly. The ADC12DJ3200 EVM is put into JMODE2 mode to use in dual-channel mode at the full Nyquist zone of the device. The EVM is set up in external clock source selection mode with a sampling frequency of 3000 Msps. Load the configuration files in the low-level view page of the ADC12DJ3200 GUI.

The programming sequence for the ADC12DJ3200 EVM is as follows:

1. Load the configuration file *1023_ADC_EVM_LMK04828_SYSREF_Bypass.cfg* for LMK04828 and bypass the ADC SYSREF signal.
2. Load the ADC configuration file *1023_ADC12DJxx00_JMODE2_SRC_EN.cfg* for ADC programming and SYSREF auto calibration.
3. Load the ADC configuration file *1023_ADC12DJxx00_JMODE2_SRC_clear.cfg* for ADC SYSREF auto calibration OFF.

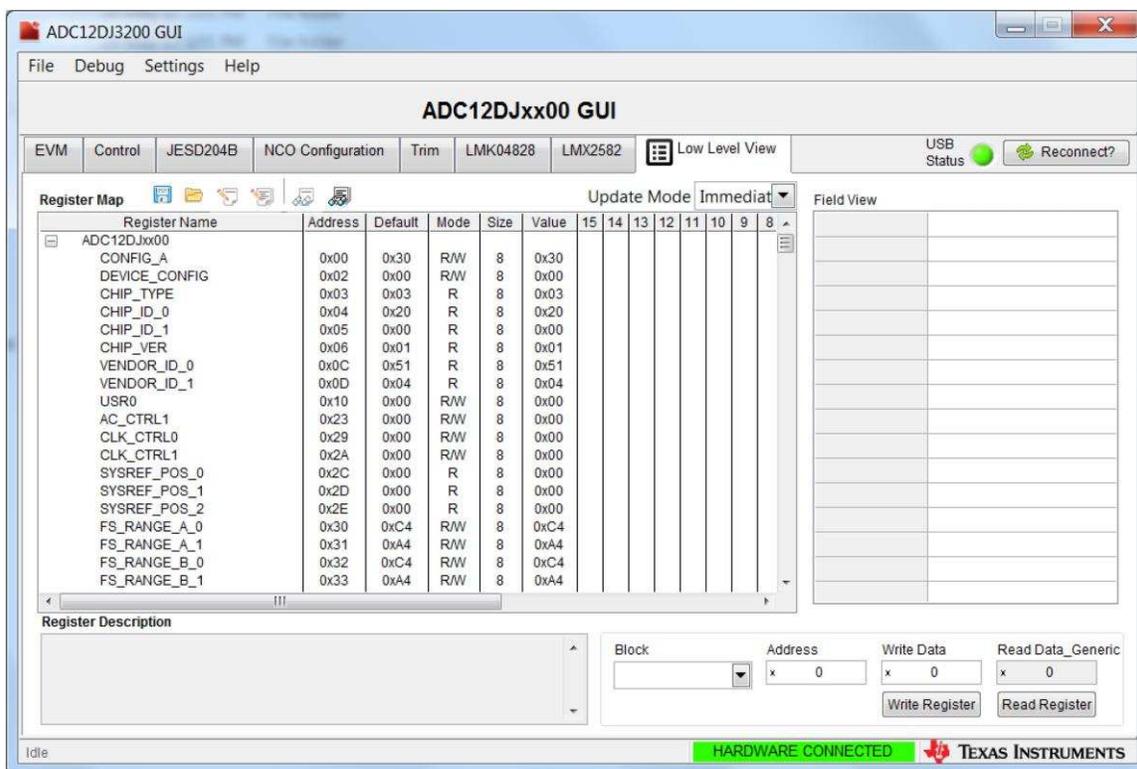


Figure 10. ADC12DJ3200 EVM Programming

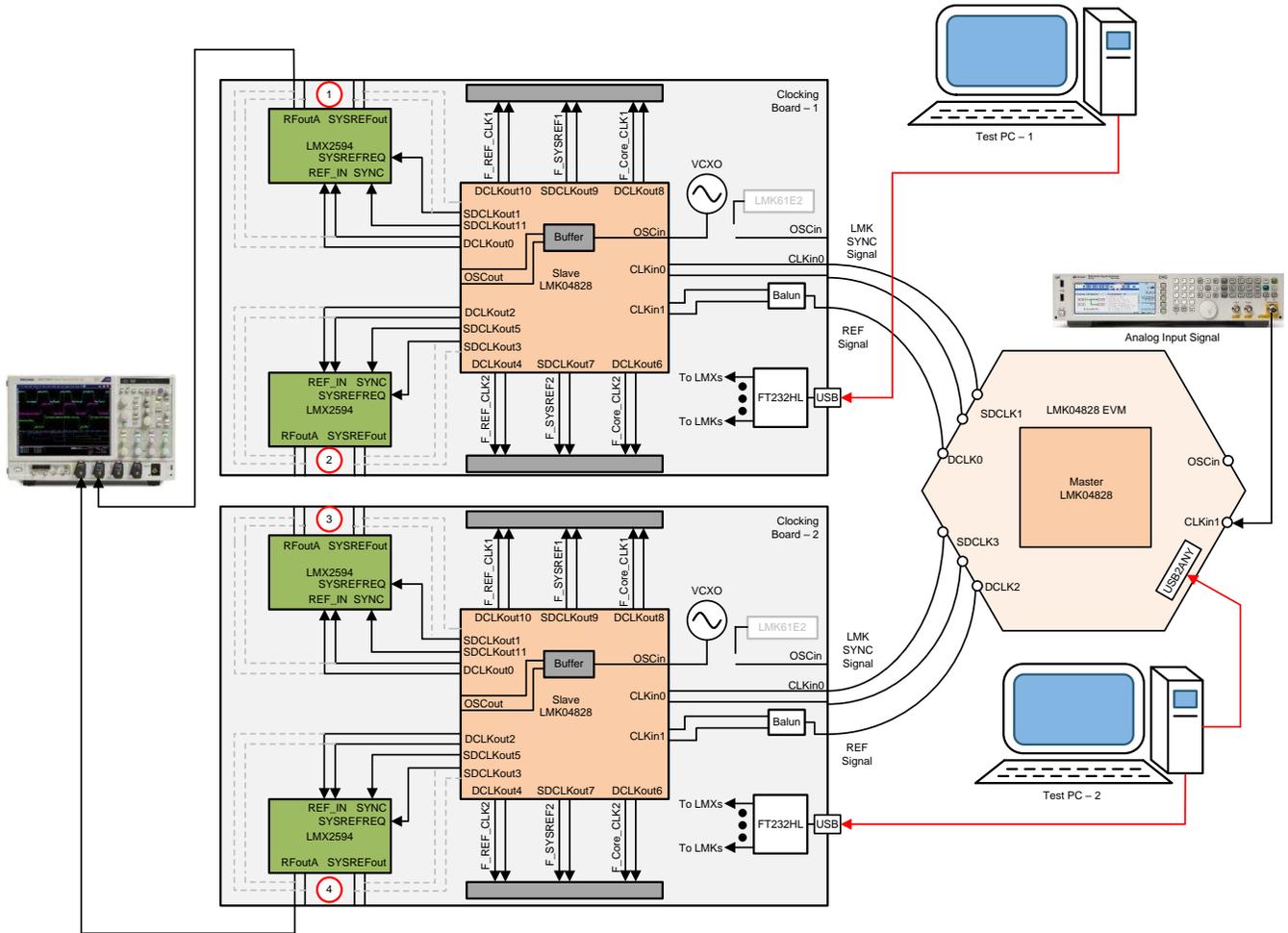
3.1.2.3 HSDC Pro Setup

The HSDC Pro software interfaces with the TSW14J56 device to capture and analyze the digital data from the ADC12DJ3200 regarding SNR measurements. See [TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide](#) for the HSDC Pro setup to capture and analyze the data.

3.2 Testing and Results

3.2.1 Test Setup

Figure 11 shows the test setup for multiboard clock skew. Figure 12 shows the test setup for ADC SNR and channel-to-channel skew measurement. In both figures, the circled number shows the clock channel number.



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Figure 11. Test Setup for Multiboard Clock Skew Measurement

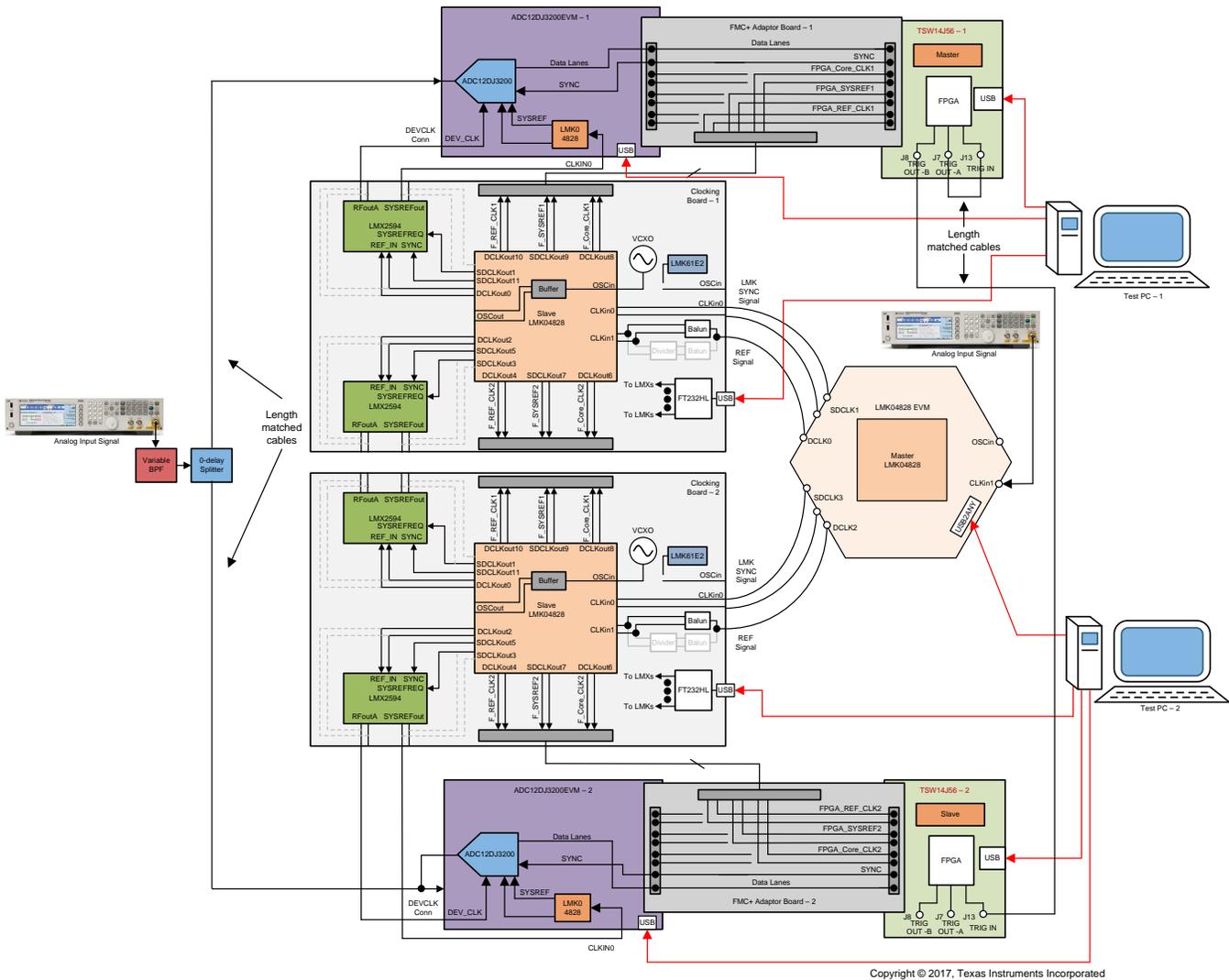


Figure 12. Test Setup for ADC12DJ3200 SNR and Channel-to-Channel Skew Measurement

3.2.2 Test Results

3.2.2.1 Board-to-Board Clock Phase Alignment

As explained in Section 2.3.1, scaling up the synchronized clocks is critical for high-channel-count systems. In this test, the clocks of the multiboard are synchronized at 3-GHz DEV_CLKs, which are generated by the LMX2594s devices. The minimum skew between the clocks reflects the minimum channel-to-channel skew in multichannel systems. Figure 13 shows the clock skew between channel 1 and 4 (as shown in Figure 11), which is less than 10 ps. The skew of the clocks among all channels is less than 10 ps, which the results do not show. As a result, the channel-to-channel skew in high-count multichannel systems is reduced.



Figure 13. Board-to-Board Clock Measured Skew

3.2.2.2 Multichannel Signal Performance and Skew Measurement

Table 3 shows the measured SNR performance of the ADC12DJ3200 EVM-1 at various frequencies for -1 -dBFS differential inputs and dual-channel mode (JMODE2). The ADC12DJ3200 EVM-2 channels also show the same performance as ADC12DJ3200 EVM-1. The measured SNR of the ADC12DJ3200 with the proposed TIDA-01023 clocking solution is improved as compared to the ADC12DJ3200 EVM onboard clocks.

Table 3. Measured SNR

INPUT FREQUENCY (MHz)	ADC DATA SHEET SNR (dBFS)	MEASURED SNR ON ADC12DJ3200EVM WITH ONBOARD CLOCK (dBFS)	MEASURED SNR ON ADC12DJ3200EVM WITH TIDA-01023 CLOCKS (dBFS)
997	56.3	55.25	55.4
2482	55.2	52.71	53.5

Figure 14 and Figure 15 show the spectrum results at a 3000-MHz sampling frequency in dual-channel mode.

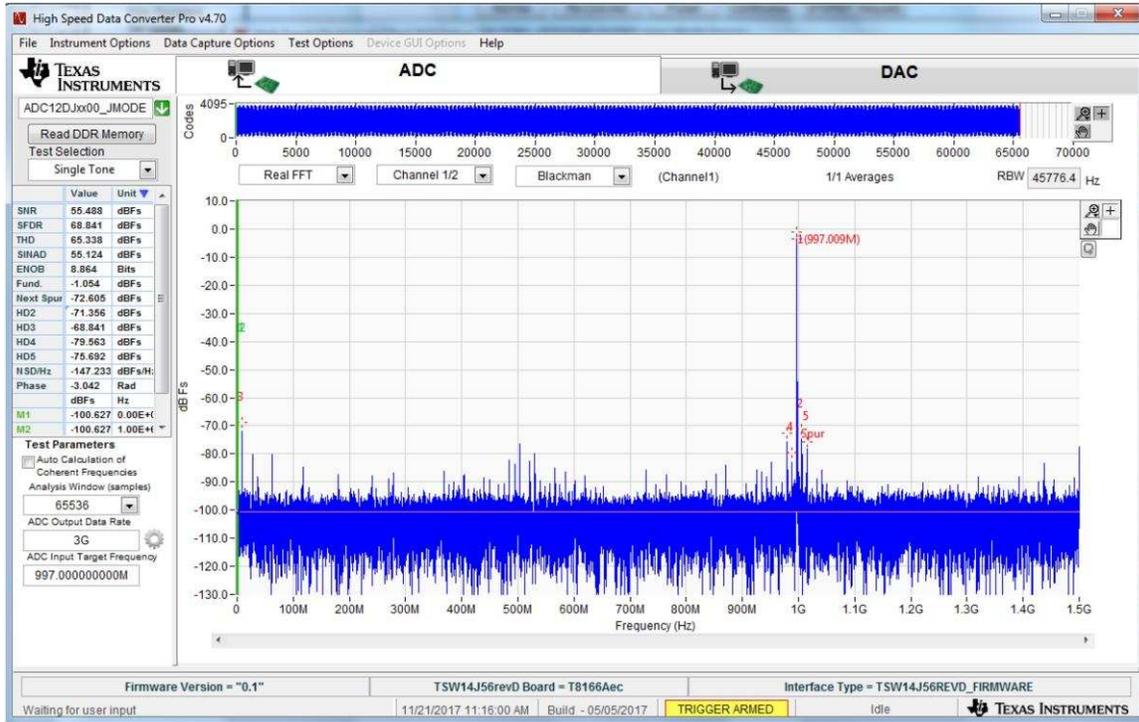


Figure 14. Spectrum at 997-MHz Input

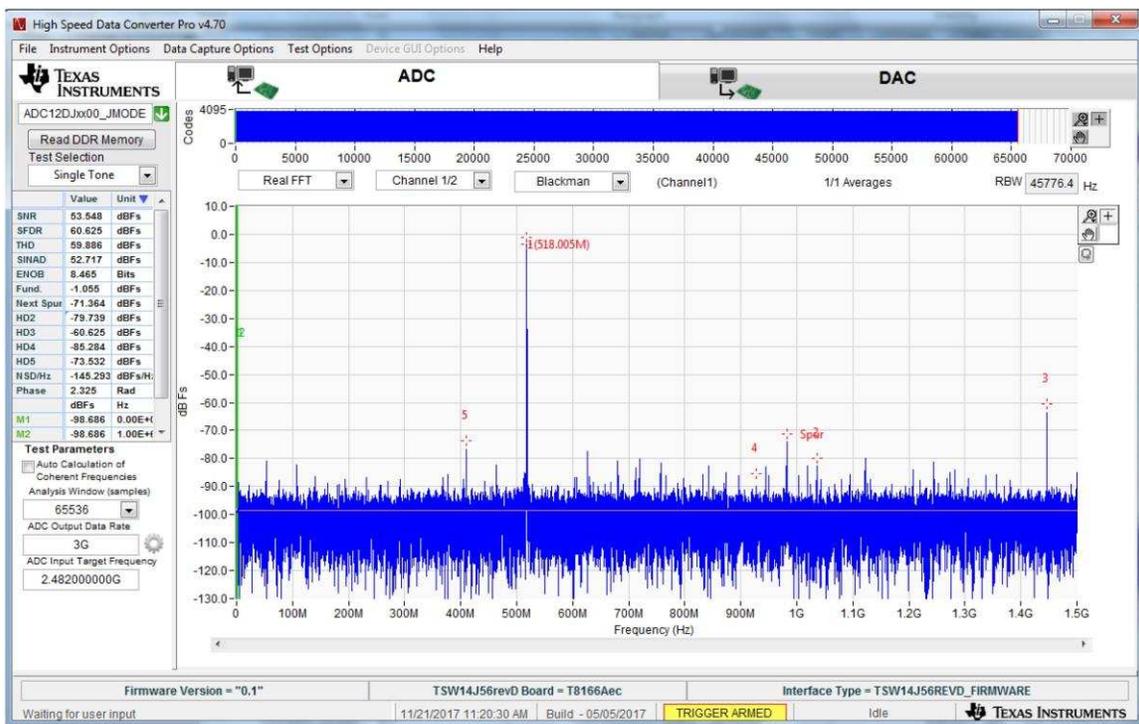


Figure 15. Spectrum at 2482-MHz Input

Table 4 shows the time skew between two ADC12DJ3200 EVM channels at different input frequencies. Evaluate this skew by calculating the phase difference between the signals captured from each ADC using MATLAB and the example program in Appendix A. The clocks are fed to both ADC12DJ3200 devices from clock channel 1 and 4, as Figure 12 shows, and the measured time skew is valid for any clock channel combination. The measurements taken at a 3-GHz sampling frequency and measured time skew was less than 50 ps for each of the input frequencies.

Table 4. Measured Channel-to-Channel Skew

INPUT FREQUENCY (MHz)	MEASURED TIME SKEW (ps)
997	6.4
2482	10.4

Figure 16 shows a plot of the output samples of the two ADCs for a 997-MHz input, which is in the first Nyquist zone for a 3000-MHz sampling clock. Figure 17 shows a plot of the output samples for a 2482-MHz input, which is in the second Nyquist zone for a 3000-MHz sampling clock. The 2482-MHz input signal aliases to 518 MHz and a phase difference of 9.3° is measured, which translates to a channel-to-channel skew of 10.4 ps for the 2482-MHz input.

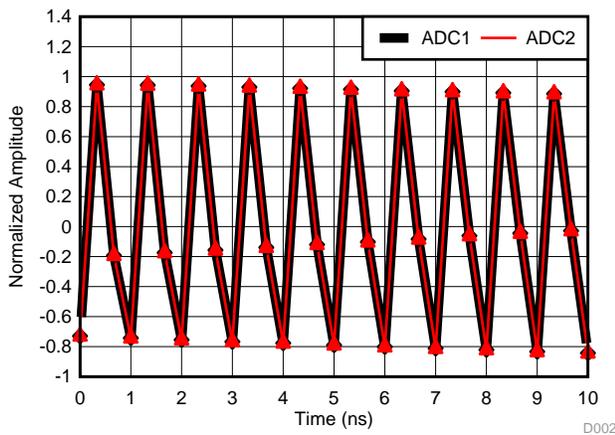


Figure 16. Sampled Signals at 997-MHz Input

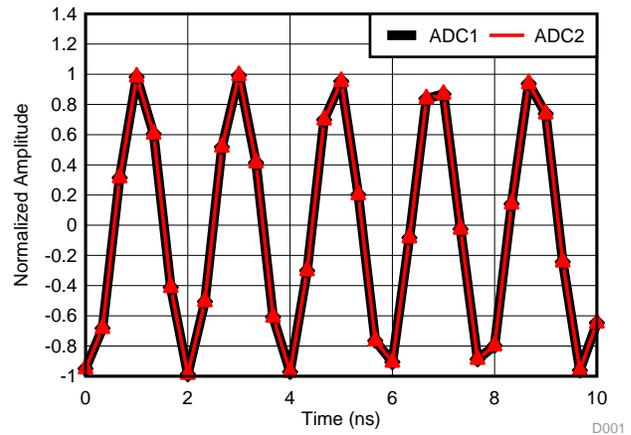


Figure 17. Sampled Signals at 2482-MHz Input

3.2.3 Summary and Conclusion

The TIDA-01023 design is a high-channel-count, JESD204B-compliant clocking reference design that can be used for radar and 5G wireless testers. This reference design demonstrates multichannel, high-performance (low phase noise), phase-synchronized clock generations in a tree configuration using the LMX2594 and LMK04828 devices with a high-frequency external clock source and an achieved clock-to-clock skew less than 10 ps. This design also demonstrates the clocking impact on ADC12DJ3200 EVM system performance after replacing the onboard clocks with TIDA-01023 output clocks. The system SNR improves by 0.2 dB to 0.5 dB using the ADC12DJ3200EVM with the proposed clocking solution and with a clock skew of less than 10 ps. The system shows deterministic latency behavior for every power ON cycle with the analog input channel-to-channel skew at less than 50 ps.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-01023](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01023](#).

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01023](#).

4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01023](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01023](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01023](#).

5 Software Files

To download the software files, see the design files at [TIDA-01023](#).

6 Related Documentation

1. Texas Instruments, [LMK04826/28 User's Guide](#)
2. Texas Instruments, [ADC12DJ3200 Evaluation Module User's Guide](#)
3. Texas Instruments, [TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide](#)

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7 About the Author

AJEET PAL is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the Test and Measurement sector. Ajeet has six years of experience in RF and wireless subsystem design for cellular and wireless systems. Ajeet earned his Bachelor of Engineering in electronics and communication engineering from the Institute of Technology & Management (ITM) University at Gwalior and his Masters of Technology in RF and microwave engineering from the Indian Institute of Technology (IIT) Kharagpur, India.

SANKAR SADASIVAM is a system architect at Texas Instruments where he is responsible for architecting and developing reference design solutions for the industrial systems with a focus on Test and Measurement for the Industrial Systems Engineering team. Sankar brings his extensive experience in analog, RF, wireless, signal processing, high-speed digital, and power electronics to this role. Sankar earned his Master of Science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

8 Acknowledgment

The authors would like to thank their colleague Timothy Toroni for his critical feedback on multidevice synchronization for this design.

Appendix A

Example Matlab Program for Analyzing Skew

```

%-----%
% Import Data                                %
%-----%

data1 = xlsread('read_csv1.csv',1,'A1:A65536');
data2 = xlsread('read_csv2.csv',1,'A1:A65536');

Fs = 3000e6;
Fin = 997e6;
N = length(data1);
num_bits = 15;

samples_board_1 = data1;

% remove offset for board 1
samples_board_1 = double(samples_board_1);
samples_board_1 = samples_board_1 - mean(samples_board_1);
mean(samples_board_1)

samples_board_2 = data2;

% remove offset for board 2
samples_board_2 = double(samples_board_2);
samples_board_2 = samples_board_2 - mean(samples_board_2);
mean(samples_board_2)

%-----%
% Analyze Skew                                %
%-----%

% Plot time domain data for each board.
figure(1);
plot(1:length(samples_board_2),samples_board_2,...
1:length(samples_board_1),samples_board_1);
title('Time Domain Plot');

% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);

figure(3);
plot((0:N/2)*(Fs/N), 20*log10(abs(X*2/N/A)));
title('FFT Plot of Board 2');

figure(2);
plot((0:N/2)*(Fs/N), 20*log10(abs(Y*2/N/A)));
title('FFT Plot of Board 1');

% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_y));

```

```
% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff_deg = phase_diff / pi * 180;

Fin = 0.5*Fs*((index_x-1)/(length(X)-1));

skew_ps = phase_diff / (2*pi*Fin) / 1e-12;

if(skew_ps >= 0)
    fprintf('Board2 lags Board1 by %f degrees or %f ps for Fin = %f MHz',...
        phase_diff_deg, skew_ps, Fin*1e-6);
else
    fprintf('Board1 lags Board2 by %f degrees or %f ps for Fin = %f MHz',...
        -phase_diff_deg, -skew_ps, Fin*1e-6);
end
```

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