*TI Designs: TIDA-01527*

# *Discrete Resolver Front-End Reference Design With C2000™ Microcontroller and ±0.1° Accuracy*

## Description

This reference design is an excitation amplifier and analog front end for resolver sensors. The design implements only discrete components and standard operational amplifiers (op amps) on a 1-in$^2$ printed-circuit board (PCB). The provided algorithm and code example uses a C2000™ microcontroller (MCU) LaunchPad™ Development Kit with the TMS320F28069M MCU for signal processing and angle calculation. The reference design uses an innovative, scattered-signal processing method (see Section 3). This method improves the system accuracy by 250% while maintaining hardware costs and complexity to a reasonable level.

The TIDA-01527 is a low-cost companion design for the TIDA-00796 and TIDA-00363 reference designs. These designs are based on the PGA411-Q1 and offer advanced features such as protections and diagnostics.

## Features

- Minimalist Approach on 1-in$^2$ Four-Layer PCB
- Industry Standardized Components
- Low Cost
- Example Firmware for TMS320F28069M C2000™ MCU Including Source Code
- Undersampling Algorithm for Angle Calculation
- Allows for Performance Upgrade
- ±0.25° Angle Readout Accuracy or ±0.1° Using Innovative Scattering Signal Processing Method

## Applications

- AC Drive Position Feedback
- HEV/EV - Inverter and Motor Control
- E-Bike
- Servo Drive Position Feedback

## Resources

| | |
|---|---|
| TIDA-01527 | Design Folder |
| TLV4171 | Product Folder |
| TLV431B-Q1 | Product Folder |
| TMS320F28069M | Product Folder |

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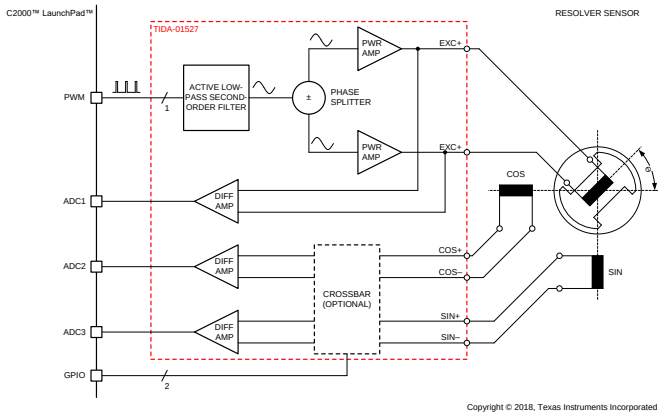
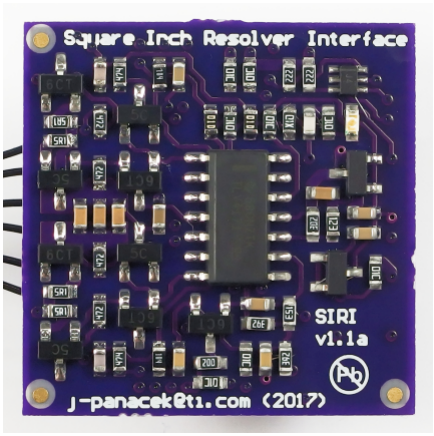


# 1 System Description

High-performance motor control applications traditionally require a speed or position sensor for the control loop feedback. Various methods and new algorithms are available which may eliminate the requirement for a physical sensor; however, many applications cannot achieve the required performance and reliability through sensorless control. Examples include traction inverters for hybrid-electric vehicles (HEV) and electric vehicles (EV), electric power steering, motor drives and servos in industrial applications. A resolver is one of the most popular angular sensors due to its reliability (even in an harsh environment) and the ratiometric output, which suppresses common-mode noise.

This discrete resolver front-end reference design provides a simple implementation of a resolver interface. The design uses a small PCB which implements an excitation amplifier for the primary winding and the analog signal front end for the feedback windings. The PCB connects to the C2000 LaunchPad with the TMS320F28069M MCU over a flat ribbon cable or by using a small PCB adapter. The provided code example for the MCU uses the undersampling algorithm for readback signals demodulation and the arc tangent goniometric function for the angle calculation.

Components used in this design have been rated for automotive applications or have an automotive-qualified alternative. The guide also suggests more customized components with higher integration for performance upgrade.

**NOTE:** The TIDA-01527 reference design has not been tested for any automotive or industrial requirements (for example, functional safety or electromagnetic compatibility). The design serves as a practical guidance and inspiration for the customer's system implementation.

## *1.1 Key System Specifications*

**Table 1. Key System Specifications**

| PARAMETER | SPECIFICATIONS |
|---|---|
| Resolver excitation voltage | Typically 4 $V_{RMS}$ or 7 $V_{RMS}$ |
| Input voltage | 12 V to 15 V |
| Resolver excitation frequency | Scalable, optimized for 5 kHz |
| PCB dimensions | 25.4 mm × 25.4 mm |
| Output signal levels | 0 V to 2.54 V |
| Supported excitation current | < 80 mA, upgrade possible |
| Protection mechanisms (e.g. current, voltage, temperature, electrostatic discharge (ESD)) | None |
| Excitation amplifier modulation | Sine-wave-modulated pulse width modulation (PWM), fixed frequency f = 312.5 kHz, variable duty cycle |
| Accuracy | ±0.25° angle readout accuracy or ±0.1° using the innovative scattering signal processing method (see *Test Results*) |
| Resolution | 12 b |

## 2 System Overview

The TIDA-01527 reference design consists of a host MCU and resolver sensor. The host MCU generates a pulse-width modulated (PWM) signal with a variable duty cycle. The duty-cycle modulation matches the desired resolver excitation frequency. The second-order active low-pass filter only preserves the excitation frequency and converts the PWM signal into a harmonic signal. The analog phase-splitter circuit splits the harmonic signal into two complementary harmonic signals. Two power amplifiers boost these harmonic signals to match the resolver excitation voltage levels. A set of difference amplifiers monitor all resolver windings and interface to the analog-to-digital converter (ADC) in the host MCU. The system uses an optional analog crossbar circuit for advanced analog processing techniques, system calibration, and basic diagnostics. For details on the scattered signal processing method, see Section 3.

Figure 1 shows the reference design from the top and the bottom side.

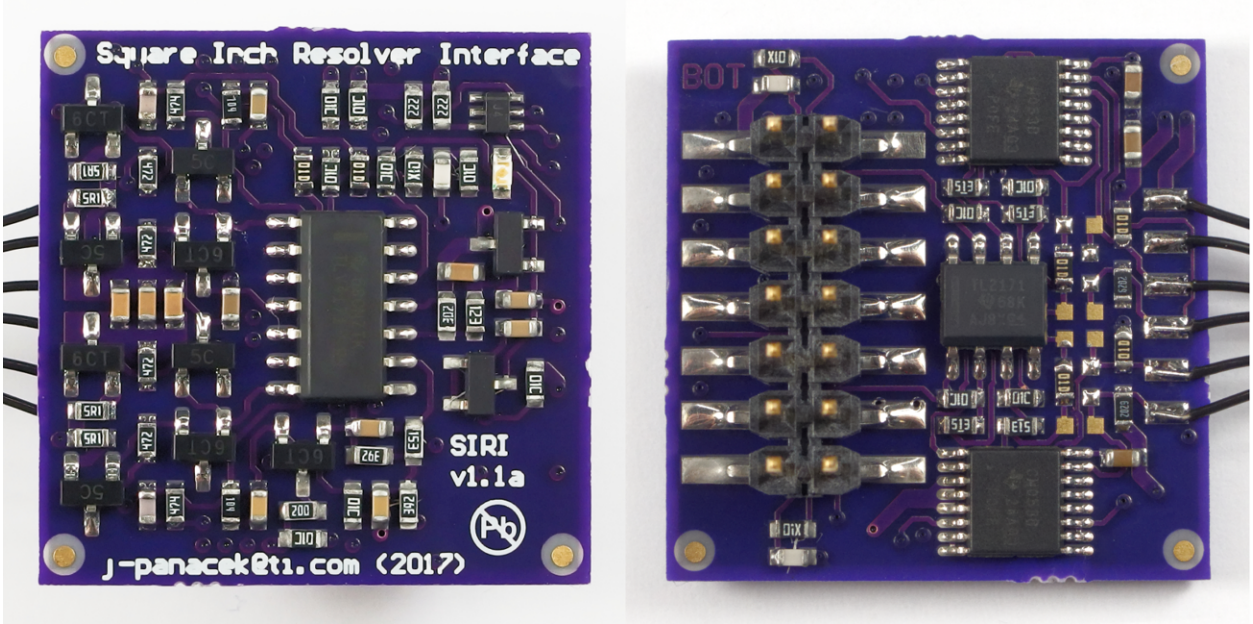



**Figure 1. TIDA-01527 Board (Top and Bottom)**

## 2.1 Block Diagram

Figure 2 shows a block diagram of the TIDA-01527 reference design, host MCU, and resolver sensor.

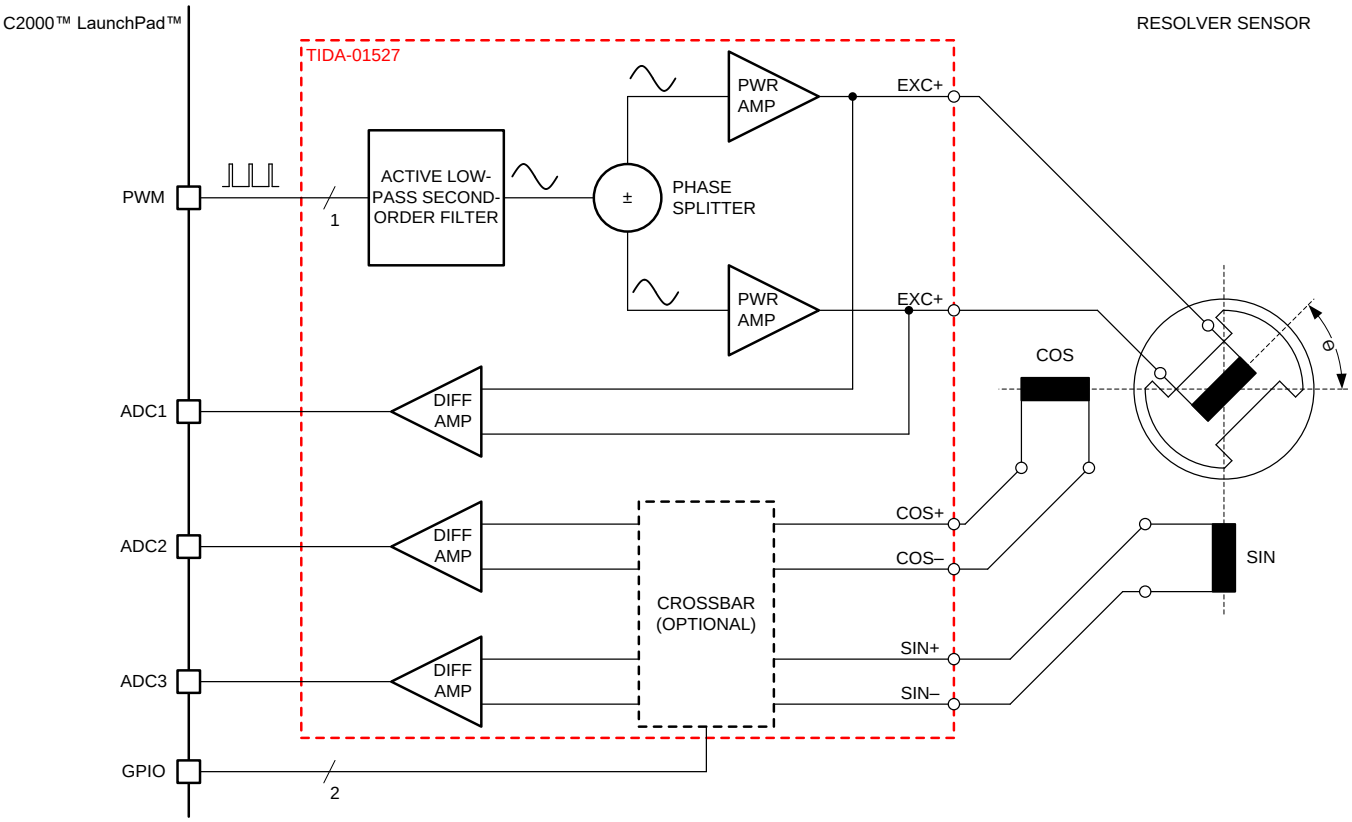





**Figure 2. TIDA-01527 Block Diagram**

## 2.2 Highlighted Products

### 2.2.1 TLV4171

The TLVx171 family of devices is a 36-V, single-supply, low-noise operational amplifier (op amp) with the ability to operate on supplies ranging from 2.7 V (± 1.35 V) to 36 V (±18 V). This series is available in multiple packages and offers low offset, drift, and low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the TLVx171 family of devices is specified from 2.7 V to 36 V. Input signals beyond the supply rails do not cause phase reversal.

The TLVx171 family of devices is stable with capacitive loads up to 200 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. The device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The TLVx171 op amp family is specified from –40°C to +125°C.

### 2.2.2 TLV431x-Q1

The TLV431x-Q1 device is a low-voltage three-terminal adjustable voltage reference with specified thermal stability over applicable industrial, automotive, and commercial temperature ranges. The output voltage can be set to 1.24 V on stand-alone mode or any value between $V_{REF}$ (1.24 V) and 6 V with two external resistors. These devices operate from a lower voltage (1.24 V) than the widely-used TL431 and TL1431 shunt-regulator references. When used with an optocoupler, the TLV431 device is an ideal voltage reference in isolated feedback circuits for 3-V to 3.3-V switching-mode power supplies. These devices have a typical output impedance of 0.25 Ω. Active output circuitry provides a very-sharp turnon characteristic, making them excellent replacements for low-voltage Zener diodes in many applications, including onboard regulation and adjustable power supplies.

### 2.2.3 C2000™ TMS320F28069M MCU

The F2806x Piccolo™ family of microcontrollers (MCUs) provides the power of the C28x core and control law accelerator (CLA) coupled with highly-integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, and also provides a high level of analog integration.

An internal voltage regulator allows for single-rail operation. Enhancements have been made to the high-resolution pulse width modulator (HRPWM) module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the ePWM outputs. The ADC converts from a 0- to 3.3-V fixed full-scale range and supports ratio-metric $V_{REFHI}/V_{REFLO}$ references. The ADC interface has been optimized for low overhead and latency.

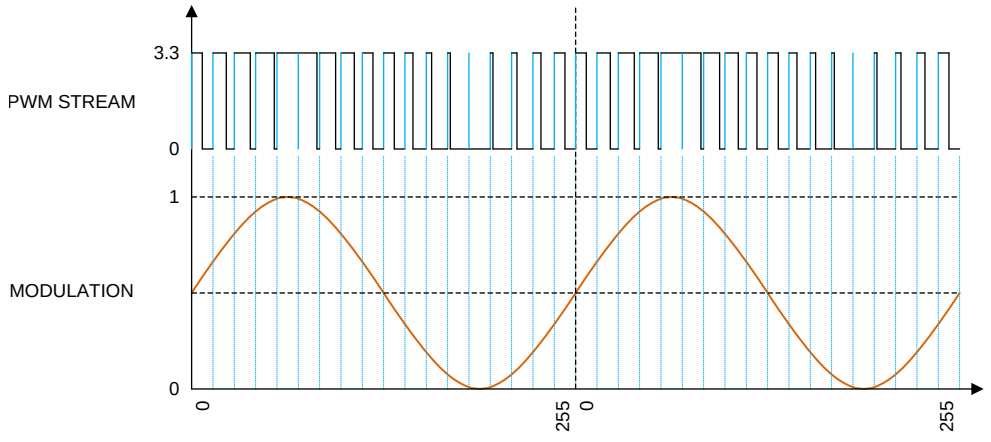
## 2.3 System Design Theory

The following chapters describe the system design in the order which corresponds to the signal flow.

- *PWM Generation* (C2000, software)
- *Active Low-Pass Second-Order Filter and Phase Splitter* (hardware)
- *Power (Excitation) Amplifiers* (hardware)
- *Resolver Sensor* (hardware)
- *Crossbar—Optional* (hardware)
- *Analog Front-End Difference Amplifiers* (hardware)
- *A/D Conversion and Signal Processing* (C2000, software)

### 2.3.1 PWM Generation

The C2000 MCU generates a PWM signal with a fixed frequency and variable duty cycle. The PWM period is significantly higher than the period of the resolver excitation signal. Figure 3 shows the PWM stream (not in scale).




Note: X-axis is not in scale

**Figure 3. PWM Generation From MCU**

Every new period of the PWM triggers an interrupt service routine where the controller calculates a new duty cycle using the sinus function. The period of the PWM modulator is set as per Equation 1.

$$T_{PWM} = 2^n \times T_{SYSCLK} \quad (1)$$

This method allows conversion of the excitation signal into a discrete time signal with an n-bit resolution. An internal variable-counter counts every interrupt from 0 to $2^n - 1$ and automatically resets when it reaches $2^n$. The software example uses the IQ math library. After casting the internal variable-counter to IQ*n* number, the result takes the value between 0..1, which corresponds to 0..2π angle on the unity circle. For this reason, the internal variable-counter is called the excitation angle, or *ExcAngle*. This variable is very important because all signal processing refers to it.

The designer can also adjust the PWM duty-cycle modulation index (depth). Typically, the modulation index is 1.0, which corresponds to a duty cycle from 0% to 100%. When set to 0.5, the duty cycle varies from 25% to 75%. This variation reduces the output amplitude of the excitation signal. For this reason, the modulation index variable is called *ExcGain* and may be used to fine-tune the output amplitude. Note that lowering the modulation index reduces the effective resolution and increases harmonic distortion of the excitation signal.

Another important aspect to understand is that the required bit-resolution *n* and the system clock period $T_{SYSCLK}$ define the period $T_{PWM}$ of the generated PWM signal, as per Equation 2. A lower resolution increases the total harmonic distortion (THD) while a lower operating frequency requires a higher-order low-pass filter.

$$T_{PWM} = \frac{T_{EXC}}{2^n} \quad (2)$$

Finally, the MCU sets the duty cycle, as per Equation 3:

$$\text{duty} = 0.5 \times \left[1 + \left(\sin\left(\text{ExcAngle}\right) \times \text{ExcGain}\right)\right] \quad (3)$$

where,

- duty = 0…1,
- ExcAngle = 0…2π,
- ExcGain = 0…1.

Adding 1 ensures that the duty cycle is always positive with the center at 0.5.

*Example calculation for TIDA-01527:*

Desired excitation frequency $f_{EXC}$ = 5 kHz → $T_{EXC}$ = 200 µs

System clock $f_{SYSCLK}$ = 80 MHz → $T_{SYSCLK}$ = 12.5 ns

Choosing PWM resolution = 8 b

PWM period as per Equation 4:

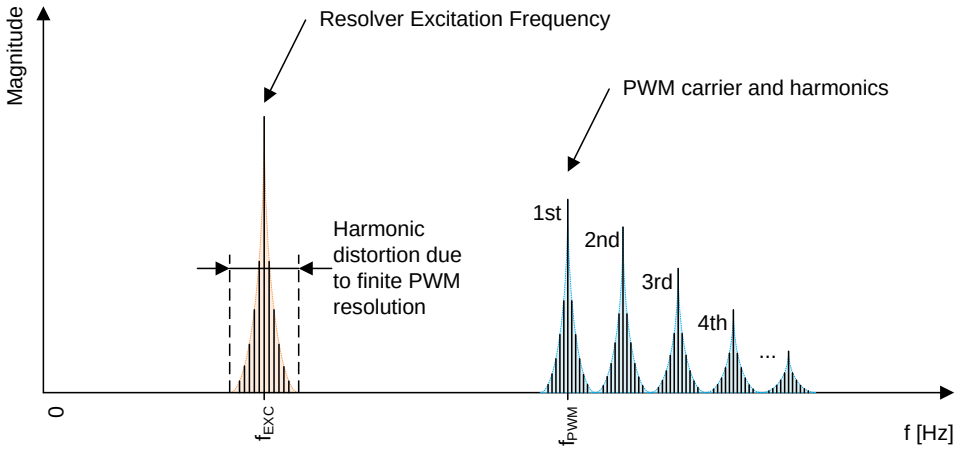
$$T_{PWM} = 2^8 \times 12.5\ \text{ns} = 3.2\ \mu\text{s} \quad (4)$$

The excitation angle variable resolution per Equation 1 then turns into Equation 5

$$T_{PWM} = \frac{T_{EXC}}{2^n} \rightarrow n = \frac{\log\left(\frac{T_{EXC}}{T_{PWM}}\right)}{\log 2} = \frac{\log\left(\frac{200e-6}{3.2e-6}\right)}{\log 2} = 5.96 \Rightarrow 6\ \text{bit} \quad (5)$$

### 2.3.2 Active Low-Pass Second-Order Filter and Phase Splitter

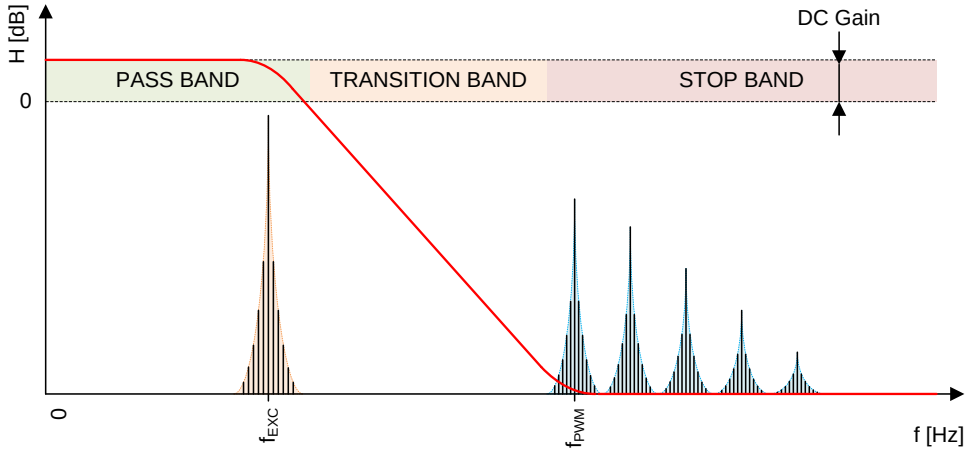
Figure 4 shows a simplified magnitude spectrum of the generated PWM signal described in Section 2.3.1.




Note: X-axis is not in scale

**Figure 4. Magnitude Spectrum of Generated PWM Signal**

A properly-set low-pass filter suppresses the PWM carrier and harmonics to a minimum but passes the resolver excitation signal content, as Figure 5 shows. This process converts the modulated PWM stream to a sine wave. Note that increasing the difference between $f_{EXC}$ and $f_{PWM}$ lowers the requirement for filter rolloff (filter order). Setting the DC gain and the rolloff point is worth the practical experiment. The DC gain compensates for the excitation frequency attenuation and different combinations provide different results. Matching the –3-dB cutoff to the excitation frequency is the starting point when designing the filter.




Note: X-axis is not in scale

**Figure 5. Suggested Low-Pass Filter Response for PWM Signal Filtering**

The reference design uses a second-order low-pass active filter with a multiple feedback topology, as Figure 6 shows.

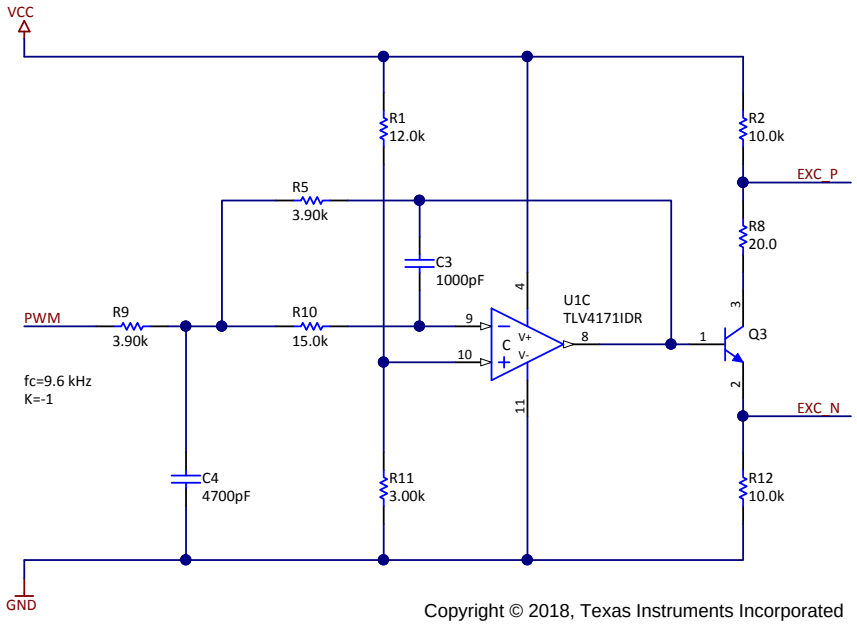



**Figure 6. Multiple-Feedback Filter (MFB) in TIDA-01527**

During development, this topology was proven to be a better solution rather than the popular Sallen-Key topology. Another benefit is that the resistor divider (R1, R11), which sets the DC offset, connects to the high-impedance non-inverting input of the op amp. The Sallen-Key filter requires buffering for floating ground (DC offset), which adds to the circuit complexity. R5 and R9 set the DC gain of the filter as per Equation 6.

$$A_{DC} = -\frac{R5}{R9} = -\frac{3900}{3900} = -1 \tag{6}$$

Equation 7 calculates the –6-dB cutoff frequency of the filter.

$$f_{c-6\ db} = \frac{1}{2\pi\sqrt{R5 \times R10 \times C4 \times C3}}$$

$$f_{c-6\ db} = \frac{1}{2\pi\sqrt{3900 \times 15000 \times 4.7e-9 \times 1e-9}}$$

$$f_{c-6\ db} = 9589\ Hz \tag{7}$$

Equation 8 calculates the more-common approximation of a –3-dB cutoff from the –6-dB point.

$$f_{c-3\ db} = f_{c-6\ db}\sqrt{2^{\left(\frac{1}{n}\right)} - 1} = 9589\sqrt{2^{\left(\frac{1}{n}\right)} - 1} = 6171\ Hz \tag{8}$$

**NOTE:** The cutoff frequency is typically identified as the point where the transfer function of a filter drops by –3 dB. This drop corresponds to approximately half of the power transfer. However, higher-order filters have a steeper rolloff (for example: –40 dB/dek for a second-order filter) and the cutoff frequency is defined as *n*(–3 dB) where *n* is the filter order. This definitionoften causes confusion because some technical articles or online calculators use formulas referring to the –3-dB point whereas others use *n*(–3 dB). TI recommends checking the calculation using a simulation tool.

As Section 2.3.4 describes, a resolver is a transformer. Eliminating any DC current through the primary winding is important to avoid magnetic circuit saturation. For this reason, the system uses differential excitation with two output amplifiers with a phase shift of 180°. The resolver then registers only the differential voltage $V_R$ as per Equation 9:

$$V_R = (V_{EXC+} + V_{DC}) - (V_{EXC-} + V_{DC}) \quad (9)$$

where,

$$V_{EXC+} = -V_{EXC-} \quad (10)$$

and then,

$$V_R = 2 \times V_{EXC} \quad (11)$$

A simple analog phase splitter using the transistor Q3 and resistors (R2, R12) creates well-matched complementary sine waves, as per Equation 10. The resistor R8 compensates for the intrinsic emitter resistance of Q3. This compensation helps to roughly match output impedances between the collector and emitter node.

### 2.3.3 Power (Excitation) Amplifiers

A pair of excitation amplifiers directly drive the primary winding of the resolver sensor. Both amplifiers are identical, so this documentation only describes the first one. The amplifier is practically a single-supply audio amplifier with a band-pass filter response. Figure 7 shows the circuit diagram.

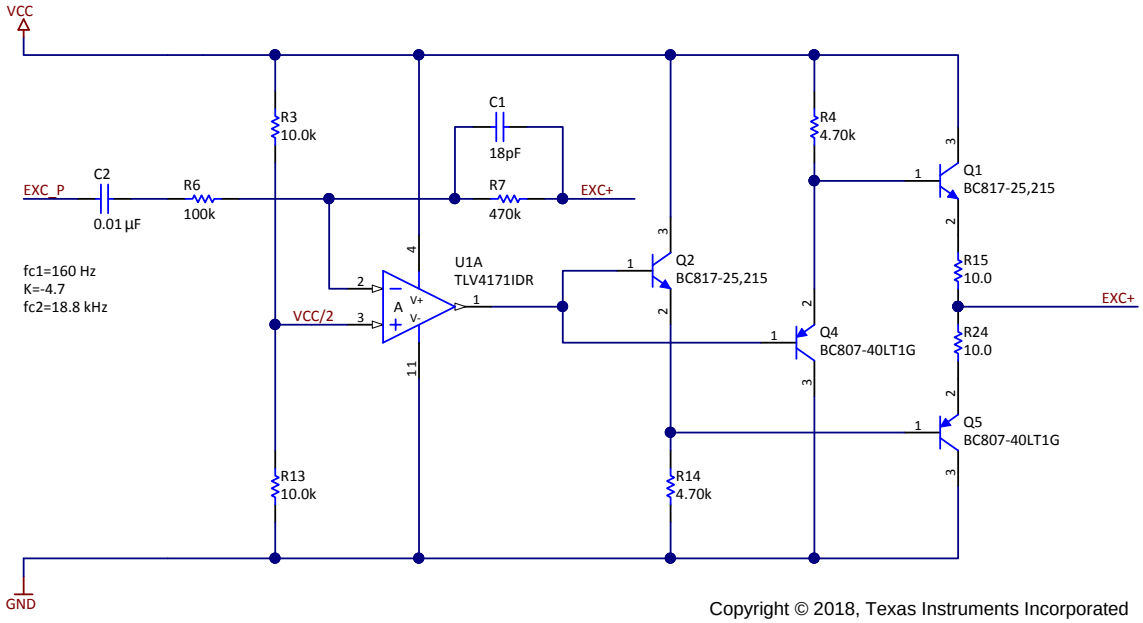





**Figure 7. TIDA-01527 Excitation Amplifier—Single Channel**

Resistors R3 and R13 create a virtual ground and set the DC offset to the middle of the operating voltage range. Resistors R6 and R7 set the pass-band gain as per Equation 12 . Note that keeping these resistors reasonably high is important because R6 also defines the input impedance of the power stage.

$$A_{PASS-BAND} = -\frac{R7}{R6} = -\frac{470e3}{100e3} = -4.7 \quad (12)$$

The power stage is AC-coupled because the virtual ground (DC offset) of the power stage does not match the EXC_P, EXC_N outputs of the phase splitter. The capacitor C2 and resistor R6 set the lower cutoff frequency as per Equation 13. The cutoff frequency is set significantly lower than the excitation frequency to prevent signal of interest attenuation.

$$f_{low-3\,dB} = \frac{1}{2\pi \times R6 \times C2} = \frac{1}{2\pi \times 100e3 \times 10e-9} = 159.2\,Hz \quad (13)$$

Equation 14 defines the upper cutoff frequency of the amplifier. Similar to the low-pass filter in Section 2.3.2, the designer must set the cutoff frequency as low as possible to further reduce the PWM spectral content but high enough to pass the excitation frequency without attenuation.

$$f_{high-3dB} = \frac{1}{2\pi \times C1 \times R7}$$

$$f_{high-3dB} = \frac{1}{2\pi \times 18e-12 \times 470e3}$$

$$f_{high-3dB} = 18.81 \text{ kHz} \quad (14)$$

Texas Instruments offers integrated power amplifiers that fit this application. An integrated solution solves many problems, such as:

- Output stage biasing
- Crossover distortion
- Overcurrent protection
- Temperature protection
- Temperature (runaway) stability

Adding these features by using discrete components usually results in very complex circuits which are typically known for their use in high-end audio amplifiers.

Recommended parts: ALM2402, OPA564-Q1

Verifying the minimal slew rate for the excitation amplifier is also very important. Equation 15 defines the minimal slew-rate *SR*.

$$SR_{min} \geq f_{EXC} \times 2\pi \times V_{amp} \quad (15)$$

where,

- $V_{amp}$ is the amplitude (single-ended) of the generated sine wave.

Figure 8 shows the relationship between excitation frequency, resolver excitation voltage, and the amplifier slew rate for applications using the differential type of an excitation amplifier.

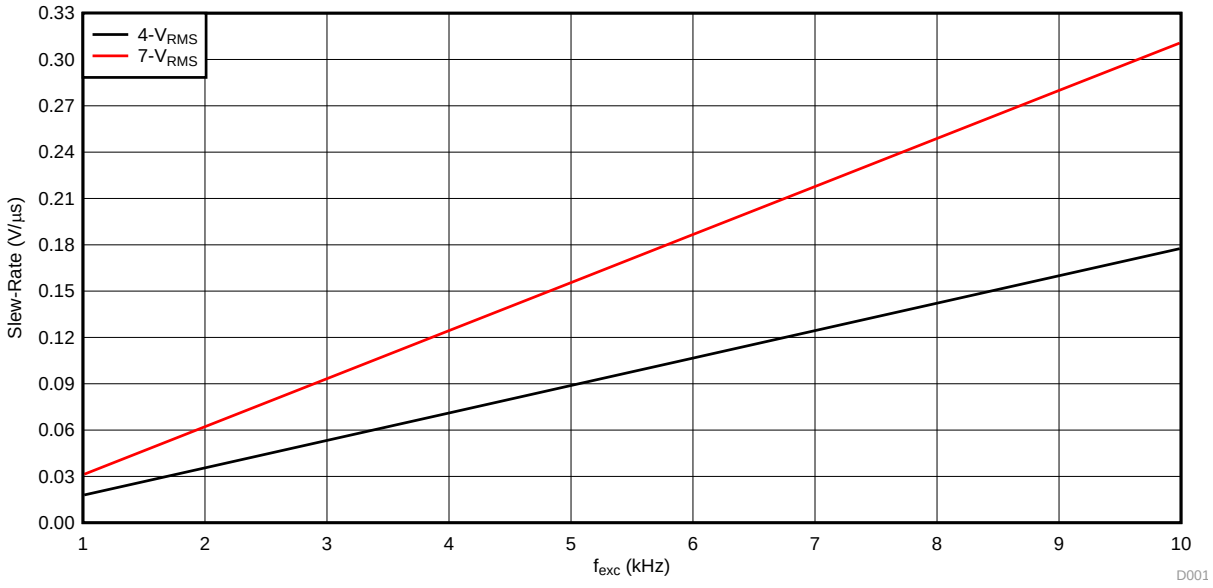



**Figure 8. Minimum Required Slew Rate per Amplifier (Single-Ended) for 4-$V_{RMS}$ and 7-$V_{RMS}$ Resolvers**

### 2.3.4 Resolver Sensor

A resolver uses the principle of a rotating transformer with a single primary winding and two secondary windings positioned in a right angle from each other (see Figure 9). The generated sine wave $V_R$ excites the primary winding and creates the magnetic flux $\Phi$, which is distributed through secondary windings with respect to the rotor angle $\Theta$. Equation 16 then calculates the rotor angle $\Theta$ from the ratio of voltages $V_S$, $V_C$ on the secondary windings.

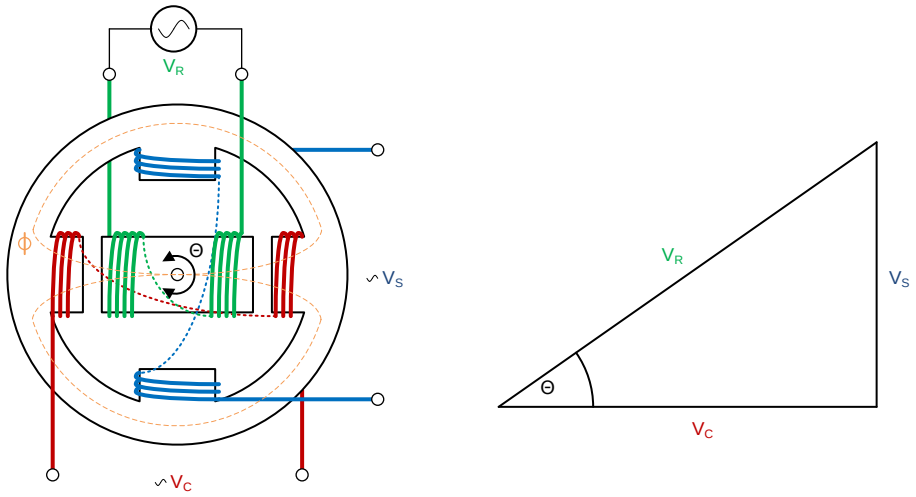





**Figure 9. Resolver as Rotating Transformer**

$$V_S = \sin\Theta \times V_R \times TS$$
$$V_C = \cos\Theta \times V_R \times TS$$
$$\frac{\sin\Theta \times V_R \times TS}{\cos\Theta \times V_R \times TS} = \frac{\sin\Theta}{\cos\Theta} = \frac{V_S}{V_C}$$
$$\tan\Theta = \frac{V_S}{V_C} \rightarrow \Theta = \arctan\frac{V_S}{V_C} \quad (16)$$

Understanding the spectral content of a resolver sensor is important. The signal that each resolver winding produces is amplitude modulated with a modulation index of m = 2 (overmodulation). When a resolver is steady and at a fixed angle (highlighted by the green color in Figure 10), then the output spectrum only has a single spectral line at the excitation frequency $f_{EXC}$, unless the output signal has zero amplitude (every 180°). When a resolver spins with angular frequency$f_{VELOCITY}$ (highlighted by red color in Figure 10), then the effect of overmodulation (m = 2) completely suppresses the carrier (excitation) frequency $f_{EXC}$. This effect is important to consider when designing a signal processing algorithm.

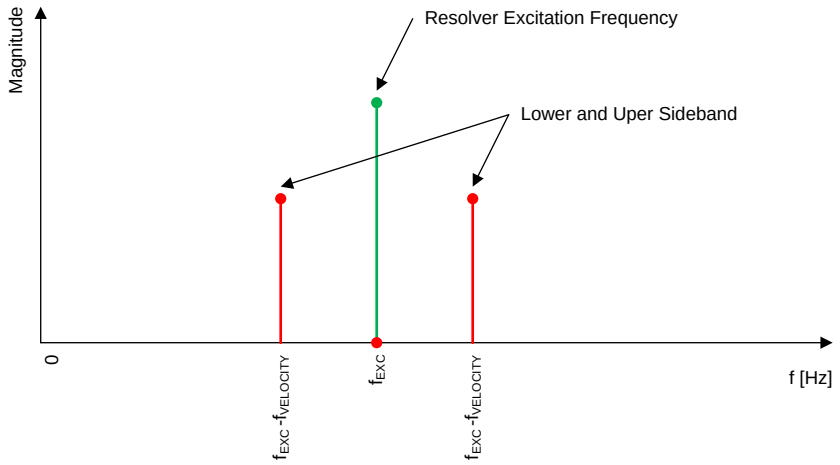



**Figure 10. Magnitude Spectrum of Resolver Sensor Output Signal**

For further details on resolvers, see *EMC Compliant Single-Chip Resolver-to-Digital Converter (RDC) Reference Design* or *Synchro and Resolver Engineering Handbook*.

### 2.3.5 Crossbar—Optional

A pair of CMOS multiplexers (U5, U6) form an analog crossbar, as Figure 11 shows. This crossbar is an experimental circuitry further used in the signal processing algorithm. This circuit also allows for swapping input signals between each difference amplifier or the complete disconnection of resolver windings. This circuitry, together with an advanced algorithm in the MCU, reduces system error and enables basic diagnostics features. Transistors Q10A, Q10B and resistors R48, R48 convert logic levels from the MCU.

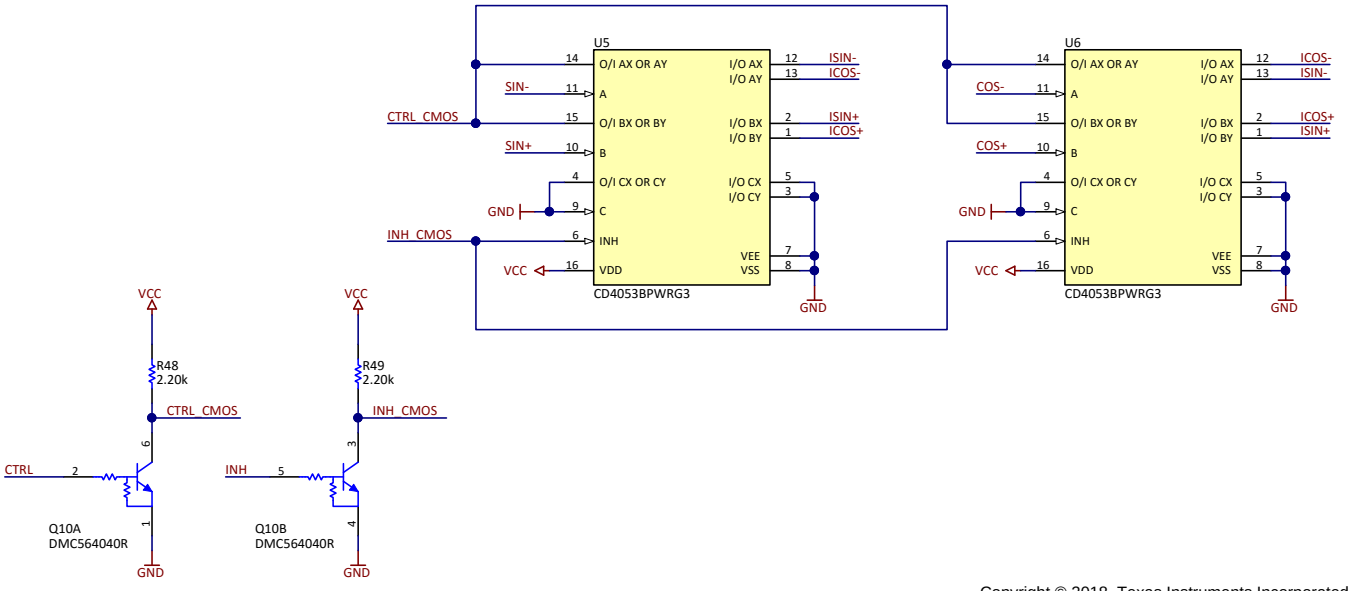



**Figure 11. Analog Crossbar (Experimental)**

### 2.3.6 Analog Front-End Difference Amplifiers

The system uses three difference amplifiers for the feedback.

Figure 12 shows the first amplifier, which monitors the excitation outputs. Monitoring the excitation amplifier is extremely useful because a diagnostic routine in the MCU can compensate the tolerances of parts and precisely adjust the output voltage using the *ExcGain* variable. Additionally, this monitoring enables the system to measure the phase lag of the active filter and excitation amplifier or detect a faulty excitation amplifier. Set the DC gain of the difference amplifier per Equation 17.

$$A = \frac{R19}{R20} = \frac{10k}{100k} = 0.1 \text{ when } R19 = R23 \text{ and } R20 = R22 \quad (17)$$

The resistor R21 and capacitor C7 form a charge bucket filter for the ADC. The difference amplifier uses the DC offset (VREF1/2) to match the bidirectional signal from the resolver with the single-ended ADC input.

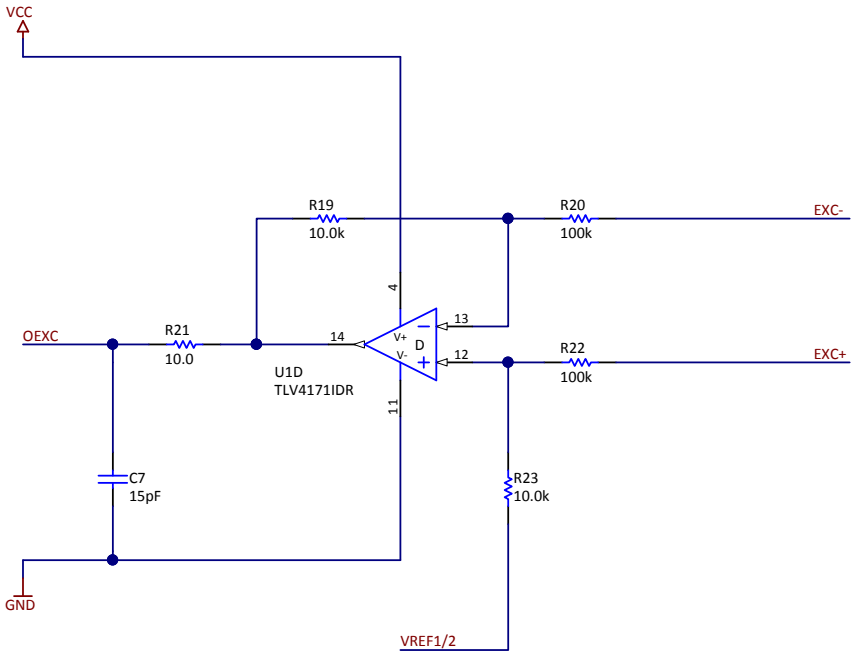





**Figure 12. Excitation Amplifier Output Monitoring**

The other two difference amplifiers monitor the sinus and cosinus windings from the resolver sensor. Because both amplifiers are identical, this documentation only describes the first one (see Figure 13).

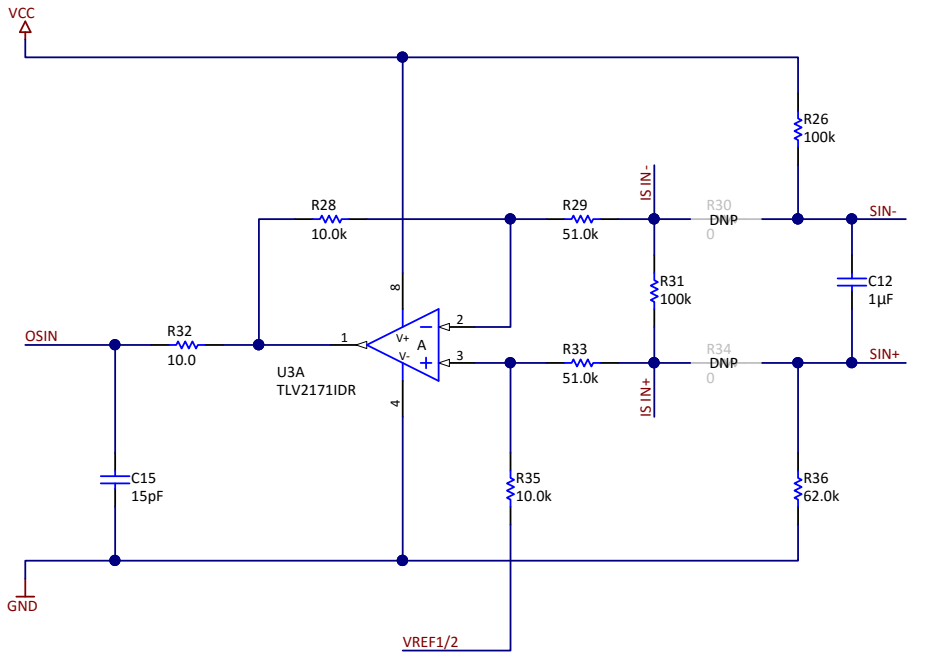





**Figure 13. Resolver Feedback Winding Monitoring**

Set the DC gain of the difference amplifier per Equation 18. The resistor R32 and capacitor C15 form a charge bucket filter for the ADC. The difference amplifier uses the DC offset (VREF1/2) to match the bidirectional signal from the resolver with the single-ended ADC input.

$$A = \frac{R28}{R29} = \frac{10k}{51k} = 0.196 \text{ when } R28 = R35 \text{ and } R29 = R33 \quad (18)$$

The signal from the resolver secondary winding is floating. Resistors R26, R31, and R36 provide the appropriate DC biasing. Keeping the inputs of the op amps within the specified common mode range is important. C12 is an optional filtering capacitor (do not assemble). The 0-Ω resistors R30, R34 must be populated when the analog crossbar circuitry is not in use.

Two inexpensive voltage references U2, U4 create a 1.24 V and 2.48 V for the ADC. Resistor R27 provides biasing and capacitors C13, C14 provide basic filtering.

**NOTE:** Always check the stability boundary conditions and minimal bias current for the x431 series of shunt references. The criteria is subject to change between manufacturers.

Texas Instruments recommends the use of integrated difference amplifiers such as the INA1650-Q1 as a potential performance upgrade. An integrated multichannel solution provides better channel matching and precise gain setting without the requirement of expensive precision resistors.

### 2.3.7 A/D Conversion and Signal Processing

The system uses the undersampling method for demodulating the signals from the resolver sensor. This technique is one of the simplest, yet very effective. An example of another method is to use a digital envelope detector and various digital filters. Such a solution is also effective, especially in a noisy environment; however, every filter causes phase lag and a delay in the system, which is often undesirable in high-performance feedback control loops.

Figure 14 shows the typical waveforms of a resolver spinning at angular speed as per Equation 19.

$$\omega = \frac{2 \times \pi}{T_{VELOCITY}} \tag{19}$$

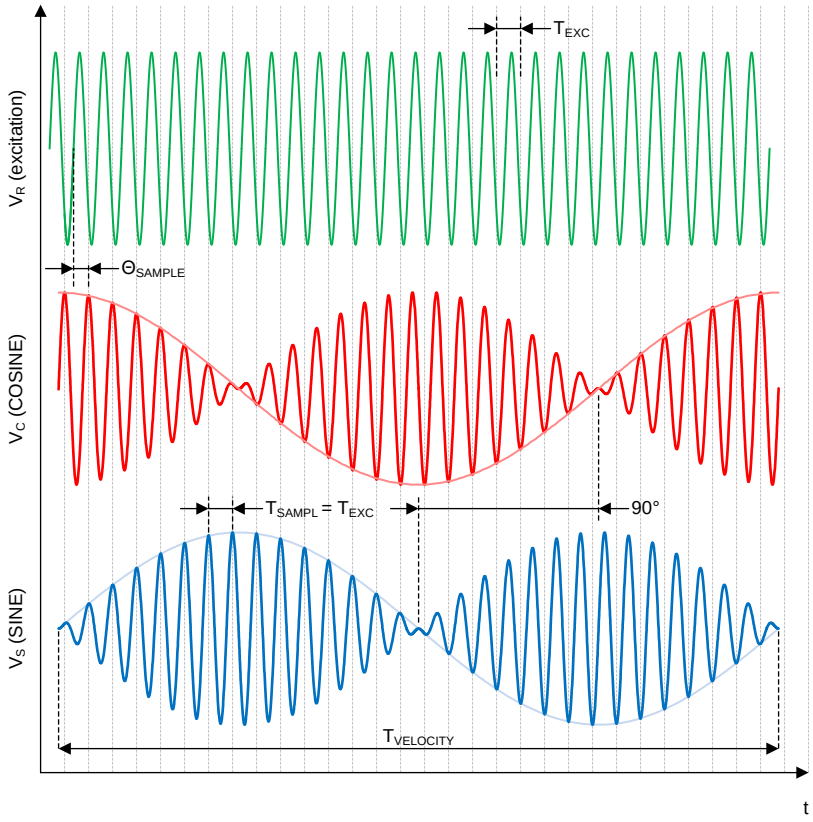



**Figure 14. Typical Resolver Waveforms**

The physical placement of the secondary windings defines the phase shift between the sine and cosine signal, which is ideally 90°.

Sampling $V_S$ and $V_C$ with period $T_{SAMPL} = T_{EXC}$ demodulates the signal and preserves only the signal envelope that is required for angle calculation, as per the previous Equation 16. The ADC converter is set in such a way that it always samples the signal when the amplitude reaches the maximum. This setting increases the signal-to-noise ratio and delivers the best results. The ADC sampling time derives from the *ExcAngle* parameter described in Section 2.3.1. For this reason, the code uses the name *SamplAngle.* Ideally, the sampling time *SamplAngle* occurs when *ExcAngle* is 0.25, 0.75, or both. However, two sources of phase lag exist for which the system must compensate. The first source of phase lag is on the active low-pass filter and the excitation amplifier. Resolver impedance, which varies with every model, defines the second source of phase lag. A diagnostic routine, which sweeps the *SamplAngle* variable during the start-up and picks the time point when either $V_C$ or $V_S$ is highest, makes the system compatible with various resolvers with different impedance. The ADC samples both resolver signals ideally at the same time. The MCU offers two independent sample-and-hold circuits which enable this simultaneous sampling. For this reason, $V_C$ and $V_S$ connect to ADCINA0 and ADCINB0, respectively.

## 3 Scattered Signal Processing Method

A typical resolver system uses a difference amplifier, which interfaces with the ADC for each output ($V_S$, $V_C$), as Figure 15 shows.

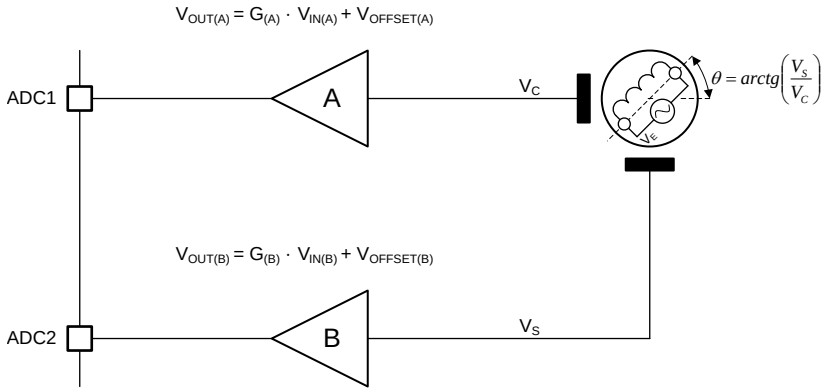



**Figure 15. Typical Resolver-to-Digital Signal Chain**

Matching the transfer function of the difference amplifiers is critical for system accuracy. Any difference between the gain or DC offset creates a non-linear error in angle measurement, as per Equation 20.

$$\Theta = \text{arctg}\left(\frac{V_S}{V_C}\right) = \text{arctg}\left(\frac{G_{(B)} \times V_S + V_{OFFSET(B)}}{G_{(A)} \times V_C + V_{OFFSET(A)}}\right) \quad (20)$$

The blue trace in Figure 16 shows how a 1% gain imbalance between the amplifiers contributes to the angle error. The red trace shows the effect of the DC offset on the angle error when $V_{OFFSET(A)} = 0.05 \times V_{S(MAX)}$.

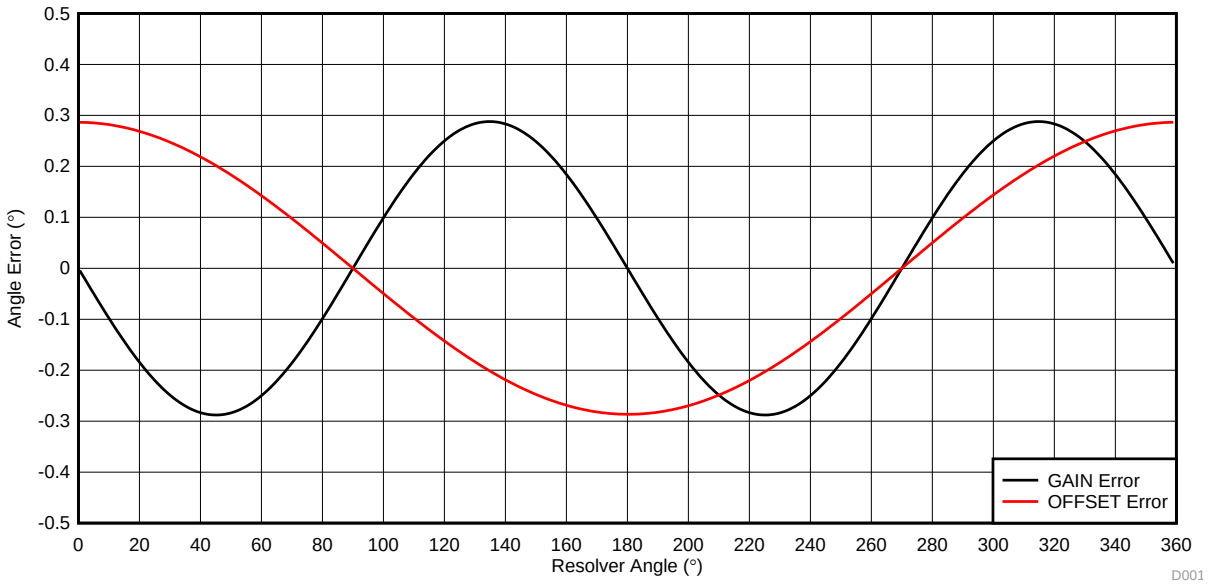



**Figure 16. Effect of DC Offset and Gain Imbalance on Angle Error**

Higher accuracy systems require precision components for the difference amplifiers and system calibration, which increases system and manufacturing costs. This consideration is valid for discrete as well as integrated circuits.

The reference design implements a novel method called *scattered signal processing*. The method uses the analog crossbar described in Section 2.3.5 and a modified algorithm in the firmware.

The scattered signal processing method adds an inexpensive analog multiplexer with an inhibit function (for example, the CD4053) between each resolver output and difference amplifier. This analog multiplexer allows disconnecting the resolver outputs or swapping them between the difference amplifiers on-the-fly when the system is running. Swapping resolver outputs *scatters* the signal between two signal paths, which is the key action of this concept.

The system operates in the following three steps, which repeat periodically:

1. DC offset calibration with disconnected resolver sensor
2. Sampling the output of both differential amplifiers with the normally-connected resolver outputs $V_S$, $V_C$ (direct mode)
3. Sampling the output of both differential amplifiers with swapped resolver outputs $V_S$, $V_C$ (inversed mode)

Figure 17 shows the first step, which is DC offset calibration. The resolver sensor is completely disconnected and the output of each difference amplifier corresponds to the DC offset $V_{OFFSET(A,B)}$.

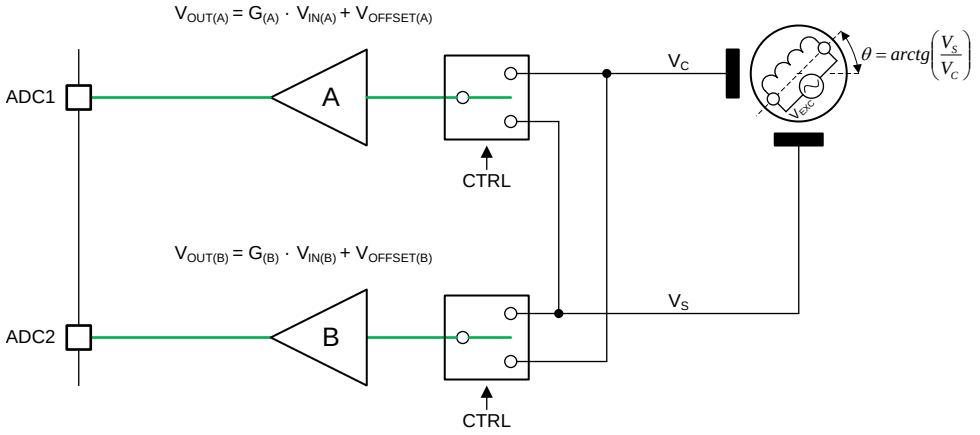



**Figure 17. Scattered Signal Processing Method—Step 1:DC Offset Calibration**

In the next step, the ADC samples the output of both differential amplifiers in direct mode (see Figure 18).

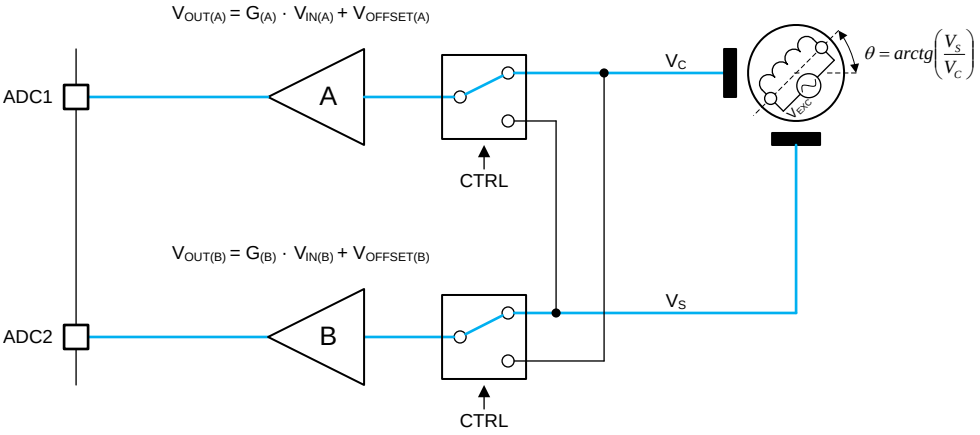



**Figure 18. Scattered Signal Processing Method—Step 2: Direct Mode**

In the last step, the ADC samples the output of both differential amplifiers in inversed mode (see Figure 19).

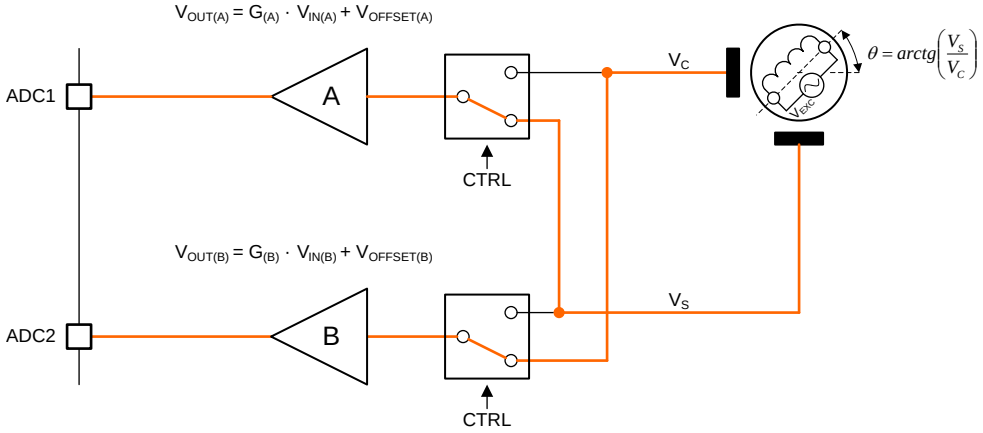



**Figure 19. Scattered Signal Processing Method—Step 3: Inversed Mode**

Table 2 lists the values that the ADC reads during all three steps.

**Table 2. ADC Samples Taken During Steps 1 Through 3**

| ADC INPUT | STEP 1 | STEP 2 | STEP 3 |
|---|---|---|---|
| ADC1 | $V_{OFFSET(A)}$ | $G_{(A)} \times V_C + V_{OFFSET(A)}$ | $G_{(A)} \times V_S + V_{OFFSET(A)}$ |
| ADC2 | $V_{OFFSET(B)}$ | $G_{(B)} \times V_S + V_{OFFSET(B)}$ | $G_{(B)} \times V_C + V_{OFFSET(B)}$ |

The angle calculation algorithm uses all three results for gain imbalance and DC offset elimination. First, the algorithm adds the results from step 2 and step 3, as per Equation 21.

$$\Theta = \text{arctg}\left(\frac{V_S}{V_C}\right) = \text{arctg}\left(\frac{G_{(B)} \times V_S + V_{OFFSET(B)} + G_{(A)} \times V_S + V_{OFFSET(A)}}{G_{(A)} \times V_C + V_{OFFSET(A)} + G_{(B)} \times V_C + V_{OFFSET(B)}}\right) \quad (21)$$

The system obtains the DC offset information for both channels from step 1 and compensates it. This compensation results in the simplified formula as per Equation 22.

$$\Theta = \text{arctg}\left(\frac{V_S}{V_C}\right) = \text{arctg}\left(\frac{G_{(B)} \times V_S + G_{(A)} \times V_S}{G_{(A)} \times V_C + G_{(B)} \times V_C}\right) \quad (22)$$

Mathematical manipulation eliminates the gain variables from the formula as per Equation 23.

$$\Theta = \text{arctg}\left(\frac{V_S}{V_C}\right) = \text{arctg}\left(\frac{V_S \times \left(G_{(B)} + G_{(A)}\right)}{V_C \times \left(G_{(A)} + G_{(B)}\right)}\right) \rightarrow \Theta = \text{arctg}\left(\frac{V_S}{V_C}\right) \quad (23)$$

*At this point note that the gain imbalance and DC offset no longer contribute to the error calculation.* Also note that the method compensates for any imperfections in the ADC transfer function (gain or offset).

**NOTE:**

- Embedded algorithms typically use Atan2 function which is defined at ±π radians.
- The scattered-signal processing method is effective for signals with a significantly lower bandwidth than the ADC sampling and algorithm execution frequency.
- The current firmware implementation only performs step 1 during the system start-up.

The scattered-signal processing technique has additional positive side effects. The system allows for "limp mode" operation due to the redundant signal path and allows for additional diagnostics, the process for which is as follows:

1. The hardware engineer calculates the worst-case tolerances for the DC offset and gain imbalance and parametrizes the system (for example, a 1.5% tolerance span).
2. The algorithm then periodically checks if readout data are within the given tolerance boundaries, typically for:
   - DC offset for both channels
   - Maximum acceptable difference between ADC samples taken in step 2 and step 3
   - $V_S$ and $V_C$ amplitude
3. If one of the diagnostic results fails, the system is able to detect the defective channel and eventually work in the "limp mode" with reduced performance, using only one analog front-end channel. This measureis important and beneficial in robust systems and in safety-critical applications (SIL/ASIL).

# 4 Hardware, Software, Testing Requirements, and Test Results

## 4.1 Required Hardware and Software

### 4.1.1 Hardware

The following hardware is necessary for exploring the TIDA-01507 reference design:

- The TIDA-01527 discrete resolver front-end board
- The LAUNCHXL-F28069M LaunchPad development board (or similar)
- The adapter board or a custom ribbon cable for interfacing the TIDA-01527 with the LaunchPad
- A resolver sensor matching the system specification
- Laboratory power supply specified at 0 V to 15 V, 0 mA to 200 mA, preferably with current limitation or overcurrent protection
- A computer capable of running Code Composer Studio™ (CCS) software

Figure 20 shows the reference design pinout and Table 3 lists the connections to the LaunchPad and the pin mapping. To access the quick start guide for the LAUNCHXL-F28069M including a pins overview, see *TMS320F28069M LaunchPad Development Kit Quick Start Guide*.

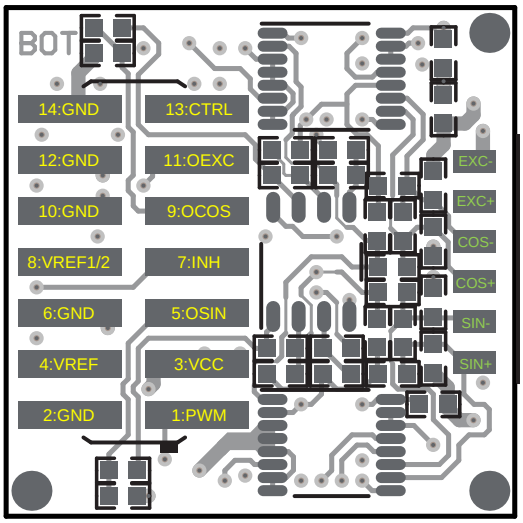



**Figure 20. TIDA-01527 Pinout**

Figure 21 shows a properly-assembled TIDA-01527 reference design with the LaunchPad adapter and LAUNCHXL-F28069M development board.

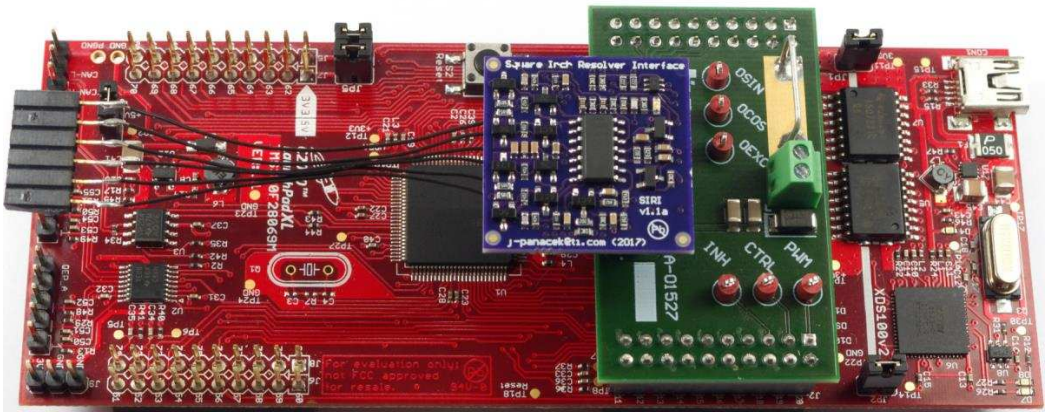



**Figure 21. LAUNCHXL-F28069M Development Board With TIDA-01527 and LaunchPad™ Adapter**

**Table 3. TMS320F28069M Pin Mapping for TIDA-15027 Reference Design**

| SIGNAL | DESCRIPTION | TMS320F28069M (LAUNCHXL PIN) |
|---|---|---|
| PWM | Sine-modulated PWM | EPWM1A (J4 pin 40) |
| GND | Common ground | GND (J2 pin 20, J3 pin 22) |
| VCC | Power supply 12 V to 15 V | Provided externally |
| OSIN | Sinus difference amplifier output | ADCINA0 (J3 pin 27) |
| INH | Analog crossbar inhibit | GPIO02 (J4 pin 38) |
| OCOS | Cosinus difference amplifier output | ADCINB0 (J3 pin 28) |
| OEXC | Excitation amplifier monitoring output | ADCINA1 (J3 pin 29) |
| CTRL | Analog crossbar control | GPIO01 (J4 pin 39) |
| VREF1/2 | Voltage reference 1.24 V | (Optional) ADCINB2 (J3 pin 26) |
| VREF | Voltage reference 2.48 V | (Optional) ADCINA2 (J3 pin 25) |

### 4.1.2 Software

This reference design comes with a complete example software package with a precompiled binary file and source codes. The following software tools were used during development with the LAUNCHXL-F28069M development board.

1. Code Composer Studio v7 with C2000 compiler TI v16.9.1 LTS
2. controlSUITE™ software (optional) – Provides extensive database of schematics, libraries, code examples, and manuals for C2000-based solutions
3. C2000Ware (optional) – A lightweight version of the controlSUITE package

Texas Instruments also offers a set of free-of-charge online development tools at dev.ti.com that can be used for programming the MCU or code modifications.

**NOTE:** For detailed tutorials on how to program, compile, and debug using TI's MCUS, see processors.wiki.ti.com. Alternatively, TI also offers live support within the E2E™ online community.

### 4.1.3 Quick-Start With TIDA-01527

Software:

1. Install the CCS software and import the TIDA-01527 project files using the *File→ Import* menu and then select the *CCS Project*.
2. Connect the C2000 LaunchPad to the PC and make sure that the device drivers have been properly installed.
3. Compile the TIDA-01527 code. The compilation process proceeds with no errors or warnings.
4. Run the code using the *Run→ Debug* menu, then click the *Resume* button. The binary code loads to the MCU. The code then executes, even without the TIDA-01527 connected.
5. Add system variables to the *Expressions* window and activate an automatic refresh. This action enables real-time monitoring and allows for modifications to system variables.

Hardware:

1. Connect the TIDA-01527 board to the LaunchPad using either a flat ribbon cable or the provided adapter board.
2. Connect a resolver to the TIDA-01527 board.
3. Set the laboratory power supply to 14 V with the current limitation set to 100 mA and power the TIDA-01527 board.
4. The light-emitting diode (LED) on the TIDA-01527 board illuminates.
5. Run the software from CCS. Check the resolver waveforms and compare them with the results from *Test Results*.

## 4.2 Testing and Results

### 4.2.1 Test Setup

Figure 22 shows the test setup used during the TIDA-01527 reference design development. The test bench uses the following:

- Keithley 2230-30-1 multiple-output laboratory power supply
- R&S®RTB2004 (Rohde & Schwarz) or Tektronix TDS5054B oscilloscope
- TIDA-00176 reference design with ROD480-1024 Sin/Cos encoder as the reference encoder
- TIDA-01527 reference design (test subject) with LTN58 (R58CURE151B04-021-07AX) resolver

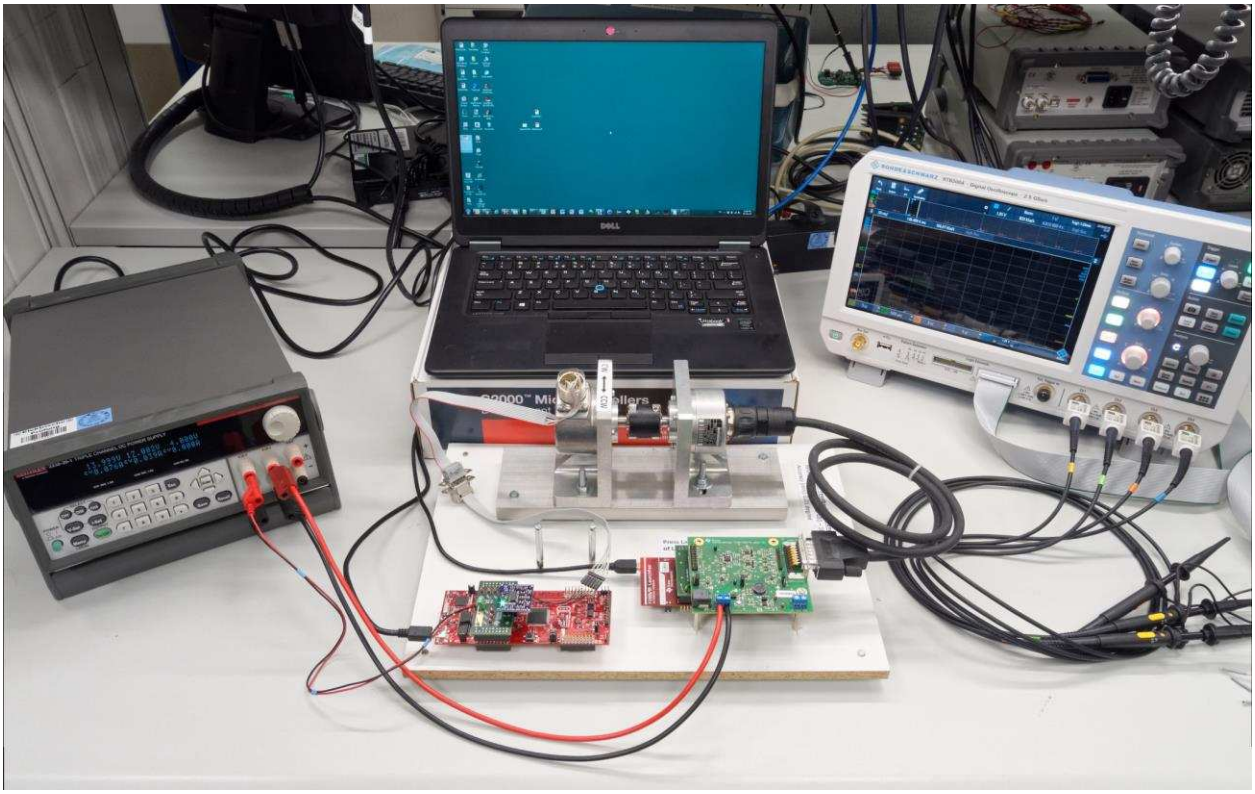
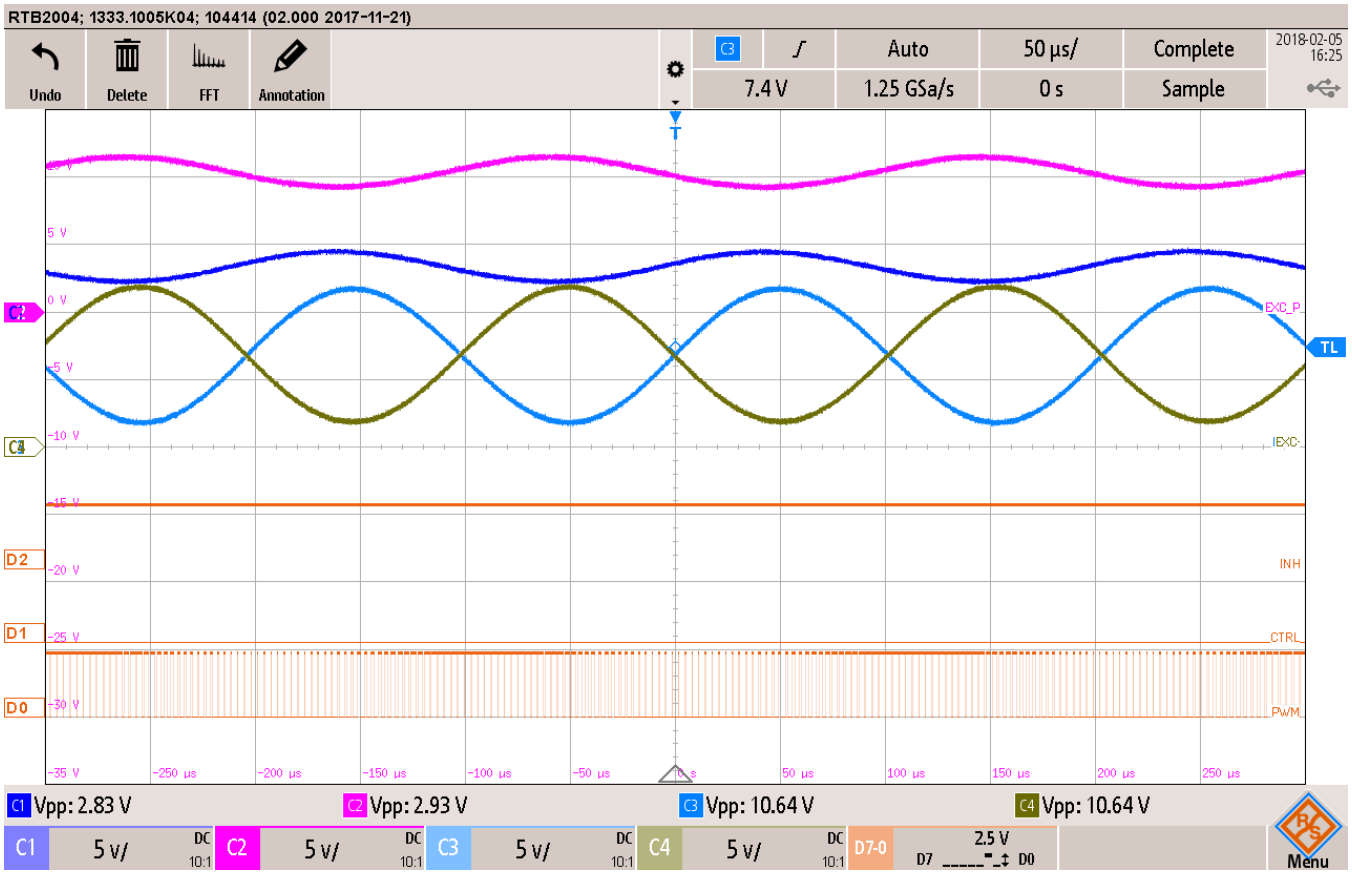


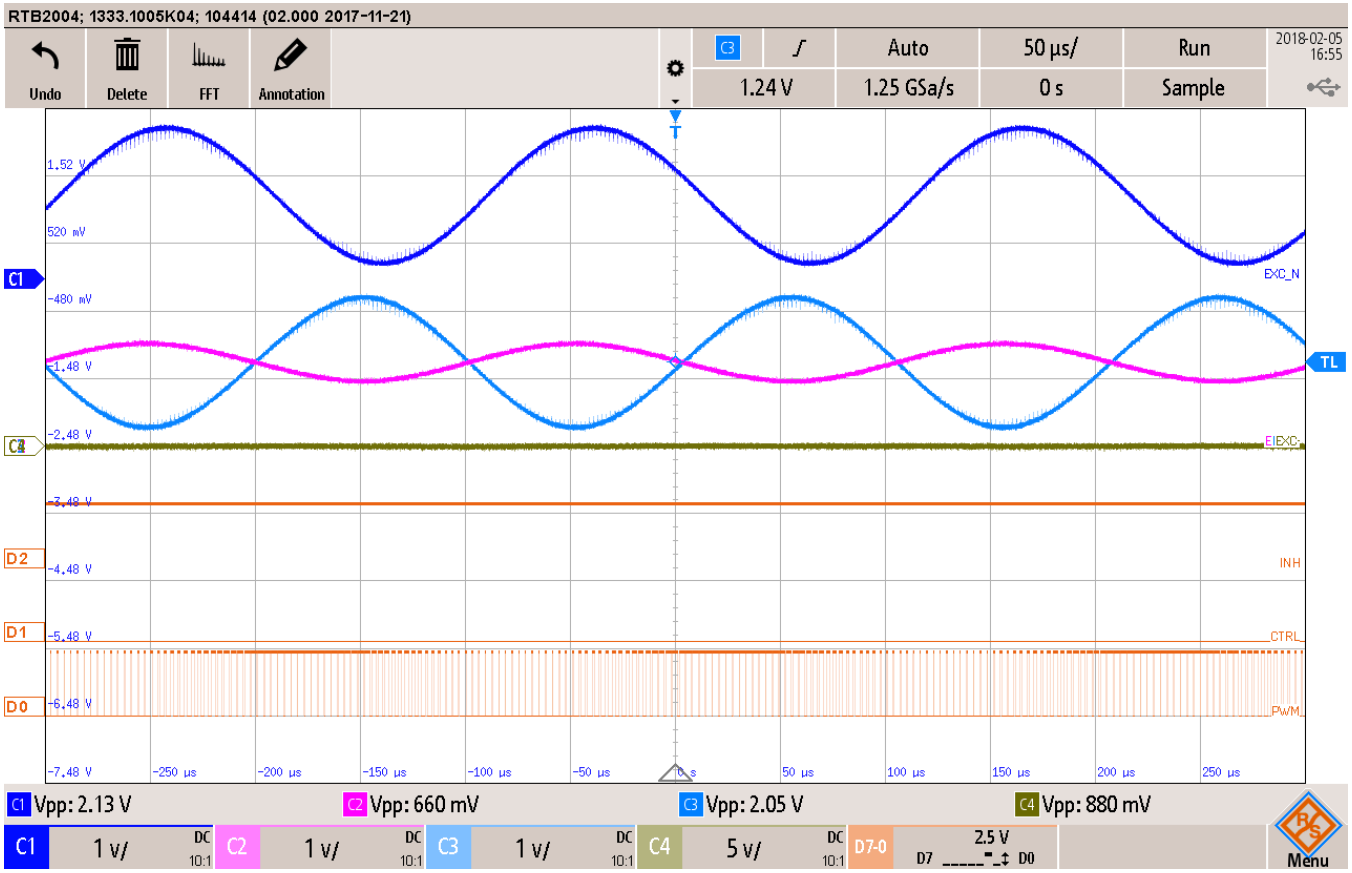
**Figure 22. TIDA-01527 Test Setup Used for Development and Measurements**

### 4.2.2 Test Results



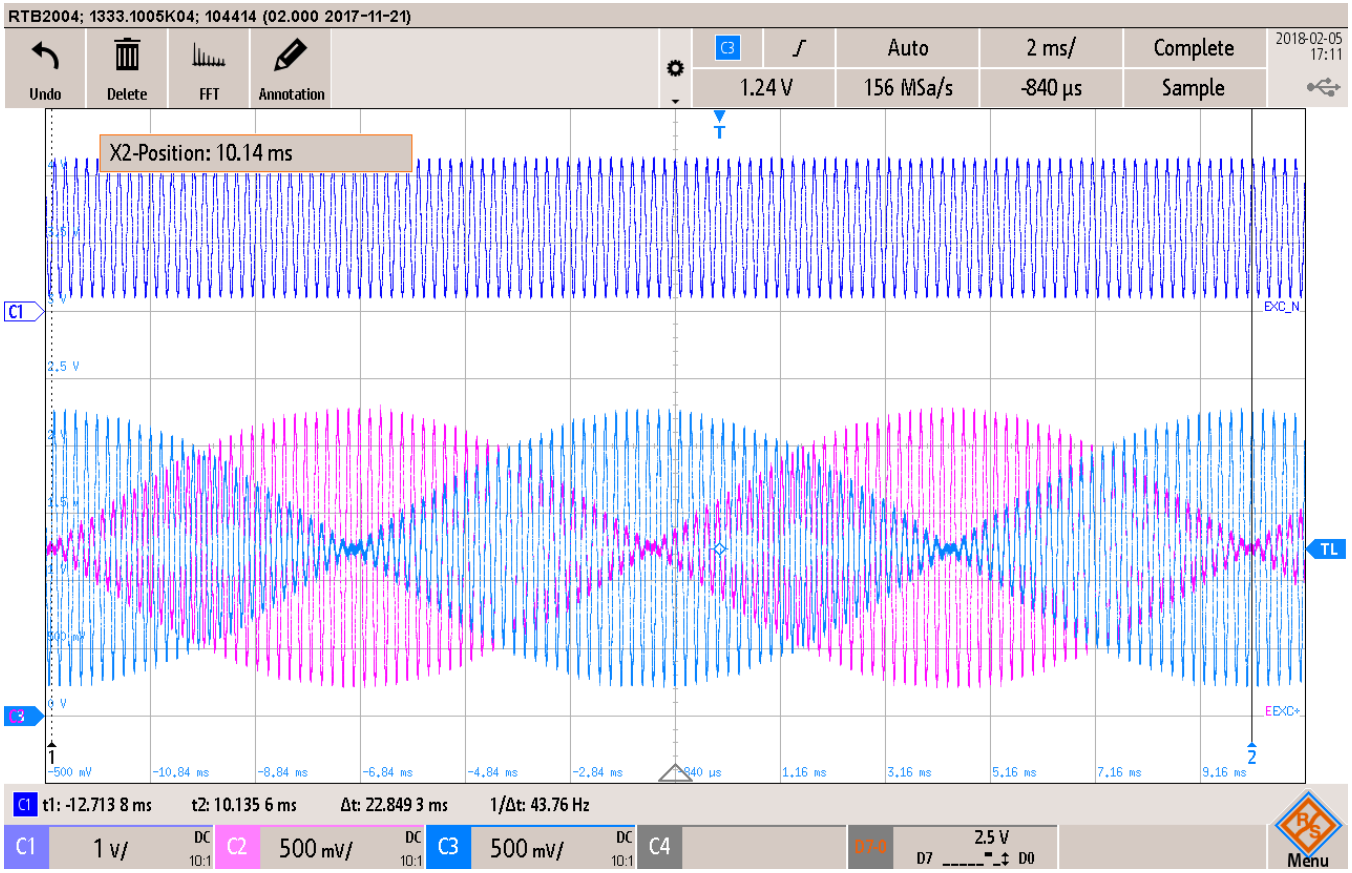

D0 – Input PWM from the C2000 MCU; D1, D2 – Control (CTRL) and Inhibit (INH) signals for the analog crossbar; CH1, CH2 – Generated sine wave after the analog phase-splitter (EXC_N, EXC_P); CH3, Ch4 – Excitation amplifier outputs (EXC+, EXC–)

**Figure 23. Active Low-Pass Filter and Excitation Amplifier Waveforms**



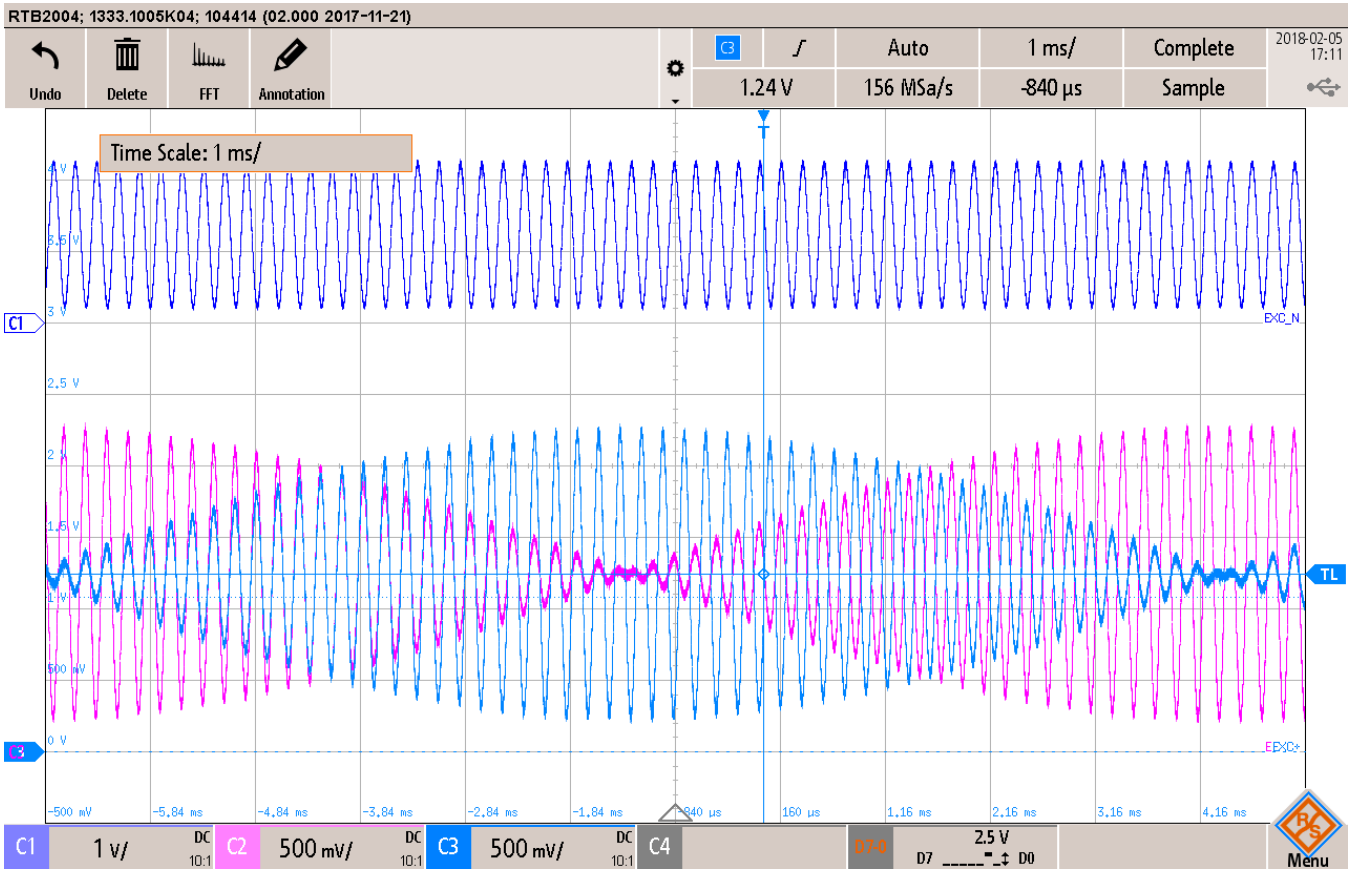

D0 – Input PWM from the C2000 MCU; D1, D2 – Control (CTRL) and Inhibit (INH) signals for the analog crossbar; CH1 – Exciter voltage monitoring (OEXC), CH2 – Sine-winding voltage monitoring (OSIN), CH3 – Cosine winding voltage monitoring (OCOS)

**Figure 24. Analog Front-End Waveforms (Steady Operation)**



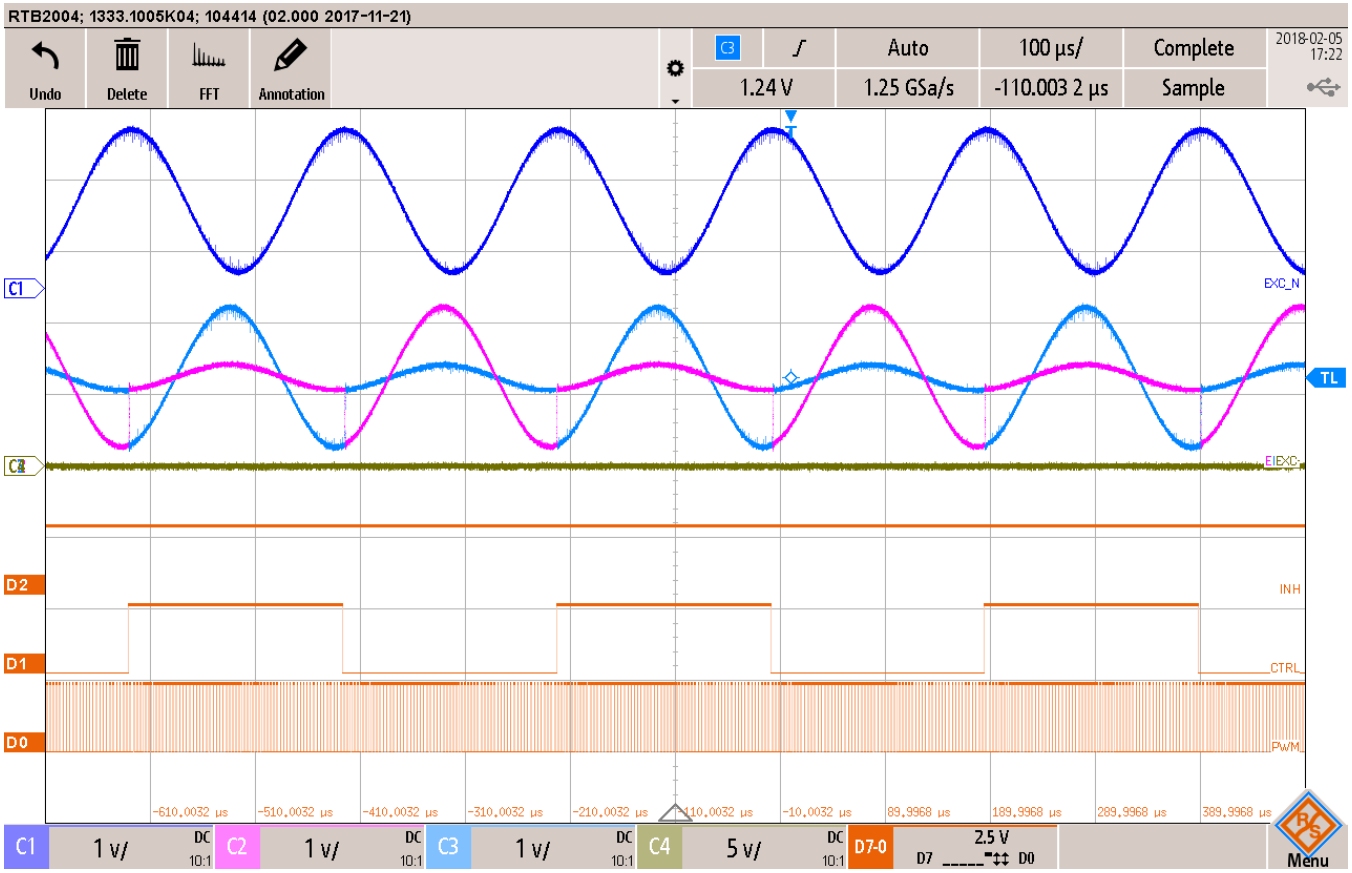

CH1 – Exciter voltage monitoring (OEXC); CH2 – Sine-winding voltage monitoring (OSIN); CH3 – Cosine-winding voltage monitoring (OCOS)

**Figure 25. Analog Front-End Waveforms (Resolver Spins at ≈ 2625 RPM)**




CH1 – Exciter voltage monitoring (OEXC); CH2 – Sine-winding voltage monitoring (OSIN); CH3 – Cosine-winding voltage monitoring (OCOS)

**Figure 26. Analog Front-End Waveforms (Resolver Spins at ≈ 2625 RPM With Detail)**




D0 – Input PWM from the C2000 MCU; D1, D2 - Control (CTRL) and Inhibit (INH) signals for the analog crossbar; CH1 – Exciter voltage monitoring (OEXC), CH2 – Sine-winding voltage monitoring (OSIN); CH3 – Cosine-winding voltage monitoring (OCOS).

Note that the provided example performs offset calibration (step 1) during the start-up and then alternates only to step 2 and step 3.

**Figure 27. Analog Front-End Waveforms With Scattered Signal Processing Enabled**

Figure 28 shows the result of the diagnostic routine described in Section 2.3.7, which finds the right sampling time for the envelope detector. The rising edge on the debug pin GPIO3 represents the OSIN and OCOS sampling, and the falling edge represents the sampling of the OEXC signal.

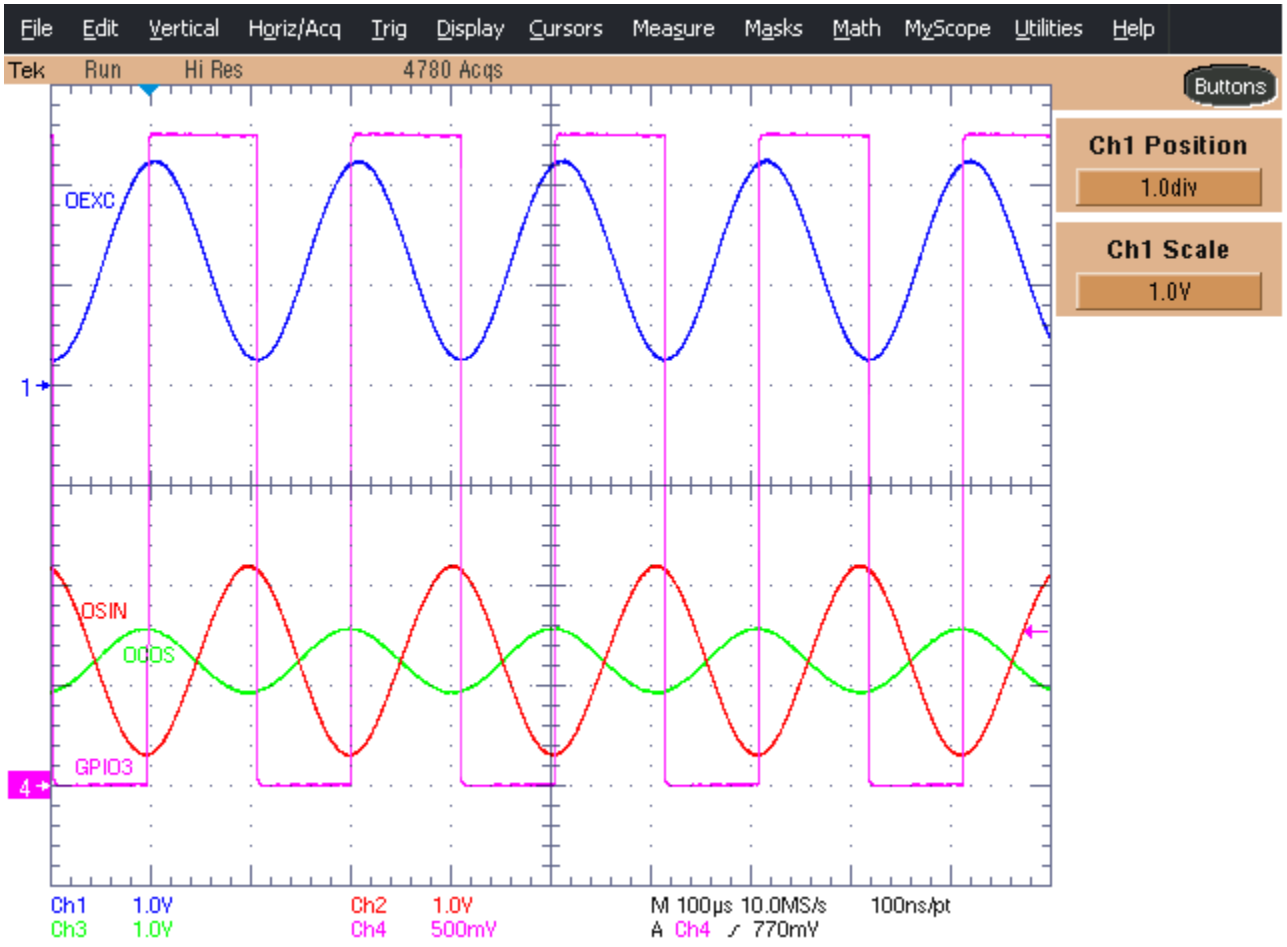



**Figure 28. Sampling Times for OSIN, OCOS, and OEXC Signals**

Figure 29 shows the accuracy plot. Figure 30 and Figure 31 show the same data in a different format.

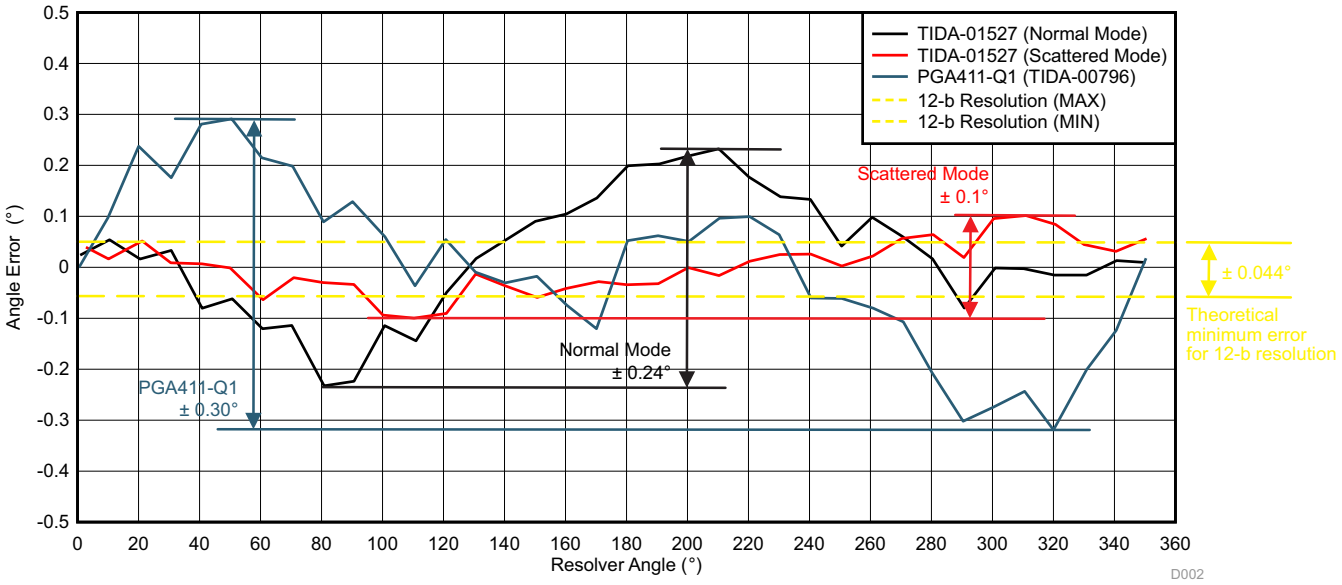



**Figure 29. TIDA-01527 Accuracy Plot**

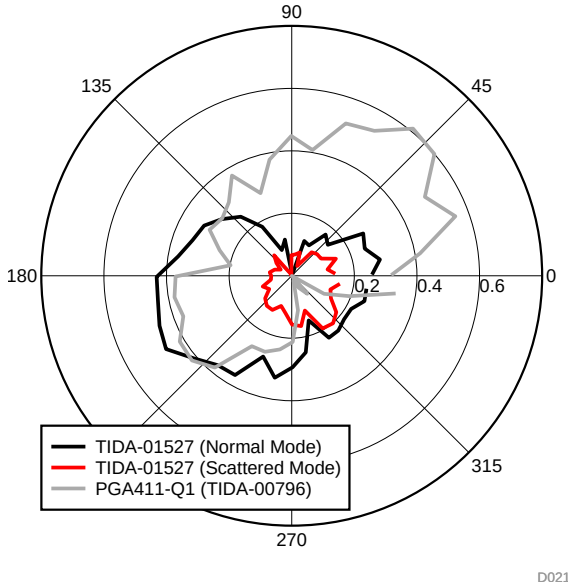



**Figure 30. TIDA-01527 Unity Circle Accuracy Plot (Absolute to Zero)**

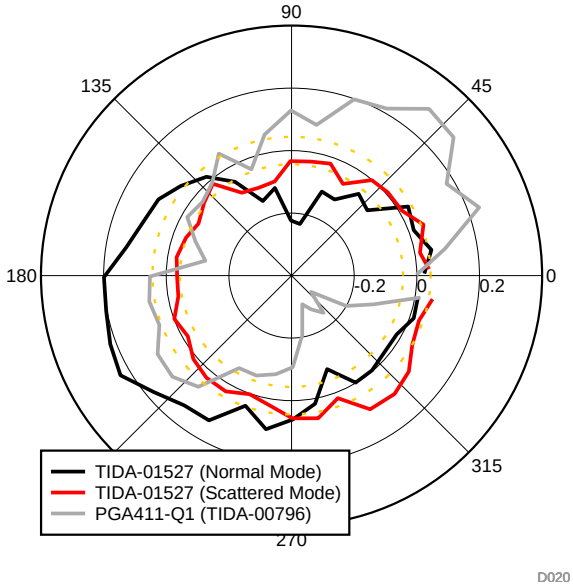



**Figure 31. TIDA-01527 Unity Circle Accuracy Plot**

As mentioned in Section 2.3.1, the system uses the IQ math library in the angle calculation routine. The plot in Figure 32 shows the calculation error due to the finite Q-number resolution. The reference data use RAW results from the ADC with post processing (calculation) in the PC using Microsoft® Excel. The error is negligible and significantly below the system resolution.

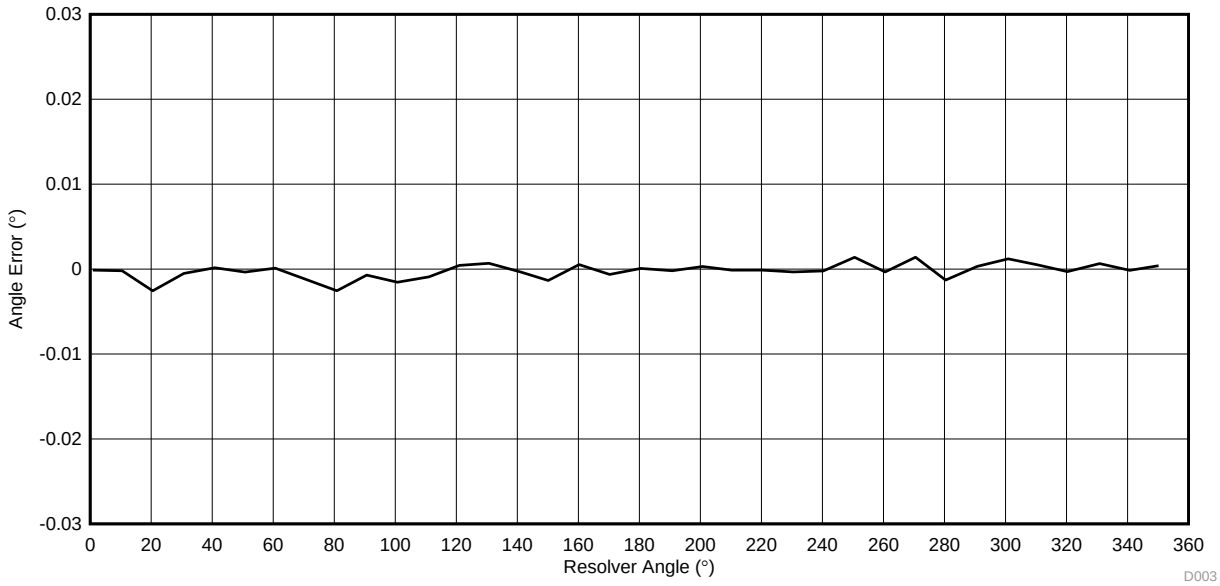



**Figure 32. Effect of Fixed Point IQ-Math Library on Error**

Figure 33 shows a photo from the thermal imaging camera when the TIDA-01527 reference design drives the LTN58 resolver at 5 kHz with a 7-$V_{RMS}$ excitation at a 22°C ambient temperature. Not many options are available for reducing the dissipation of an AB-class amplifier other than lowering voltage drop across and current through the power stage.

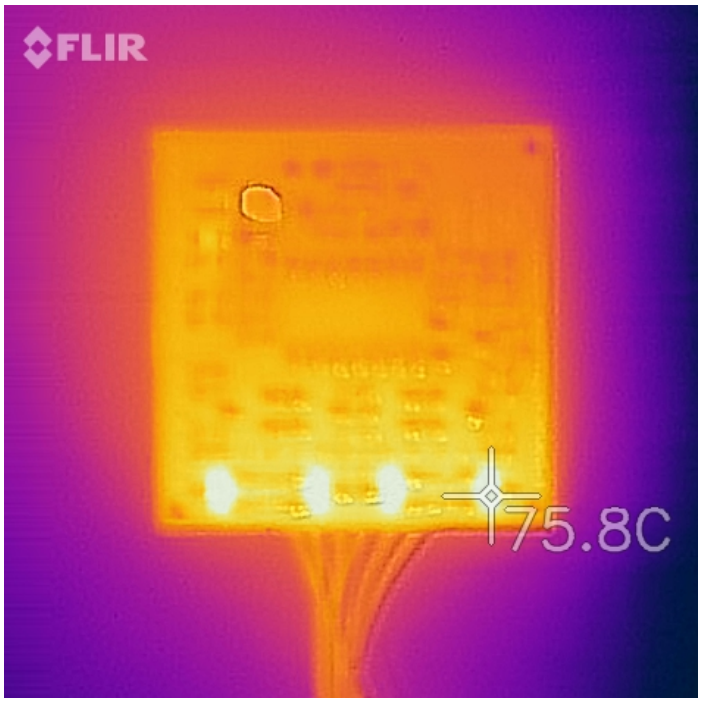



**Figure 33. TIDA-01527 Thermal Imaging Camera Picture**

# 5 Design Files

## 5.1 Schematics

To download the schematics, see the design files at TIDA-01527.

## 5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01527.

## 5.3 PCB Layout Recommendations

The design does not require any special PCB layout considerations. The TIDA-01527 uses a four-layer PCB with double-side component placement. The top side (Figure 34) primarily carries circuitry for the excitation amplifier and voltage references. Signal conditioning amplifiers for the resolver secondary windings and the system connector are located on the bottom side (Figure 35). The other two internal layers (Figure 36 and Figure 37) carry the power, ground, and signals, too.

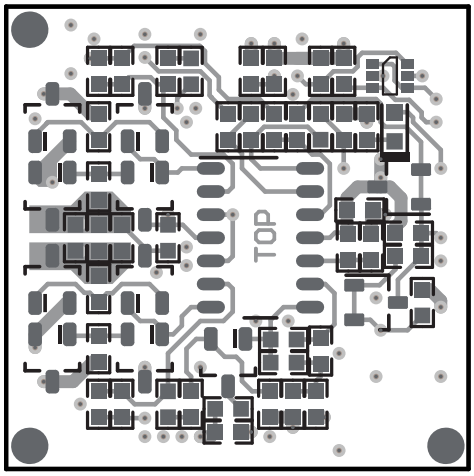



**Figure 34. Top PCB Side and Components Placement**

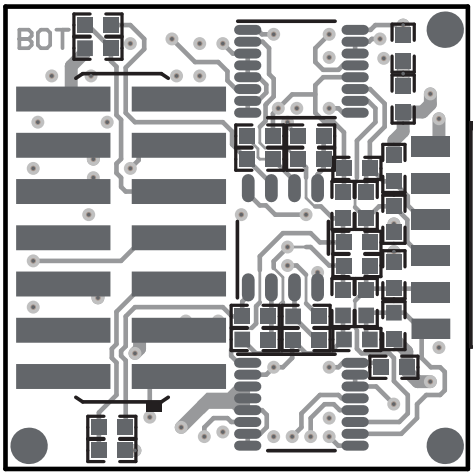



**Figure 35. Bottom PCB Side and Components Placement**

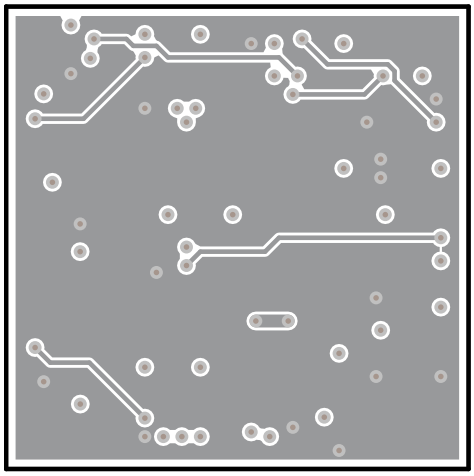


**Figure 36. Internal Layer 1 With Common Ground GND and Signals**

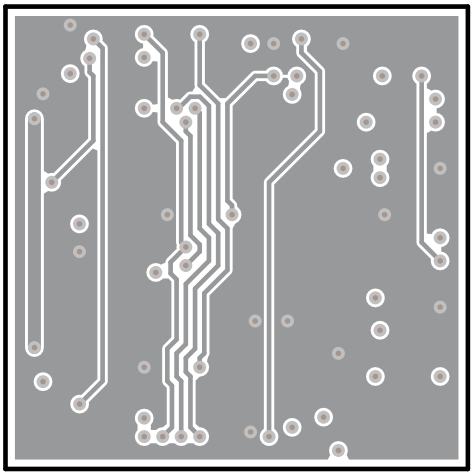


**Figure 37. Internal Layer 2 With Power Rail VCC and Signals**

### 5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01527.

## 5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01527.

## 5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01527.

## 5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01527.

# 6 Software Files

To download the software files, see the design files at TIDA-01527.

# 7 Related Documentation


1. Texas Instruments, *TLVx171-Q1 36-V, Single-Supply, General-Purpose Operational Amplifier for Cost-Sensitive Automotive Systems Data Sheet*
2. Texas Instruments, *TLV431x-Q1 Low-Voltage Adjustable Precision Shunt Regulator Data Sheet*
3. Texas Instruments, *TMS320F2806x Piccolo™ Microcontrollers Data Manual*
4. Texas Instruments, *Automotive Resolver-to-Digital Converter for Safety Applications Design Guide*
5. Texas Instruments, *EMC Compliant Single-Chip Resolver-to-Digital Converter (RDC) Reference Design*
6. Texas Instruments, *Reduce system costs with resolver-to-digital conversion implementation on C2000™ microcontrollers (white paper)*
7. Texas Instruments, *TMS320F240 DSP Solution for Obtaining Resolver Angular Position and Speed Application Note*
8. Texas Instruments, *C28x IQmath Library Module User's Guide*
9. (2004) *Synchro and Resolver Engineering Handbook* . Moog Components Group. Retrieved from http://www.moog.com/literature/MCG/synchrohbook.pdf


## 7.1 Trademarks



# 8 Glossary

**ADC—** Analog-to-digital converter

**CCS—** Code Composer Studio™

**CLA—** Control law accelerator

**ESD—** Electrostatic discharge

**EV—** Electric vehicle

**HEV—** Hybrid-electric vehicle

**HRPWM—** High-resolution pulse width modulator

**LED—** Light-emitting diode

**MCU—** Microcontroller

**Op Amp—** Operational amplifier

**PCB—** Printed-circuit board

**PWM—** Pulse-width modulation

**RMS—** Root mean square

## 9 About the Author

**JIRI PANACEK** is a systems engineer in the Powertrain Automotive Systems team at Texas Instruments where he develops reference designs. Jiri has five years of field experience in the industrial automation and most recently the EV/HEV automotive segment. Jiri earned his master's degree in microelectronics from the Brno University of Technology in the Czech Republic.

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