TI Designs: TIDA-01416
Small, Efficient, Flexible Power Supply Reference Design for NXP™ i.MX7 Series Application Processors

Description

This small, efficient and flexible power supply reference design demonstrates a complete power solution for NXP™ i.MX7 processors. This simple solution uses just five DC/DC converters and one sequencer integrated circuit (IC) to power the i.MX7 in a very cost-effective design. This reference design supports numerous industrial applications and any application that requires a small, high-efficiency, flexible power supply solution.

Resources

TIDA-01416	Design Folder
TLV62080, TLV62084A	Product Folder
TLV62085	Product Folder
LM3880	Product Folder

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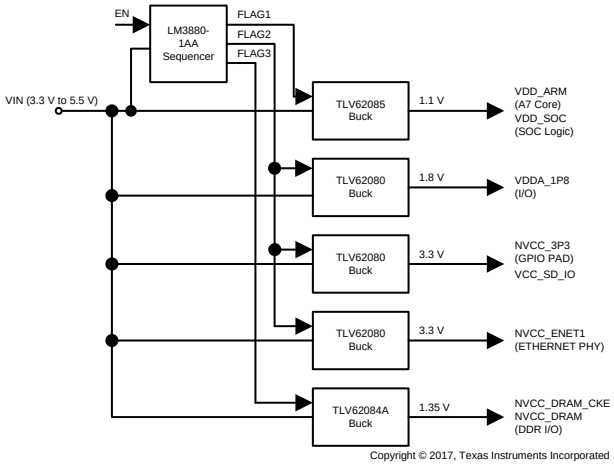
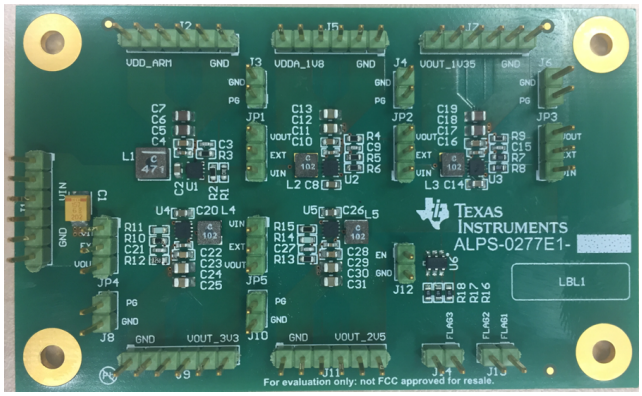
Features

- 3.3-V to 5.5-V Input Voltage Range
- DCS-Control™ Topology for Fast Transient Response
- High Efficiency and Low Quiescent Current
- Automatic Power Save Mode for Light Load Efficiency
- TLV6208x Family Approach for Low-Cost Solutions

Applications

- Appliances
- Test and Measurement
- Electronic Point of Sale
- Internet of Things





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1 System Description

The i.MX7 series application processor from NXP is a highly-integrated, multi-market applications processor designed to enable various applications. This TIDA-01416 reference design provides a scalable power solution for several i.MX7 processor versions supporting space-constrained and cost-sensitive systems. The power architecture follows the source material in *i.MX 7Dual Family of Applications Processors Datasheet*. A 1.1-V rail is required for the core and system on chip (SoC), a 1.8-V rail for the input/output (I/O) pads, a 3.3-V rail for I/O and SD card pads, a 3.3-V rail for Ethernet controller, and a 1.35-V rail for DDR3 I/O pad supply.

This reference design achieves high efficiency by using efficient, integrated DC/DC converters and no low dropout (LDO) linear regulators. High efficiency results in a low self-temperature rise and higher reliability.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER		SPECIFICATIONS	DETAILS
Input voltage range		3.3 V to 5.5 V	—
OUTPUTS PROVIDED			
VDD_ARM, VDD_SOC	Voltage setpoint	1.1 V	Section 3.1.1
	Ripple	< 20 mV	
	Transient response	< 5%	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4%	
VDDA_1P8	Voltage setpoint	1.8 V	Section 3.1.2
	Ripple	< 25 mV	
	Transient response	< 5%	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4 %	
NVCC_3P3, NVCC_ENET1	Voltage setpoint	3.3 V	Section 3.1.3
	Ripple	< 20 mV	
	Transient response	< 5 %	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4 %, V_{IN} > 3.3 V	
NVCC_DRAM	Voltage setpoint	1.35 V	Section 3.1.4
	Ripple	< 20 mV	
	Transient response	< 5%	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4%, V_{IN} > 3.3 V	
Efficiency (each regulator at half of its rated load)		—	Section 3.1.1, Section 3.1.2, Section 3.1.3, Section 3.1.4
Efficiency (each regulator at its full rated load)		—	Section 3.1.1, Section 3.1.2, Section 3.1.3, Section 3.1.4
Sequencing order (power up)		1. VDD_ARM and VDD_SOC; 2. VDDA_1P8, NVCC_3P3, NVCC_SD_IO, and NVCC_ENET1; 3. NVCC_DRAM_CKE	Section 3.1.5
Sequencing order (power down)		1. NVCC_DRAM_CKE; 2. VDDA_1P8, NVCC_3P3, and NVCC_SD_IO; 3. VDD_ARM and VDD_SOC	

2 System Overview

2.1 Block Diagram

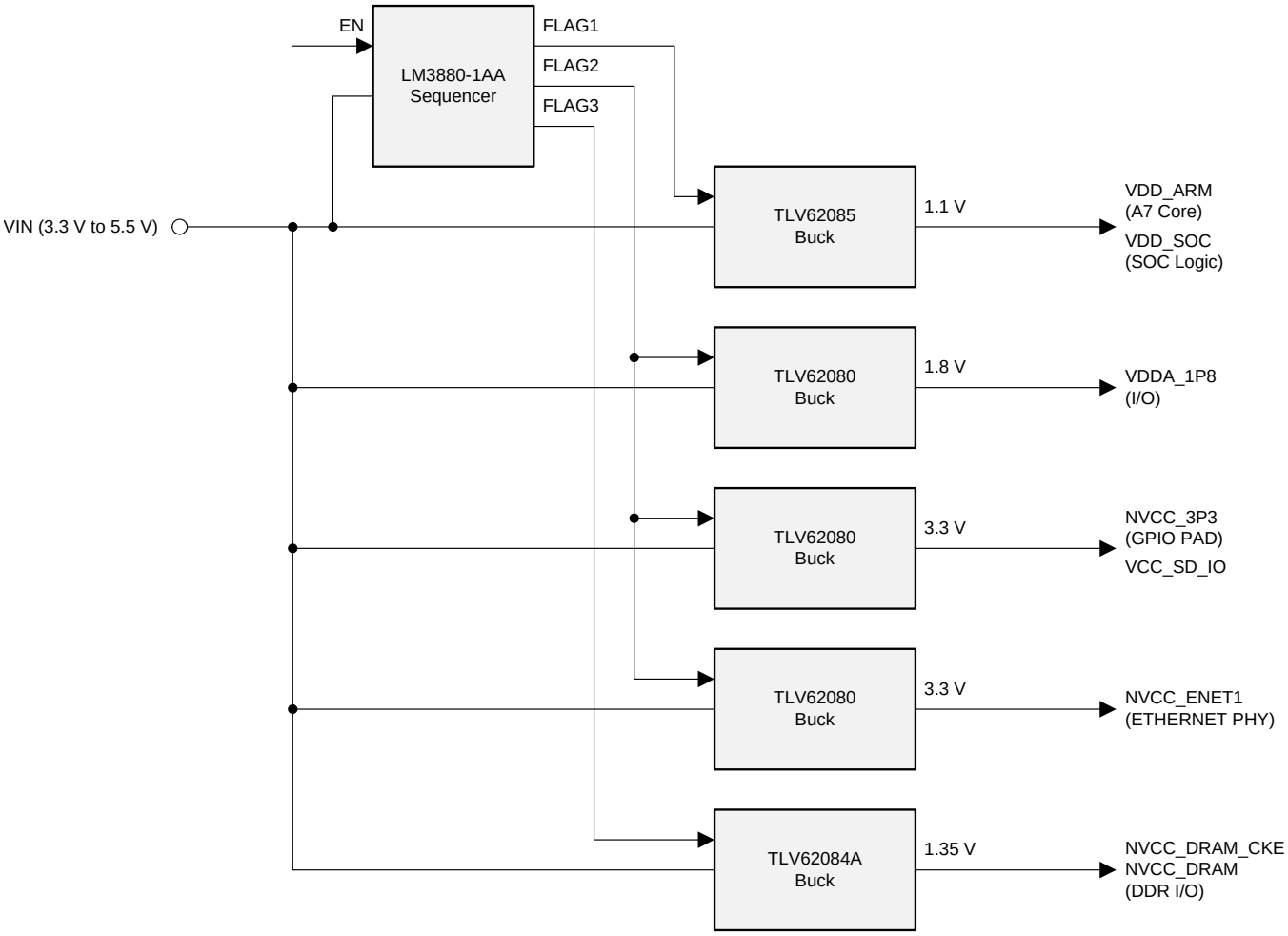

Figure 1. Block Diagram

2.2 Highlighted Products

2.2.1 TLV62085

The TLV62085 is a 3-A, high-frequency, synchronous step-down converter optimized for small solution size and high efficiency. At medium to heavy loads, the converter operates in pulse-width modulation (PWM) mode and automatically enters power save mode operation at light load to maintain high efficiency over the entire load current range. Its DCS-Control™ topology (**D**irect **C**ontrol with **S**eamless transition into power save mode) enables a very-fast transient response to regulate the output voltage during heavy load changes, while its high switching frequency enables the use of a small inductor and output capacitor.

2.2.2 TLV62080, TLV62084A

The TLV6208x family of devices are small buck converters with few external components that enable cost-effective solutions. The 1.2-A (TLV62080) and 2-A (TLV62084A) synchronous step-down converters provide high-efficiency over a wide output current range. At medium to heavy loads, the TLV6208x converters operate in PWM mode and automatically enter power save mode operation at light-load currents to maintain high efficiency over the entire load current range. With DCS-Control architecture, excellent load transient performance and output voltage regulation accuracy are achieved.

2.2.3 LM3880

The LM3880 Simple Power Supply Sequencer offers the easiest method to control power-up sequencing and power-down sequencing of multiple independent voltage rails. The LM3880 contains a precision enable pin and three open-drain output flags. When the LM3880 is enabled, the three output flags sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags follow a reverse sequence during power down when the enable pin is pulled down.

2.3 System Design Theory

The application processor power requirements are a function of the specific functionality used in a given application. In most cases, the current drawn by each rail is not known precisely during the design phase. Only gross estimates are available when the power supply is designed. For this reason, this reference design uses DC/DC converters that are high enough power to support the majority of i.MX7 applications, while still supplying a small solution size and high efficiency. Use 2-A converters to provide the 1.8-V and 3.3-V I/O rails and a 3-A converter for the common 1.1-V core and SoC rail. The output voltages of the converter are adjustable with external resistor feedback dividers.

The i.MX7 application processor only requires a simple sequencing of the power rails. VDD_SOC must be stable before NVDCC_DRAM and NVDCC_DRAM_CKE start to ramp. For down sequencing, first NVCC_DRAM and NVDCC_DRAM_CKE must be powered down before VDD_SOC is disabled. Though no specific sequencing is required for the other rails, this reference design also applies a controlled sequencing of the other rails to reduce the inrush current drawn from the input source, as well as to provide a controlled system start-up. The LM3880-1AA Simple Sequencer starts VDD_SOC and VDD_ARM first; then VDD_1P8, NVCC_3P3 VCCA, and NVCC_ENET1 second; and then finally, the 1.35-V converter (NVCC_DRAM_CKE and NVCC_DRAM rail). This reference design uses the 1AA version of LM3880, which provides a sequencing power-up order of FLAG1, FLAG2, and FLAG3 with a delay time (t_{DELAY}) of 10 ms. Power-up sequencing starts when the enable pin of the LM3880 device is pulled high and power-down sequencing starts when the enable pin is pulled low (see Figure 2). An external enable signal must be applied at jumper J12, such as from a microcontroller (MCU) or signal generator.

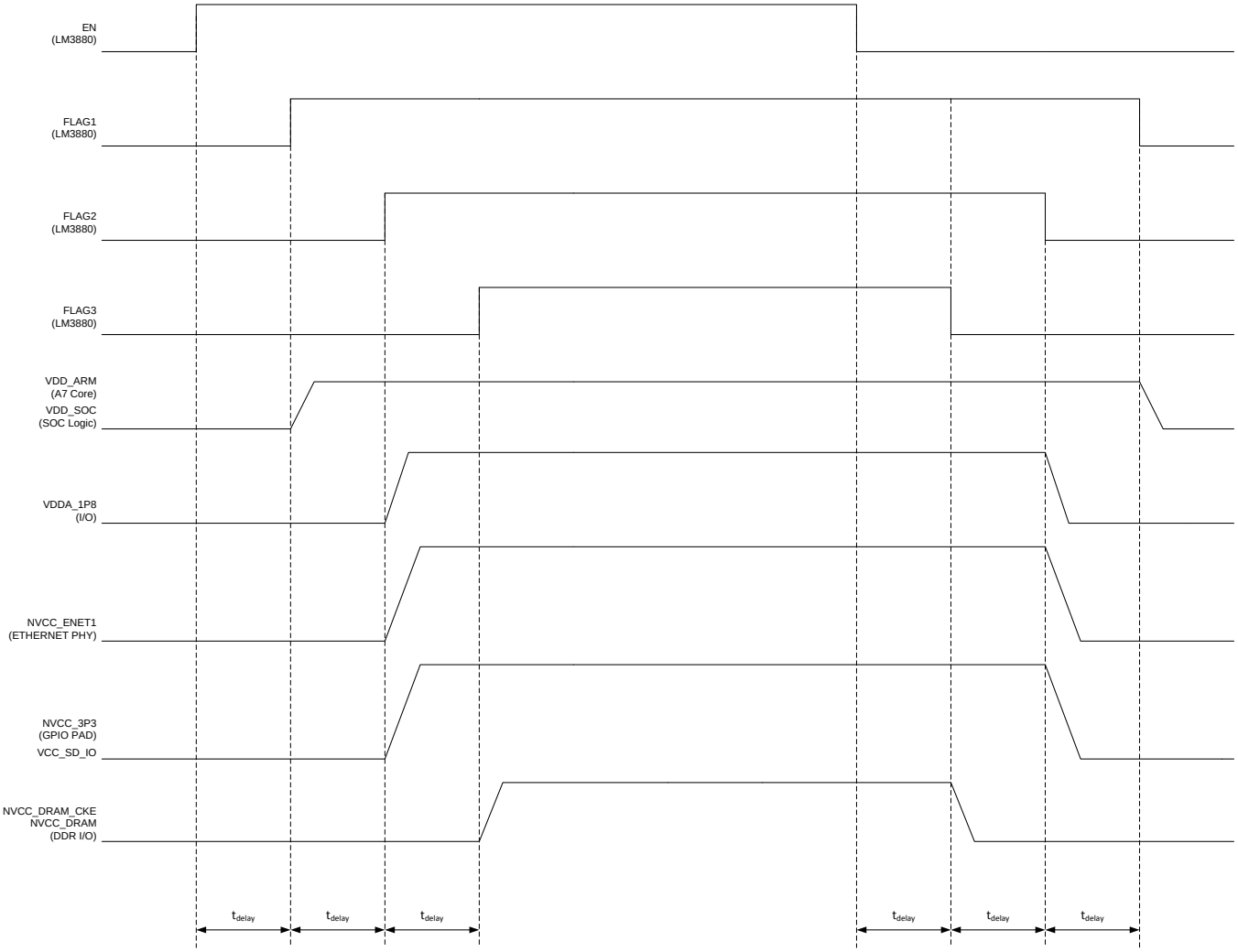

Figure 2. Power Sequencing

3 Hardware, Software, Testing Requirements and Test Results

To test this reference design, apply an input voltage (typically 3.6 V) to the J1 input connector. Apply an enable signal to jumper J12 with a signal generator to initiate the power-up sequencing of the output rails. For the high level, apply at least 1.4 V (maximum level is V_{IN}); for the low level, apply less than 1.0 V.

3.1 Testing and Results

This section includes the relevant test results to power the i.MX7 application processor. Unless otherwise noted, all testing was conducted with 3.6 V_{IN} and at room temperature.

3.1.1 VDD_ARM, VDD_SOC

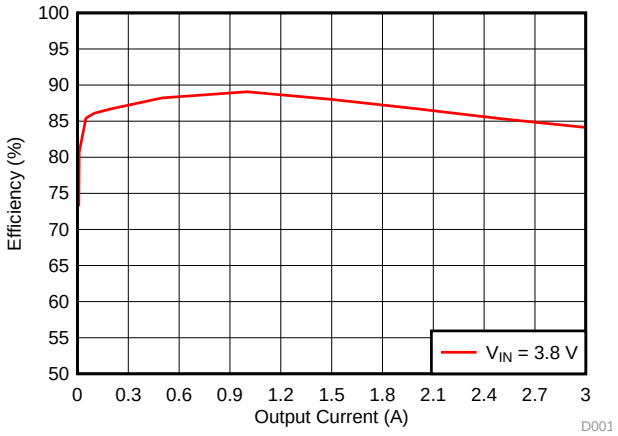

Figure 3. VDD_ARM, VDD_SOC Efficiency (3.8 V_{IN})

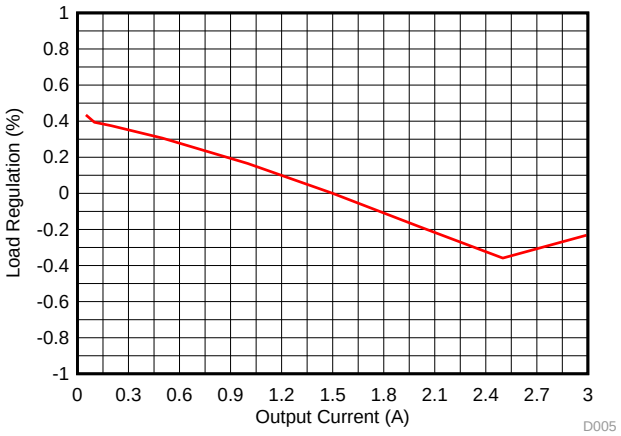

Figure 4. VDD_ARM, VDD_SOC Load Regulation (3.8 V_{IN})

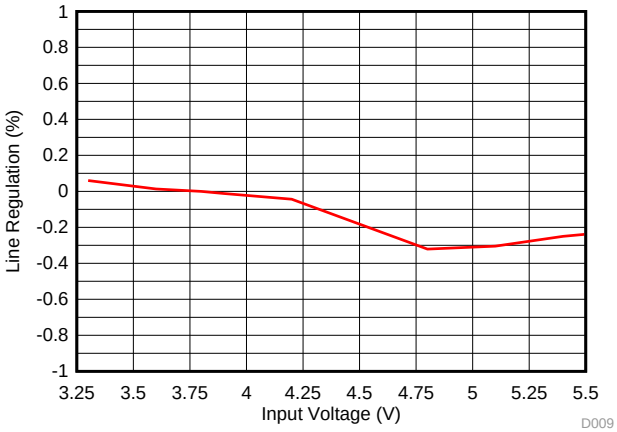

Figure 5. VDD_ARM, VDD_SOC Line Regulation (3-A Load)

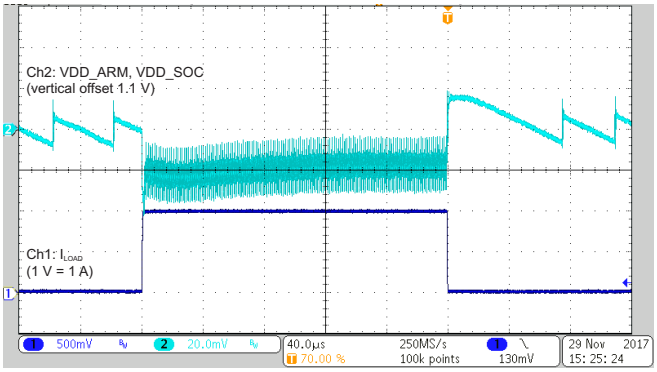

Figure 6. VDD_ARM, VDD_SOC Transient Response (V_{IN} = 3.8 V, 10-mA to 2-A Load Step)

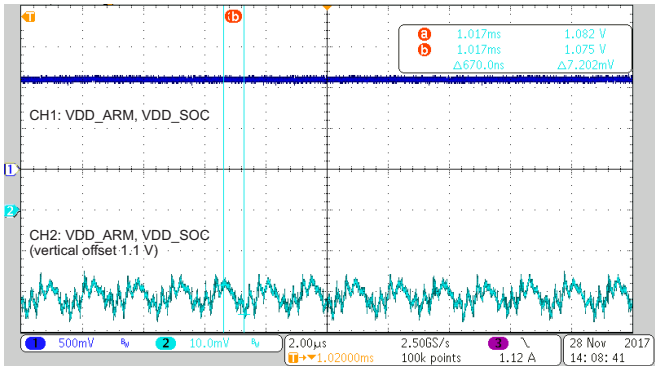

Figure 7. VDD_ARM, VDD_SOC Ripple (V_{IN} = 3.8 V, 3-A Load)

3.1.2 VDDA_1P8

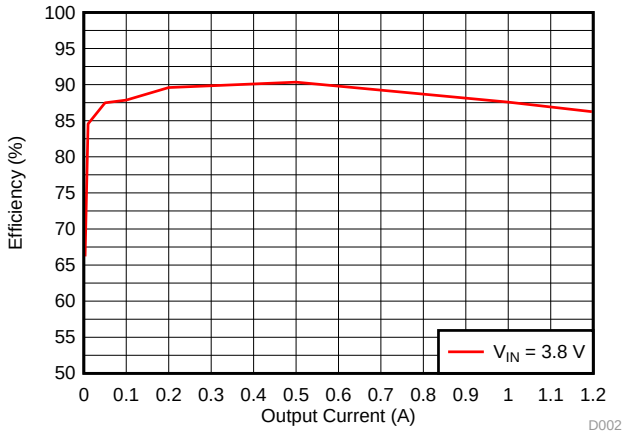

Figure 8. VDDA_1P8 Efficiency (3.8 V_{IN})

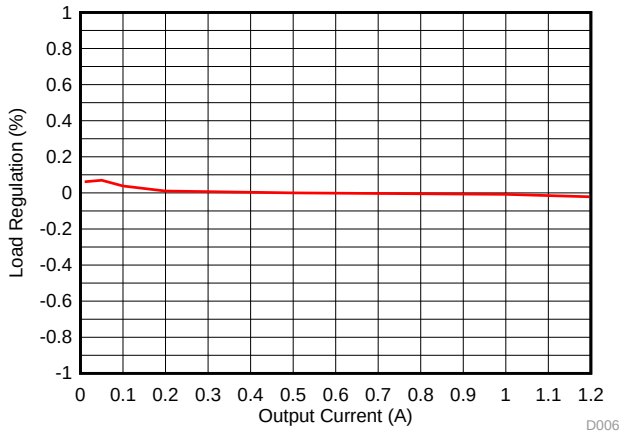

Figure 9. VDDA_1P8 Load Regulation (3.8 V_{IN})

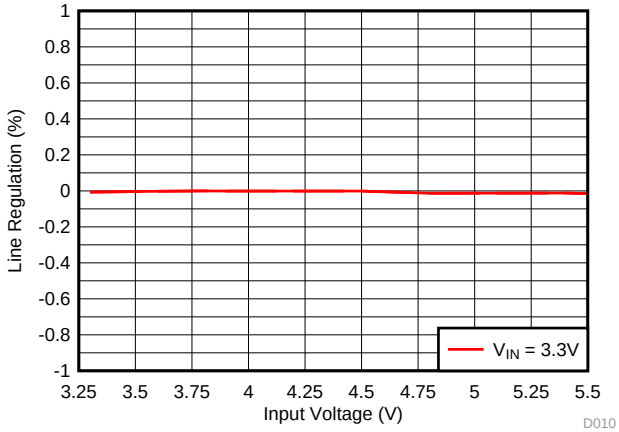

Figure 10. VDDA_1P8 Line Regulation (1.2-A Load)

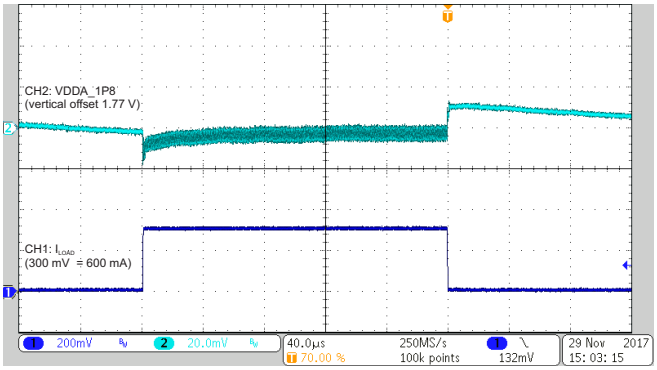

Figure 11. VDDA_1P8 Transient Response (V_{IN} = 3.8 V, 1-mA to 600-mA Load Step)

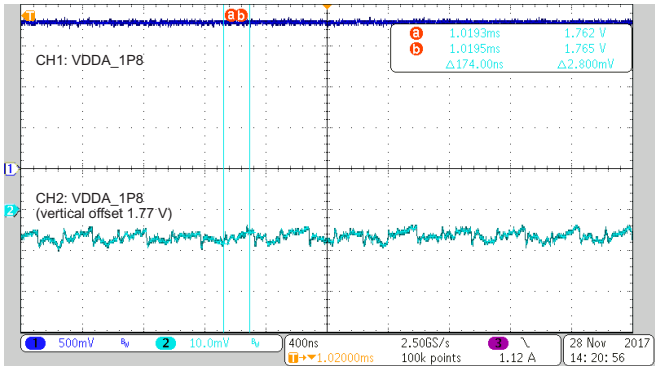

Figure 12. VDDA_1P8 Ripple (V_{IN} = 3.8 V, 1.2-A Load)

3.1.3 NVCC_3P3

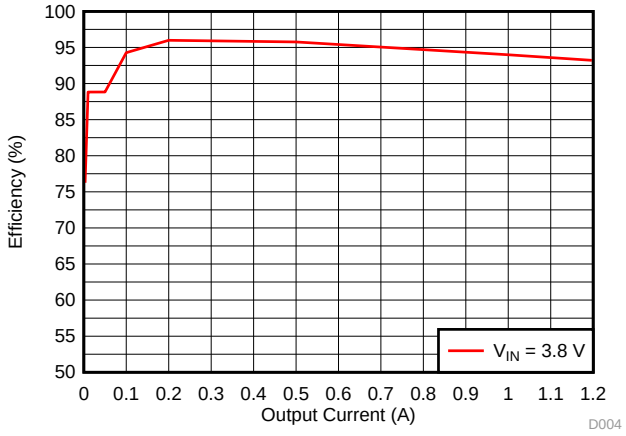

Figure 13. NVCC_3P3 Efficiency (V_{IN} = 3.8 V)

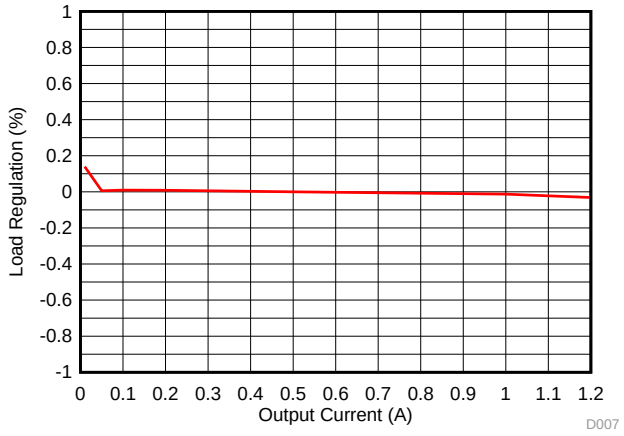

Figure 14. NVCC_3P3 Load Regulation (V_{IN} = 3.8 V)

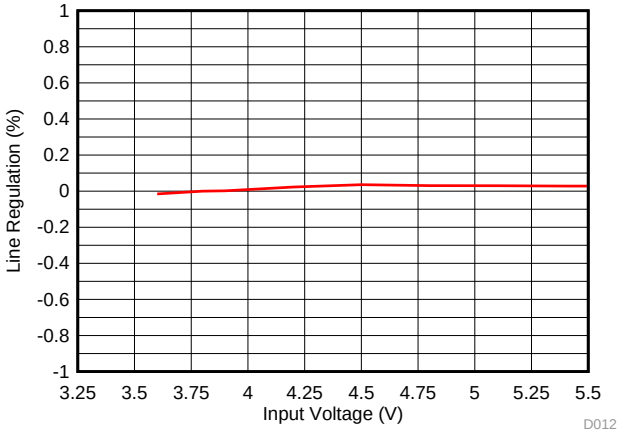

Figure 15. NVCC_3P3 Line Regulation (1.2-A Load)

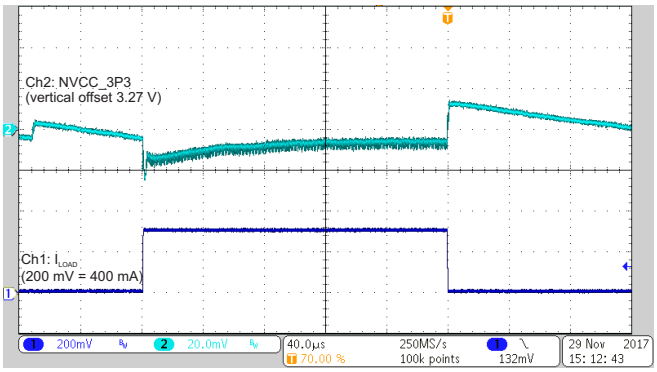

Figure 16. NVCC_3P3 Transient Response (V_{IN} = 3.8 V, 1-mA to 600-mA Load Step)

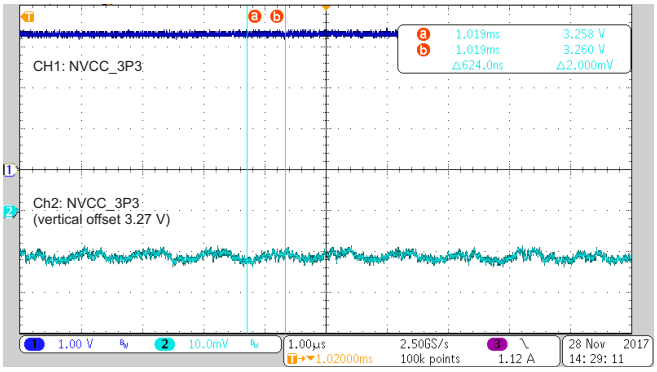

Figure 17. NVCC_3P3 Ripple (V_{IN} = 3.8 V, 1.2-A Load)

3.1.4 NVCC_DRAM

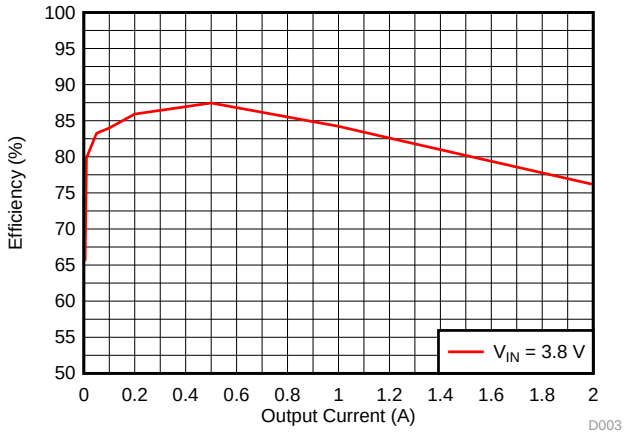

Figure 18. NVCC_DRAM Efficiency (V_{IN} = 3.8 V)

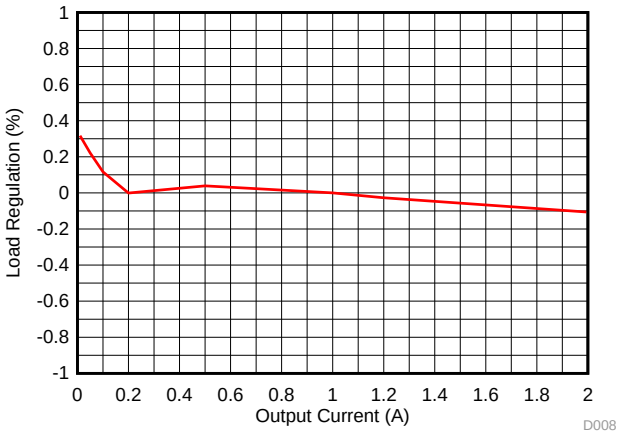

Figure 19. NVCC_DRAM Load Regulation (V_{IN} = 3.8 V)

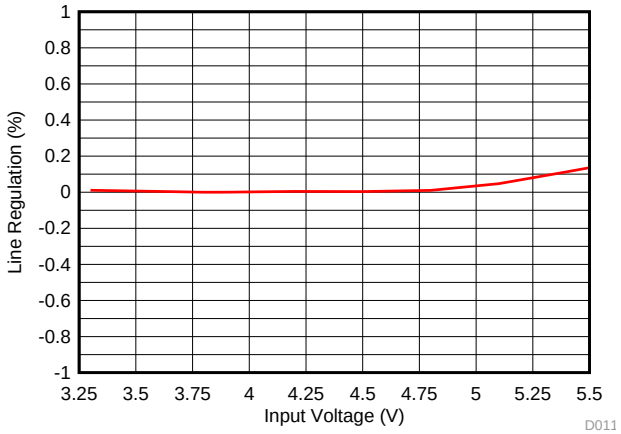

Figure 20. NVCC_DRAM Line Regulation (2-A Load)

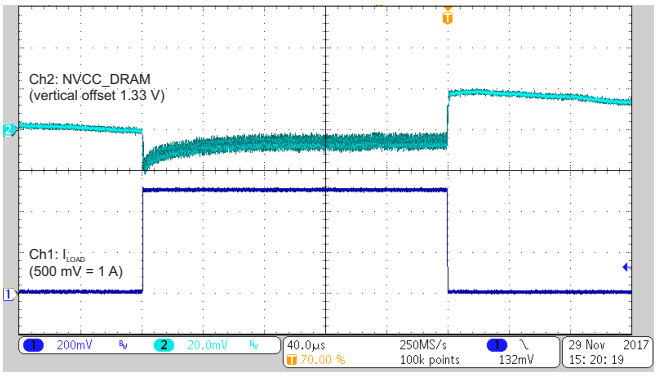

Figure 21. NVCC_DRAM Transient Response (V_{IN} = 3.8 V, 1-mA to 1-A Load Step)

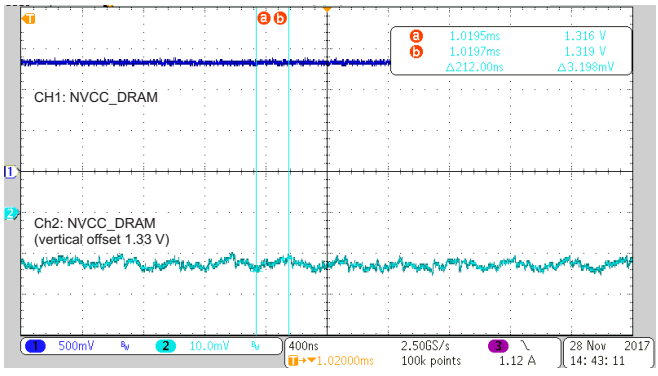

Figure 22. NVCC_DRAM Ripple (V_{IN} = 3.8 V, 2-A Load)

3.1.5 System Power Up and Power Down

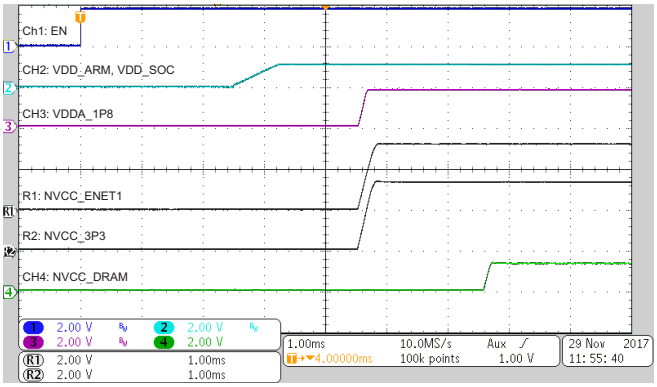

Figure 23. Power Up (V_{IN} = 3.8 V, No Load)

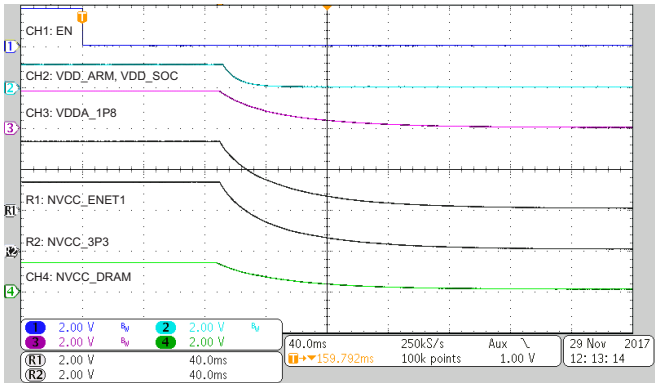

Figure 24. Power Down (V_{IN} = 3.8 V, No Load)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01416.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01416.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01416.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01416.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01416.

5 Related Documentation

1. NXP, *i.MX 7Dual Family of Applications Processors Datasheet*
2. Texas Instruments, *High Efficiency 3-A Step-Down Converterin 2-mm×2-mm VSON Package*
3. Texas Instruments, *1.2-A and 2-A High-Efficiency Step-Down Converter in 2-mm×2-mm WSON Package*
4. Texas Instruments, *Simple Power Sequencer*
5. Texas Instruments, *High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions*

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