Design Guide: TIDA-01413

ADAS 8-Channel Sensor Fusion Hub Reference Design With Two 4-Gbps Quad Deserializers

Description

This sensor fusion hub reference design allows the connection of up to four 2-megapixel cameras and up to four radar modules over coaxial cable. This design utilizes these coaxial cables to provide power, back-channel communication, and clock synchronization to the sensors. The two 4-Gbps FPD-Link III quad deserializers support dual-outputs of the Mobile Industry Processor Interface (MIPI) Camera Serial Interface-2 (CSI-2) over a Samtec connector to application processors.

Resources

TIDA-01413		Design Folder
DS90UB960-Q1	LM74610-Q1	Product Folders
LM5141-Q1	LM5121-Q1	Product Folders
TPS65263-Q1	TPS25940-Q1	Product Folders
HD3SS3411-Q1	TS3USB221A-Q1	Product Folders
MSP430F2272		Product Folders

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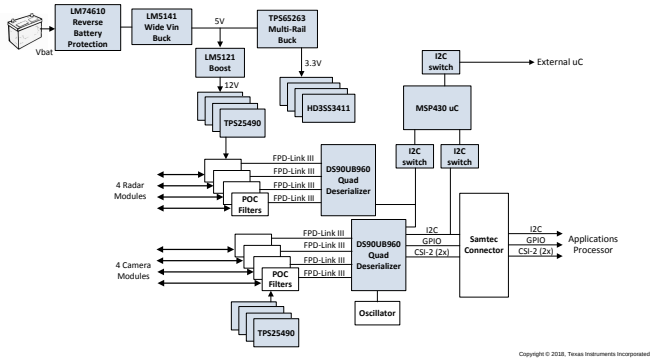
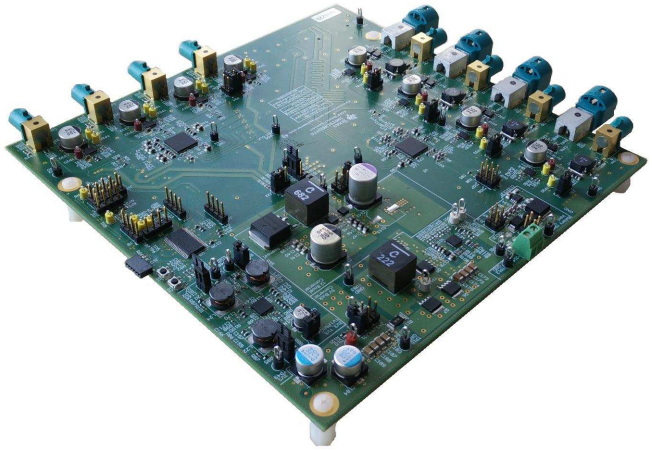
Features

- Accepts 8 High-Speed Data Inputs Over FPD-Link III Synchronization Capability
- Provides Wide-Range Supply Voltage for Power Over Coax (4 V to 14 V)
- Directly Connects to TDA2Plus EVM Through CSI-2 Interface
- Car Battery can Directly Supply Board Power With Protection From Reverse Current
- Utilizes MSP430™ Microcontroller (MCU) to Initialize and Configure Video Pipeline
- Design Compatible With Onboard MCU, Without MCU, or With External MCU
- Works With Any Camera That Uses Compatible FPD-Link III DS90UB953 Serializer

Applications

- Advanced Driver Assistance Systems (ADAS)
- Surround View
- CMS and Mirror Replacement
- ADAS Domain Controller





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1 System Overview

1.1 System Description

For many automotive ADAS and self-driving car systems, multiple sensors are required. This TI-Design addresses these needs by combining the outputs from up to eight sensors such as Megapixel Imagers, RADAR and LIDAR sensors into two digital MIPI CSI-2 output ports. These ports are available on an external connector that can attach to a TDA2Px EVM or similar SoC or Processor.

1.2 Block Diagram

The block diagram in Figure 1 shows the components used to achieve a sensor fusion system. Note that typical sensor fusion ECUs include the applications processor and other object data fusion processing to make intelligent decisions during driving conditions. This specific design focuses on the input side data interface of different sensors (radar and cameras) to demonstrate synchronization of this using an off-board applications processor such as the TDA2Plus.

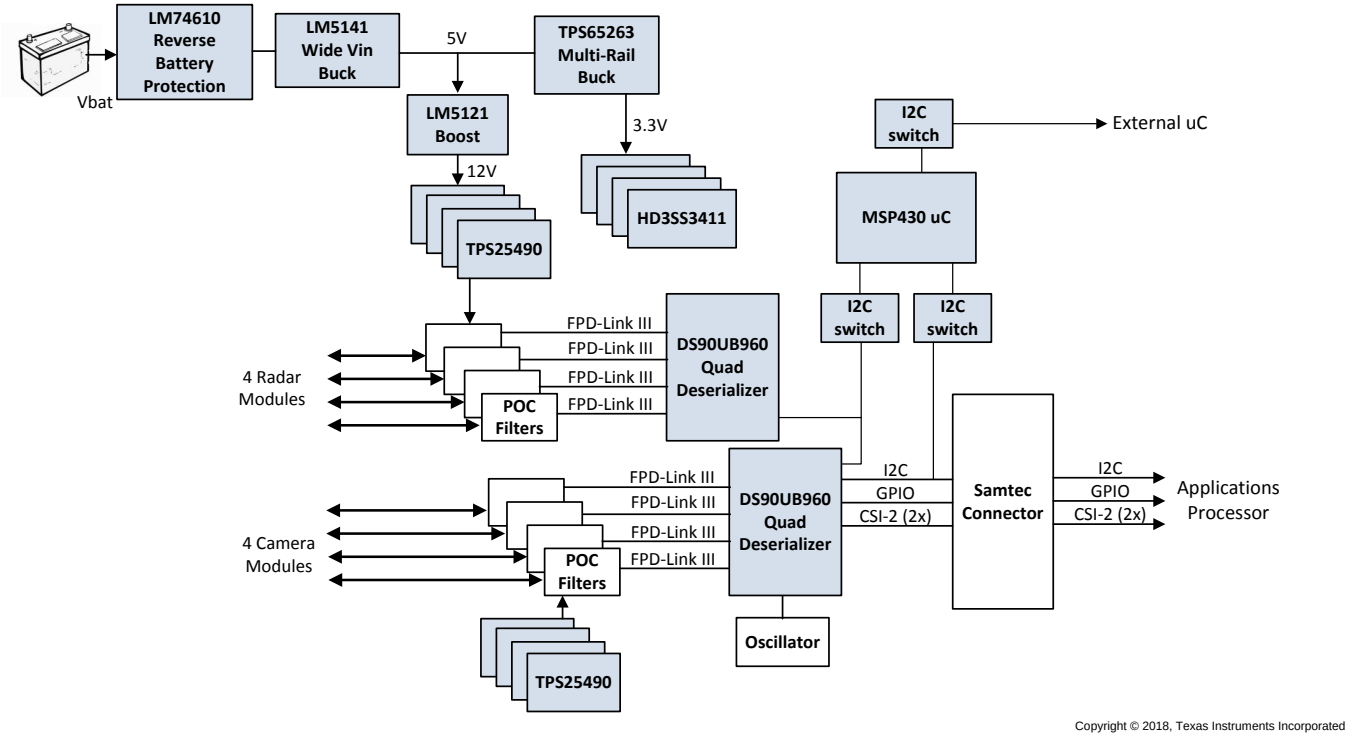


Figure 1. TIDA-01413 Block Diagram

1.3 Highlighted Products

1.3.1 DS90UB960-Q1

The DS90UB960-Q1 is a versatile hub capable of connecting serialized high-speed data received from 4 independent data streams via an FPD-Link III interface. For example, when paired with the DS90UB953-Q1 serializer, the DS90UB960-Q1 receives data from imagers supporting 2-MP resolution at 60-Hz frame rates.

1.3.2 LM74610-Q1

The LM74610-Q1 is a controller device that can be used with an N-Channel MOSFET in a reverse polarity protection circuitry. It is designed to drive an external MOSFET to emulate an ideal diode rectifier when connected in series with a power source. A unique advantage of this scheme is that it is not referenced to ground and thus has Zero Iq.

1.3.3 LM5141-Q1

The LM5141-Q1 is a synchronous buck controller, intended for high-voltage wide VIN step-down converter applications. The control method is peak current mode control. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting, and ease-of-loop compensation. The LM5141-Q1 features slew-rate control to simplify the compliance with CISPR and Automotive EMI requirements.

1.3.4 LM5121-Q1

The LM5141-Q1 is a synchronous buck controller, intended for high-voltage wide VIN step-down converter applications. The control method is peak current mode control. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting, and ease-of-loop compensation. The LM5141-Q1 features slew rate control to simplify the compliance with CISPR and Automotive EMI requirements.

1.3.5 TPS65263-Q1

The TPS65263-Q1 is a monolithic triple synchronous step-down (buck) converter with 3 A, 2 A, and 2 A output currents. A wide 4.0-V to 18-V input supply voltage range encompasses the most intermediate bus voltages operating off 5-V, 9-, 12-, or 15-V power bus. The converter, with constant frequency peak current mode, is designed to simplify its application while giving designers options to optimize the system according to targeted applications.

1.3.6 TPS25490-Q1

The TPS25940-Q1 eFuse Power Switch is a compact, feature-rich power-management device with a full suite of protection functions. The wide operating range allows control of many popular DC bus voltages. Integrated back-to-back FETs provide bidirectional current control making the device well-suited for systems with load-side holdup energy that must not drain back to a failed supply bus.

1.3.7 TS3USB221A-Q1

The TS3USB221A-Q1 is a high-bandwidth switch which is specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB input and output (I/O) connections.

1.3.8 MSP430F2272-Q1

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally-controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 1 μs.

1.3.9 HD3SS3411-Q1

The HD3SS3411-Q1 is a high-speed bidirectional passive switch in multiplexer or de-multiplexer configurations. Based on control pin SEL, the device provides switching of differential channels between Port B to Port A or Port C to Port A.

1.3.10 TIDA-01130

This reference design frequently makes references to the TIDA-01130 TI Design, which is an automotive 2-megapixel camera module built around a DS90UB953 serializer and an OmniVision OV2775 imager. For more details, see *Automotive 2-MP Camera Module Design with MIPI CSI-2 Video Output Interface and Power Over Coax*.

1.4 Design Considerations

1.4.1 DS90UB960-Q1

Using a serializer, deserializer to combine high-speed data with a bidirectional control signal onto one coaxial cable or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The DS90UB960-Q1 four-channel deserializer takes that simplification one step further. Each sensor in the system is connected to one deserializer through a single coaxial cable. Using *Power Over Coax* (POC) filters, the power for each sensor is also included on the single coaxial connection. In this way, sensor data, I^2C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coaxial cable. For more information on the cable itself, see *Cable Requirements for the DS90UB913 & DS90UB914A*.

In this design, the DS90UB960-Q1 can be paired with the DS90UB913A-Q1, or the DS90UB953-Q1 (or both), that is on a separate high-speed data sensor board (for example, the TIDA-01130). The DS90UB913A-Q1 or DS90UB953-Q1 serializer is intended to link with high-speed sensor front-ends such as Megapixel Imagers, RADAR- or LIDAR- Modules. It transforms a parallel LVCMOS or MIPI CSI-2 data bus along with a bidirectional control bus (I^2C port) into a single high-speed differential pair. The DS90UB953-Q1 can accept up 4 MIPI CSI-2 lanes, operating at 830Mbps each. The integrated bidirectional control channel transfers data over the same differential pair. Therefore, it eliminates the need for additional wires to program the registers of the image sensors.

In addition, the serializer provides up to four GPO pins. They can act as outputs for the input signals that are fed into the deserializer general-purpose input/output (GPIO) pins triggering the logic of the image sensor. For example, the deserializer and the serializer can be configured in a way so that one GPIO pin on the deserializer side causes one GPO pin on the serializer side to toggle. In other words, the output pins of the serializer reflect the assigned input pins from the deserializer. Alternatively, the GPO 2 pin can be configured to become a clock output pin when set in external oscillator mode (CLKOUT). In turn, the GPO 3 pin acts as an input for an external clock source (CLKIN). It allows the serializer to drive the system clock input (XVCLK) of the sensor module.

1.4.2 LM74610-Q1

Protection against reverse polarity is a basic requirement for every automotive hardware design, to prevent damage to internal electronic devices from reversed battery connections or other wrong operations. The easiest and most straightforward approach to ensure protection against reverse polarity would be to place a diode in forward direction in the supply line. The drawback is the voltage drop in forward direction. A much more convenient solution is to use the LM74610-Q1 device. It provides reverse polarity protection with a technique called smart-diode controlling. The LM74610-Q1 features the diodes advantage of reverse polarity protection, without the voltage drop disadvantage. It drives an external MOSFET in case of a positive supply voltage and disconnects the supply line in case of reversed polarity.

1.4.3 LM5141-Q1

Key benefits for this design:

- Wide input range of 3.8 V–65 V to directly connect with vehicles onboard supply.
- Qualified for automotive applications as it meets – AEC-Q100– HBM ESD Classification Level2 – CDM ESD Classification Level C4B.

- Configurable output voltage: the voltage is set to 5 V. However, it is possible to configure other voltages as well.
- Configurable switching frequency to manage switching losses. In addition, to avoid electromagnet Interference, due to AM radio insertion from 530 kHz to 1710 kHz, for example.

1.4.4 LM5121-Q1

In this design, the boost converter does not need any wide input-voltage range. However, requirements for automotive components apply. Therefore, the device provides disconnection switch control, which completely disconnects the output from the input during an output short or a shutdown condition. In addition, during the start-up sequence, inrush current is limited. The LM5121-Q1 boost controller operates with external transistors as the high power demand for this design makes external MOSFETs mandatory.

1.4.5 TPS65263-Q1

The last power conversion stage generates the three lowest system voltages: 3.3 V, 1.8 V, and 1.1 V. There is no need for high currents, which allows use of a different technology, a step-down converter with internal transistors. The TPS65263 is a triple synchronous step-down converter. Even though the device utilizes the buck topology, no external components are required. All low- and high-side switches are integrated. Just an inductor and an output capacitor need to be connected to each channel, along with a feedback voltage divider, to set the output voltage.

1.4.6 TPS25940-Q1

An important safety aspect is, if a camera or radar module is about to fail, to ensure the main circuit remains unaffected. A short circuit on one of the sensor modules or their supply lines would result in a failure of the entire power rail. To void this occurrence, eFuses are chosen. Integrated eFuses have great advantages over regular PCB fuses. For instance, they cannot actually blow.

1.4.7 HD3SS3411-Q1

The device has been selected as it operates up to 10Gbps, which is far sufficient for the 1.5-Gbps links of the FPD-Link III components. It routes through one of the two FPD-Link III connectors. Either the coaxial or the HSD connector can be selected.

1.4.8 TS3USB221A-Q1

This design utilizes these high-bandwidth USB switches to dynamically configure the I^2C bus on the board. These parts are much faster than what is required, but they work well and are very simple to implement. For more information on the configuration of the I^2C bus, see Section 1.4.9, which addresses the MCU.

1.4.9 MSP430F2272-Q1

This version of the MSP430 is used in this design as a housekeeping and configuration MCU, which allows the main SoC in the system to boot in parallel with the configuration of the SERDES links and camera imagers.

2 System Design Theory

2.1 PCB and Form Factor

The board is designed to match the size of various processor evaluation modules (EVM), such as the TDA2xEco EVM or the TDA2Px EVM. Those EVMs offer a convenient way of testing an application processor. The TDA2Px processor as part of the TDAxx series is a processor designed for automotive ADAS and self-driving car applications. The board size of the TDA3x EVM is larger than the other EVMs mentioned, but the mounting holes are placed in the same position on all boards, to maintain the overall compatibility. As a result, the connection between the board and the evaluation module must be in a fixed position. See Figure 2 and Figure 3).

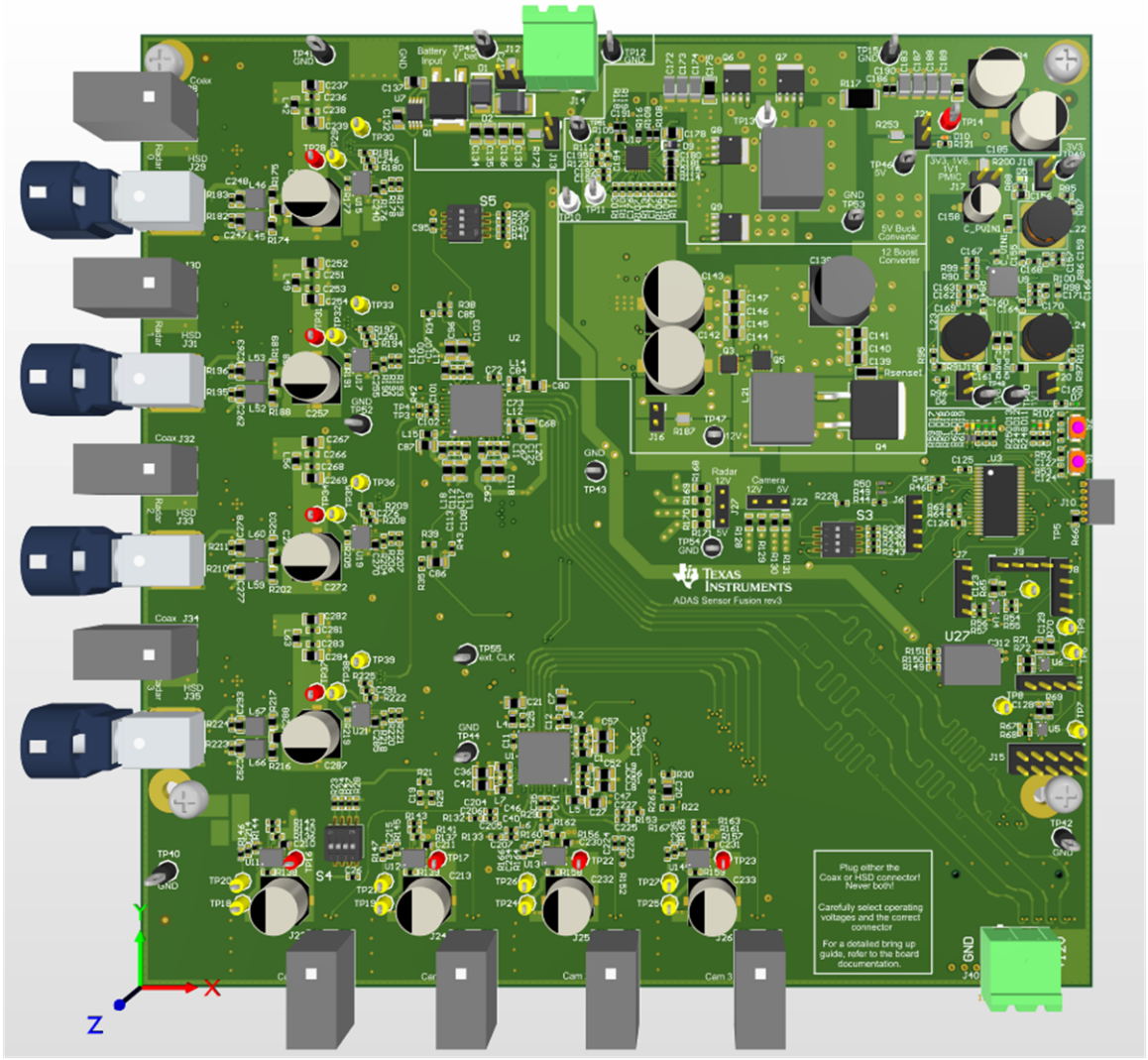


Figure 2. Board—Top View

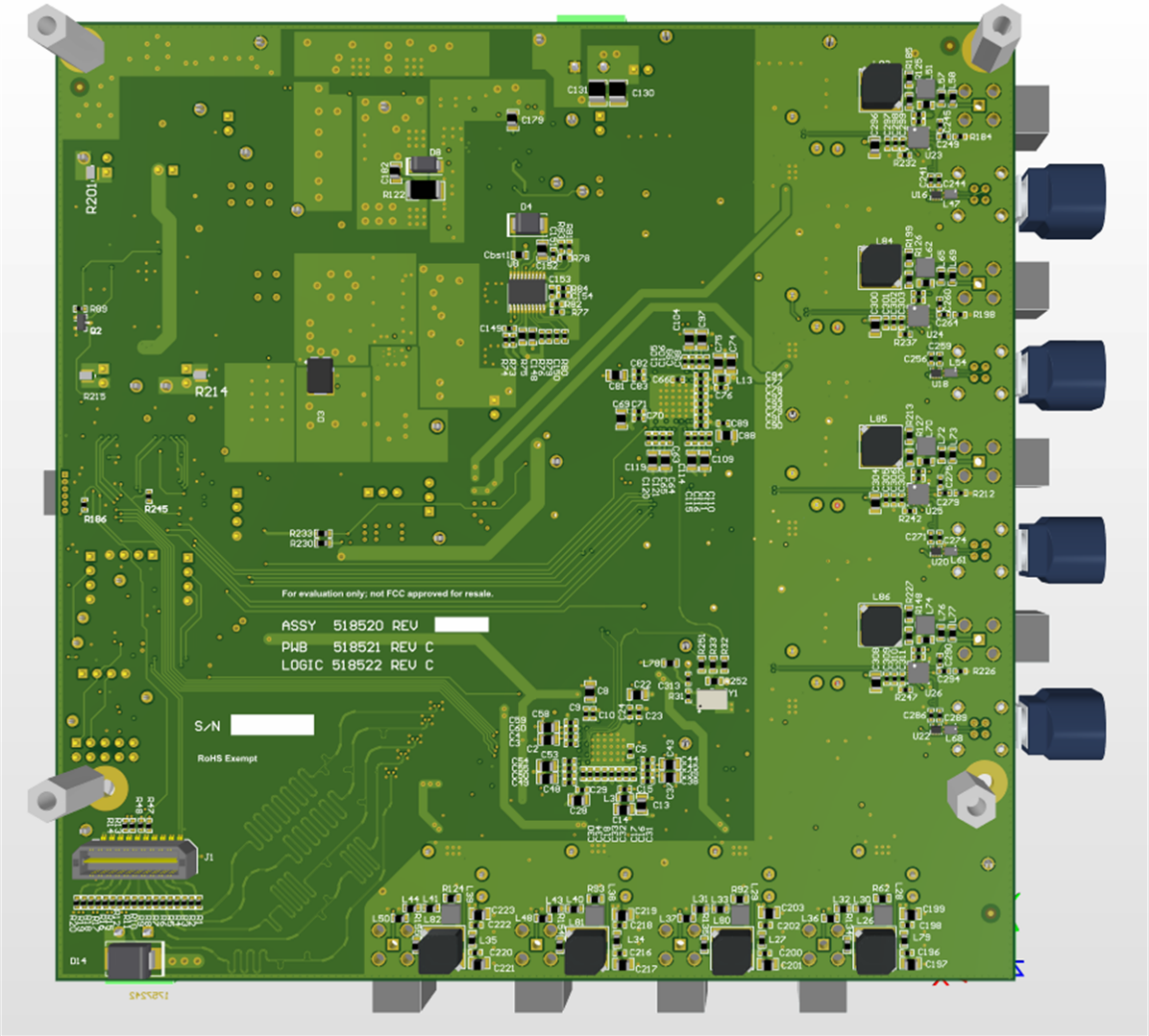


Figure 3. Board—Bottom View

2.2 I²C Addressing

2.2.1 Multiple Device Addressing (Aliasing)

Sensor fusion architectures for ADAS and self-driving applications require multiple sensor modules in a single system. Often, it is desirable for the sensor devices to be built alike, and therefore fixed to the same physical I²C address. If these modules are all to be accessed on the same I²C bus, there must be a method of assigning each camera an alias that will be used to address them. The FPD-Link serializer and deserializer parts provide this functionality to assign a slave ID (alias) to each camera. This allows the slave devices to be independently addressed. These physical slave addresses and its associated alias IDs are configured by programming the “Slave ID” and “Slave Alias” registers on the deserializer.

From the I²C host perspective, this remaps the address of each slave to its slave alias. Multiple of the same sensor modules are used in this design. For instance, the OV2775 image sensor module. This imager default address is 0x6C (0110111x). For a system utilizing more than one imager, GPIO 2 and GPIO 1 can be used to select different addresses for each imager. However, this would require that each camera in the system be built differently. Each system would have to be built with one of each unique camera. In a production environment, this is not desirable. Instead, the aliasing feature of the DS90UB960 is used. In the deserializer, unique addresses are assigned to each imager. These aliases are used to refer to the imagers that are all addressed at 0x6C (0110111x). The host microprocessor can now communicate with each imager by using its alias, even though the imagers in each camera are physically addressed identically. Figure 4 shows an example of I²C address aliasing.

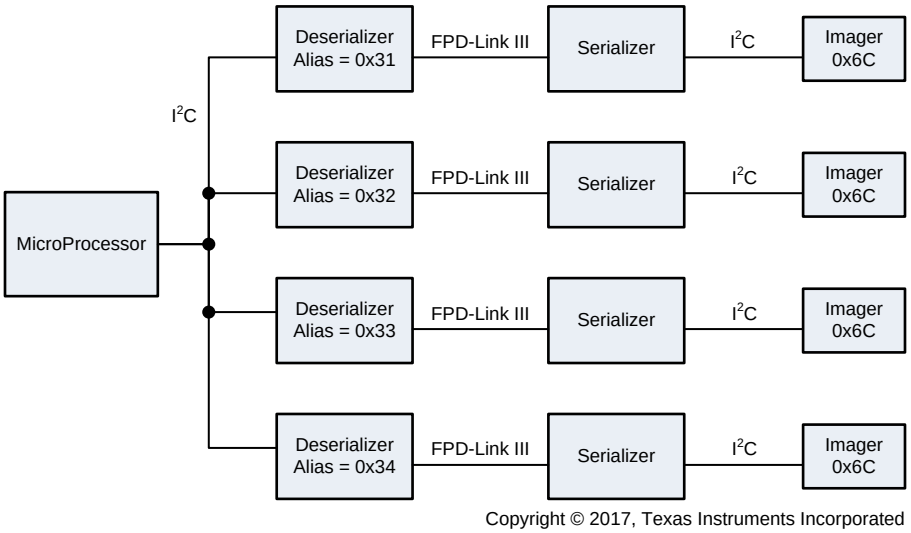


Figure 4. I²C Address Aliasing

2.2.2 I²C Bus Switches and Connections

This system offers four possible I²C hosts. Each host has a role to perform and a slave that they must configure. This requirement complicates the I²C bus connections. Figure 5 shows three I²C switches, which are used to configure the I²C bus to accomplish all of the tasks required for initialization of the system. A GPIO has been stationed on the MCU connected to the control pin of each switch. These control pins are labeled with red text under the switch in Figure 5. The functionality of these control pins can be described as:

- I²C_SW_EXT: When this switch is open, either the MSP430 or the SoC functions as the I²C host in the system. When this switch closes, it allows the external MCU to take over as host of the I²C bus. If an external MCU is used, place the MSP430 into external MCU mode by setting the jumper J19.
- I²C_SW_SOC: When this switch is open, all SoC I²C traffic is isolated from the TIDA-01413 board. This isolation allows either the local MCU or the external MCU to act as the host. Depending on when this switch is closed, the SoC can either initialize the board or just control the camera after one of the MCUs has initialized the board. Control of the cameras is done by writing I²C commands into the UB96x during normal operation.

- I²C_SW_UB960: When this switch is closed, the main I²C bus on the UB960 is connected to the main I²C bus on the board.

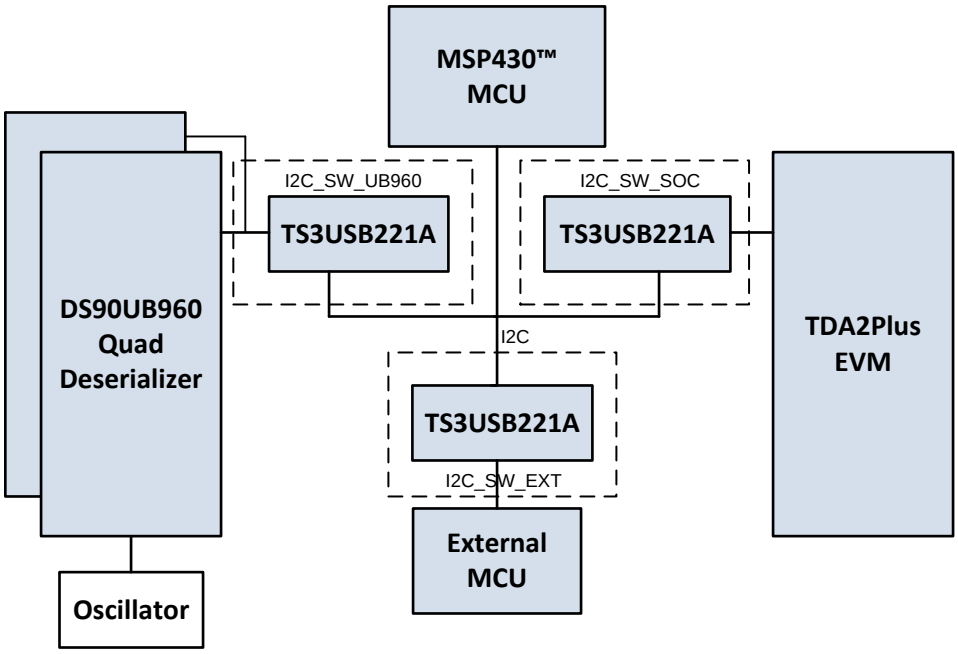


Figure 5. I²C Bus Diagram

2.2.3 Sensor Connection: Coax Versus HSD Using HD3SS3411-Q1 Switches

One set of four sensor modules can be either routed via a coaxial cable or a twisted-pair HSD connector cable. The coaxial cables poses a special challenge, as both data and power transmits over the same wire. However, the maximum power to be transmitted is limited. Instead, the HSD connection offers data and power lines separately transmitting more energy for power-hungry sensor modules. To make routing possible the high-speed switch will pass the signal either to the coax or the HSD connector. Setting four jumpers controls the SEL pin of each switch for the signal line to route.

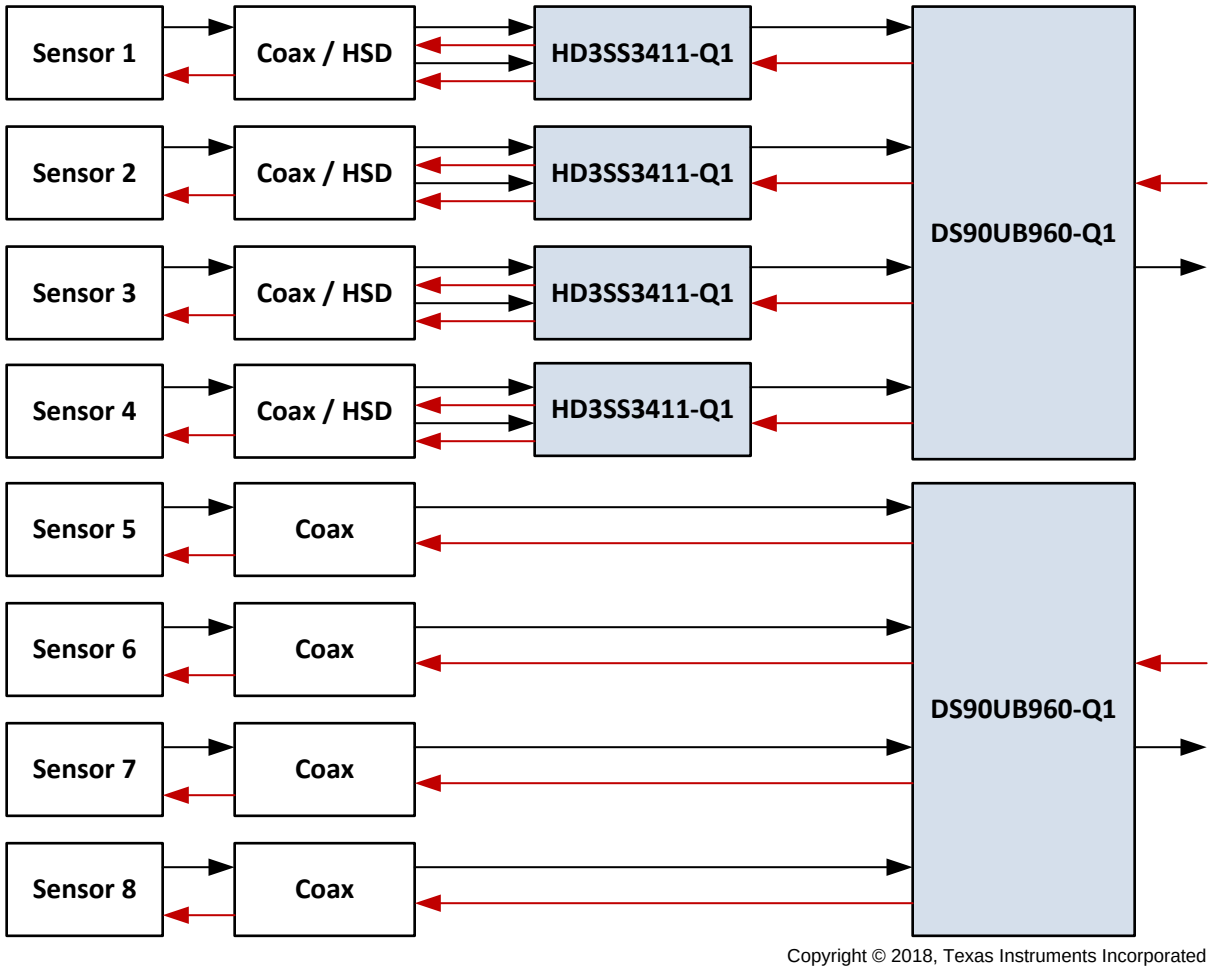


Figure 6. Coax vs HSD Connection Setup

2.2.4 Power-Over-Coaxial (PoC) Filter

One of the most critical portions of a design that uses PoC is the filter circuitry. The goal is twofold: (1) deliver a clean DC supply to the input of the switching regulators. (2) protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB953 serializer on the TIDA-01130 and DS90UB960 deserializer on this design communicate over two carrier frequencies: 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers while attempting to only pass DC.

The PoC design requires an impedance of > 2 kΩ across the 10-MHz to 2.2-GHz bandwidth to enable the forward channel and backchannel to pass uninterrupted over the coaxial cable. To accomplish this uninterrupted passing, select an inductor for filtering the 10-MHz to 1-GHz range in addition to selecting a ferrite bead for filtering the 1- to 2.2-GHz frequency band. L1 in Figure 7 represents the complete filter for inductor and ferrite beads. L2, shown in Figure 7, is the same filter design as L1; however, L1 is located on the TIDA-01130 camera module design.

Ensuring that this filter has the smallest footprint is imperative. The LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. Using this inductor eliminates the requirement for a solution that typically demands two inductors, one for the low-end frequency band and another for the high-end frequency band.

For the high-frequency, forward-channel filtering, inductors are usually not sufficient to filter above 1 GHz. Therefore, the TIDA-01413 design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2.2-GHz range. This design uses three 1.5-kΩ ferrite beads because, when in operation, the current through these devices reduces the effective impedance. Therefore, three ferrite beads instead of two allows for more headroom across the whole frequency band. Lastly, for good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the designer can minimize the solution size on the board for the PoC inductor filtering. For more details, see *Sending Power Over Coax in DS90UB913A Designs*.

Another important requirement to note in regards to filtering is to ensure that the FPD-Link signal is not interrupted by allowing DC offset on the data. Choose the AC coupling capacitors shown by the 0.033 µF and 0.015 µF in such a way to ensure the high-speed AC data signals pass through but also blocks the DC from coupling on the data lines. Capacitive values for the DS90UB953, DS90UB960 pair are smaller than previous generations due to their requirement to pass 4 Gbps of data versus the previous 2 Gbps of video data transmission from 1-MP cameras.

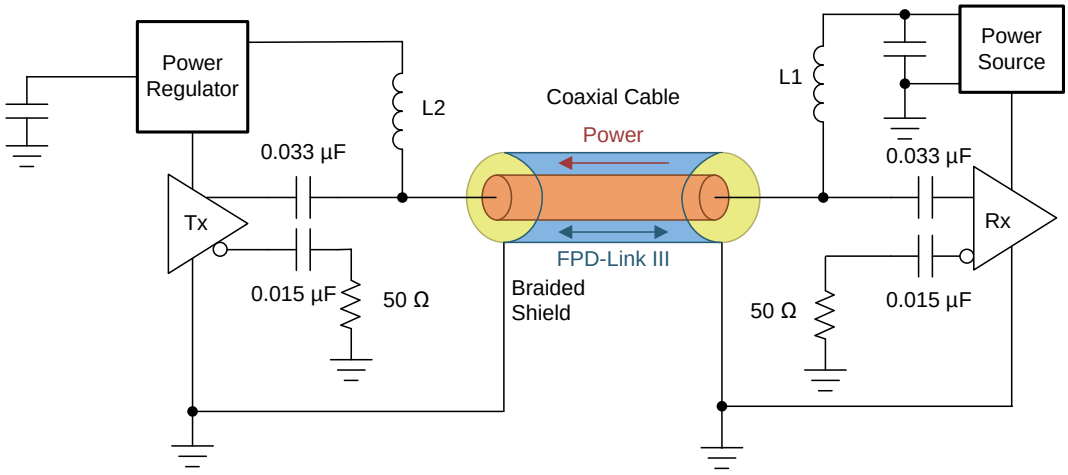


Figure 7. Power Over Coax Cable

2.3 5-V Buck Converter Stage

Figure 8 shows the LM5141 buck converter stage schematic.

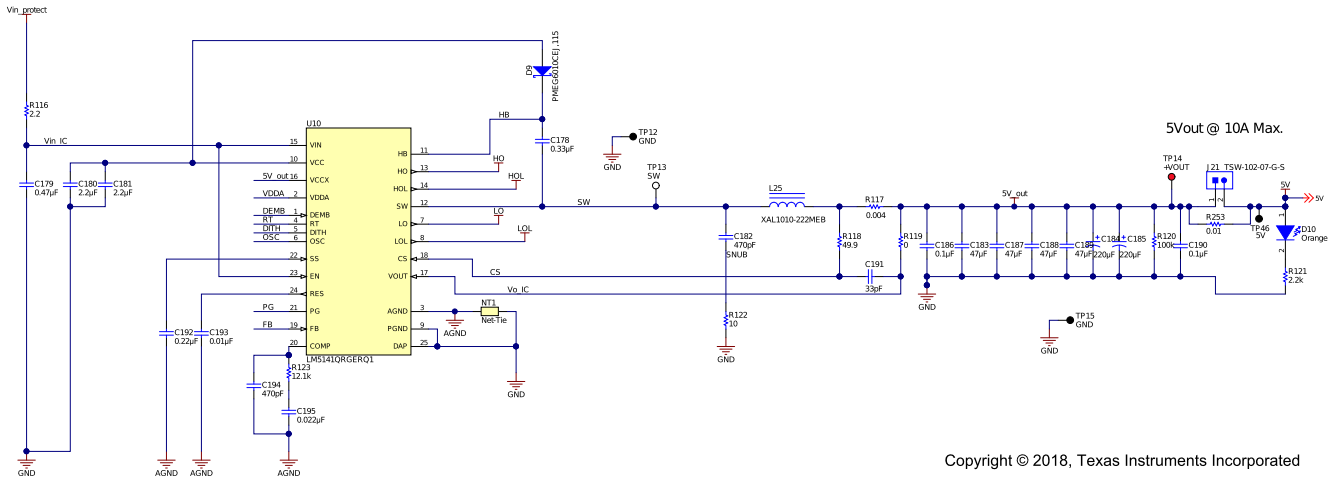


Figure 8. LM5141 Buck Converter Stage

2.3.1 Frequency Modulation and Dithering - OSC, RT and DITH Pins

The LM5141-Q1 offers two internally trimmed frequency options: 440 kHz or 2.2 MHz. The OSC pin is pulled up to VDDA to enable 2.2-MHz operation. It is possible to modulate the oscillator frequency up or down by connecting a resistor from the RT pin to ground. To disable frequency modulation, the pin must me grounded or left open.

Another option is frequency dithering, which is enabled by connecting a capacitor from the DITH pin to AGND. A triangular waveform, generated across the DITH capacitor, modulates the oscillator frequency by ±5% of the nominal frequency. Dithering can help to decrease electromagnetic interferences by spreading the noise spectrum, but lowering the energy emission amplitudes from the formerly narrow frequency band. To disable frequency dithering, the DITH pin can be connected to AGND directly.

2.3.2 Output Voltage Level - FB Pin

The output voltage can either be fixed to 3.3 V or 5 V or custom output voltages can be set using a resistor network. 3.3-V output is achieved by connecting the FB pin to VDDA, 5-V output by connecting the FB pin to ground with a maximum resistance of 500 Ω. The output voltage in this design is fixed at 5 V.

2.3.2.1 Loop Compensation - COMP Pin

In *Current Mode Control* (CMC), a Type II compensation network is sufficient for proper compensation. Three components used for compensation, RCOMP (R123), CCOMP (C195), and CHF (C194) configure the error amplifier gain and phase characteristics. The network creates a pole at DC, a mid-band zero and a high-frequency pole. The compensation network is connected between the COMP pin and ground. Since it is difficult to calculate the exact values for the compensation components, use design software such as TI's WEBENCH® to calculate initial values. Fine-tuning can be achieved as an empirical approach after first power up.

2.4 12-V Boost Converter Stage

Figure 9 shows the LM5121 boost converter stage schematic.

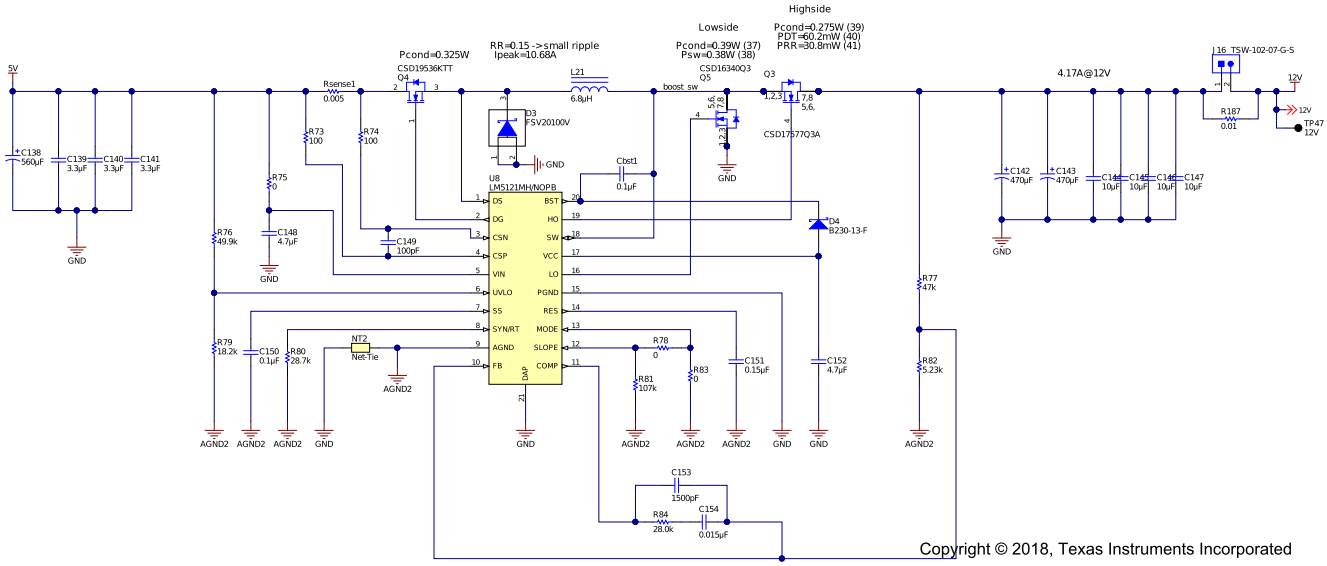


Figure 9. LM5121 Boost Converter Stage

Remember that the load may change continuously; therefore, the boost circuit must be able to cope with it in the design. As the 5-V buck converter supplies the boost converter there is no need for a wide input voltage range to fulfill. The LM5121-Q1 boost controller does not offer internal transistors. However, the extended power demand of the design requires external MOSFETs in any case.

Table 1. Design Parameters

Design Parameters	Value
Output Voltage (V_{OUT})	12 V
Full Load Current(I_{OUT})	4.2 A
Output Power	50 W
Minimum Input Voltage ($V_{IN\ (MIN)}$)	4.5 V
Typical Input Voltage ($V_{IN\ (TYP)}$)	5 V
Maximum Input Voltage ($V_{IN\ (MAX)}$)	5.5 V
Switching Frequency (F_{SW})	313.5 kHz
Disconnection Switch Control	Yes

The input inductor sets the ripple of the output current. Typical values for the current ripple are between 15% and 40% of the full load current. The ripple can be reduced with the selection of a bigger inductor. This design targets a very small ripple ratio (RR = 0.15), because a big ripple places a burden on the output capacitors. With a targeted RR and a set switching frequency, the inductor size can be calculated.

$$L_{IN} = \frac{V_{IN}}{\left(I_{IN} \times RR \times F_{SW}\right)} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) = \frac{5\,V}{10\,A \times 0.15 \times 313.5\,kHz} \times \left(1 - \frac{5\,V}{12\,V}\right) = 6.20\ \mu H$$

A standard value of 6.80 µH is selected. With the selected inductor, it is possible to calculate the resulting peak current.

$$L_{PEAK} = I_{IN} + 0.5 \times \frac{V_{IN}}{L_{IN} \times F_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) = 10\,A + 0.15 \times \frac{5\,V}{6.2\ \mu H \times 313.5\,kHz} \times \left(1 - \frac{5\,V}{12\,V}\right) = 10.68\ A$$

2.5 Low-Voltage Multi-Rail Buck Converter Stage

The Step-Down Converter generates the three lowest system voltages: 3.3 V, 1.8 V, and 1.1 V. There is no need for high currents allowing the use of a step-down converter with internal transistors. Even though the IC utilizes the buck topology, no external semiconductors are required, as all the low- and high-side switches are integrated on a single IC. It is only necessary to attach an inductor and an output capacitor to each channel, along with a feedback voltage divider, to set the output voltage. Here all inductors and output capacitors are of same values (L = 4.7 µH, C = 22 µF) for all three channels.

Figure 10 shows the TPS65263 multi-rail converter stage schematic.

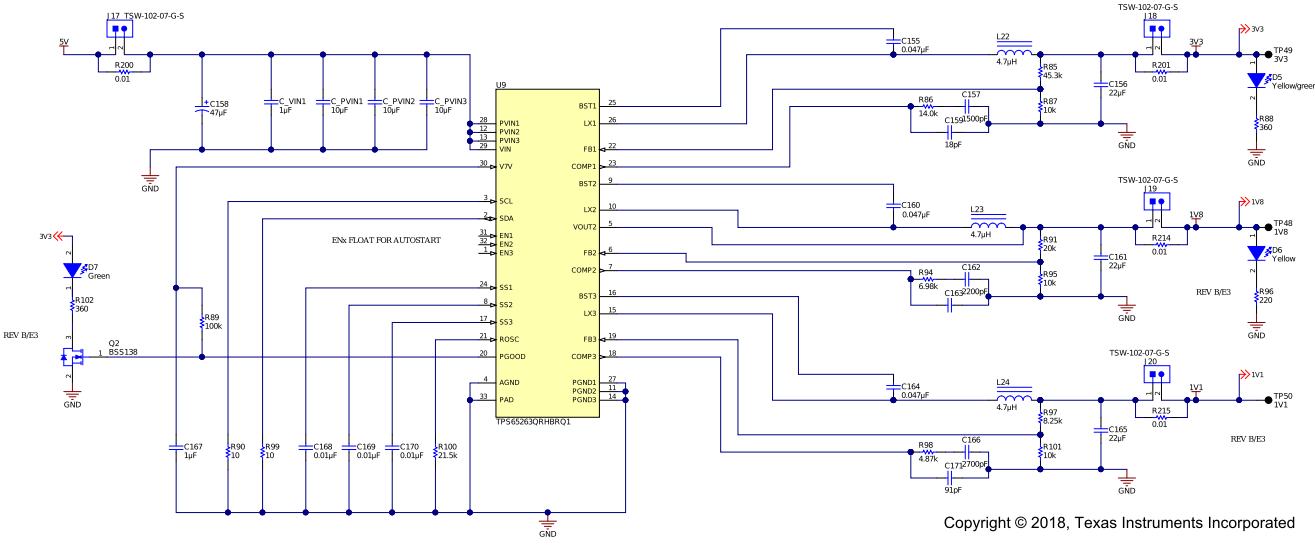


Figure 10. TPS65263 Multi-Rail Converter Stage

The feedback voltage reference for the buck converter is 0.6 V. The output voltage feeds back with a simple voltage divider. The low-side resistor of the divider is set to 10 kΩ. The resistors for the feedback system are R (3.3 V) = 45 kΩ, R (1.8 V) = 20 kΩ and R (1.1 V) = 8.33 kΩ.

$R – (10\ k\Omega – 0.6\ V / V_{OUT} \times 10\ k\Omega) \times (V_{OUT} / 0.6\ V)$

3 Getting Started Hardware

3.1 Hardware Configuration

Configure the TIDA-01413 before use. Complete the following configuration steps in the order provided to avoid damage to system components. The following configuration is for an 8-channel sensor system using a TDA2Px EVM. The EVM is powered from the included power supply, while this board will be powered from a supply similar to a car battery. Dismount every jumper off the board to avoid the wrong configuration during startup. The following steps revisit all the necessary hardware settings:

1. Select *Coax Mode* and *I2C_SOC override control* (see Figure 11):
   a. Set switch S3 to 1-ON, 2-ON, 3-ON and 4-OFF
2. Set the *Mode* setting for the DS90UB960 devices
   1. Set switch S4 and S5 to 1-OFF, 2-ON, 3-OFF, and 4-ON (Sets up both devices in CSI-2 and Coax Mode for compatibility to the DS90UB953.)
3. Install a short on the J22 and J27 jumper on pin 2 and pin 3 for a 12-V supply to sensor modules. If using a 5-V supply, short J22 and J27 across pin 1 and pin 2.
4. System connection setup:
   1. Connect the TIDA-01413 to the TDA2Plus EVM by connecting SAMTEC connectors between boards.
   2. Connect up to four cameras (such as the TIDA-01130) and up to four radar modules to the TIDA-01413.
   3. Connect HDMI OUT on the TDA2Plus EVM to monitor using an HDMI cable.
   4. Connect the power supply provided with the TDA2Plus EVM to the input power connector on the EVM.
   5. Connect 12 V of input power to J14.

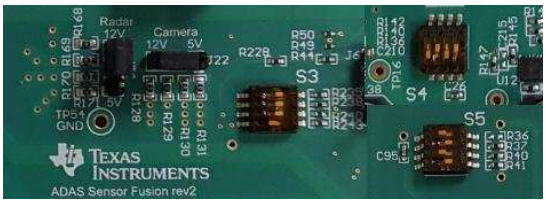


Figure 11. Board Jumper and Switch Settings

4 Test Setup

A successful bring-up of the single sub-circuits allows observing power rails to ramp up and I^2C communication to execute.

4.1 Power Supply Startup

Ramp up of the systems voltage rails. The oscilloscope channels are configured as follows:

- Channel 1 (Blue): 5-V buck converter (TP14)
- Channel 2 (Red): 12-V boost converter with 50-Ω load (TP47)
- Channel 3 (Green): 3.3-V output of TPS65263 (TP49)
- Channel 4 (Pink): Supply voltage (15 V, limited to 1 A) (TP51)

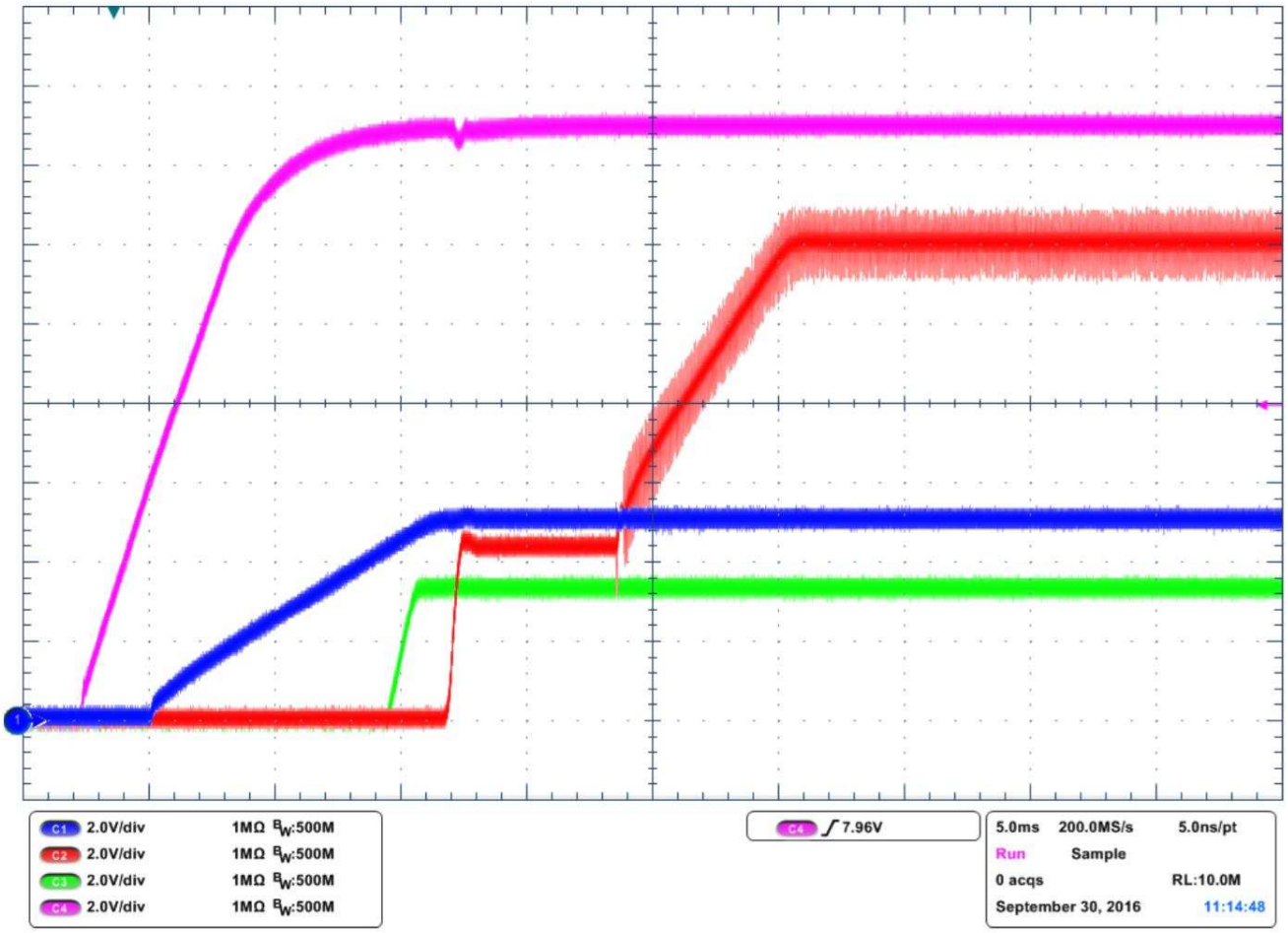


Figure 12. Power Supply Startup Waveform

Figure 12 highlights useful information about the system. It can be observed that the buck converter (Channel 1, blue) begins to ramp up at 6-V input voltage (Channel 4, pink). Both the input voltage and the buck converter output reach their respective maximum after approximately 15 ms. The TPS65263 (Channel 3, green) begins to ramp up to 3.3 V, as soon as the buck converters output reaches 4.4 V. Finally, the boost converter (Channel 2, red) ramps up to 12 V.

Due to the undervoltage lockout feature, the boost converter is prevented from operation until the buck converter (Channel 1, blue) is fully operational. After surpassing the undervoltage lockout, the boost converter output almost reaches the input voltage (around 5 V). The step draws a lot of current, which can be seen by the dent in the input voltage (Channel 4, pink), as the input voltage reaches the current limit of 1 A for a brief moment. To prevent further stresses, the boost converter introduces a delay in startup. The

plateau on channel 2 in red (4.5 V) reflects this. Past the delay, the boost converter begins with its soft-start sequence. Note, the start-up sequence reveals an unusual behavior, as the output voltage of the boost converter is superimposed by voltage surges of up to ± 500 mV. Further analysis might need to take place limiting the surge. However, the 12-V boost-converter output is acceptable in this design as the generated voltage surpasses additional filter circuitry for the external module to supply.

4.2 I²C Communication

The communication initiates from the MSP430 uController, by pulling down the data lane (Channel 3, green) showing in Figure 13. It indicates the start condition. Channel 4 (pink) is the clock line on the board. The I²C clock frequency on this side of the deserializer is 400 kHz. The I²C bus transmits to the sensor modules side. The transmission can be seen in channel 1 (blue) and channel 2 (red, 75-kHz clock lane). As the clock speed on the sensor side is much lower than on the deserializer side, the host on the deserializer side has to wait relatively long for the acknowledge signal from the slave.

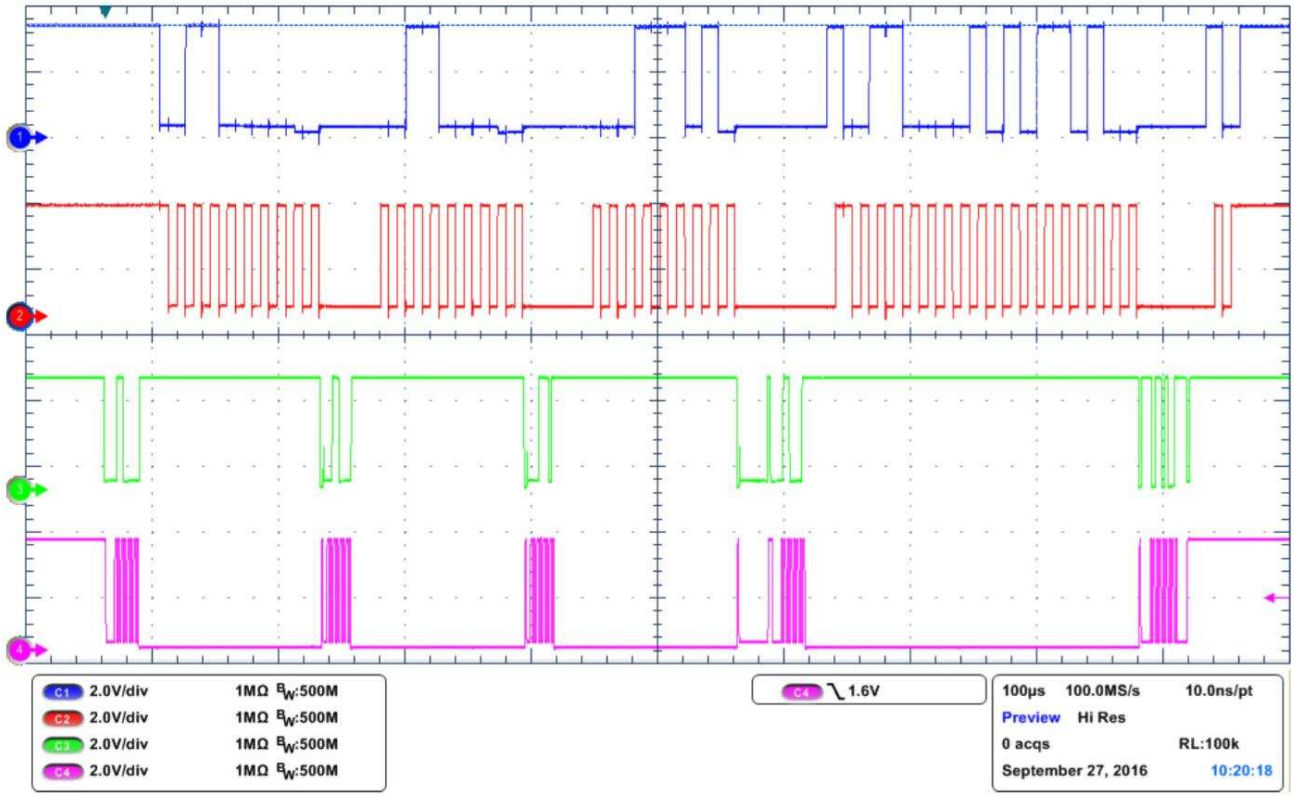


Figure 13. I²C Communication Waveforms

4.3 CSI-2 Signal Conditions

As follows, the CSI-2 data bus is captured next to the CSI- 2 connector (J1). The signal shown is part of one of the CSI-2 data lanes. The area within the red box indicated as (b) is enlarged and shown in Figure 14.

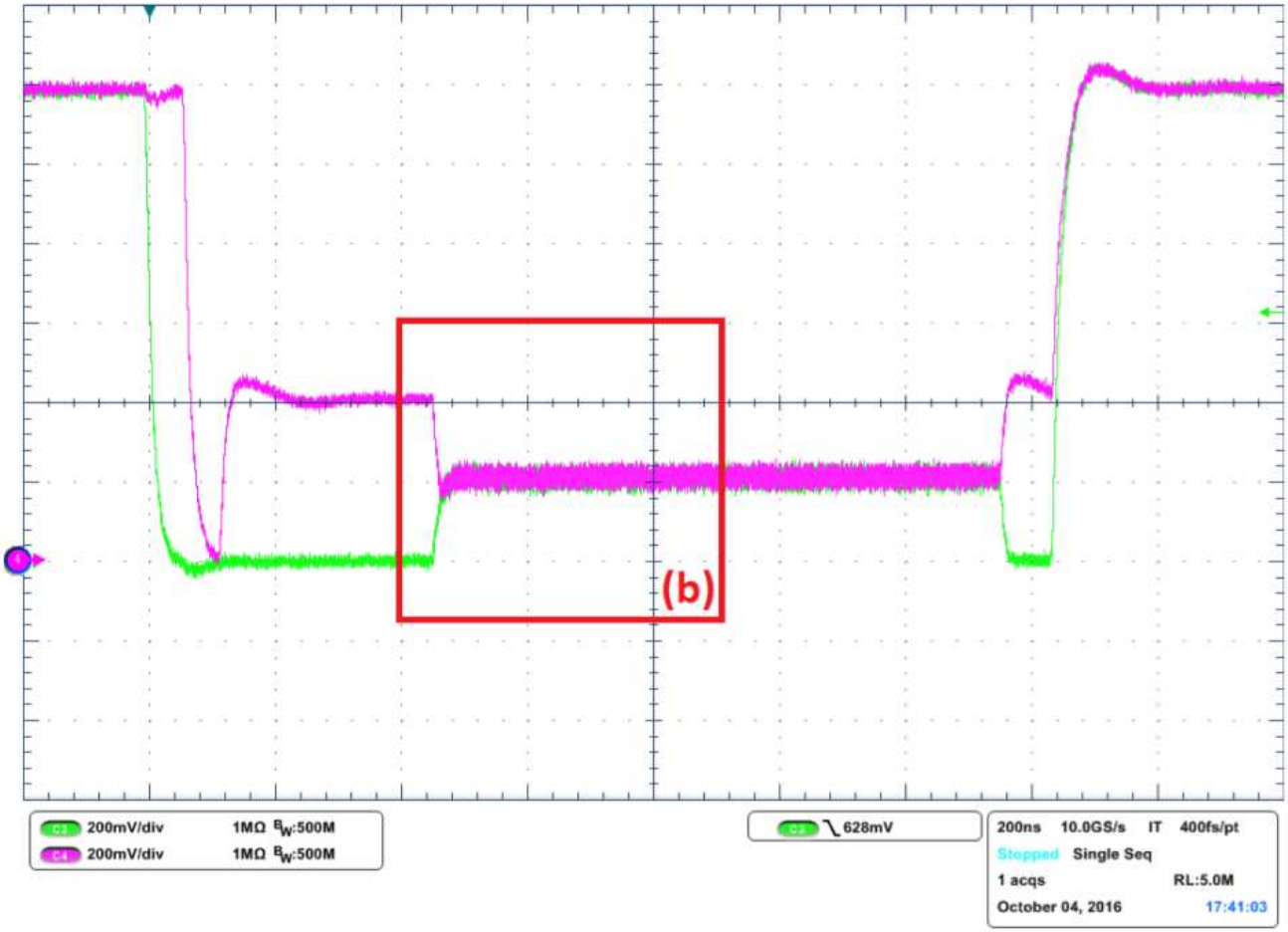


Figure 14. CSI-2 Switching Behavior

Figure 14 shows a transition phase on one data line. Again, the red box within the transition phase indicated as (c) is zoomed and shows an excerpt from the actual differential signals in Figure 15.

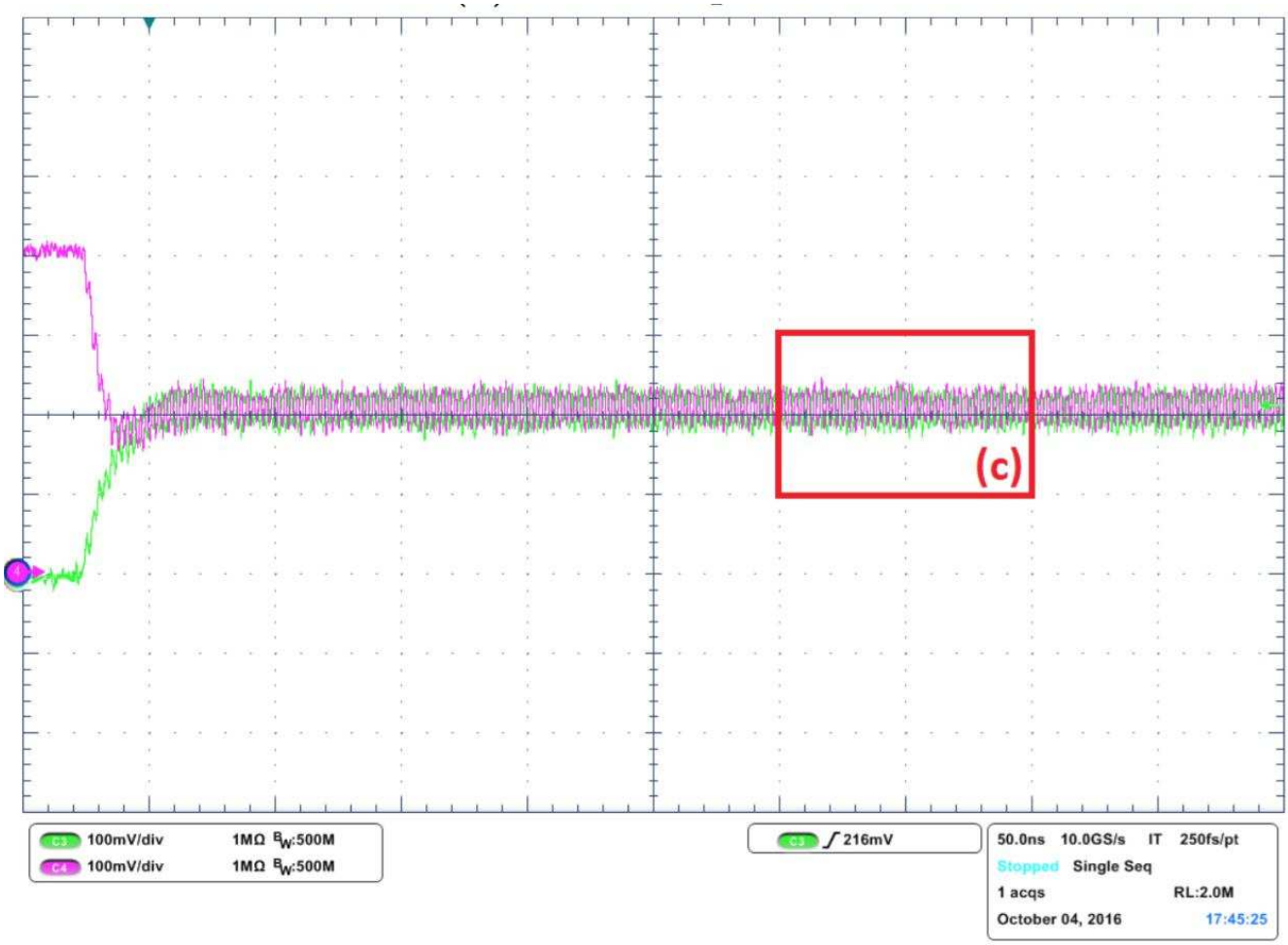


Figure 15. Zoomed in CSI-2 Switching Behavior

Figure 16 shows the positive CSI-2 differential signal in green (channel 3) and negative differential signal in pink (channel 4). The M1 channel in blue is a math function, which calculates the difference between the two signal voltages.

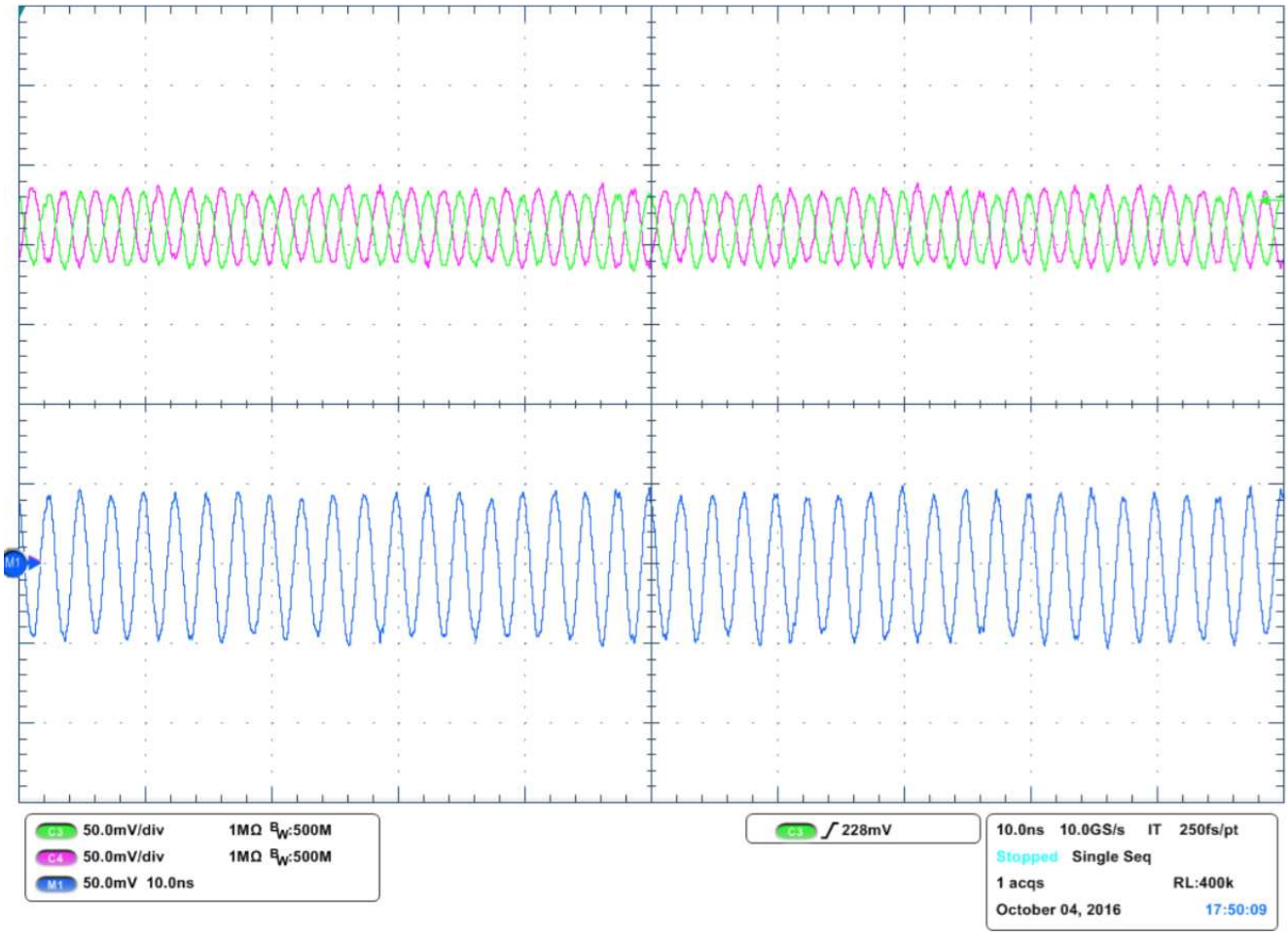


Figure 16. CSI-2 Positive and Negative Differential Voltages Measured

LVDS effectively doubles the amplitude, while using very small voltages. The data stream illustrated here consists of alternating 0 and 1 digits for better visibility and testing. Therefore, the deserializer hub (DS90UB960-Q1) is configured to output patterns generated by its internal “Pattern Generator”. It is offered as one feature for PCB validation.

4.4 FPD-Link III I²C Initialization

With cameras and TDA2Plus connected to the TIDA-01413 and the power supplies or interface verified, the initialization of cameras can be completed. The writes to initialize the deserializer and serializer are as follows:

- Deserializer slave I²C address 0x7A (8-bit) or 0x3D (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x58 with 0x5E: I²C pass through enabled and backchannel frequency select
  - Register 0x5C with 0x74: Sets serializer alias to 74 for camera on port 0
  - Register 0x5D with 0x6C: Sets slave ID for imager to 6C
  - Register 0x65 with 0x40: Sets slave alias for imager to 40
  - Register 0x6D with 0x7C: Configures port to Coax mode and FPD III to CSI mode
  - Register 0x32 with 0x01: Enables TX write enable for port 0 and port 1
  - Register 0x33 with 0x03: Enables 960 CSI output and sets to 4 lane mode
  - Register 0x21 with 0x03: Sets round robin forwarding for CSI0 and CSI1
  - Register 0x20 with 0x00: Forwarding enabled for all RX ports and all ports mapped to CSI-2 Port 0.
- Serializer slave I²C address 0x74, 0x76, 0x78 and 0x7A (write to all cameras)
  - Register 0x06 with 0x41: Sets HS_CLK_DIV and DIV_M_VAL for CLKOUT from 953 to OV2775
  - Register 0x07 with 0x28: Sets DIV_N_VAL for CLKOUT from 953 to OV2775
  - Register 0x0E with 0xF0: Sets GPIOs on 953 as outputs
  - Register 0x0D with 0x00: Drives GPIOs from 953 low to force imager PWDN and RESET pins low
  - Register 0x0D with 0x0C: Pulls PWDN and RESET pins on OV2775 high to bring imager out of reset

Remember that the deserializer setup registers listed are only showing writes for one camera. To initialize all four cameras, select each camera using port select register 0x4C.

4.5 OV2775 Initialization

After the FPD-Link III setup completes for the DS90UB953 and DS90UB960 devices, the I²C initialization can begin on the OV2775. For these writes, see the OV2775 data sheet for register settings. There are many register settings, but as long as the 953 and 960 FPD-Link III parts have been configured, the I²C backchannel allows for the OV2775 to be accessed at address 0x6C in 8-bit addressing or 0x36 in 7-bit addressing.

5 Board Programming or Reprogramming

If the board must use the MSP430, the device can be programmed with the following procedure:

1. Connect the EZ430 development tool to J10.
2. Connect the USB cable to the PC and to the EZ430 development tool.
3. Open the TI Code Composer Studio™ (CCS) software.
4. Open the project files for software to be loaded.
5. Select "Debug" to load the software into the MSP430.
6. Press "Run" to run in a debug environment or remove EZ430
7. Press the MSP430 RESET button (S1) on the TIDA-01413 board
8. The software begins to run on the board

To use the TDA2Plus software, see the TDA2Plus EVM documentation for further details.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01413.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01413.

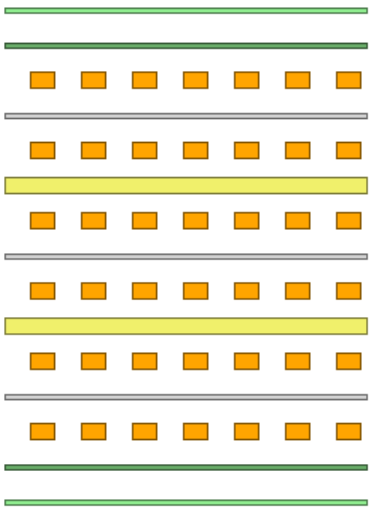
6.3 PCB Layout Recommendations

6.3.1 PCB Layer Stackup Recommendations

The PCB layer recommendations are as follows:

- Use at least a four-layer PCB with a power and ground plane. Locate the LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines.
- If using 4 layers, layer 2 should be a ground plane. Since most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.

An additional two layers were used to simplify BGA fan out and routing. Figure 17 shows the six-layer stackup used in this board.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.5	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.7		
Dielectric1	Dielectric	Prepreg	4.055	370HR	4.2
Layer 2 - GND	Signal	Copper	1.181		
Dielectric2	Dielectric	Core	27.95	370HR	4.2
Layer 3 - PWR	Signal	Copper	1.181		
Dielectric3	Dielectric	Prepreg	8.11	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.181		
Dielectric4	Dielectric	Core	27.95	370HR	4.2
Layer 5 - GND	Signal	Copper	1.181		
Dielectric5	Dielectric	Prepreg	4.055	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.7		
Bottom Solder	Solder Mask/Co...	Surface Material	0.5	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 17. Layer Stackup

6.3.2 Switching DC-DC Converter

During part placement and routing, always consider the path the current takes through the circuit. The yellow line in Figure 18 shows the path the input current travels from the input capacitor (C43), through the switch in the converter (U4), to the inductor (L18), and then out across the output capacitors (C44 and C45). Any return currents from the input capacitor (C43) or the output capacitors (C44 and C45) are joined together on the top side of the board before they are connected to the ground (return) plane (inside the green circle). This occurrence reduces the amount of return currents in the internal ground plane, which allows other circuits on the board to register voltage gradients. This occurrence may not be noticeable in the performance of the converter, but it does reduce its coupled noise into other devices. Figure 18 shows the layout of the switch-mode power supply with the routing outlined and solid.

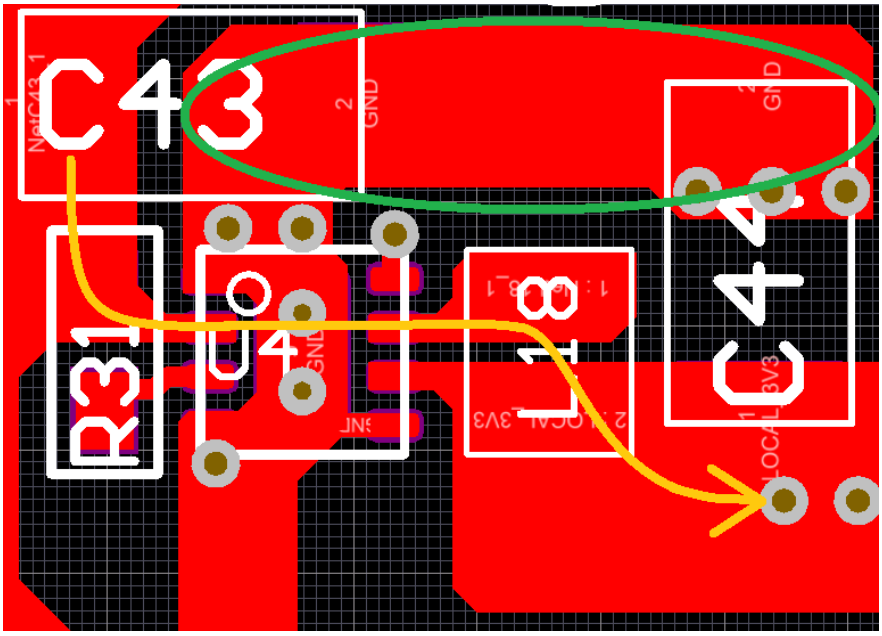


Figure 18. Step-Down Switched-Mode Power Supply Routing

Input capacitors must be placed as close to the integrated circuit (IC) as possible to reduce the parasitic series inductance from the capacitor to the device that it supplies. This placement is especially important for DC/DC converters because the inductance from the capacitor to the high-side switching FET can cause high-voltage spikes and ringing on the switch node, which can be damaging to components and cause problems such as electromagnetic interference (EMI).

6.3.3 Deserializer Layout Recommendations

Both the deserializers require a higher number of power input pins demanding low-noise inputs; therefore, a set of decoupling capacitors and filter ferrite beads were added. The smallest capacitors are placed extremely close to the device or under the device alternatively. The supply pins can be identified due to their wide traces ensuring good power connections. The four differential pairs fanned out to the bottom of Figure 19 are FPD- Link input lanes. Instead, five differential pairs fanned out to the top of Figure 19 are MIPI CSI-2 output lanes. Those traces are very sensitive to layout. It is recommended to keep at least three times the trace width between differential pairs. In addition, avoid sharp turns. Taking rounded corners for traces helps to reduce reflections.

Figure 19 shows the decoupling capacitors to the right and left of the DS90UB960. The loop from 1.8 V to GND is short because of the small capacitor value for high-frequency capacitors and because the accompanying larger capacitors are kept very close to U1, which results in a very-small current loop.

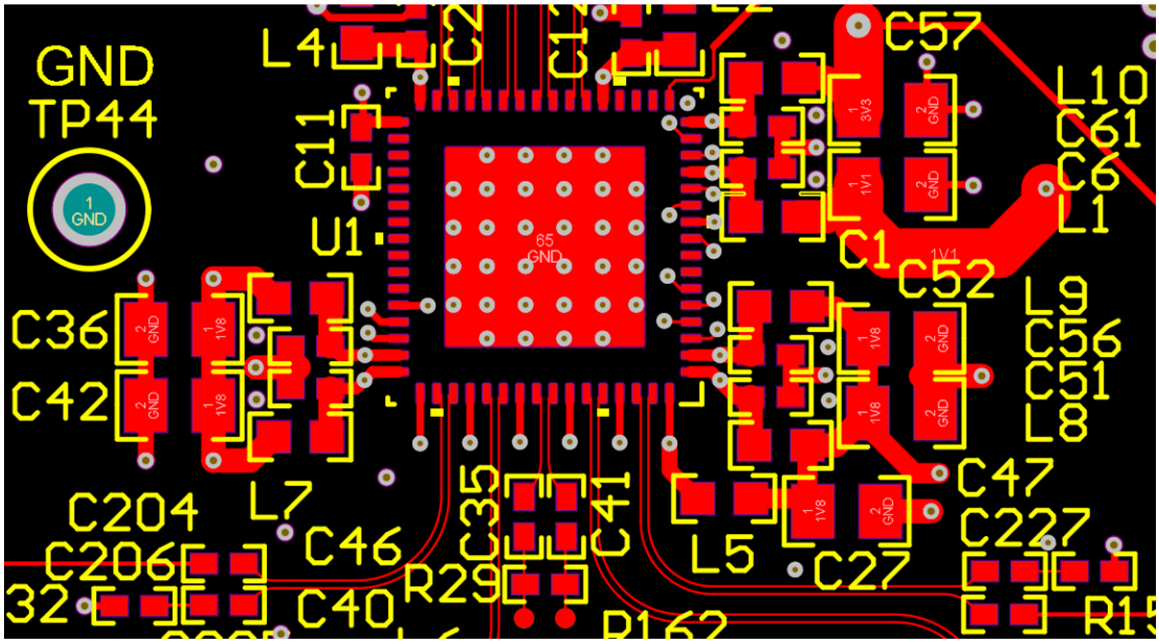


Figure 19. FPD-Link Input, MIPI CSI-2 Differential Pairs, and Decoupling Current Loop

When routing the coaxial input to the PoC filter, be aware of potential signal stubs on the low-voltage differential signaling (LVDS) nets. In Figure 20, the high-speed signal for Camera 1 comes in from J24 and passes through C205 to U1 (DS90UB960). DC is blocked by C205 and the DC current path shown in Figure 21 flows through ferrite beads L48, L43, and L40, which blocks high-frequency AC data and inductor L29, which blocks low-frequency AC data. While the PoC filter is intended to provide the required impedance for the high-speed signal and only pass DC current, the ferrite beads and inductor of the PoC filter, or any copper trace between the high-speed trace and the first ferrite can act as a weak stub. Minimizing the length of this stub reduces reflections on the LVDS lines and leads to better signal integrity. If possible, it is recommended to use the smallest component pad possible for the first ferrite bead that interfaces directly with the high-speed signal path trace. In addition, the high-speed signal path trace from the C205 and C207 AC capacitors must be length- and impedance-matched with each other to reduce reflections.

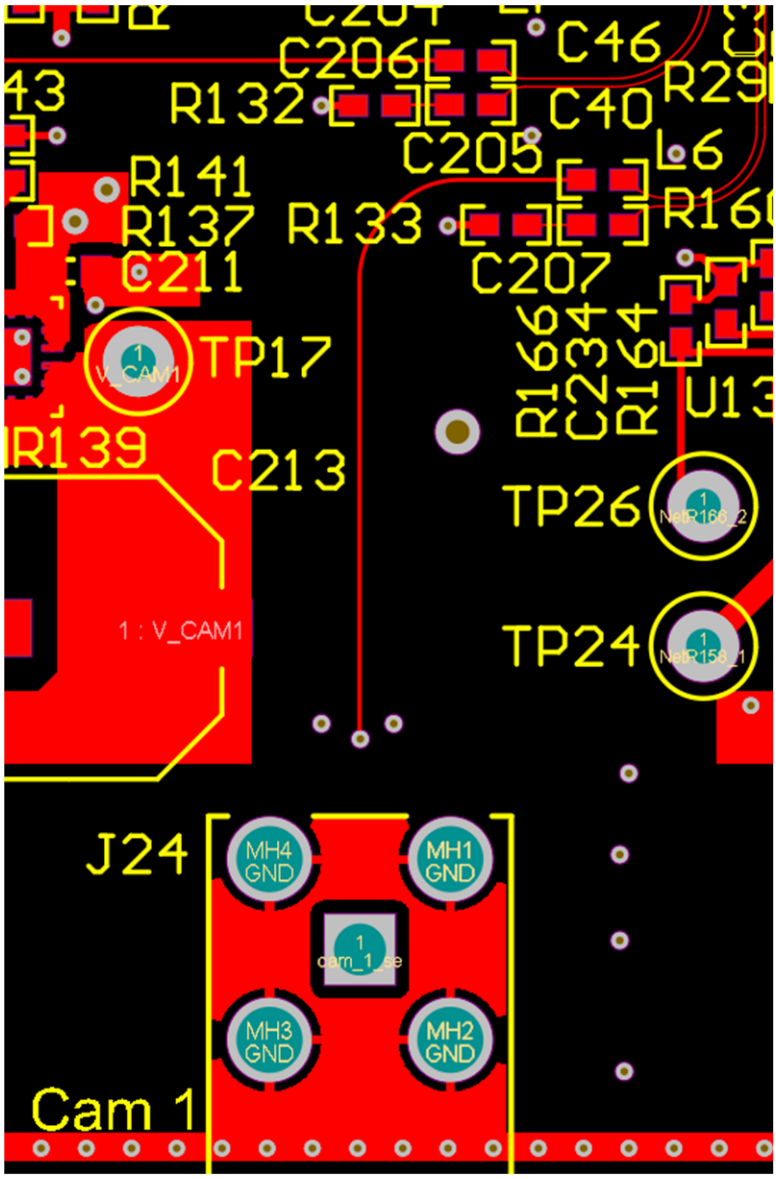


Figure 20. LVDS Signal Pair Routing

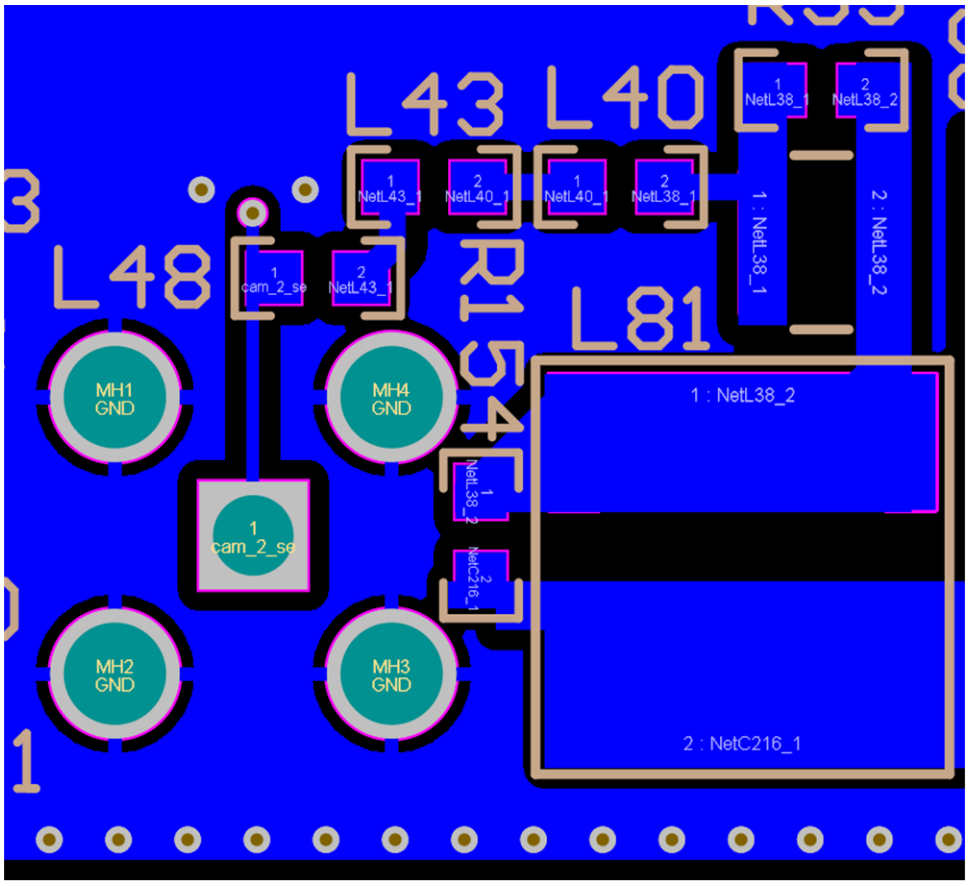


Figure 21. Power Over Coax DC Current Path

The last layout guideline, which is most important, is the CSI-2 routing from TX port 0 and port 1 to the SAMTEC connector for interfacing with TDA2Plus. The following list provides the guidelines for routing the differential CSI-2 traces. Figure 22 shows the routing for the TIDA-01413 and Figure 23 confirms that the routed lengths are within the guidelines for trace length matching within pairs. There is a bit more mismatch between each pair past 25 mils.

1. Route the CSI-2 differential pair traces with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep the length difference between a differential pair to 5 mils of each other.
3. Match the trace lengths between pairs to be < 25 mils.
4. Each pair must be separated by at least three times the signal trace width.
5. Length matching must be near the location of the mismatch.
6. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ≥ 135°. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
7. Route all differential pairs on the same layer.
8. Keep the number of VIAS to a minimum—TI recommends keeping the VIA count to two or fewer.
9. Keep traces on layers adjacent to the ground plane.
10. Do *not* route differential pairs over any plane split.

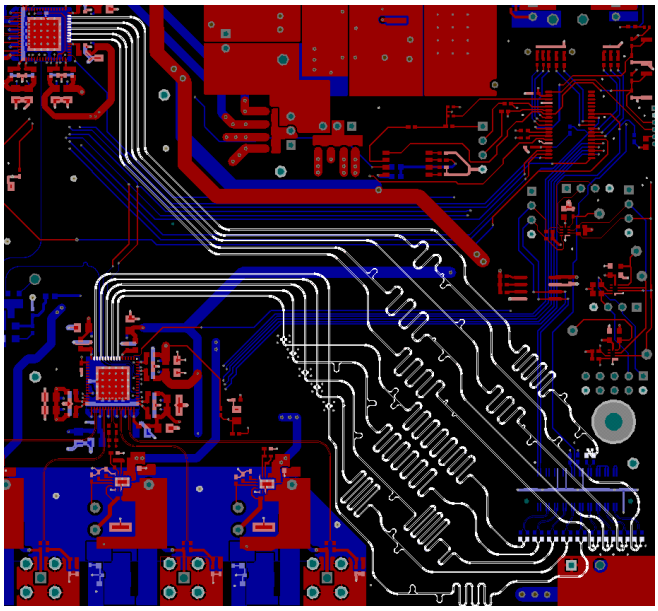


Figure 22. CSI-2 Differential Trace Routing

10 Differential Pairs (0 Highlighted)

Designator	Average Length (...	Longest Signal L...
CAM_CSI0_CLK	7085.642	7088.371
CAM_CSI0_D0	7107.633	7108.186
CAM_CSI0_D1	7125.382	7127.418
CAM_CSI0_D2	7141.103	7141.978
CAM_CSI0_D3	7151.384	7152.115
RADAR_CSI0_CLK	7142.05	7141.212
RADAR_CSI0_D0	7127.548	7126.705
RADAR_CSI0_D1	7110.452	7109.608
RADAR_CSI0_D2	7089.471	7088.684
RADAR_CSI0_D3	7226.771	7225.088

Figure 23. CSI-2 Length Matching

6.4 Layout Prints

To download the layer plots, see the design files at TIDA-01413.

6.5 Altium Project

To download the Altium project files, see the design files at TIDA-01413.

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-01413.

6.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01413.

7 Software Files

To download the software files, see the design files at TIDA-01413.

8 Related Documentation

1. Texas Instruments, *Automotive 2-MP Camera Module Design with MIPI CSI-2 Video Output Interface and POC Reference Design*
2. Texas Instruments, *DS90UB953-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer Data Sheet*
3. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs Application Report*
4. Texas Instruments, *Cable Requirements for the DS90UB913A and DS90UB914A Application Report*
5. Texas Instruments, *High Performance SoCs w/ options for Graphics, Imaging, Video and Vision Acceleration for ADAS)*
6. Texas Instruments, *Processor SDK for TDAx ADAS SoCs - Linux and TI-RTOS Support*

8.1 Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2018) to A Revision **Page**

- Changed *Board—Top View* image 6
- Changed *Board—Bottom View* image 7
- Changed *Decoupling Current Loop* image 23
- Changed *Decoupling Current Loop* image caption to *FPD-Link Input, MIPI CSI-2 Differential Pairs, and Decoupling Current Loop* 23
- Changed ferrite beads L37, L33, and L31 to L48, L43, and L40 23
- Added information regarding the PoC filter 23
- Added recommendation to use the smallest component pad possible for the first ferrite bead that interfaces directly with the high-speed signal path trace 23
- Changed *LVDS Signal Pair Routing* image 24
- Changed *Power Over Coax DC Current Path* image 25

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