

TI Designs: TIDA-01565

Wired OR MUX and PGA Reference Design



Description

This board demonstrates a wired-OR multiplexer (MUX) and a programmable gain amplifier (PGA) application of the OPA837 operational amplifier. These applications are made possible with the high-impedance output of the amplifier and the high-impedance inverting input while in power-down (PD) mode. It is possible to select the output of the MUX or PGA with the onboard dual-inline package (DIP) switches or transistor logic inputs from SMA connectors. The board is single or dual-supply compatible up to 5.25 V. An optional noise filter is included at the output to eliminate broadband noise for PGA designs with lower bandwidth.

Features

- Change between MUX and PGA configurations
- Drive with single or dual supplies
- Supplemental DIP switch input provides simple output selection
- True input to output isolation

Applications

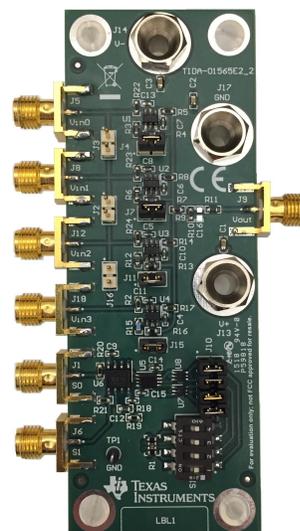
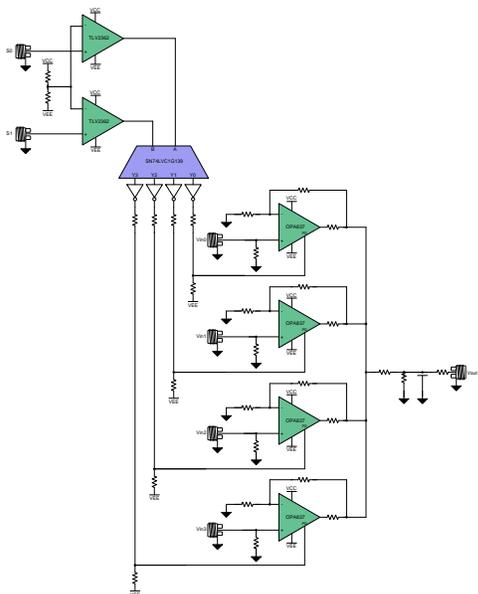
- Wide-Dynamic Range Acquisition System
- Multi-Channel Input Data Acquisition
- Analog Video Multiplexer

Resources

TIDA-01565	Design Folder
OPA837	Product Folder
SN74LVC1G139	Product Folder
SN74LVC2G04	Product Folder
TLV2362	Product Folder



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1 System Description

High-speed analog multiplexers are required in a wide range of applications such as data acquisition, video multiplexing, and so forth. TIDA-01565 is a basic analog multiplexing or programmable gain amplifier circuit using the OPA837. When disabled, an internal switch opens from the inverting input through the active channel, creating isolation between the input and the output. This isolation allows the OPA837 to act as a high-speed analog MUX.

A PGA is an amplifier where the gain can be externally controlled instead of using a single preset gain. This board supports this using the OPA837 devices as a PGA by tying the inputs together. Setting different gain settings for each OPA837 allows the user to have a PGA with four different gain settings. Similarly to controlling the MUX channel output, the gain setting is controlled by selecting which device turns on from the onboard DIP switch or controlling S0 and S1. For more details on configuring the board for PGA mode, see [Section 4.2.1.2](#).

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input power source	± 2.5 V
Unity-gain bandwidth	105 MHz
Gain bandwidth product	50 MHz
Turnon time delay	300 ns
Turnoff time delay	100 ns
Multiplexer	4:1

2 System Overview

2.1 Block Diagram

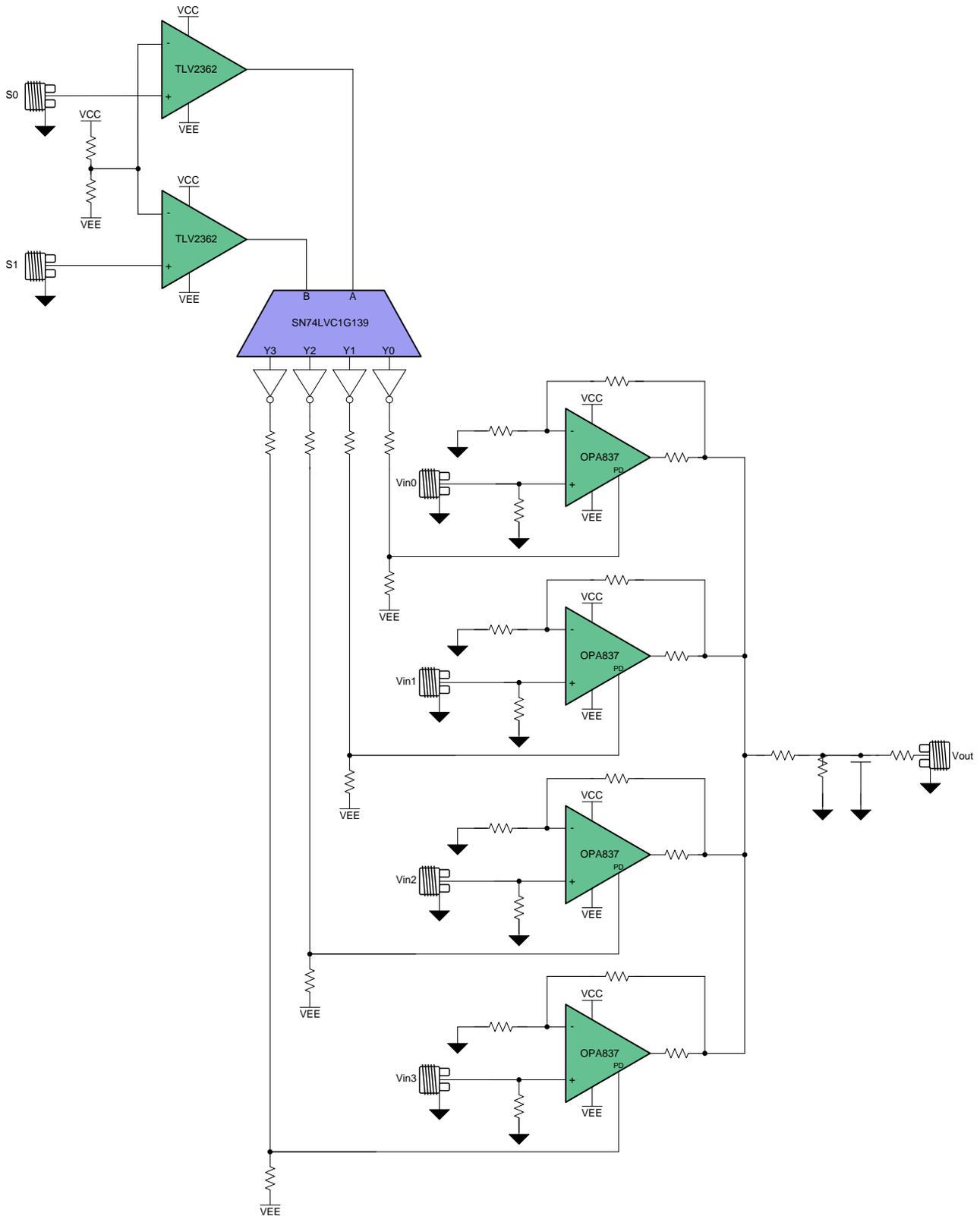


Figure 1. TIDA-01565 Block Diagram

2.2 Highlighted Products

2.2.1 OPA837

- Bandwidth: 105 MHz ($A_V = 1$ V/V)
- Very Low (Trimmed) Supply Current: 600 μ A
- Gain Bandwidth Product: 50 MHz
- Slew Rate: 105 V/ μ s
- Negative Rail Input, Rail-to-Rail Output
- Single-Supply Operating Range: 2.7 V to 5.4 V
- 25°C Input Offset: ± 130 μ V (Maximum)
- Input Offset Voltage Drift (DCK Package): $< \pm 1.6$ μ V/°C (Maximum)
- Input Voltage Noise: 4.7 nV/ $\sqrt{\text{Hz}}$ (> 100 Hz)
- HD2: -120 dBc at 2 VPP, 100 kHz
- HD3: -145 dBc at 2 VPP, 100 kHz
- Settling Time: 35 ns, 0.5-V Step to 0.1%
- 5- μ A Shutdown Current With Fast Recovery From Shutdown for Power-Scaling Applications
- Built-In Disable PD Pin
- When the device is powered down, the internal switch opens the inverting input

2.2.2 SN74LVC1G139

- A logic low 2-to-4 line decoder or demultiplexer
- Controls all four PD pins on the OPA837
- Short propagation delay times

2.2.3 SN74LVC2G04

- Dual inverter gate
- Inverts the logic from the SN74LVC1G139 to a logic high rather than a logic low

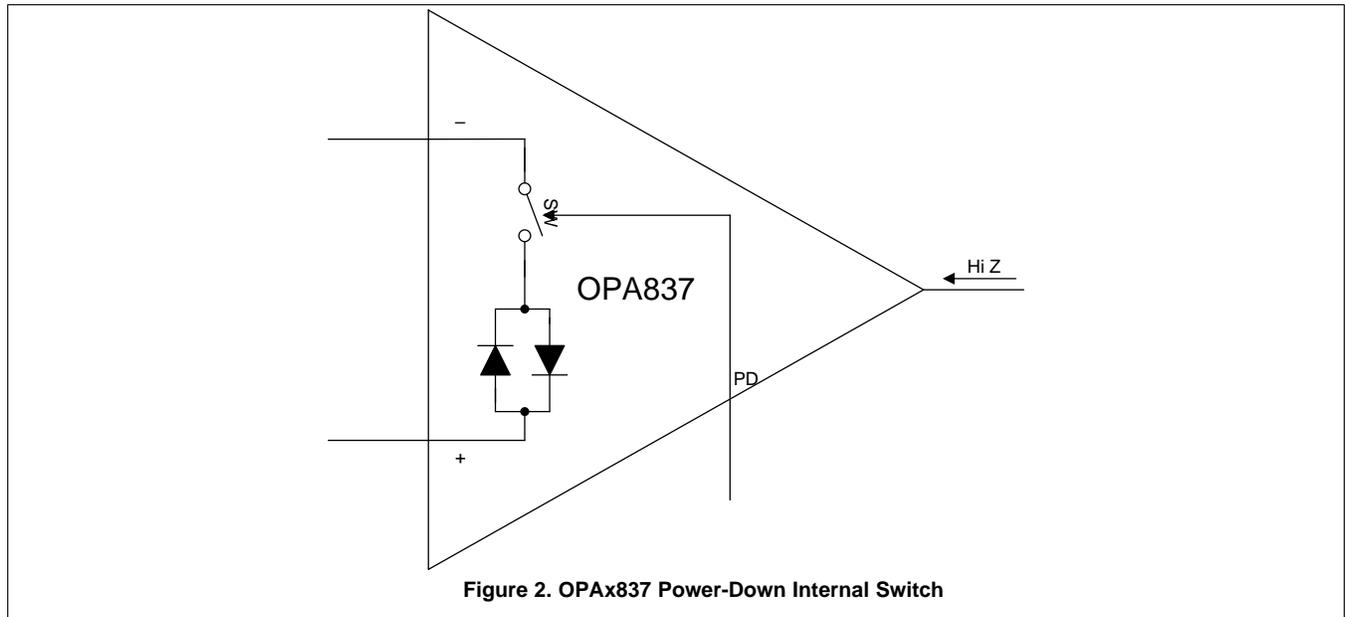
2.2.4 TLV2362

- Wide Bandwidth
- Wide Output Voltage Swing
- High Slew Rate

3 System Design Theory

3.1 OPA837 Power-Down

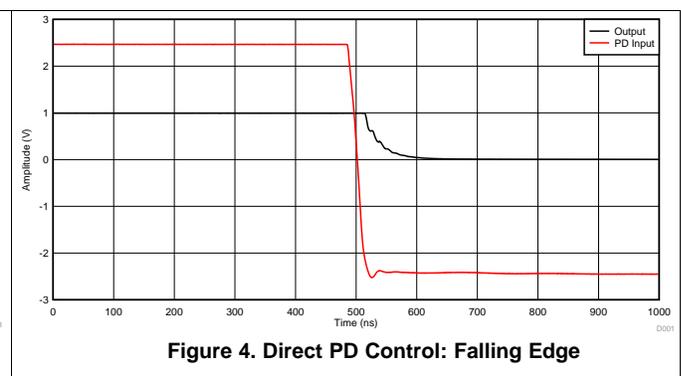
The OPA837 is selected because the device isolates the output from the signal in PD mode. Unlike most high-speed op amps that have a PD function place a high-impedance on only on the output when the amplifier is disabled, the OPA837 places a high-impedance on the output as well as an internal switch opening on the inverting input as seen in Figure 2. This creates true input to output isolation.



The turnon and turnoff time delay varies slightly from device to device. The turnoff time must be faster than the turnon time. This helps prevent two of the OPA837 devices from operating at the same time and prevents any possible damage.

To enable the OPA837, the PD pin must be higher than 1.5 V above the negative voltage rail.

Figure 3, Figure 4, and Figure 5 show that the output of the amplifier has little delay when a single ± 2.5 -V pulse is inserted into the PD pin of the OPA837. Figure 3 shows that the OPA837 output as a high voltage spike before settling down. Section 4.2.2 shows that this causes a noticeable distortion to the signal.



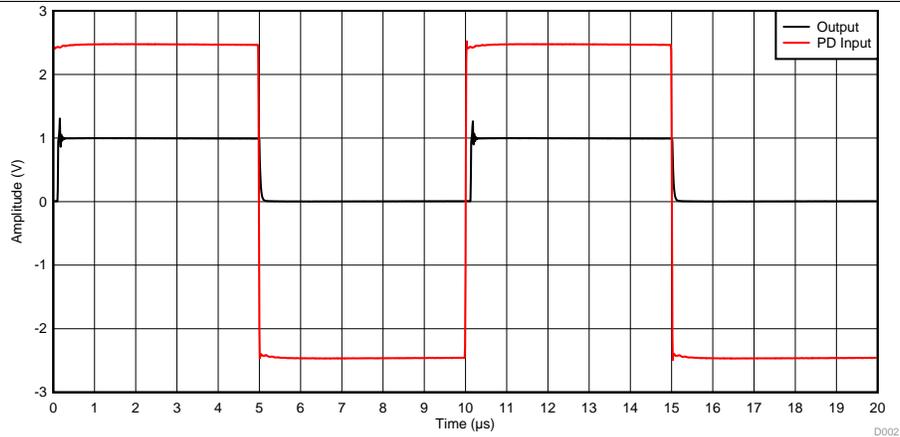


Figure 5. Direct PD Control: Full Pulse

3.2 Power-Down Control Circuit

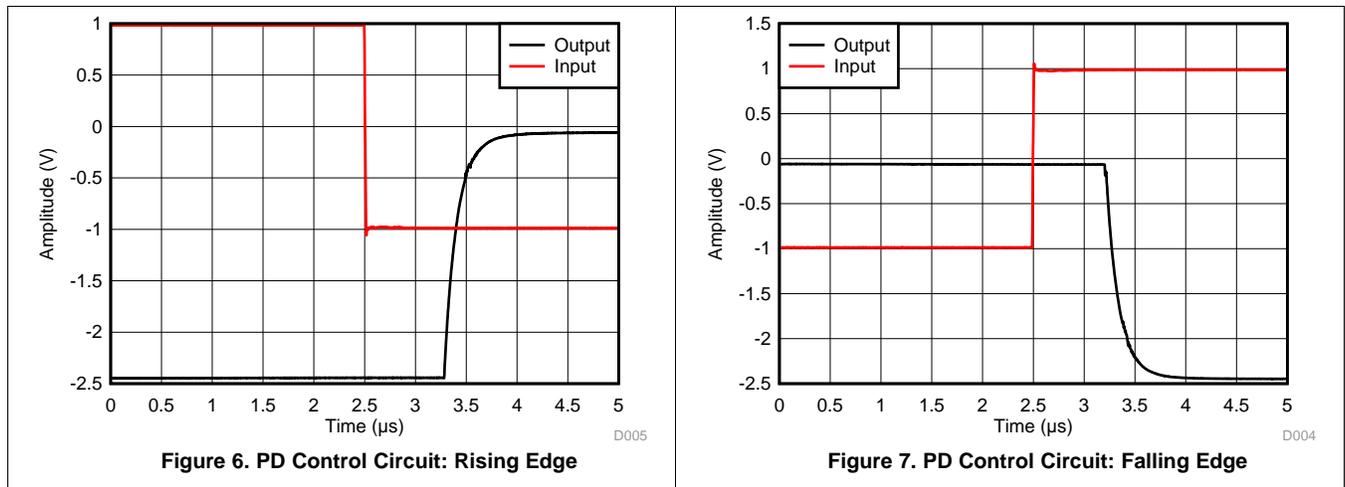
The PD control circuit is essential to switch between the four OPA837 devices. The device has a 4-bit switch, but the SMA input logic control is more practical for a system with a microcontroller to control switching.

Using this built-in circuit, two inputs (S0 and S1) are required to control all four channels because of an onboard 2-to 4-bit demultiplexer. The SN74LVC1G139 has a logic low output, so an inverter along the signal path is required to output a logic high. Table 2 lists the truth table for the system after the inverters.

Table 2. Power-Down Control Circuit Truth Table

S1	S0	CHANNEL THAT PASSES ARGUMENT
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

The results in Figure 6 and Figure 7 were achieved by applying a ± 1 -V 100-kHz input signal on S0 while leaving S1 floating. The output is taken on the output of the SN74LVC2G04 inverters. As shown in Section 3.1, the OPA837 must have a voltage applied to the PD pin that is 1.5 V above the negative voltage rail to turn on. In this case, 0 V satisfies this parameter and the device powers on. This circuit introduces a delay to the PD response of approximately 0.7 μ s to 0.8 μ s.



3.3 Different Configurations

3.3.1 MUX Operation

The TIDA-01565 is configured as a MUX with the support of up to four channels. The default is set to unity gain but can change based on system requirements. At unity gain, the system has a small-signal bandwidth of 105 MHz. [Figure 8](#) shows a simplified block diagram of the MUX circuit.

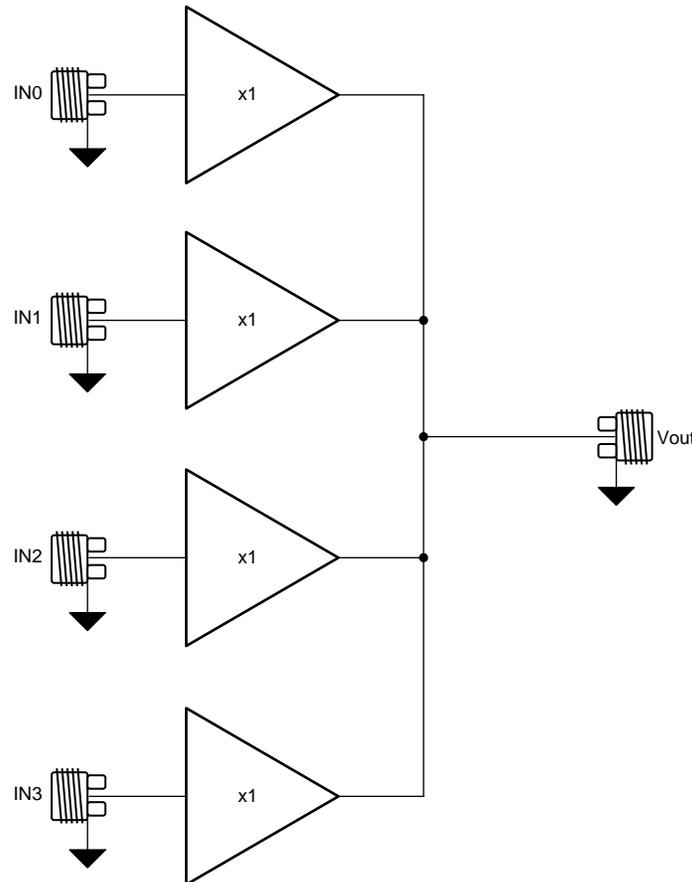


Figure 8. MUX-OR Block Diagram

3.3.2 PGA Operation

PGA operations are similar to the MUX operations described above except with two differences:

- The inputs are tied together, so the system requires one input.
- Generally, the OPA837 is set up with a different gain setting for each channel.

[Figure 9](#) shows a simplified block diagram of the PGA mode with arbitrary gain settings.

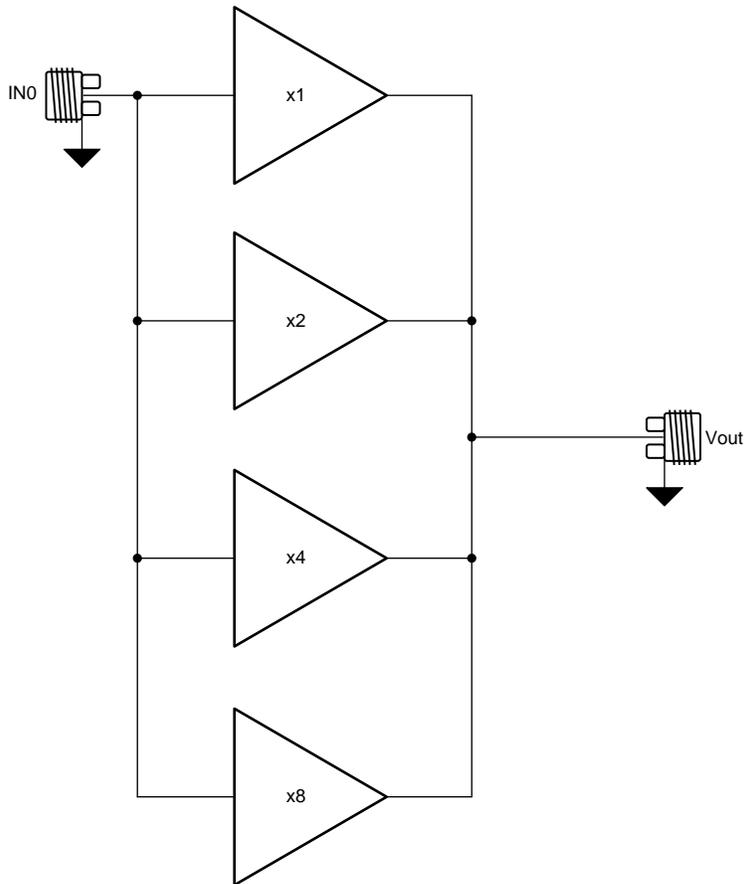


Figure 9. PGA Block Diagram

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Required Hardware

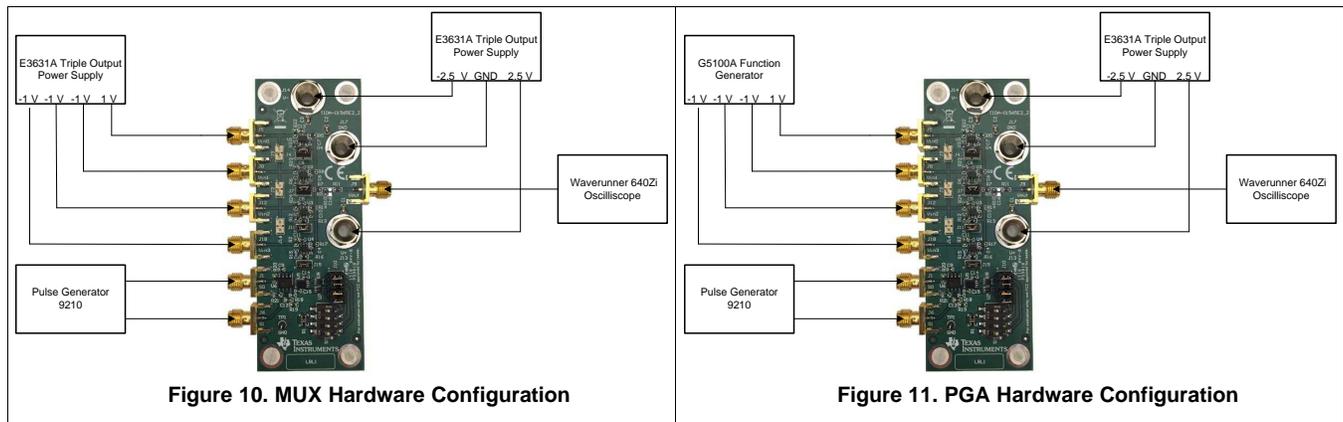
Table 3 lists the connector designator and the connector type.

Table 3. Connector Details for TIDA-01565

CONNECTOR	TYPE OF CONNECTOR
J13	V+
J14	V-
J17	GND
J5, J8, J12, J18	Inputs (Vin0, Vin1, Vin2, Vin3)
J9	Output (Vout)
J1, J6	PD control inputs (S0, S1)
J10	Switch isolator jumpers
J2, J3, J16	Input tie jumpers
J4, J7, J11, J15	Unity-gain jumpers

4.2 Testing and Results

Figure 10 and Figure 11 show the hardware setup diagram for evaluating the reference design for MUX operations and PGA operations, respectively. A **Lecroy** Pulse Generator 9210 generates two ± 1 -V, 100-kHz square wave to control S0 and S1. A generic dual or triple DC power supply generates a ± 2.5 -V supply voltage. The PGA tests use a G5100A function generator. For the MUX tests, a 1-V supply was connected to Vin0 and a -1 -V supply was connected to Vin1, Vin2, and Vin3 to show the switching behavior. To show the full output swing without attenuating the output, set the oscilloscope to 1 M Ω and set the output resistor with a 20-k Ω to ground.



4.2.1 Test Setup

Switches or logic can control the MUX or PGA. To use the switches, disconnect the four jumpers in J10 and ensure all four switches in S1 are OFF before applying power. Then, switch on one amplifier at a time. There are make-before-break protection resistors to protect the amplifiers from damage if two are switched on at the same time. To use the logic, set all switches in S1 to OFF and connect the first two jumpers on S1. Use a logic signal to select channels 1 or 2 using SMA input J16. The logic input comparator supports single-supply 2-V to 5-V logic and ± 2.5 -V dual-supply logic.

To analyze resistive and capacitive load driving, use R9, R10, R11, and C16 for loading and measurement impedance matching. As shown in Figure 12 to directly connect to an ADC, remove R10 and replace R9 with a 0- Ω resistor and then connect the output to the input of an ADC filter. As an alternative option, configure R9 and C16 as the input filter for the ADC.

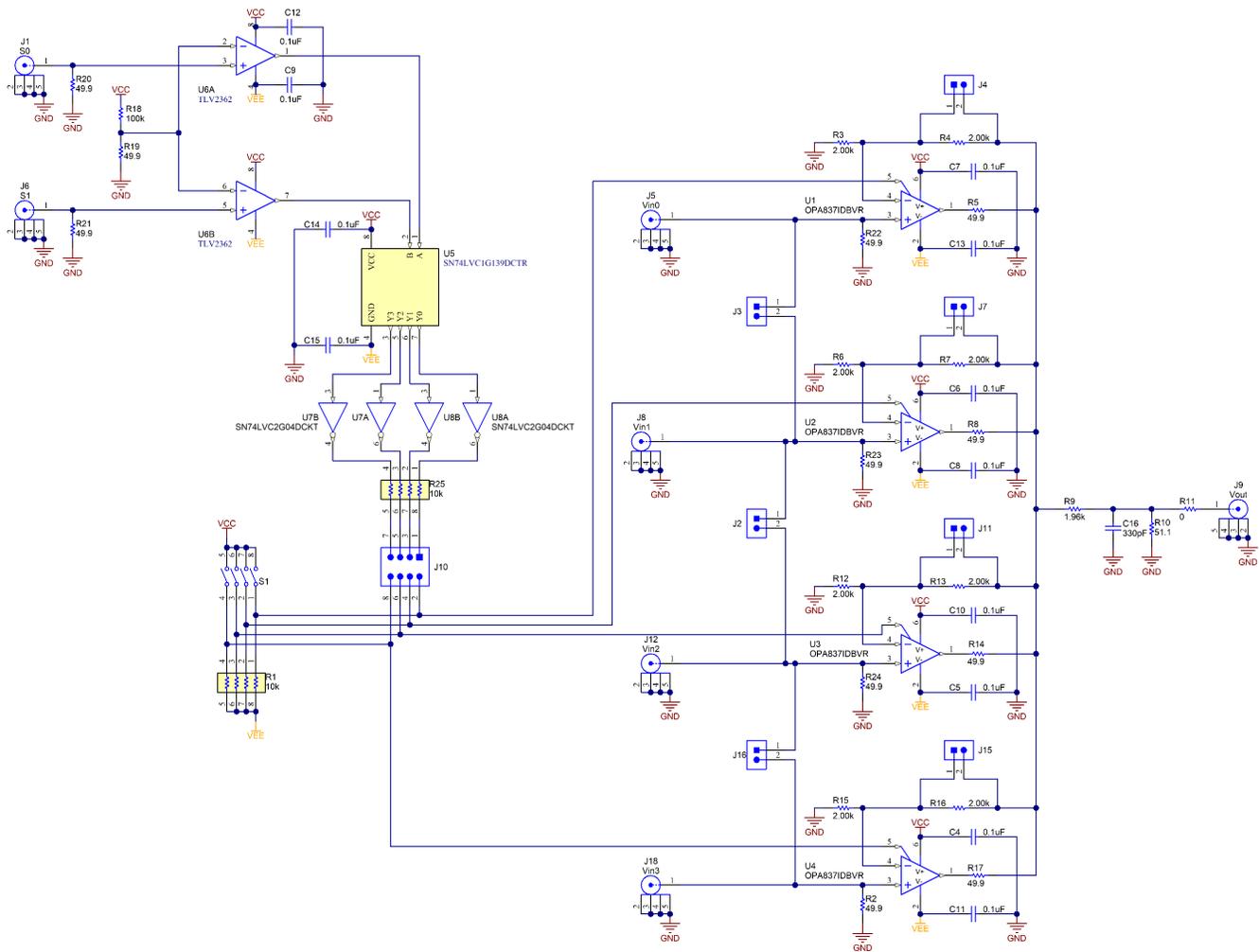


Figure 12. TIDA-01565 Schematic

4.2.1.1 MUX Test Configuration

For use as a MUX mode:

- Connect four input SMA cables to Vin0, Vin1, Vin2, and Vin3.
- Remove jumpers J2, J3, and J16 because these cables short the inputs.

This MUX is used as a buffer or with gain. To use as a buffer, connect feedback-shorting jumpers J4, J7, J11, and J15. To use with gain, remove these jumpers and select the appropriate feedback resistor values for R4, R8, R13, and R16. Select the appropriate gain resistor values for R3, R6, R12, and R16.

Table 4 lists the jumper configuration for unity-gain MUX mode.

Table 4. Jumper Configuration (MUX-OR Mode)

JUMPER	CONNECTION
J2	OPEN
J3	OPEN
J4	SHORTED
J7	SHORTED
J11	SHORTED

Table 4. Jumper Configuration (MUX-OR Mode) (continued)

J15	SHORTED
J16	OPEN

4.2.1.2 PGA Test Configuration

For use as a PGA mode:

- Connect one input SMA cable to Vin0, Vin1, Vin2, or Vin3.
- Connect jumpers J2, J3, and J16 to short the inputs.
- Remove jumpers J4, J7, J11, and J15.
- Select the desired feedback and gain resistors for each amplifier.

[Table 5](#) lists the PGA mode jumper configurations.

Table 5. Jumper Configuration (PGA Mode)

JUMPER	CONNECTION
J2	Shorted
J3	Shorted
J4	Open
J7	Open
J11	Open
J15	Open
J16	Shorted

4.2.2 Test Results

4.2.2.1 MUX Operation Results

The gain settings for all four channels are set in unity gain as [Figure 8](#) shows. Input Vin0 had 1 V applied to the input while Vin1, Vin2, and Vin3 had -1 V applied to the inputs. To see all four channels switching effects, ± 1 -V, 100-kHz pulses were applied to the S0 and S1 inputs. The S1 input had a 2.5-ns delay. [Figure 13](#) shows the output of the OPA837 MUX function as different channels are selected. The high frequency transient spikes are caused by the internal power down circuitry switching and can be eliminated by post-filtering. 1 V is applied to the input of Vin0 and -1 V is applied to the inputs of Vin1, Vin2, and Vin3.

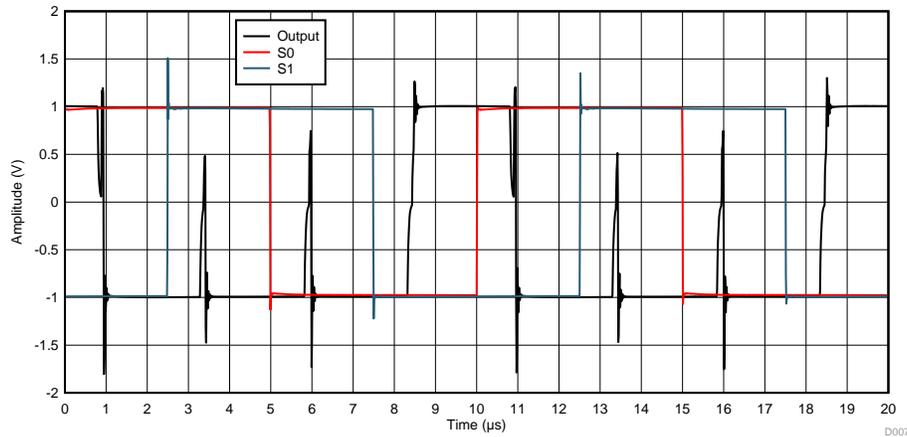


Figure 13. MUX-OR Operation Results

4.2.2.2 PGA Operation Results

During the PGA operation test, a 1-MHz, $1-4 V_{pp}$ signal is applied to the input. [Figure 9](#) shows the gain settings for this circuit. For this test, the channels are set to the following values:

- Channel 1: Unity Gain
- Channel 2: Gain of 2
- Channel 3: Gain of 4
- Channel 4: Gain of 8

± 1 -V, 100-kHz pulses were applied to the S0 and S1 inputs to control which output can be viewed. The S1 input has a delay of 2.5 ns. [Table 6](#) lists the truth table for the PGA output in this configuration.

Table 6. PGA Test Truth Table

S1	S0	Gain on Output
0	0	$\times 1$
0	1	$\times 2$
1	0	$\times 4$
1	1	$\times 8$

Figure 14 shows the output of the PGA switching between the different gain settings. Similar to the MUX function, the high frequency transient spikes are caused by the internal power down circuitry switching and can be eliminated with post-filtering.

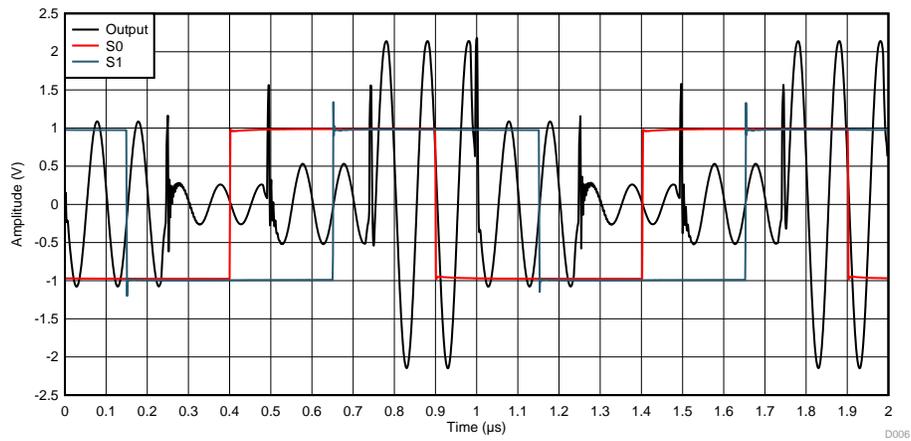


Figure 14. PGA Operation Results

5 Design Files

5.1 Schematics

To download the schematics, see the design files at [TIDA-01565](#) .

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01565](#) .

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01565](#).

5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01565](#).

5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01565](#).

5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01565](#).

6 Software Files

To download the software files, see the design files at [TIDA-01565](#).

7 About the Authors

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