TI Designs: TIDA-01453
MIPI® DSI to OLDI/LVDS Bridge Reference Design for Automotive Infotainment Head Unit

TEXAS INSTRUMENTS

Description

This reference design offers two display interface options: an Automotive processor with MIPI® DSI output and an Automotive infotainment video display panel with OpenLDI (OLDI) / LVDS input The reference design provides two variations. Setup one converts the system on chip (SoC) DSI video output signal to OLDI/LVDS video signal then connects directly to the panel for an integrated display application. Setup two adopts FPD-Link III SerDes technology to transmit the OLDI/LVDS video signal and I²C control signal to the panel over a long cable for a remote display application.

Resources

TIDA-01453	Design Folder
SN65DSI85EVM	Product Folder
DS90UB947-Q1EVM	Product Folder
DS90UB948-Q1EVM	Product Folder

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Features

- First to Market AEC-Q100 Automotive Qualified Dual-channel MIPI DSI to Dual-link OLDI/LVDS Bridge
- Supports up to 154-MHz OLDI/LVDS Output Clock in Dual-link Mode
- Supports up to 24-bpp DSI Video Packets With RGB888 Formats
- Supports up to 60-fps WQXGA 2560 × 1600 Resolution at 24-bpp Color
- Supports up to 15 m Coaxial or STP Cable
- Offers Two Setups: Setup One Direct To Panel and Setup Two Using FPD-Link III Chipset

Applications

- Automotive Head Units With Integrated Display
- Automotive Head Units With Remote Display
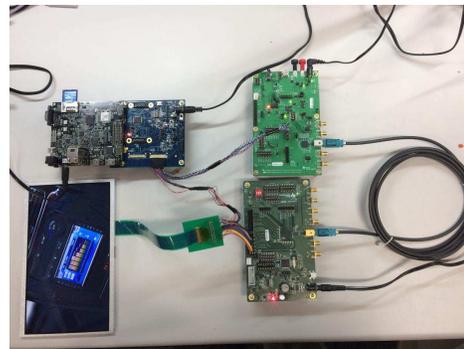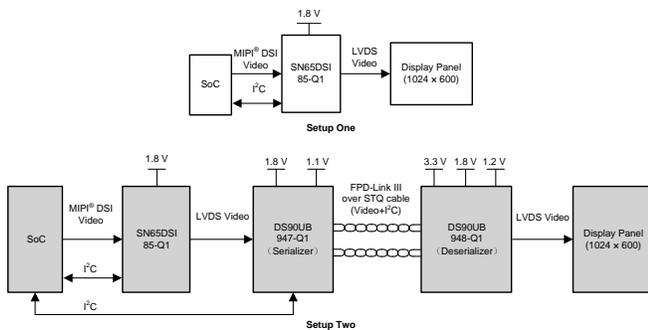
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1 System Description

In Automotive infotainment display applications, Automotive processors tend to integrate MIPI DSI output interface; however, most of the Automotive video display panels only take OLDI/LVDS inputs. To solve this problem, an AEC-Q100 Automotive qualified bridge is needed to convert MIPI DSI video signal to OLDI/LVDS video signal.

This TIDA-01453 TI design addresses this requirement by linking a SoC with MIPI DSI output directly to a display panel with OLDI/LVDS input for integrated display application, or incorporating FPD-Link III chipset between SoC and the display panel for remote display application.

This reference design combines existing EVMs and provides two variations: setup one connects the SN65DSI85-Q1 EVM directly to the display panel, and setup two connects the SN65DSI85-Q1 EVM to the display panel with a pair of DS90UB947-Q1 and DS90UB948-Q1 EVMs over a long cable.

1.1 Key System Specifications

This reference design is configured to interface an SoC with a 24-bpp single-channel DSI output to a display panel with a 18-bpp single-link OLDI/LVDS input, which supports 1024 × 600 resolution at 60 frames per second. For different DSI and OLDI/LVDS channel configuration requirements, SN65DSI85-Q1 can be easily replaced by SN65DSI83-Q1 (single-channel DSI to single-link OLDI/LVDS bridge) or SN65DSI84-Q1 (single-channel DSI to dual-link OLDI/LVDS bridge) as these devices are pin-to-pin compatible. Note that configuration for SN65DSI85-Q1 is the same for setup one and setup two.

Table 1 gives the key system specifications. Following the system configuration guidelines in Section 2.3, this reference design can be easily extended for dual-channel and higher-resolution applications.

Table 1. Key System Specifications

DESIGN PARAMETER	VALUE
Power supply for SN65DSI85-Q1	1.8 V
Power supply for DS90UB947-Q1	1.8 V and 1.1 V
Power supply for DS90UB948-Q1	3.3 V, 1.8 V, and 1.2 V
DISPLAY PANEL INFORMATION	
OLDI/LVDS Clock frequency	50.4 MHz
Resolution	1024 × 600
Frame rate	60 Hz
Horizontal active (HActive)	1024 pixels
Horizontal sync pulse width (HSPW)	136 pixels
Horizontal back porch (HBP)	160 pixels
Horizontal front porch (HFP)	24 pixels
Horizontal total (HTotal)	1344 pixels
Vertical active (VActive)	600 lines
Vertical sync pulse width (VSPW)	3 lines
Vertical back porch (VBP)	22 lines
Vertical front porch (VFP)	0 lines
Vertical total (VTotal)	625 lines
Horizontal sync pulse polarity	Negative
Vertical sync pulse polarity	Negative
Data enable polarity	Positive
Color bit depth	6-bit (18-bpp)
Number of OLDI/LVDS lanes	1 × [3 data lanes + 1 clock lane]
DSI INFORMATION	
Number of DSI lanes	1 × [4 data lanes + 1 clock lane]
DSI video packet	RGB888 (24-bpp)
Dual DSI configuration (odd/even or left/right)	—

Table 1. Key System Specifications (continued)

DESIGN PARAMETER	VALUE
FPD-LINK III INFORMATION	
Cable type	STQ cable with HSD connectors
Cable length	3 m

MIPI® DSI to OLDI/LVDS Bridge Reference Design for Automotive Infotainment Head Unit 3

2   System Overview

2.1   *Block Diagram*

Figure 1 and Figure 2 show the two setup block diagrams of the design:

- Setup one: SoC to SN65DSI85-Q1 EVM to display panel
- Setup two: SoC to SN65DSI85-Q1 EVM to DS90UB947-Q1 EVM and DS90UB948-Q1 EVM to display panel
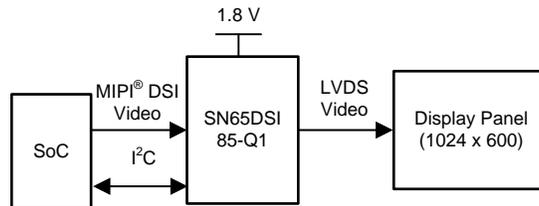
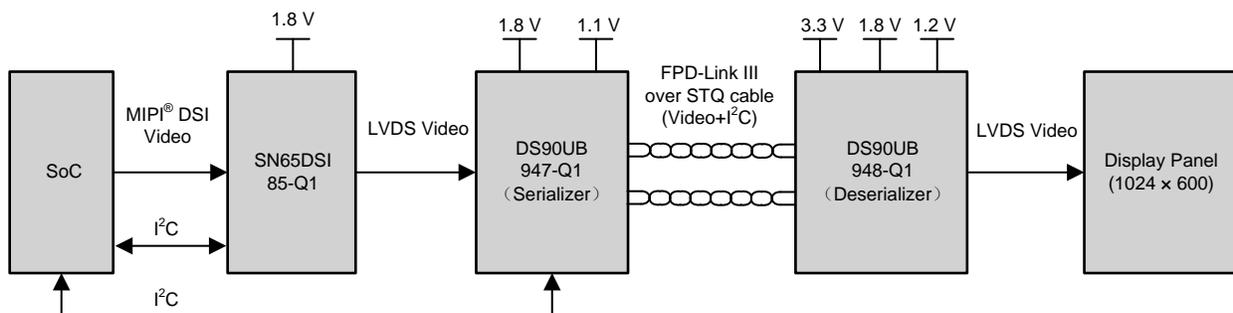**Figure 1. Setup One: SOC With DSI Output Directly Driving OLDI/LVDS Panel**

Figure 2. Setup Two: SOC With DSI Output Driving Remote Display Over Single Twisted Pair Cable

2.2   *Design Considerations*

2.2.1   Setup One: Integrated Display Considerations

Setup one is aimed at Automotive integrated display applications. This setup connects SoC and display panel directly using SN65DSI85-Q1 EVM.

2.2.1.1   *Display Panel Requirements*

The first step to designing the system is to check the display panel's datasheet for key specifications such as resolution, link mode (dual- or single-link), color bit depth (24-bpp or 18-bpp), timing parameters, and so on. Next complete the following calculations based on the requirements of the display panel:

- Calculate total horizontal pixels:
  HTotal = HActive + HSPW + HBP + HFP
- Calculate total vertical lines:
  VTotal = VActive + VSPW + VBP + VFP
- Calculate needed pixel clock:
  Pixel_Clock = HTotal × VTotal × Frame_Rate
- Calculate needed OLDI/LVDS clock:
  OLDI/LVDS_Clock = Pixel_Clock ÷ i (i=1 for single-link, i=2 for dual-link)
- Calculate necessary line time (HSync-to-HSync time):
  Line_Time = HTotal ÷ Pixel_Clock

In this reference design, a display panel with 18-bpp single-link OLDI/LVDS input, which supports 1024 × 600 resolution at 60 frames per second, is adopted. Table 1 lists the key system specifications. Calculation results can be derived based on the panel specifications.

HTotal = 1024 + 136 + 160 + 24 = 1344 pixels

VTotal = 600 +3 + 22 + 0 = 625 lines

Pixel_Clock = 1344 × 625 × 60 = 50.4 MHz

OLDI/LVDS_Clock = 50.4 ÷ 1 = 50.4 MHz

Line_Time = 1344 ÷ 50.4 = 26.6 µs

2.2.1.2   DSI Output Requirements

The DSI output requirements can be derived from the calculation results in Section 2.2.1.1. Note that the maximum DSI data rate per lane is 1 Gbps while maximum DSI clock is 500 MHz.

- Calculate necessary total DSI throughput:
  Total_DSI_Throughput = Pixel_Clock × (18-bpp or 24-bpp)
- Calculate minimum numbers of DSI data lanes:
  Min_DSI_ DataLane _Numbers = Total_DSI_Throughput ÷ 1Gbps
- Calculate minimum DSI clock:
  Min_DSI_Clock = Total_DSI_Throughput ÷ DSI_ DataLane _Numbers ÷ 2

If Min_DSI_DataLane_Numbers > 4, dual-channel DSI output is required.

Based on these formulas, DSI requirements of this reference design can be calculated as:

Total_DSI_Throughput = 50.4 × 24 = 1.2096 Gbps

Min_DSI_ DataLane _Numbers = 1.2096 Gbps ÷ 1 Gbps = 2

- This result means two or more DSI data lanes are required. For this reference design, four DSI data lanes plus one DSI clock lane are adopted.

Min_DSI_Clock = 1.2096 Gbps ÷ 4 ÷ 2 = 151.2 MHz

- This result is used as the DSI clock.

Based on above analysis, four DSI data lanes with a 151.2-MHz DSI clock will meet the display panel's requirements. The DSI line time should match 26.6 µs.

2.2.2   Setup Two: Remote Display Considerations

Setup two is aimed at Automotive remote display application. Aside from the considerations described in Section 2.2.1, more considerations are required in remote display application.

2.2.2.1   Why FPD-Link III?

For remote display application, long cables are typically required for the video transmission. If a 24-bpp dual-link display panel is adopted, the panel will require at least ten pairs of long cables for a direct connection, which significantly increases the system cost. TI FPD-Link III SerDes technology enables the transport of high-definition digital video as well as a bidirectional control channel over a low-cost twisted pair or coax cable, which in turn reduces cable weight and simplifies the physical connection.

2.2.2.2   Cable Requirements

Automotive cables and connectors were defined by 1394 Trade Association. However, this definition did not become an industry standard. Therefore, there is no cable standardization for Automotive.

Figure 3 shows typical Automotive cables and connectors, which include:

- Shielded-twisted quad (STQ): Two differential pairs; uses high-speed data (HSD) connectors
- Shielded-twisted pair (STP): One differential pair; uses Molex® HSAL II (HSAutoLink II™) connectors
- Coax: uses FAKRA connectors

A variety of cable assemblies meeting this generic description are available on the market, but not all perform equally. For DS90UB947-Q1 and DS90UB948-Q1 chipset, Table 2 and Table 3 show the cable characteristics to be considered.

Insertion loss describes the attenuation of a signal after it has traversed the length of the cable. Return loss describes the reflected energy from a transmitted signal. The greater the impedance discontinuities, the higher the return loss value.

For this reference design, a 3-meters STQ cable with HSD connector is adopted.
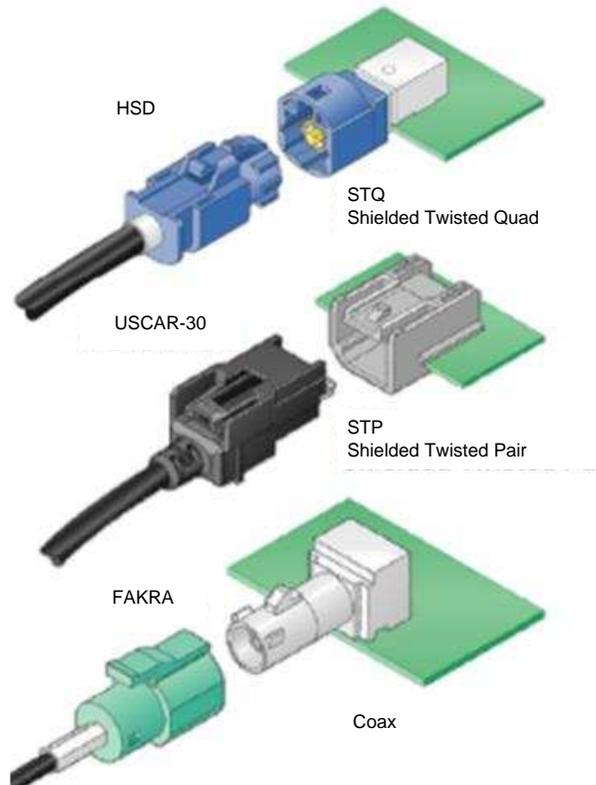
Figure 3. Automotive Cables and Connectors

Table 2. DS90UB947-Q1, DS90UB948-Q1 Cable Requirements One

CABLE TYPE	STQ	STP	COAX
Maximum cable length	10 m	10 m	15 m
Characteristic resistance	Differential 100 Ω ± 10%		Single-ended 50 Ω ± 10%

Table 3. DS90UB947-Q1, DS90UB948-Q1 Cable Requirements Two

FREQUENCY	100 MHz	450 MHz	660 MHz	800 MHz	1.5 GHz	2.5 GHz
Return loss	–20 dB	–15 dB	–13 dB	–10 dB	–9 dB	–9 dB
Insertion loss	–27dB at 1.5 GHz					

2.2.3 Highlighted Products

This reference design features the SN65DSI85-Q1, DS90UB947-Q1, and DS90UB948-Q1 devices.

2.2.3.1 *SN65DSI85-Q1*

The SN65DSI8x-Q1 product family is the first AEC-Q100 Automotive qualified MIPI DSI to OLDI/LVDS bridges in the market. The devices are all pin-to-pin compatible and can be adopted between the SoC with DSI output and the display panel with OLDI/LVDS inputs. Table 4 summarizes the feature sets of this product family.

Table 4. SN65DSI8x-Q1 Product Family Features Summary

PART NUMBER	DESCRIPTION	MAXIMUM RESOLUTION
SN65DSI83-Q1	Single-channel DSI to single-link OLDI/LVDS	Suitable for 1366 × 768 60 fps at 24-bpp or 18-bpp Maximum resolution up to 1920 × 1200 60 fps at 24-bpp with reduced blanking
SN65DSI84-Q1	Single-channel DSI to dual-link OLDI/LVDS	1920 × 1200 60 fps at 24-bpp or 18-bpp
SN65DSI85-Q1	Dual-channel DSI to dual-link OLDI/LVDS	2560 × 1600 60 fps, 1920 × 1080p 120 fps at 24-bpp or 18-bpp

This reference design uses the SN65DSI85-Q1. Aside from the features listed in Table 4, other key features of SN65DSI85-Q1 include:

- Implements MIPI D-PHY version 1.00.00 physical layer front end and DSI version 1.02.00
- Dual-channel DSI receiver configurable for one, two, three, or four D-PHY data lanes per channel operating at up to 1 Gbps per lane
- Supports dual-channel DSI odd or even and left or right operating modes
- OLDI/LVDS output clock range of 25 MHz to 154 MHz in dual-link or single-link mode
- OLDI/LVDS pixel clock may be sourced from free-running continuous D-PHY clock or external reference clock
- Low-power features include SHUTDOWN mode, reduced OLDI/LVDS output voltage swing, common mode, and MIPI ultra-low power state (ULPS) support
- OLDI/LVDS channel SWAP, OLDI/LVDS pin order reverse feature for ease of PCB routing
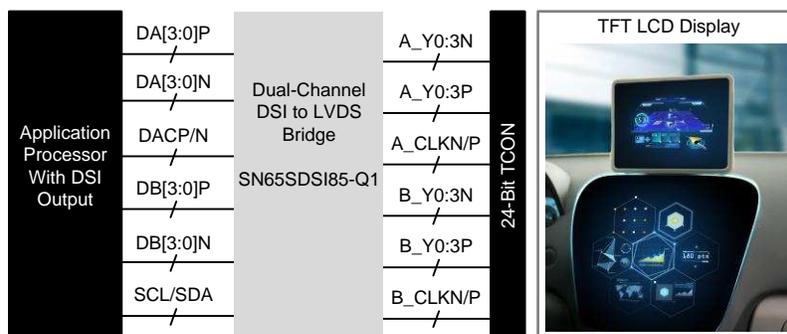
Refer to [1] [2] [3] for more details.

Figure 4. SN65DSI85-Q1 Typical Application

2.2.3.2   DS90UB947/8-Q1

The FPD-Link III interface supports video and audio data transmission and full duplex control, including I²C and SPI communication, over the same differential link.

The DS90UB947-Q1 is an OpenLDI-to-FPD-Link III serializer that takes the data from OpenLDI serial stream and translates the data into either a single- or dual-lane FPD-Link III interface.

The DS90UB948-Q1 is a FPD-Link III deserializer that recovers the data from one or two FPD-Link III serial streams and translates the data into either a single- or dual-pixel OpenLDI stream.

The key features of DS90UB947/8-Q1 FPD-Link III chipset include:

- Supports video resolutions up to WUXGA (1920 × 1200) and 1080p60 with 24-bit color depth
- Single or dual FPD-Link III
  - Single-link: Up to 96-MHz pixel clock
  - Dual-link: Up to 170-MHz pixel clock
- Supports 50-Ω single-ended coaxial or 100-Ω differential STP cables
- Supports up to 15 m of cable with automatic temperature and aging compensation
- Supports 7.1 multiple I2S (4 data) channels

Refer to [4] [5] for more details.
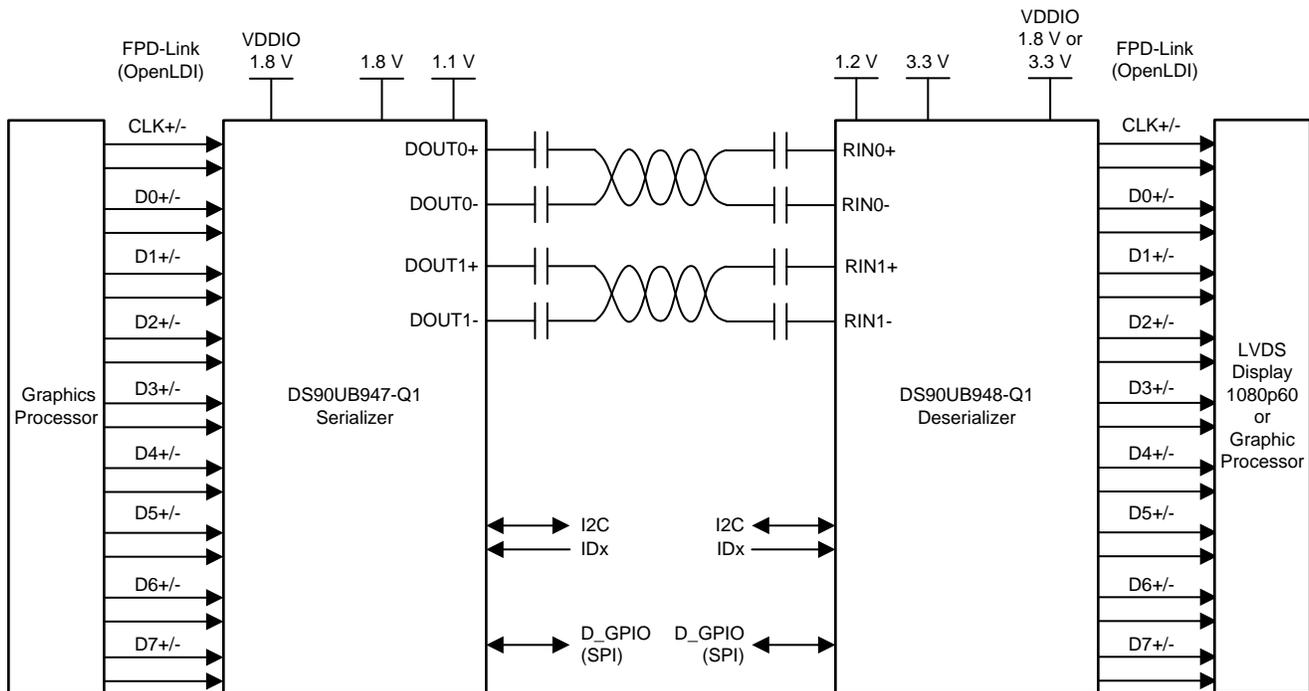
Figure 5. DS90UB947-Q1, DS90UB948-Q1 Typical Application

2.3   System Design Theory

This section describes the key system configuration for this reference design. Note that configuration of SN65DSI85-Q1 is the same for both setup one and setup two. The DS90UB947-Q1 and DS90UB948-Q1 FPD-Link III chipset is adopted in setup two, which is aimed for remote display application.

2.3.1   SN65DSI85-Q1

2.3.1.1   Operating Mode

The SN65DSI85-Q1 is a dual-channel MIPI DSI to dual-link OLDI/LVDS bridge, which supports dual-channel ODD or EVEN and LEFT or RIGHT DSI modes. According to different application, SN65DSI85-Q1 can be configured to several different operating modes including:

- Single DSI input to single-link OLDI/LVDS
- Single DSI input to dual-link OLDI/LVDS
- Dual DSI input (Odd/Even) to single-link OLDI/LVDS
- Dual DSI input (Odd/Even) to dual-link OLDI/LVDS
- Dual DSI input (Left/Right) to single-link OLDI/LVDS
- Dual DSI input (Left/Right) to dual-link OLDI/LVDS
- Dual DSI inputs (two streams) to two single-link OLDI/LVDS

To configure operating mode, the following CSR bits must be set:

- CSR 0x18[4]
- CSR 0x10[7]
- CSR 0x10[6:5]

In each of the modes, video data can be 18-bpp or 24-bpp. Table 5 summarizes the configurations of operating mode.

Table 5. SN65DSI85-Q1 Operating Modes

MODE	CSR 0x18[4]	CSR 0x10[7]	CSR 0x10[6:5]	DESCRIPTION
	OLDI/LVDS_LINK_CFG	LEFT_RIGHT_PIXES	DSI_CH_MODE	
Single DSI input to single-link OLDI/LVDS	1	—	01	Single DSI input on channel A to single-link OLDI/LVDS output on channel A.
Single DSI input to dual-link OLDI/LVDS	0	—	01	Single DSI input on channel A to dual-link OLDI/LVDS output with odd pixels on channel A and even pixels on channel B.
Dual DSI input (odd or even) to single-link OLDI/LVDS	1	0	00	Dual DSI input with odd pixels received on channel A and even pixels received on channel B. Data is output to single-link OLDI/LVDS on channel A.
Dual DSI input (odd or even) to dual-link OLDI/LVDS	0	0	00	Dual DSI input with odd pixels received on channel A and even pixels received on channel B. Data is output to dual-link OLDI/LVDS with odd pixels on channel A and even pixels on channel B.
Dual DSI input (left or right) to single-link OLDI/LVDS	1	1	00	Dual DSI input with left pixels received on channel A and right pixels received on channel B. Data is output to single-link OLDI/LVDS on channel A.

Table 5. SN65DSI85-Q1 Operating Modes (continued)

MODE	CSR 0x18[4]	CSR 0x10[7]	CSR 0x10[6:5]	DESCRIPTION
	OLDI/LVDS_LINK_CFG	LEFT_RIGHT_PIXES	DSI_CH_MODE	
Dual DSI input (left or right) to dual-link OLDI/LVDS	0	1	00	Dual DSI input with left pixels received on channel A and right pixels received on channel B. Data is output to dual-link OLDI/LVDS with odd pixels on channel A and even pixels on channel B.
Dual DSI inputs (two streams) to two single-link OLDI/LVDS	0	—	10	One video stream input on DSI channel A and output to single-link OLDI/LVDS on channel A. Another video stream input on DSI channel B and output to single-link OLDI/LVDS on channel B.

For this reference design, single DSI input to single-link OLDI/LVDS operating mode is configured.

2.3.1.2 Clock Configuration

The SN65DSI85-Q1 provides two options for OLDI/LVDS clock source, which can be configured using CSR 0x0A[0].

- DSI channel A clock (CSR 0x0A[0]=1)
- External reference clock (CSR 0x0A[0]=0)

When DSI channel A clock is used as OLDI/LVDS clock source, the D-PHY clock lane must operate in HS mode. This feature eliminates the requirement for an external reference clock reducing system costs. DSI channel A clock is divided by the factor in CSR 0x0B[7:3] (DSI_CLK_DIVIDER) to generate the OLDI/LVDS output clock:

OLDI/LVDS output clock = DSI Channel A input clock ÷ DSI_CLK_DIVIDER

When external reference clock is selected for OLDI/LVDS clock source, the clock must be between 25 MHz and 154 MHz. The external reference clock is multiplied by the factor in CSR 0x0B[1:0] (REFCLK_MULTIPLIER) to generate the OLDI/LVDS output clock:

OLDI/LVDS output clock = External reference clock × REFCLK_MULTIPLIER

Additionally, the OLDI/LVDS output clock range and DSI channel A input clock range must be set respectively for the internal PLL to operate correctly by following resistors:

- OLDI/LVDS output clock range (CSR 0x0A[3:1])
- DSI channel A input clock range (CSR 0x12)

For this reference design, DSI channel A clock is selected as OLDI/LVDS clock source. According to the calculation in Section 2.2.1, OLDI/LVDS output clock is 50.4 MHz while DSI channel A clock is 151.2 MHz. To generate OLDI/LVDS output clock, DSI_CLK_DIVIDER is configured as:

DSI_CLK_DIVIDER = 151.2MHz ÷ 50.4 MHz = 3

Therefore, clock ranges for DSI input and OLDI/LVDS output are:

37.5 MHz ≤ OLDI/LVDS output clock < 62.5 MHz

150 MHz ≤ DSI input clock < 155 MHz

2.3.1.3 Video Registers

The SN65DSI85-Q1 offers two kinds of video registers. The video registers must be programmed to match the line time requirement of the display panel.

- *Test Pattern Only* registers are for test pattern generation use only. For normal operation, these registers are not required.
- *Normal Operation* registers are for normal operation unless the test pattern generation feature is enabled.

Table 6 lists the entire channel A video registers. Channel B video registers are used only when the device is configured for the dual-channel application.

For this reference design, the channel A video registers are all configured to match the timing parameters of the display panel given in Table 1 to make it convenient to switch between test pattern generation and normal operation.

It is also important to maintain the data rate to not underflow or overflow the internal buffer.

The SN65DSI85-Q1 supports a programmable delay value to help maintain the data rate and the availability of data in internal buffers. The delay value, also referred as *sync delay*, is used to delay the outgoing data, up to 0xFF number of pixels, by programming the corresponding register field:

- Channel A sync delay (CSR 0x28 and 0x29)
- Channel B sync delay (CSR 0x2A and 0x2B)

Table 6. SN65DSI85-Q1 Channel A Video Registers

REGISTER	FUNCTION	COMMENT
0x20	CHA horizontal active	Normal operation
0x21		
0x24	CHA vertical active	Test pattern only
0x25		
0x2C	CHA horizontal sync pulse width	Normal operation
0x2D		
0x30	CHA vertical sync pulse width	
0x31		
0x34	CHA horizontal back porch	
0x36	CHA vertical back porch	Test pattern only
0x38	CHA horizontal front porch	
0x3A	CHA vertical front porch	

2.3.1.4 OLDI/LVDS Output Format

The SN65DSI85-Q1 processes DSI packets and produces video data driven to the OLDI/LVDS interface in an industry standard format. The OLDI/LVDS output format must match the data format of the display panel. When the OLDI/LVDS output is implemented in a dual-link configuration, channel A carries the odd pixel data, and channel B carries the even pixel data.

Figure 6 shows a dual-link 24-bpp application using format two. In data format two, the two MSBs per color are transferred on the Y3P/N OLDI/LVDS lane. Figure 7 shows a 24-bpp single-link application using format one. In data format one, the two LSBs per color are transferred on the Y3P/N OLDI/LVDS lane. Data format can be configured through:

- Channel A data format (CSR 0x18[1])
- Channel B data format (CSR 0x18[0])
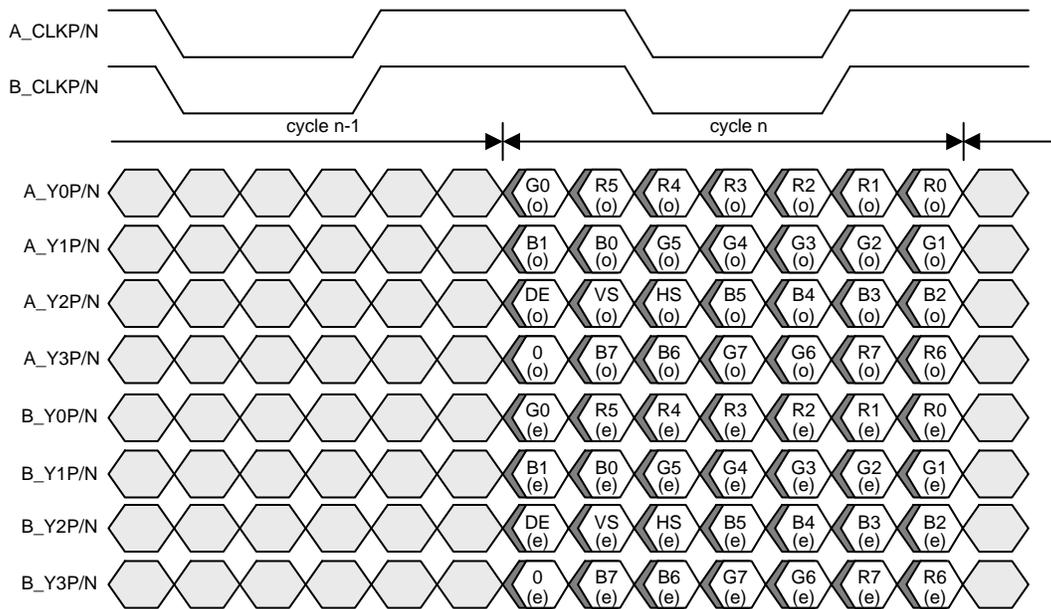
Figure 6. OLDI/LVDS Dual-Link 24-bpp Output Data (Format Two)
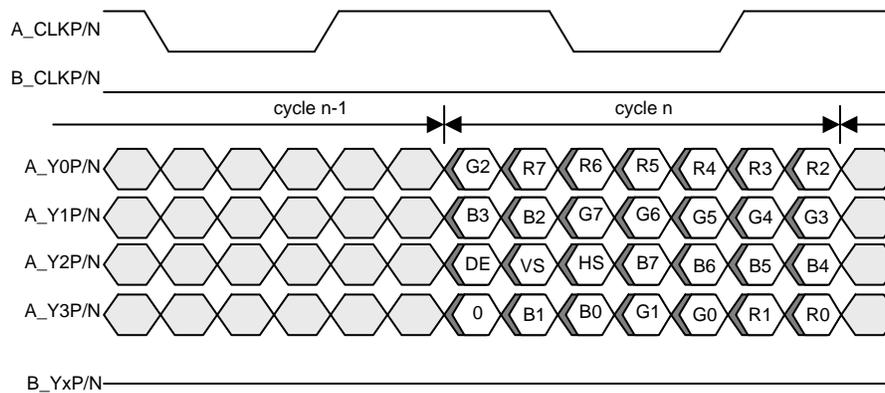
DE = Data Enable; Channel B Clock and Data are Output Low

Figure 7. OLDI/LVDS Single-Link 24-bpp Output Data (Format One)

For this reference design, RGB888 24-bpp data is received from DSI while an 18-bpp display panel is adopted. In this case, format one must be selected. The two LSBs per color that transferred on the Y3P/N OLDI/LVDS lane are discarded.

2.3.1.5 Registers Setting Summary

Table 7 summarized the SN65DSI85-Q1 registers settings, which are suitable both for setup one and setup two.

Table 7. SN65DSI85-Q1 Registers Setting Summary

REGISTER	VALUE	FUNCTION
0x0A	0x03	OLDI/LVDS clock source: DSI channel A clock OLDI/LVDS clock range: 37.5 MHz to approximately 62.5 MHz
0x0B	0x10	OLDI/LVDS clock = DSI Channel A clock ÷ 3
0x0D	0x01	PLL enabled
0x10	0x20	Operating mode: single-channel DSI input; CHA DSI four lanes enabled
0x12	0x1E	DSI channel A clock range: 150 MHz to approximately155 MHz
0x18	0x72	DE: positive HS: negative VS: negative Operating mode: Single-link OLDI/LVDS output CHA Force 18 bpp: CHA Y3P/Y3N disabled CHA format one: CHA Y3P/Y3N transmits two LSBs
0x20	0x00	CHA horizontal active = 1024
0x21	0x04	
0x22	0x00	CHB horizontal active = 0
0x23	0x00	
0x24	0x58	CHA vertical active = 600
0x25	0x02	
0x26	0x00	CHB vertical active = 0
0x27	0x00	
0x28	0x00	CHA sync delay = 512
0x29	0x02	
0x2A	0x00	CHB sync delay = 0
0x2B	0x00	
0x2C	0x88	CHA horizontal sync pulse width = 136
0x2D	0x00	
0x2E	0x00	CHB horizontal sync pulse width = 0
0x2F	0x00	
0x30	0x03	CHA vertical sync pulse width = 3
0x31	0x00	
0x32	0x00	CHB vertical sync pulse width = 0
0x33	0x00	
0x34	0xA0	CHA horizontal back porch = 160
0x35	0x00	CHB horizontal back porch = 0
0x36	0x16	CHA vertical back porch = 22
0x37	0x00	CHB vertical back porch = 0
0x38	0x18	CHA horizontal front porch = 24
0x39	0x00	CHB horizontal front porch = 0
0x3A	0x00	CHA vertical front porch = 0
0x3B	0x00	CHB vertical front porch = 0
0x3C	0x00	Test pattern disabled

2.3.1.6 *Example Script*

Note that CSR 0x0D (PLL_EN) must be set at least after CSR 0x0A and CSR 0x0B are configured.

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="1"/> <i2c_bitrate khz="100"/>
======ADDR 0D======
======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
  <i2c_write addr="0x2D" count="1" radix="16">0D 00</i2c_write> <sleep ms="10"/>
======ADDR 0A======
    <i2c_write addr="0x2D" count="1" radix="16">0A 03</i2c_write> <sleep ms="10"/>
======ADDR 0B======
    <i2c_write addr="0x2D" count="1" radix="16">0B 10</i2c_write> <sleep ms="10"/>
======ADDR 10======
    <i2c_write addr="0x2D" count="1" radix="16">10 20</i2c_write> <sleep ms="10"/>
======ADDR 12======
    <i2c_write addr="0x2D" count="1" radix="16">12 1E</i2c_write> <sleep ms="10"/>
======ADDR 18======
    <i2c_write addr="0x2D" count="1" radix="16">18 72</i2c_write> <sleep ms="10"/>
======ADDR 20======
======CHA_LINE_LENGTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">20 00</i2c_write> <sleep ms="10"/>
======ADDR 21======
======CHA_LINE_LENGTH_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">21 04</i2c_write> <sleep ms="10"/>
======ADDR 22======
======CHB_LINE_LENGTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">22 00</i2c_write> <sleep ms="10"/>
======ADDR 23======
======CHB_LINE_LENGTH_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">23 00</i2c_write> <sleep ms="10"/>
======ADDR 24======
======CHA_VERTICAL_DISPLAY_SIZE_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">24 58</i2c_write> <sleep ms="10"/>
======ADDR 25======
======CHA_VERTICAL_DISPLAY_SIZE_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">25 02</i2c_write> <sleep ms="10"/>
======ADDR 26======
======CHB_VERTICAL_DISPLAY_SIZE_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">26 00</i2c_write> <sleep ms="10"/>
======ADDR 27======
======CHB_VERTICAL_DISPLAY_SIZE_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">27 00</i2c_write> <sleep ms="10"/>
======ADDR 28======
======CHA_SYNC_DELAY_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">28 00</i2c_write> <sleep ms="10"/>
======ADDR 29======
======CHA_SYNC_DELAY_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">29 02</i2c_write> <sleep ms="10"/>
======ADDR 2A======
======CHB_SYNC_DELAY_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">2A 00</i2c_write> <sleep ms="10"/>
======ADDR 2B======
======CHB_SYNC_DELAY_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">2B 00</i2c_write> <sleep ms="10"/>
======ADDR 2C======
======CHA_HSYNC_PULSE_WIDTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">2C 88</i2c_write> <sleep ms="10"/>
======ADDR 2D======
======CHA_HSYNC_PULSE_WIDTH_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">2D 00</i2c_write> <sleep ms="10"/>
======ADDR 2E======
======CHB_HSYNC_PULSE_WIDTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">2E 00</i2c_write> <sleep ms="10"/>
======ADDR 2F======
======CHB_HSYNC_PULSE_WIDTH_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">2F 00</i2c_write> <sleep ms="10"/>
```

```
======ADDR 30=======
======CHA_VSYNC_PULSE_WIDTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">30 03</i2c_write> <sleep ms="10"/>
======ADDR 31=======
======CHA_VSYNC_PULSE_WIDTH_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">31 00</i2c_write> <sleep ms="10"/>
======ADDR 32=======
======CHB_VSYNC_PULSE_WIDTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16">32 00</i2c_write> <sleep ms="10"/>
======ADDR 33=======
======CHB_VSYNC_PULSE_WIDTH_HIGH========
    <i2c_write addr="0x2D" count="1" radix="16">33 00</i2c_write> <sleep ms="10"/>
======ADDR 34=======
======CHA_HOR_BACK_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">34 A0</i2c_write> <sleep ms="10"/>
======ADDR 35=======
======CHB_HOR_BACK_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">35 00</i2c_write> <sleep ms="10"/>
======ADDR 36=======
======CHA_VER_BACK_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">36 16</i2c_write> <sleep ms="10"/>
======ADDR 37=======
======CHB_VER_BACK_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">37 00</i2c_write> <sleep ms="10"/>
======ADDR 38=======
======CHA_HOR_FRONT_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">38 18</i2c_write> <sleep ms="10"/>
======ADDR 39=======
======CHB_HOR_FRONT_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">39 00</i2c_write> <sleep ms="10"/>
======ADDR 3A=======
======CHA_VER_FRONT_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">3A 00</i2c_write> <sleep ms="10"/>
======ADDR 3B=======
======CHB_VER_FRONT_PORCH========
    <i2c_write addr="0x2D" count="1" radix="16">3B 00</i2c_write> <sleep ms="10"/>
======ADDR 3C=======
======CHA/CHB TEST PATTERN(bit4 CHA, bit0 CHB)========
  <i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write> <sleep ms="10"/>
======ADDR 0D=======
======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
    <i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write> <sleep ms="10"/>
=====SOFTRESET=======
  <i2c_write addr="0x2D" count="1" radix="16">09 01</i2c_write> <sleep ms="10"/>
======Read======
    <i2c_read addr="0x2D" count="196" radix="16">00</i2c_read> <sleep ms="10"/>
======Read======
    <i2c_read addr="0x2D" count="256" radix="16">00</i2c_read> <sleep ms="10"/>
</aardvark>
```

2.3.2 DS90UB947-Q1

2.3.2.1 MODE_SEL[1:0] setting

Most of the DS90UB947-Q1 configurations can be set through MODE_SEL[1:0] including the following:

- OLDI_DUAL
- AUTO_SS
- REPEATER
- MAPSEL
- COAX

Table 8 summarizes these configuration settings.

A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs, which is shown in Figure 9.

Table 9 and Table 10 summarize the configuration select. These strapped values latch into registers during power-up, which can be viewed or modified in the following locations:

- OLDI_DUAL : Latched into register 0x4F[6] (inverted from strap value)
- AUTO_SS : Latched into register 0x01[7]
- REPEATER : Latched into register 0xC2[5]
- MAPSEL : Latched into register 0x4F[7]
- COAX : Latched into register 0x5B[7]
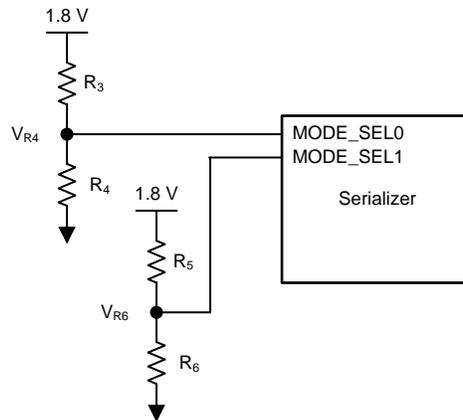
Figure 8. MODE_SEL[1:0] Connection Diagram (Ser)

Table 8. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
OLDI_DUAL: OpenLDI Interface	0	Single-pixel OpenLDI interface
	1	Dual-pixel OpenLDI interface
AUTO_SS: Auto Sleep-State	0	Disable
	1	Enable
REPEATER: Configure Repeater	0	Disable repeater mode
	1	Enable repeater mode
MAPSEL: OpenLDI Bit Mapping	0	OpenLDI bit mapping
	1	SPWG bit mapping
COAX: Cable Type	0	Enable FPD-Link III for twisted pair cabling
	1	Enable FPD-Link III for coaxial cabling

Table 9. Configuration Select (MODE_SEL0)

NUMBER	RATIO VR4/VDD18	TARGET VR4 (V)	SUGGESTED RESISTOR PULLUP R3 kΩTOL (1% TOL)	SUGGESTED RESISTOR PULLDOWN R4 kΩTOL (1% TOL)	OLDI_DUAL	AUTO_SS	REPEATER
1	0	0	OPEN	40.2	0	0	0
2	0.213	0.383	115	30.9	0	0	1
3	0.328	0.591	107	52.3	0	1	0
4	0.444	0.799	113	90.9	0	1	1
5	0.56	1.008	82.5	105	1	0	0
6	0.676	1.216	51.1	107	1	0	1
7	0.792	1.425	30.9	118	1	1	0
8	1	1.8	40.2	OPEN	1	1	1

Table 10. Configuration Select (MODE_SEL1)

NUMBER	RATIOTOL VR6/VDD18	TARGET VR6 (V)	SUGGESTED RESISTOR PULLUP R5 kΩ (1% TOL)	SUGGESTED RESISTOR PULLDOWN R6 kΩ (1% TOL)	MAPSEL	COAX
1	0	0	OPEN	40.2	0	0
2	0.213	0.383	115	30.9	0	0
3	0.328	0.591	107	52.3	0	1
4	0.444	0.799	113	90.9	0	1
5	0.56	1.008	82.5	105	1	0
6	0.676	1.216	51.1	107	1	0
7	0.792	1.425	30.9	118	1	1
8	1	1.8	40.2	OPEN	1	1

For this reference design, MODE_SEL0 is set to 1 while MODE_SEL1 is set to 5.

- OLDI_DUAL=0: Single-pixel OpenLDI interface
- AUTO_SS=0: Disable auto sleep-state
- REPEATER=0: Disable repeater mode
- MAPSEL=1: SPWG bit mapping; LSBs on D3/D7
- COAX=0: Enable FPD-Link III for STP cable

2.3.2.2   FPD-Link III Modes of Operation

The FPD-Link III transmit logic supports several modes of operation dependent on the downstream receiver as well as the delivered video. The following modes of DS90UB947-Q1 are supported, which can be configured by register 0x5B[1:0]:

- Single-link operation
- Dual-link operation
- Replicate mode
- Auto-detection mode

For this reference design, the DS90UB947-Q1 is set to single-link operation (register 0x5B[1:0]=1).

2.3.3   DS90UB948-Q1

2.3.3.1   MODE_SEL[1:0] setting

Similar to DS90UB947-Q1, most of the DS90UB948-Q1 configurations can be set through MODE_SEL[1:0], including MAP_SEL, OUTPUT_MODE[1:0], REPEATER, and MODE. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs (VR1) and VDD33. These resistors are also used to select one of the other eight possible modes, which is shown in Figure 9. Table 11 and Table 12 summarize the configuration select of MODE_SEL[1:0].
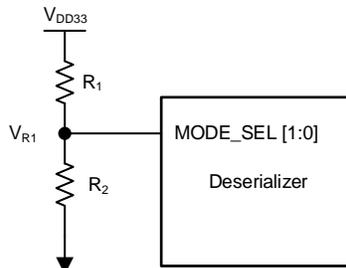
Figure 9. MODE_SEL[1:0] Connection Diagram (Des)

Table 11. Configuration Select (MODE_SEL0)

NUMBER	IDEAL RATIO VR1/VDD33	TARGET VR1 (V)	SUGGESTED RESISTOR R1 kΩ (1% TOL)	SUGGESTED RESISTOR R2 kΩ (1% TOL)	MAP_SEL	OUTPUT_MODE [0:1]	OUTPUT MODE
1	0	0	Open	40.2 or Any	0	00	Dual OLDI output
2	0.169	0.559	232	47.5	0	01	Dual SWAP output
3	0.23	0.757	107	31.6	0	10	Single OLDI output
4	0.295	0.974	113	47.5	0	11	Replicate
5	0.376	1.241	113	68.1	1	00	Dual OLDI output
6	0.466	1.538	107	93.1	1	01	Dual SWAP output
7	0.556	1.835	90.9	113	1	10	Single OLDI output
8	0.801	2.642	45.3	182	1	11	Replicate

Table 12. Configuration Select (MODE_SEL1)

NUMBER	IDEAL RATIO VR1/VDD33	TARGET VR1 (V)	SUGGESTED RESISTOR R1 kΩ (1% TOL)	SUGGESTED RESISTOR R2 kΩ (1% TOL)	REPEATER	MODE	HIGH-SPEED BACK CHANNEL	INPUT MODE
1	0	0	Open	40.2 or Any	0	00	5 Mbps	STP
2	0.169	0.559	232	47.5	0	01	5 Mbps	Coax
3	0.230	0.757	107	31.6	0	10	20 Mbps	STP
4	0.295	0.974	113	47.5	0	11	20 Mbps	Coax
5	0.376	1.241	113	68.1	1	00	5 Mbps	STP
6	0.466	1.538	107	93.1	1	01	5 Mbps	Coax
7	0.556	1.835	90.9	113	1	10	20 Mbps	STP
8	0.801	2.642	45.3	182	1	11	20 Mbps	Coax

For this reference design, MODE_SEL0 is set to 3, and MODE_SEL1 is set to 1.

- MAP_SEL=0: LSBs on D3/D7
- OUTPUT_MODE[1:0]=10: Single OLDI output
- Repeater=1: Disable repeater
- MODE=00: 5 Mbps, STP

2.3.3.2 *FPD-Link III Modes of Operation*

The DS90UB948-Q1 is capable of operating in either in one-lane or two-lane mode for FPD-Link III. By default, the FPD-Link III receiver automatically configures the input based on one-lane or two-lane mode operation. Programming register 0x34[4:3] settings override the automatic detection.

The DS90UB948-Q1 can be configured in following modes:

- 1-lane FPD-Link III input, Single-link OpenLDI output
- 1-lane FPD-Link III input, Dual-link OpenLDI output
- 2-lane FPD-Link III input, Dual-link OpenLDI output
- 2-lane FPD-Link III input, Single-link OpenLDI output
- 2-lane FPD-Link III input, Single-link OpenLDI output (Replicate)

For this reference design, the DS90UB948-Q1 is set to one-lane FPD-Link III input and single-link OpenLDI output (register 0x34[4:3]=10).

3   Hardware, Software, Testing Requirements and Test Results

3.1   *Required Hardware and Software*

3.1.1   Hardware

This reference design is realized by combining the PandaBoard 4500 with OMAP4460, SN65DSI85-Q1 EVM, DS90UB947-Q1 EVM, and DS90UB948-Q1 EVM. Figure 10 and Figure 11 show setup one and setup two. The module number of the display panel is LP101WSA-TLN1.
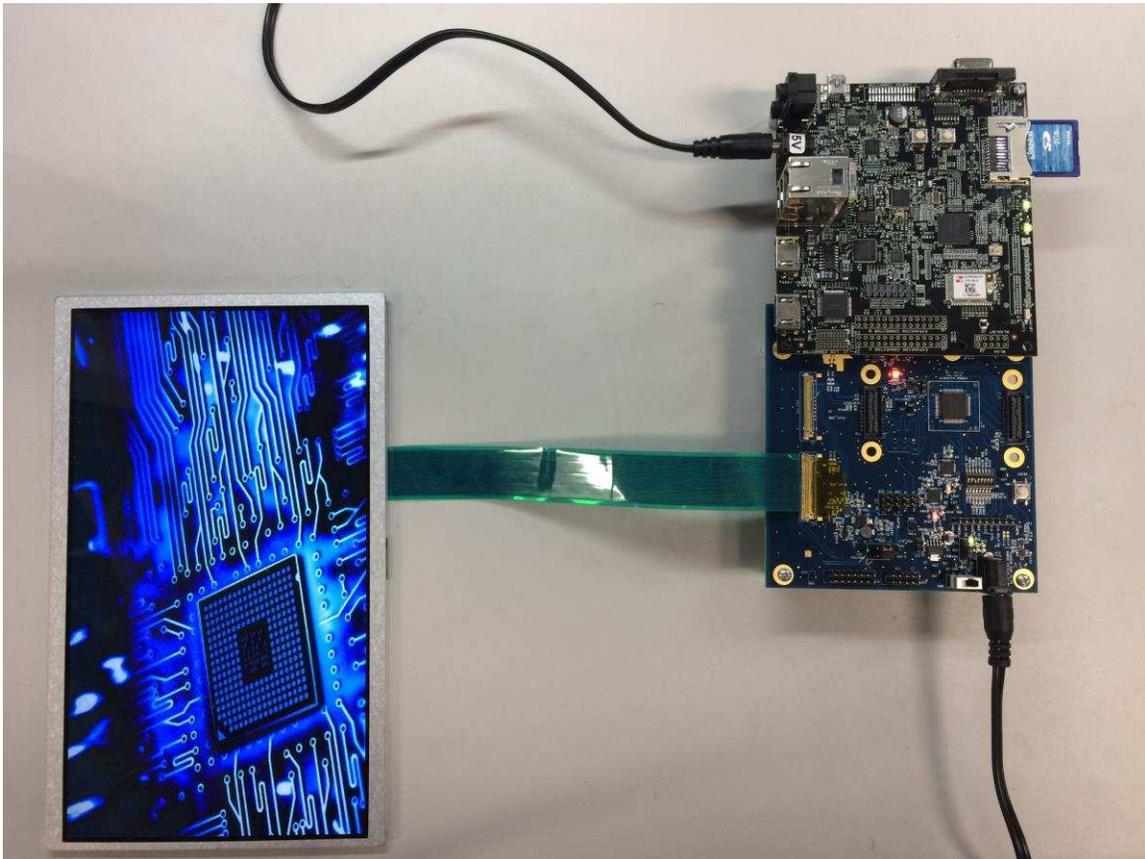
Figure 10. TIDA-01453 Reference Design Setup One
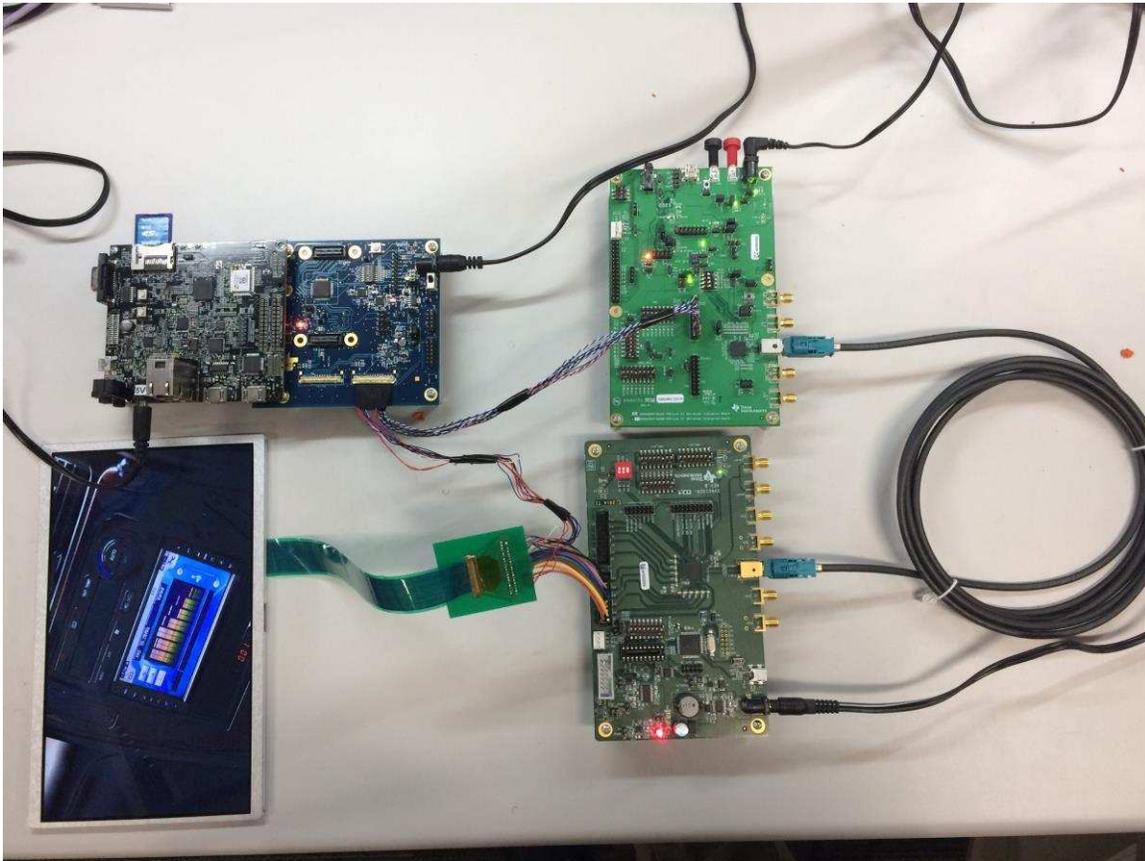
Figure 11. TIDA-01453 Reference Design Setup Two

The SN65DSI85-Q1 has two OLDI/LVDS output clocks that are generated from one clock source. The worst skew observed between the two output clocks is approximately 10 ps. When connecting SN65DSI85-Q1 to DS90UB947-Q1, the SN65DSI85-Q1 channel A output clock (A_CLKP/N) is recommended to connect to DS90UB947-Q1 clock input (CLK+/-) . Leave Chanel B output clock (A_CLKP/N) open. Figure 12 shows these connections.

For schematic reference and layout recommendation of this reference design, see [6][7][8][10].
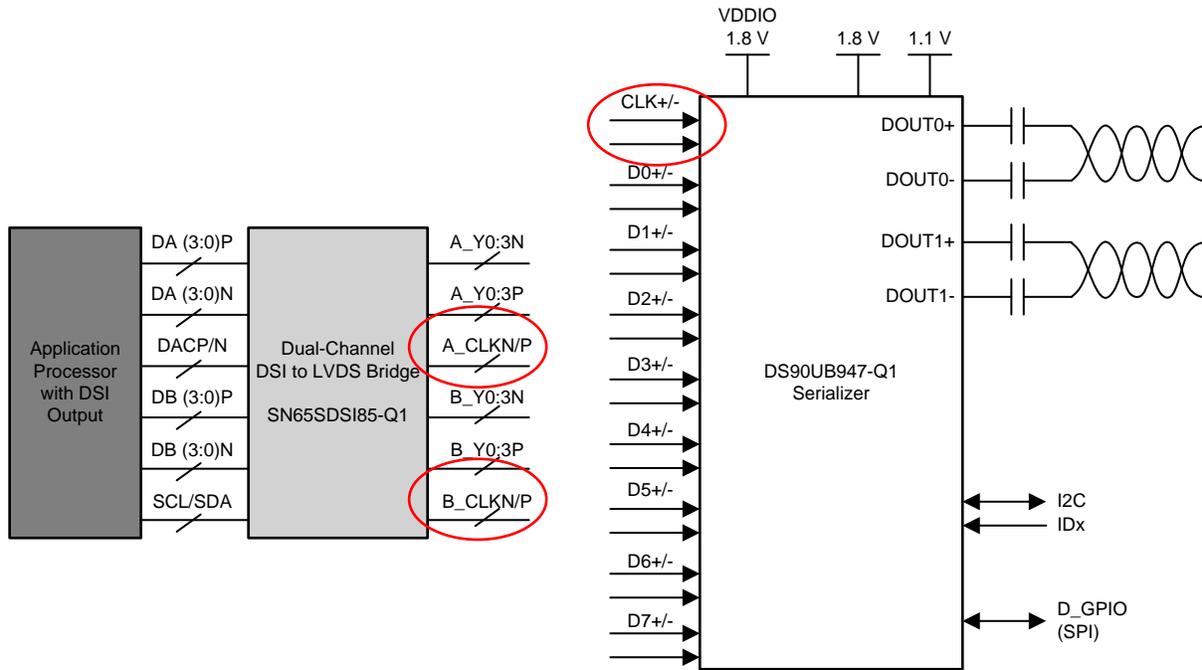
Figure 12. SN65DSI85-Q1 and DS90UB947-Q1 Connecting Considerations

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3.1.2 Software

3.1.2.1 DSI Tuner

The DSI Tuner video configuration tool can be used to generate the video timing and the register values required to transfer the DSI data to the OLDI/LVDS panel using the SN65DSI8x or SN65DSI8x–Q1 devices. Note that this tool does not set the values that must be set or cleared in a recommended sequence. The CSR 0x0D[0] (PLL_EN) and CSR 0x09[0] (SOFT_RESET) are not set as they must be set in the recommended sequence defined in the datasheet. Settings for this reference design is shown in Figure 13 and Figure 14. Figure 15 shows the timing requirements.

DSI Tuner can be downloaded from http://www.ti.com/tool/dsi-tuner. For the detailed user's guide of this tool, refer to [9].
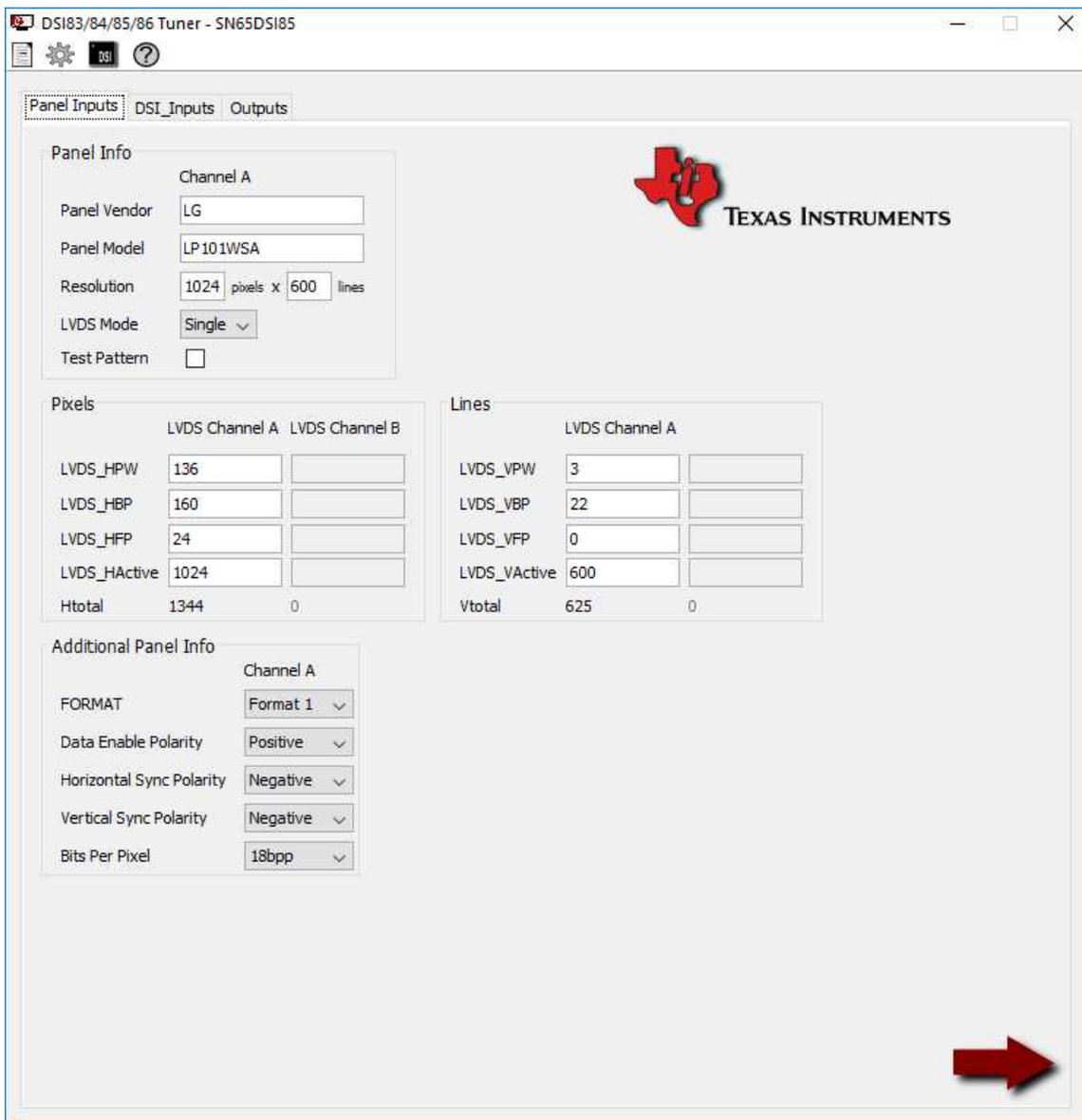
Figure 13. DSI Tuner Panel Input Setting
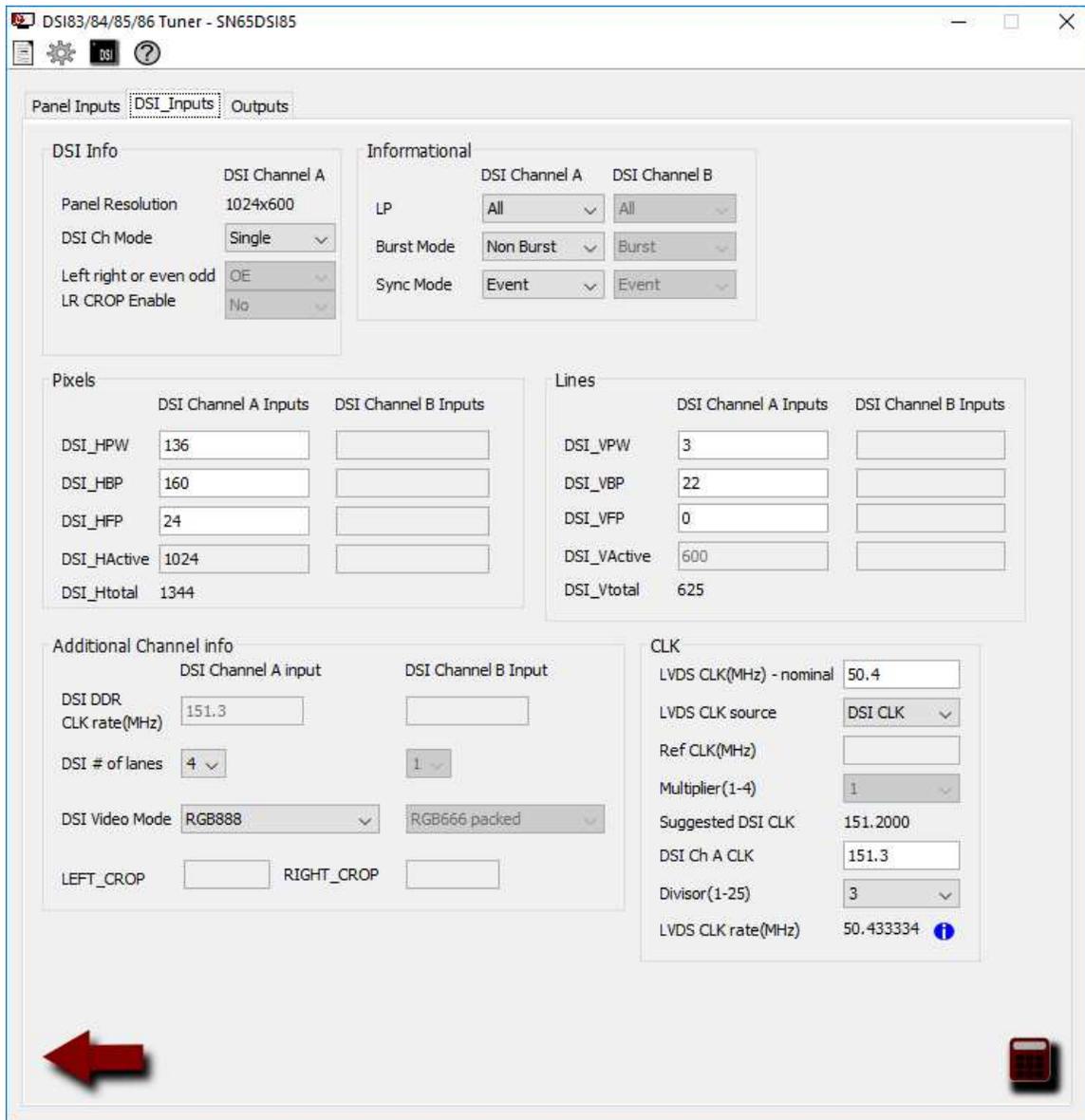
Figure 14. DSI Tuner DSI Input Setting
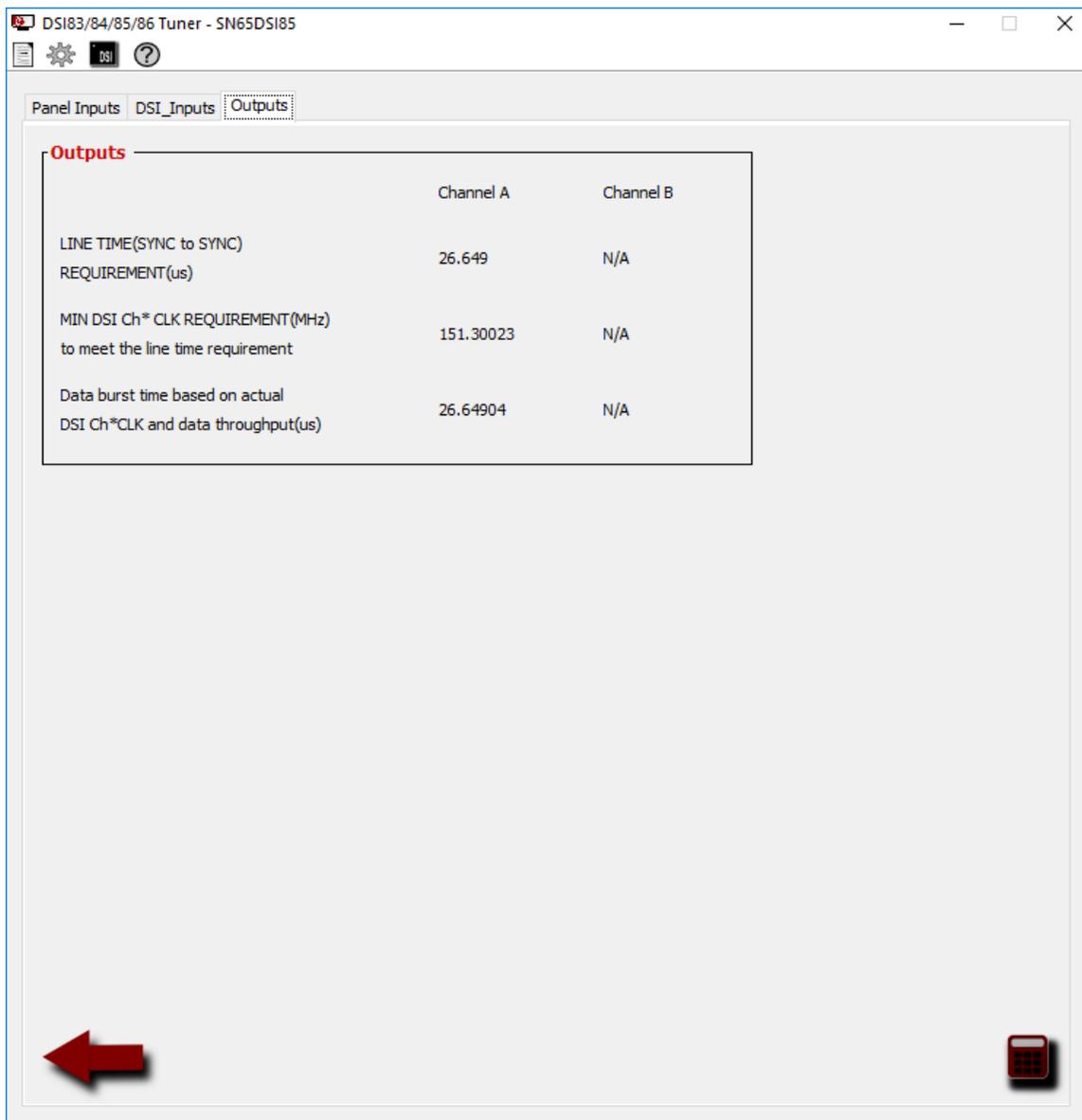
Figure 15. Timing Requirement

The CSRs settings generated by DSI Tuner are as follows:

```
//=====================================================================
// Filename   : CSR.txt
//   (C) Copyright 2013 by Texas Instruments Incorporated.
//   All rights reserved.
//=====================================================================
0x09            0x00
0x0A            0x03
0x0B            0x10
0x0D            0x00
0x10            0x26
0x11            0x00
0x12            0x1e
0x13            0x00
0x18            0x72
0x19            0x00
0x1A            0x03
0x1B            0x00
0x20            0x00
0x21            0x04
0x22            0x00
0x23            0x00
0x24            0x00
0x25            0x00
0x26            0x00
0x27            0x00
0x28            0x21
0x29            0x00
0x2A            0x00
0x2B            0x00
0x2C            0x88
0x2D            0x00
0x2E            0x00
0x2F            0x00
0x30            0x03
0x31            0x00
0x32            0x00
0x33            0x00
0x34            0xa0
0x35            0x00
0x36            0x00
0x37            0x00
0x38            0x00
0x39            0x00
0x3A            0x00
0x3B            0x00
0x3C            0x00
0x3D            0x00
0x3E            0x00
//=====================================================================
```

3.1.2.2 Analog LaunchPad™

The Analog LaunchPad development kit configuration tool can be used to configure registers of FPD-Link III devices, such as the DS90UB947-Q1 and DS90UB948-Q1. For this reference design, DS90UB947-Q1 is configured to Single FPD-Link III transmitter mode while DS90UB948-Q1 is configured to Single FPD-Link III primary input, which are shown in Figure 16 and Figure 17.

The Analog LaunchPad development kit can be downloaded from http://www.ti.com/tool/alp. For detailed user's guide of this tool, refer to [7][8].
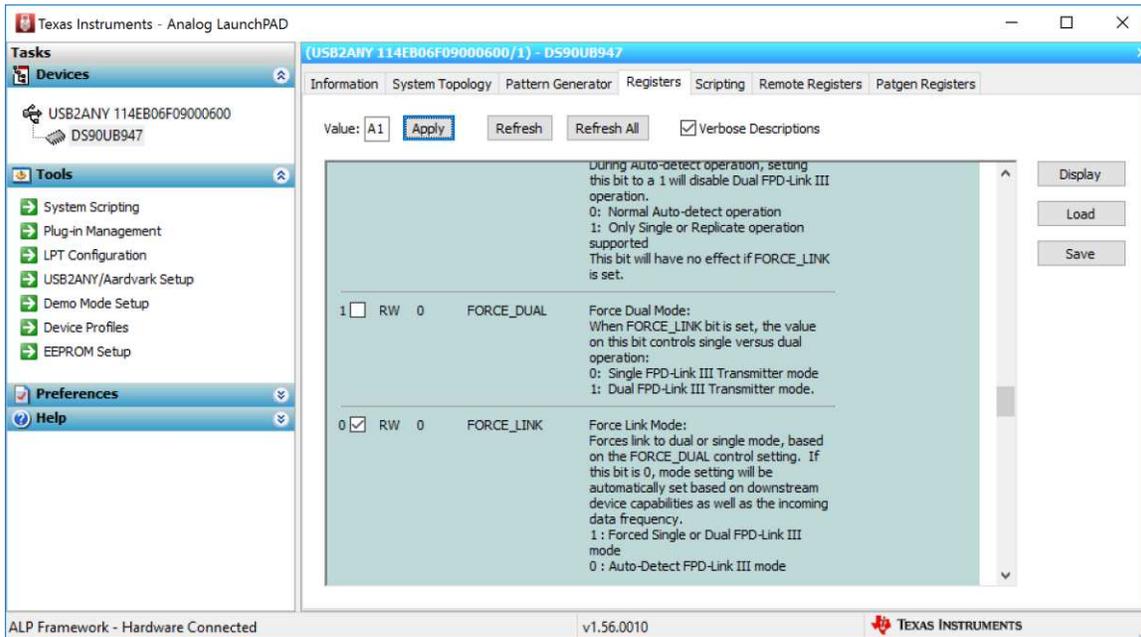
Figure 16. DS90UB947-Q1 Register 0x5B.1:0=01
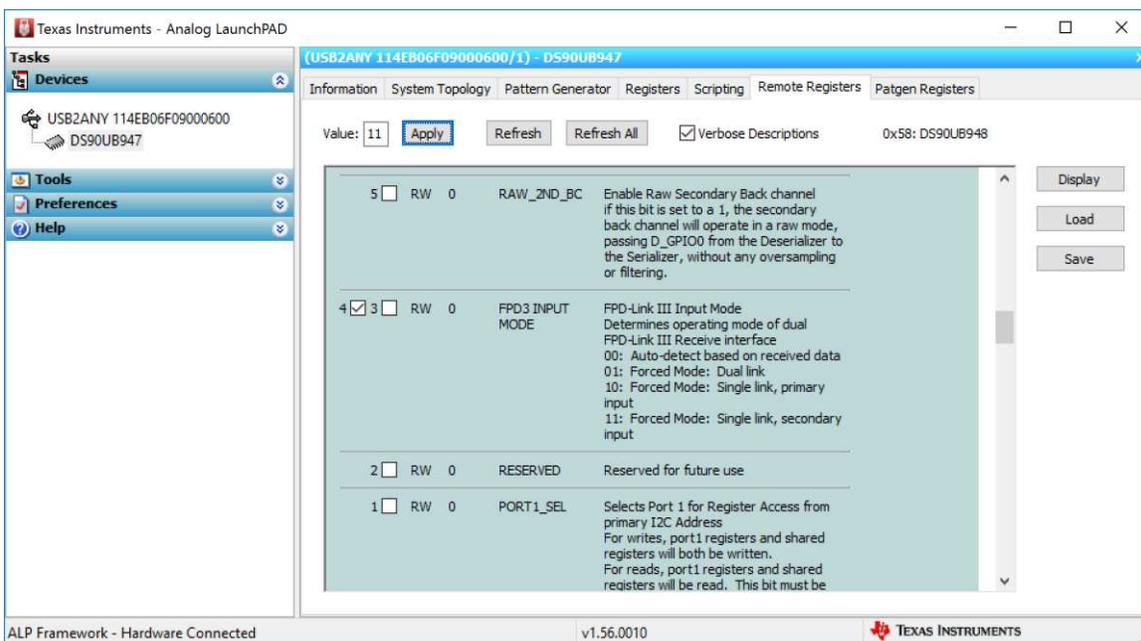
Figure 17. DS90UB948-Q1 Register 0x34.4:3=10

3.2   Testing and Results

3.2.1   Test Setup

3.2.1.1   Demonstraion Video

The reference design's demonstration video can be downloaded from:TIDA-01453, which includes English version and Chinese version. As shown in the demonstration video, the output video on the display panel is stable with no flicker.

3.2.1.2   Setup One

The testing of this reference design setup one is performed on the SN65DSI85-Q1 characterization board. Figure 18 shows the test setup.

The SN65DSI85-Q1 integrates some test registers that are not open for customers. The internal PRBS 27-1 pattern generator can be enabled by test registers for eye diagram measurement. Tektronix® AFG3252 signal generator is used to generate the reference clock. Agilent® DS08804B oscilloscope takes channel A Y0N/P output and displays the eye diagram. A 100-Ω resistor is used for termination between Y0N and Y0P.
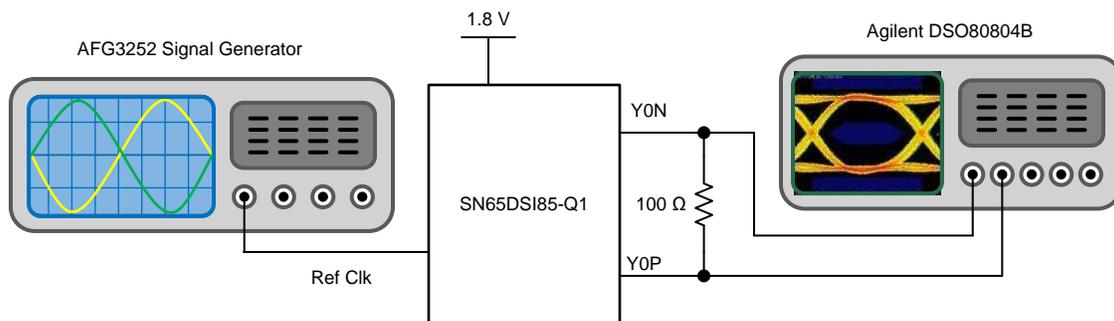
Figure 18. Eye Diagram Test Setup One

3.2.1.3   Setup Two

Figure 19 shows the eye diagram test for setup two. SoC generates the DSI video signal. Agilent DS08804B oscilloscope collects the output at DS90UB948-Q1 CMLOUT and displays the eye diagram. A 3-m STQ cable is used to transmit the FPD-Link III serialized signal.

CMLOUT of DS90UB948-Q1 outputs the recovered FPD-Link III serial stream, which can be enabled by following register:

- Register 0x56[3] = 1: enable CMLOUL loop-through driver
- Register 0x57[2:1]=01 & Register 0x52[7]=0: Recovered forward channel data from RIN0 is output on CMLOUT

Layout recommendation for the CMLOUT:

- Place 0.1-µF series capacitor on CMLOUTP and CMLOUTN
- Place 100- termination between 0.1-µF away from CMLOUTP and CMLOUTN
- Place test points from 0.1-µF capacitors
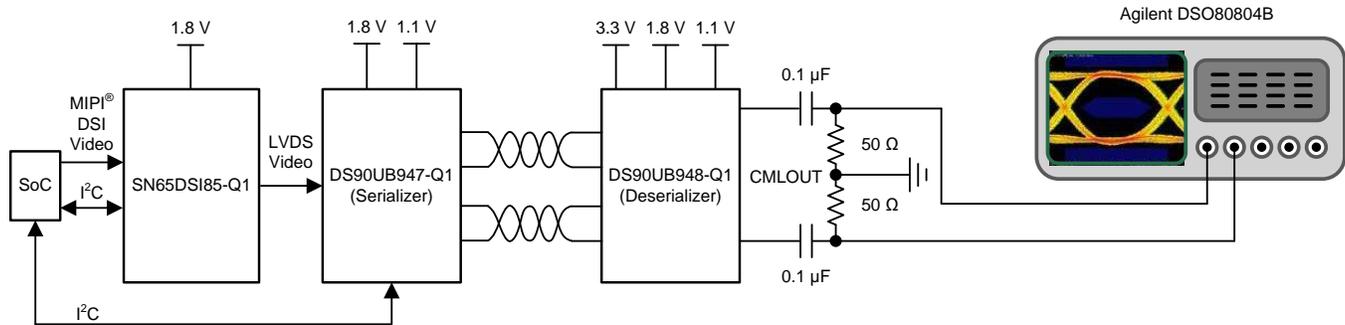
Figure 19. Eye Diagram Test Setup Two

3.2.2   Test Results

3.2.2.1   *Setup One*

The input reference clock frequency is 154 MHz, which is the highest frequency that SN65DSI85-Q1 can support. The output data rate is around 1 Gbps. Figure 20 shows the collected eye diagram at SN65DSI85-Q1 channel A Y0N/P output of setup one. Peak-to-peak jitter is around 27 ps. Eye width is around 900 ps, and eye height is around 506 mV. The more the eye is open, the better the signal integrity.
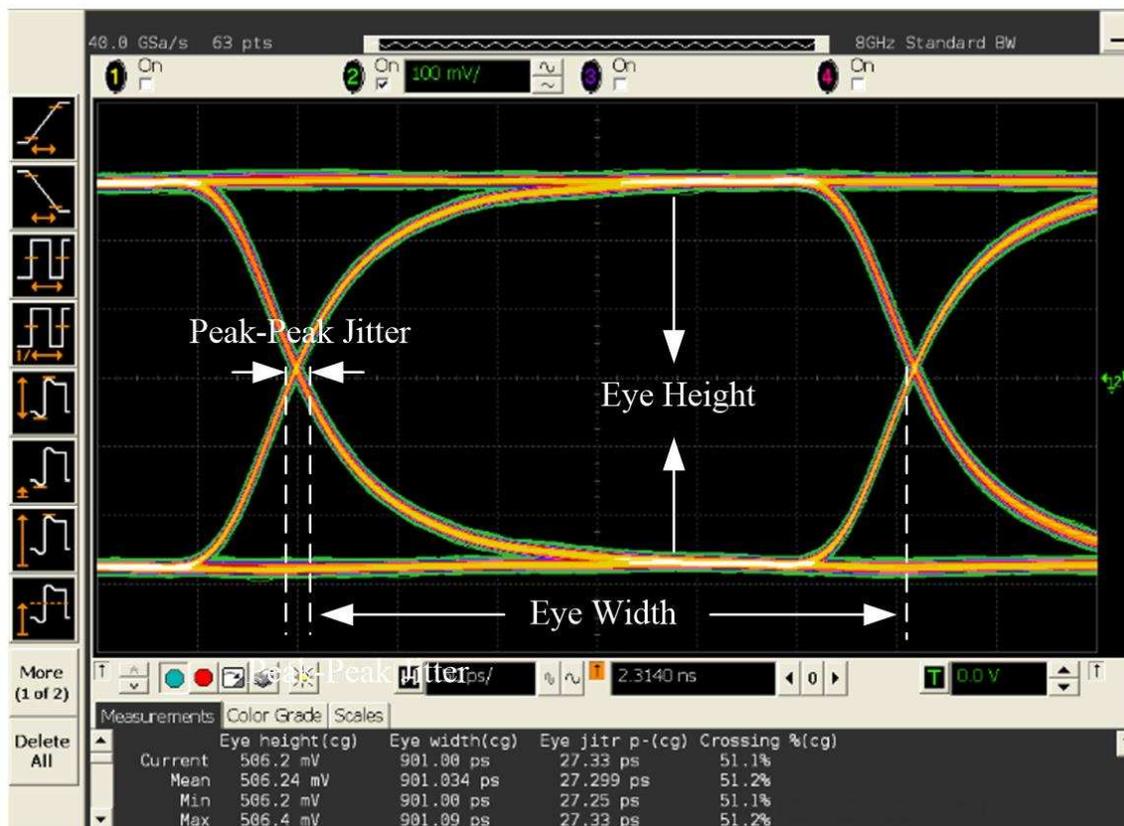
Figure 20. Setup One Eye Diagram

3.2.2.2 Setup Two

The FPD-Link III high-speed forward channel is composed of 35 bits of data containing RGB data, sync signals, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. For this reference design, the pixel clock is 50.4 MHz, and the serialized data rate is 1.764 Gbps.

Figure 21 shows the collected eye diagram at DS90UB948-Q1 CMLOUT of setup two. Peak-to-peak jitter is around 95 ps. Eye width is around 470 ps, and eye height is around 337 mV.
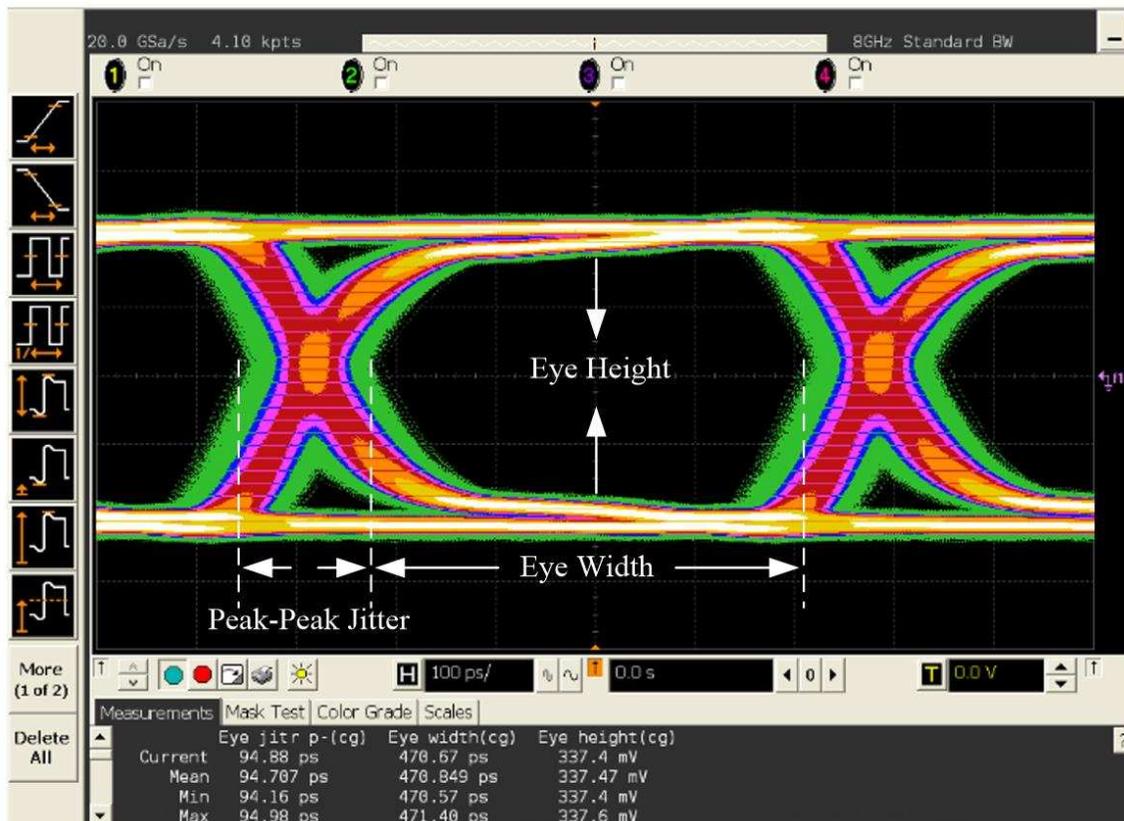
Figure 21. Setup Two Eye Diagram

4 Conclusion

This reference design addresses the cases where there are not enough OLDI/LVDS interfaces or only DSI interfaces are available in Automotive processors while display panels with OLDI/LVDS inputs are adopted. The design offers display interface options between MIPI DSI output on SoC directly to display panel (setup one) or using FPD-Link III chipset with a long cable (setup two).

This design is proved by combining existing EVMs. Test results show that this reference design is suitable for Automotive head units with integrated or remote display applications.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01453.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01453.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01453.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01453.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01453.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01453.

6 Software Files

To download the software files, see the design files at TIDA-01453.

7 Related Documentation

1. Texas Instruments, *SN65DSI85-Q1 Automotive Dual-Channel MIPI® DSI to Dual-Link OLDI/LVDS Bridge Data Sheet*
2. Texas Instruments, *SN65DSI84-Q1 Automotive Single-Channel MIPI® DSI to Dual-Link OLDI/LVDS Bridge Data Sheet*
3. Texas Instruments, *SN65DSI83-Q1 Automotive Single-Channel MIPI® DSI to Single-Link OLDI/LVDS Bridge Data Sheet*
4. Texas Instruments, *DS90UB947-Q1 1080p OpenLDI to FPD-Link III Serializer Data Sheet*
5. Texas Instruments, *DS90UB948-Q1 1080p FPD-Link III to OpenLDI Deserializer Data Sheet*
6. Texas Instruments, *SN65DSI83, SN65DSI84, and SN65DSI85 EVM User's Manual and Implementation User's Guide*
7. Texas Instruments, *DS90Ux947-Q1 EVM User's Guide*
8. Texas Instruments, *DS90UH948-Q1EVM User's Guide*
9. Texas Instruments, *SN65DSI8x Video Configuration Guide and Configuration Tool Software User's Manual Application Report*
10. Texas Instruments, *SN65DSI83, SN65DSI84, and SN65DSI85 Hardware Implementation Guide Application Report*

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