

TI Designs: TIDA-01407 Automotive 400-W, 48-V Battery Input, 12-V Output Power Reference Design

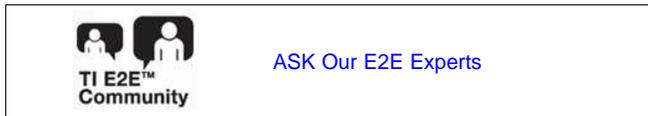


Description

This reference design is an automotive, 400-W, phase-shifted full-bridge converter which enables a 36-V to 60-V DC input and 12-V output. The enhanced phase-shifted full-bridge controller implements programmable delays which ensure zero voltage switching (ZVS) over a wide range of operating conditions. The output implements synchronous rectification, which enables fast transient response and a high loop bandwidth. The system regulates 12 V at no load with less than 100 mW of standby power. Pseudo isolation is achieved through a transformer to prevent the 48-V battery from being shorted to the secondary side. The half-bridge gate drivers can withstand a maximum boot voltage of 120-V DC.

Resources

TIDA-01407	Design Folder
UCC28951-Q1	Product Folder
UCC27212-Q1	Product Folder
UCC27511-Q1	Product Folder

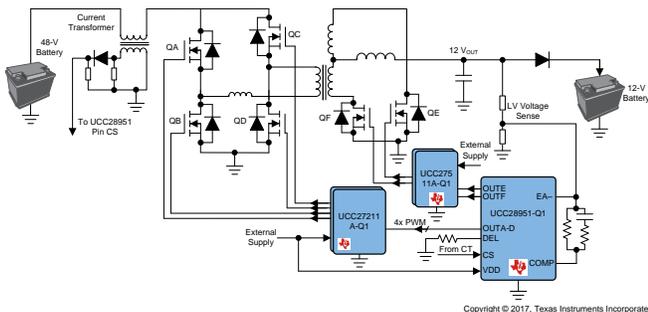


Features

- Phase-Shifted Full-Bridge Converter Over Input Voltage of 36-V to 60-V DC; Output Power up to 400 W
- Extendable to 500 W With Heatsinking; Easy to Customize per Customer Requirements
- Soft-Switching, Phase-Shifted Full Bridge Using UCC28951-Q1, Grade 1
- Synchronization Achievable for Multiple Phase Operation
- Regulated 12 V With 36-V to 60-V Input and at No Load With < 100-mW Standby Power
- Pseudo-Isolation Through Transformer; Load Does Not Register 48 V if MOSFETs Short
- Synchronous Rectification for High Efficiency
- Adaptive Delay for High Efficiency Across Load Range

Applications

- HEV/EV Traction Inverter
- Dry Double-Clutch Transmission
- Electronic Control Units
- HEV/EV DC-DC Converter

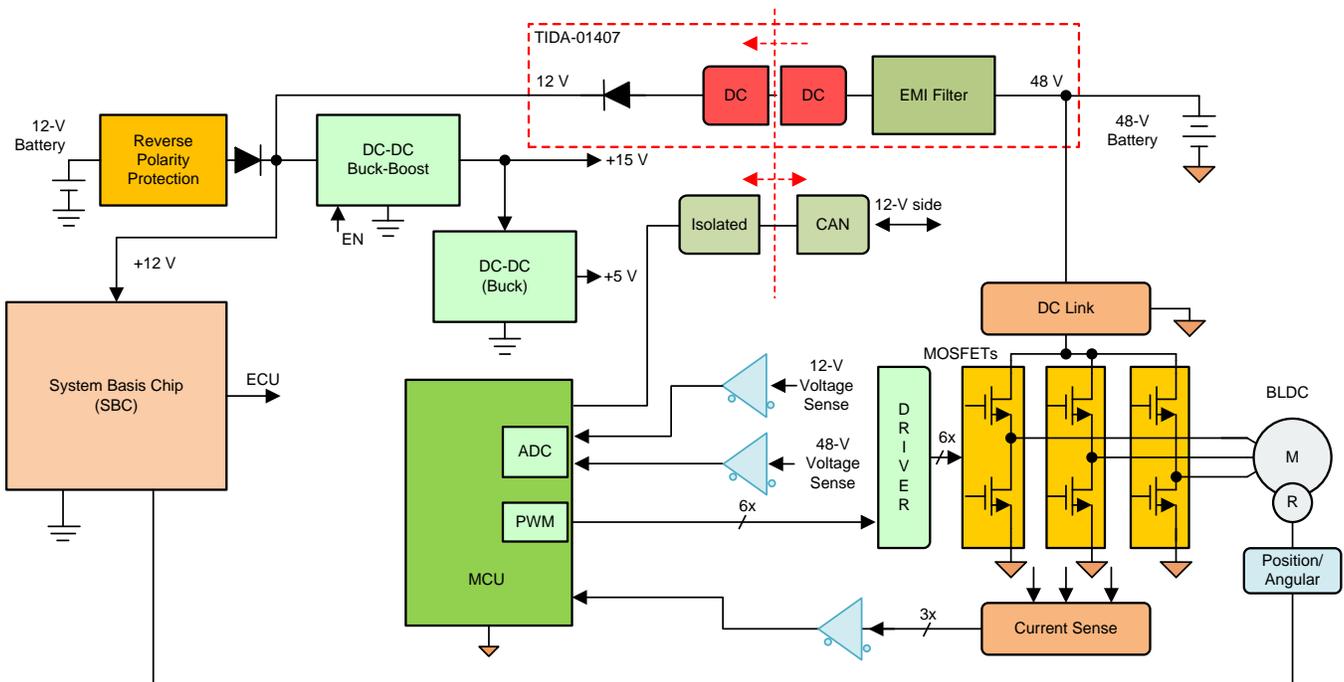


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1 System Overview

This reference design is a 400-W DC-DC power supply that generates a 12-V rail from the 48-V car battery in a mild hybrid electric vehicle (MHEV) system. The design implements a phase-shifted full-bridge topology which is capable of delivering 400 W of output power and handling an input voltage range of 36-V to 60-V DC without losing regulation. The input voltage withstand rating can be increased by increasing the MOSFET blocking voltage for the LV148 standard compliance. The enhanced, phase-shifted full-bridge controller UCC28951-Q1 implements programmable delays which ensure zero voltage switching (ZVS) over a wide range of operating conditions. The output side implements synchronous rectification, which enables fast transient response and a high loop bandwidth. The system regulates 12 V at no load with less than 100 mW of standby power. Pseudo isolation is achieved through the use of a transformer, which means the 48V does not apply to the load if the MOSFETs are shorted. The half-bridge gate drivers, which drive the high side and low side MOSFETs together at the primary side, can withstand a maximum boot voltage of 120-V DC. The controller regulates the output voltage through the transformer primary side, which eliminates the use of an Optocoupler and leads to a higher reliability and smaller form-factor board.

Figure 1 shows a block diagram example of the 48-V battery-inverter-driven motor system. The TIDA-01407 serves as a redundant supply to the 12-V battery voltage rail. As the diagram shows, the isolated DC-DC (TIDA-01407) is connected to the 48-V battery side and the non-isolated DC-DC is connected to the 12-V battery side (TIDA-01179 [1]). Both designs are in ORing configuration and provide the power to the downstream loads. TIDA-01179, which includes a buck-boost converter and a buck converter, creates the front-end power for the 12-V car battery.



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Figure 1. System Block Diagram of 48-V Battery-Driven Inverter and Implementation of TIDA-01407

1.1 Key System Specifications

Table 1 lists the key system specifications of TIDA-01407. The design can withstand a 36-V to 60-V input voltage range without losing regulation at the output. The input voltage range can be enlarged by increasing the MOSFET size for LV148 standard compliance. The output power can be increased by adding heatsinks.

Table 1. Key System Specifications

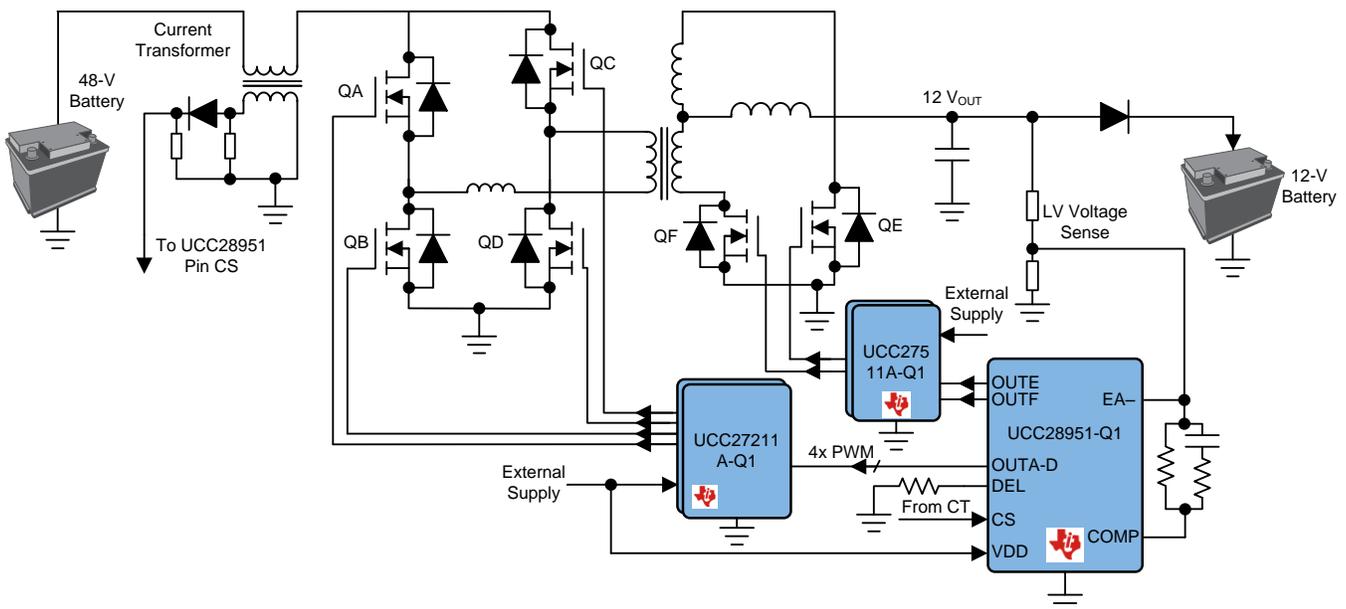
PARAMETER	SPECIFICATIONS
Input	<ul style="list-style-type: none"> • 36 V to 60 V, 48-V nominal
Output	<ul style="list-style-type: none"> • 12-V DC • 33.3-A continuous • Ripple < 3% V_{OUT} • Load step 3% to 100%; voltage deviation < 5%
Mechanics	<ul style="list-style-type: none"> • Silent power = no forced air • Efficiency > 95% • No heatsink • Slim line, maximum height < 20 mm
Extras	<ul style="list-style-type: none"> • Extendable to 500 W with heatsinking • Synchronize for multiple phase operations • No load with < 100-mW standby power • Switching frequency (\approx300 kHz) • 36-V to 60-V input without losing regulation • Pseudo isolation through transformer

2 System Description

2.1 Block Diagram

Figure 2 shows the system block diagram. The design consists of three main functional elements.

1. Current sensing at the primary side through the current transformer – This feature is for cycle-by-cycle overcurrent protection and adaptive delay control.
2. Power stage of the phase-shifted full-bridge at the primary side – This power stage implements the zero voltage soft-switching scheme and variable power-saving features for improving the efficiency over a wide load current range. The device can tolerate automotive electronics operating from a car battery, which experiences transient loads such as cold cranks and load dumps that can range up to 80 V and are easily scalable to 100 V.
3. Synchronous rectification MOSFETs at the secondary side – This element offers several benefits and functions to:
 - Boost the system efficiency by reducing the voltage drop over the drain-to-source
 - Reduce voltage overshoots and undershoots caused by the load steps
 - Enable fast transient response and a high loop bandwidth.



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Figure 2. TIDA-01407 Block Diagram

2.2 Highlighted Products

The TIDA-01407 reference design features the following Texas Instruments devices.

2.2.1 UCC28951-Q1

The UCC28951-Q1 is an enhanced phase-shifted full-bridge controller which implements programmable delays to ensure ZVS operation over a wide range of operating conditions. The device contains all of the necessary features and multiple light load management to ensure maximized efficiency at overall conditions. The UCC28951-Q1 includes support for current or voltage mode control. The device features a programmable switching frequency up to 1 MHz and a wide set of protection features including cycle-by-cycle current limit, undervoltage lockout (UVLO), and thermal shutdown.

2.2.2 UCC27212-Q1

The UCC27212-Q1 device is a half-bridge driver with 120-V boot voltage and 4-A sink. The UCC27212-Q1 has a 4-A source-peak drive-current capability, which allows for driving large power MOSFETs with minimized switching losses during the transition through the Miller Plateau of the MOSFET. The switching node of the UCC27212-Q1 (HS pin) can handle –18 V maximum, which protects the high-side channel from inherent negative voltages caused by parasitic inductance and stray capacitance. An on-chip 120-V rated bootstrap diode eliminates the external discrete diodes. UVLO is provided for both the high-side and the low-side drivers, which in turn provides symmetric turnon and turnoff behavior and forces the outputs low if the drive voltage is below the specified threshold.

2.2.3 UCC27511A-Q1

The UCC27511A-Q1 device is a single-channel, low-side, high-speed gate driver with 4-A peak source and 8-A peak sink currents with asymmetrical drive, which boosts immunity against the parasitic Miller turnon effect. The UCC27511A-Q1 is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical). The device is designed to operate over a wide VDD range of 4.5 V to 18 V and a wide temperature range of –40°C to 140°C. Internal UVLO circuitry on the VDD pin holds the output low outside the VDD operating range.

2.3 System Design Theory

The TIDA-01407 TI Design implements a phase-shifted full bridge to achieve high efficiency over a wide range of operating conditions. The ZVS on the primary side of the converter reduces the switching losses and electromagnetic interference (EMI). Synchronous rectification on the secondary side is implemented to enable fast transient response and a high loop bandwidth [2].

2.3.1 Power Budget

The power budget is set as shown in [Equation 1](#) to meet the efficiency goal.

$$P_{\text{BUDGET}} = P_{\text{OUT}} \times \frac{(1 - \eta)}{\eta} = 400 \text{ W} \times \frac{(1 - 94\%)}{94\%} = 25.5 \text{ W} \quad (1)$$

2.3.2 Transformer Parameter Calculations

This subsection introduces transformer parameter calculations, which include turns ratio, magnetizing inductance, leakage inductance, and so forth [3].

The transformer turns ratio is calculated in [Equation 2](#).

$$a_1 = \frac{N_p}{N_s} \quad (2)$$

where,

- N_p is the number of turns at the transformer primary side
- N_s is the number of turns at the transformer secondary side.

The voltage drop from the BSC072N08NS5 MOSFET (V_{RDSON}) is calculated in Equation 3 as:

$$V_{RDSON} = I_{DS} \times R_{DSON} = 11.2 \text{ A} \times 7.2 \text{ m}\Omega = 0.08 \text{ V} \quad (3)$$

where,

- I_{DS} is the current flowing through the drain-to-source of the primary MOSFETs.

The maximum duty cycle (D_{MAX}) is set as 70% at the minimum specified input voltage (V_{INMIN}). The transformer turns ratio is calculated in Equation 4 as:

$$a_1 = \frac{(V_{INMIN} - 2 \times V_{RDSON}) \times D_{MAX}}{V_{OUT} + V_{RDSON}} = \frac{(36 \text{ V} - 2 \times 0.08 \text{ V}) \times 70\%}{12 \text{ V} + 0.08} = 2.07 \quad (4)$$

Set the turns ratio to the closest whole turn as $a_1 = 2.5$. The typical duty cycle (D_{TYP}) at the maximum input voltage (60 V) is calculated in Equation 5 as:

$$D_{TYP} = \frac{(V_{OUT} + V_{RDSON}) \times a_1}{(V_{IN} - 2 \times V_{RDSON})} = \frac{(12 \text{ V} + 0.08 \text{ V}) \times 2.5}{60 \text{ V} - 2 \times 0.08 \text{ V}} = 0.504 \quad (5)$$

The maximum duty cycle is recalculated again in Equation 6 with the selected turns ratio:

$$D_{MAX} = \frac{a_1 \times (V_{OUT} + V_{RDSON})}{V_{INMIN} - 2 \times V_{RDSON}} = \frac{2.5 \times (12 \text{ V} + 0.08 \text{ V})}{36 \text{ V} - 2 \times 0.08 \text{ V}} = 0.84 \quad (6)$$

The output inductor ripple current (ΔI_{LOUT}) is calculated in Equation 7 as:

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = \frac{400 \text{ W} \times 0.2}{12} = 6.7 \text{ A} \quad (7)$$

The magnetizing inductance (L_{MAG}) of the primary of the transformer (T1) must be sufficient to ensure that the converter operates in peak current-mode control. A small L_{MAG} results in a large magnetizing current, which causes the converter to operate in voltage mode instead. L_{MAG} is calculated in Equation 8 at the maximum input voltage

$$L_{MAG} \geq \frac{V_{IN_MAX} \times (1 - D_{TYP})}{\frac{\Delta I_{OUT} \times 0.5}{a_1} \times F_{SW}} = \frac{60 \text{ V} \times (1 - 0.504)}{\frac{6.7 \text{ A} \times 0.5}{2.5}} = 74 \mu\text{H} \quad (8)$$

where,

- F_{SW} is the switching frequency of the converter.

L_{MAG} is selected as 80 μH .

Figure 3 shows the primary ($I_{PRIMARY}$) and secondary side currents flowing through the transformer (I_{QE} and I_{QF}). I_{QE} and I_{QF} are also the currents that flow through the synchronous rectifiers. Calculations of the current values are provided in the following equations.

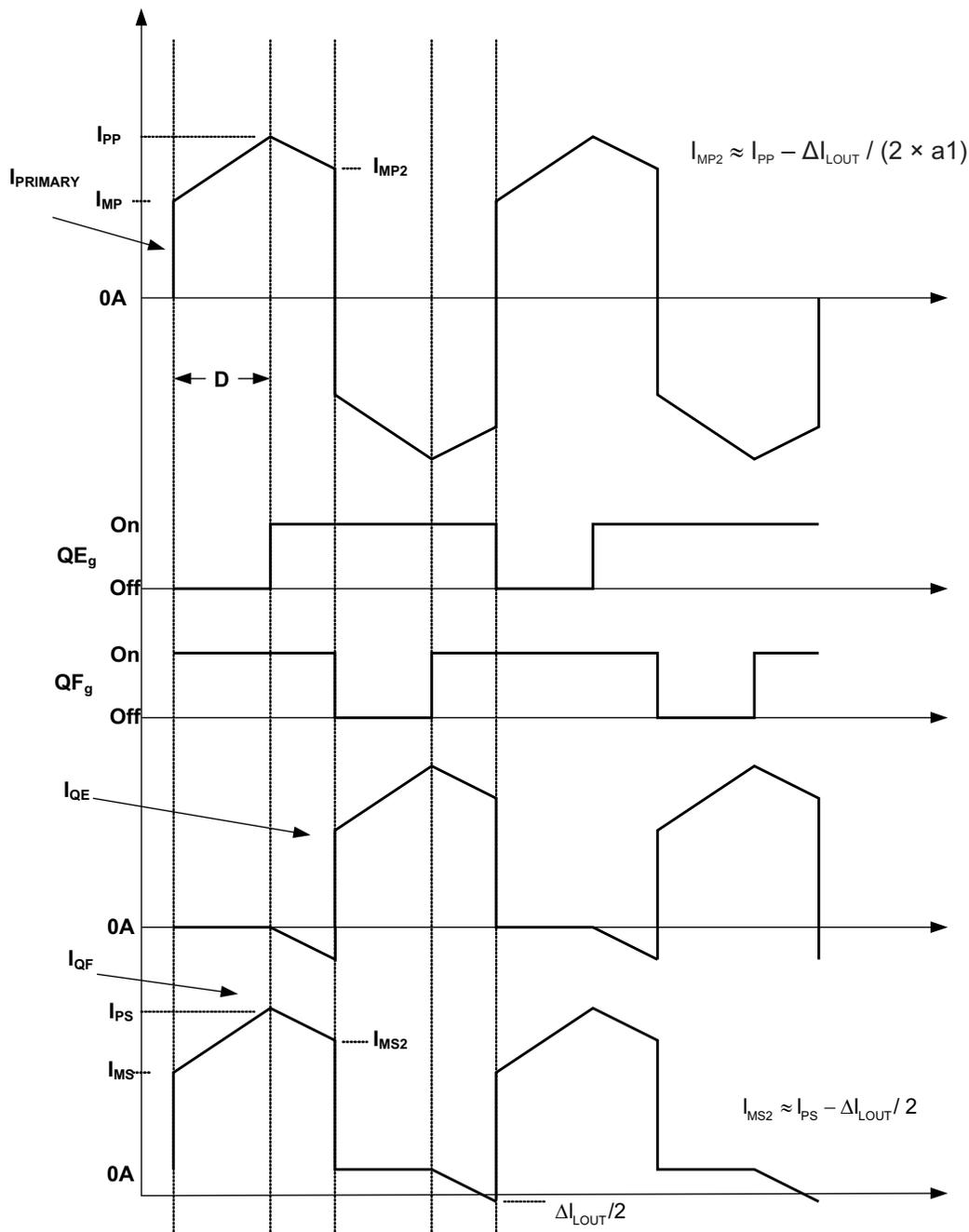


Figure 3. Transformer Primary Side and Secondary Side Currents

The peak current (I_{PS}) and the minimum current (I_{MS}) of the transformer secondary side are calculated in Equation 9, Equation 10, and Equation 11 as:

$$I_{PS} = \frac{P_{OUT}}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} = \frac{400}{12} + \frac{6.7 \text{ A}}{2} = 36.7 \text{ A} \quad (9)$$

$$I_{MS} = \frac{P_{OUT}}{V_{OUT}} - \frac{\Delta I_{LOUT}}{2} = \frac{400}{12} - \frac{6.7 \text{ A}}{2} = 30 \text{ A} \quad (10)$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{LOUT}}{2} = 36.7 \text{ A} - \frac{6.7 \text{ A}}{2} = 33.35 \text{ A} \quad (11)$$

The secondary RMS current (I_{SRMS1}) when the energy is being delivered to the secondary is calculated in [Equation 12](#):

$$\begin{aligned}
 I_{SRMS1} &= \sqrt{\left(\frac{D_{MAX}}{2}\right) \times \left(I_{PS} \times I_{MS} + \frac{(I_{PS} - I_{MS})^2}{3}\right)} \\
 &= \sqrt{\left(\frac{70\%}{2}\right) \times \left(36.7 \text{ A} \times 30 \text{ A} + \frac{(36.7 \text{ A} - 30 \text{ A})^2}{3}\right)} \\
 &= 19.8 \text{ A}
 \end{aligned} \tag{12}$$

The secondary RMS current (I_{SRMS2}) when the current is circulating through the transformer while MOSFETs Q1, Q4, Q5, Q6, A7, and Q8 are all ON is calculated in [Equation 13](#) as:

$$\begin{aligned}
 I_{SRMS2} &= \sqrt{\left(\frac{1 - D_{MAX}}{2}\right) \times \left(I_{PS} \times I_{MS2} + \frac{(I_{PS} - I_{MS2})^2}{3}\right)} \\
 &= \sqrt{\left(\frac{1 - 70\%}{2}\right) \times \left(36.7 \text{ A} \times 33.35 \text{ A} + \frac{(36.7 \text{ A} - 33.35 \text{ A})^2}{3}\right)} \\
 &= 13.6 \text{ A}
 \end{aligned} \tag{13}$$

The secondary RMS current (I_{SRMS3}) caused by the negative current in the opposing winding during the freewheeling period is calculated in [Equation 14](#) as:

$$I_{SRMS3} = \frac{\Delta I_{L_{OUT}}}{2} \times \sqrt{\left(\frac{1 - D_{MAX}}{2 \times 3}\right)} = \frac{6.7 \text{ A}}{2} \times \sqrt{\left(\frac{1 - 70\%}{2 \times 3}\right)} = 0.75 \text{ A} \tag{14}$$

As a result, the total RMS current that flows into the transformer secondary (I_{SRMS}) is calculated in [Equation 15](#) as:

$$I_{SRMS} = \sqrt{I_{SRMS1}^2 + I_{SRMS2}^2 + I_{SRMS3}^2} = \sqrt{19.8 \text{ A}^2 + 13.6 \text{ A}^2 + 0.75 \text{ A}^2} = 24 \text{ A} \tag{15}$$

The input inductor ripple current (ΔI_{LMAG}) is calculated in [Equation 16](#) as:

$$\Delta I_{LMAG} = \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times F_{SW}} = \frac{36 \text{ V} \times 70\%}{80 \mu\text{H} \times 300 \text{ kHz}} = 1.1 \text{ A} \tag{16}$$

The peak current that flows into the transformer primary side (I_{PP}) is calculated in [Equation 17](#) as:

$$\begin{aligned}
 I_{PP} &= \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{L_{OUT}}}{2}\right) \times \frac{1}{a_1} + \Delta I_{LMAG} \\
 &= \left(\frac{400 \text{ W}}{12 \times 93\%} + \frac{6.7 \text{ A}}{2}\right) \times \frac{1}{2.5} + 1.1 \text{ A} \\
 &= 16.8 \text{ A}
 \end{aligned} \tag{17}$$

The minimum current that flows into the transformer primary side (I_{MP}) is calculated in Equation 18 as:

$$\begin{aligned} I_{MP} &= \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{OUT}}{2} \right) \times \frac{1}{a_1} - \Delta I_{LMAG} \\ &= \left(\frac{400 \text{ W}}{12 \times 93\%} + \frac{6.7 \text{ A}}{2} \right) \times \frac{1}{2.5} - 1.1 \text{ A} \\ &= 14.57 \text{ A} \end{aligned} \quad (18)$$

Equation 19 calculates the minimum current at the primary (I_{MP2}) when the converter primary-side switches are freewheeling.

$$\begin{aligned} I_{MP2} &= I_{PP} - \left(\frac{\Delta I_{L_{OUT}}}{2} \right) \times \frac{1}{a_1} \\ &= 16.8 \text{ A} - \frac{6.7 \text{ A}}{2} \times \frac{1}{2.5} \\ &= 15.46 \text{ A} \end{aligned} \quad (19)$$

The RMS current (I_{PRMS1}) at the transformer primary when energy is being delivered to the secondary is calculated in Equation 20 as:

$$\begin{aligned} I_{PRMS1} &= \sqrt{D_{MAX} \times \left(I_{PP} \times I_{MP} + \frac{(I_{PP} - I_{MP})^2}{3} \right)} \\ &= \sqrt{70\% \times \left(16.8 \text{ A} \times 14.6 \text{ A} + \frac{(16.8 \text{ A} - 14.6 \text{ A})^2}{3} \right)} \\ &= 13.2 \text{ A} \end{aligned} \quad (20)$$

The RMS current at the transformer primary side (I_{PRMS2}) when the converter is freewheeling is calculated in Equation 21 as:

$$\begin{aligned} I_{PRMS2} &= \sqrt{(1 - D_{MAX}) \times \left(I_{PP} \times I_{MP2} + \frac{(I_{PP} - I_{MP2})^2}{3} \right)} \\ &= \sqrt{(1 - 70\%) \times \left(16.8 \text{ A} \times 15.46 \text{ A} + \frac{(16.8 \text{ A} - 15.46 \text{ A})^2}{3} \right)} \\ &= 8.9 \text{ A} \end{aligned} \quad (21)$$

The total RMS current flowing through the transformer primary side (I_{PRMS}) is calculated in Equation 22 as:

$$I_{PRMS} = \sqrt{I_{PRMS1}^2 + I_{PRMS2}^2} = \sqrt{13.2 \text{ A}^2 + 8.9 \text{ A}^2} = 16 \text{ A} \quad (22)$$

2.3.3 Power Stage MOSFET Selection

The MOSFET selection is important to meet the system efficiency and electric safety. The breakdown voltage is selected based on the LV148 standard and the gate charge is minimized for system efficiency. BSC072N08NS5 80-V (V_{DS}), 74-A MOSFETs with 24-nC gate charges (Q_g) are selected for this design. The drain-to-source on-resistance $R_{ds(on)}$ is 7.2 m Ω . The output capacitance (C_{OSS_SPEC}) is 280 pF measured under $V_{DS} = 40 \text{ V}$ according to the data sheet.

The average output capacitance $C_{OSS_QA_AVG}$ is calculated in Equation 23 as:

$$C_{OSS_QA_AVG} = C_{OSS_SPEC} \times \sqrt{\frac{V_{DS}}{V_{INMAX}}} = 280 \text{ pF} \times \sqrt{\frac{40 \text{ V}}{60 \text{ V}}} = 229 \text{ pF} \quad (23)$$

The applied gate voltage is $V_g = 10$ V. The losses of one MOSFET are calculated in Equation 24 as:

$$\begin{aligned}
 P_Q &= I_{PRMS}^2 \times R_{ds(on)} + 2 Q_g \times V_g \times \frac{F_{SW}}{2} \\
 &= 16 \text{ A}^2 \times 7.2 \text{ m}\Omega + 2 \times 24 \text{ nC} \times 10 \text{ V} \times \frac{300 \text{ kHz}}{2} \\
 &= 1.9 \text{ W}
 \end{aligned}
 \tag{24}$$

2.3.4 Shim Inductor

The transformer primary side requires a certain value of inductance to be equivalently in series and achieve the ZVS. This type of inductance is called shim inductance (L_s). This inductance can be obtained either from the transformer leakage inductance or from an externally-added series inductor. The value is calculated based on the amount of energy required by the resonance. This inductance must be able to deplete the energy from the parasitic capacitance at the switch node. The parasitic capacitance is the sum of the output capacitance of the MOSFET, transformer winding capacitance, and the capacitance from the PCB layout.

The shim inductance (L_s) is calculated in Equation 25 as:

$$\begin{aligned}
 L_S &\geq (2 \times C_{OSS_QA_AVG}) \times \frac{V_{INMAX}^2}{\left(\frac{I_{PP}}{2} - \frac{\Delta I_{LOUT}}{2 \times a_1}\right)^2} \\
 &= (2 \times 229 \text{ pF}) \times \frac{60 \text{ V}^2}{\left(\frac{16.8 \text{ A}}{2} - \frac{6.7 \text{ A}}{2 \times 2.5}\right)^2} \\
 &= 0.033 \text{ }\mu\text{H}
 \end{aligned}
 \tag{25}$$

This value is attainable through the transformer leakage inductance. Additionally, a 170-nH external shim inductor is added in series with the transformer primary winding to compensate the effect of circuit parasitics. Table 2 summarizes the calculated specifications of the designed transformer.

Table 2. Phase-Shifted Full-Bridge Transformer Specifications

PARAMETER	SPECIFICATIONS
Power rating	≥ 400 W
Input voltage	36 V to 60 V
Frequency	300 kHz
Maximum duty cycle	70%
primary side inductance	80 $\mu\text{H} \pm 10\%$ at 300 KHz
Leakage inductance	0.06 μH
Output voltage	12 V
Output average current	33.3 A
Turns ratio (primary to secondary)	2.5:1
Peak current (primary)	16.8 A
Peak current (secondary)	36.7 A
RMS current (primary)	16 A
RMS current (secondary)	24 A

TI recommends the planar transformer 59023 from Payton Planar Magnetics LTD for this reference design.

2.3.5 Output Inductor Selection

The output inductor is designed for obtaining the 20% ripple current ($\Delta I_{L_{OUT}}$) at the output. The ripple current is calculated in Equation 26 as:

$$\Delta I_{L_{OUT}} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = \frac{400 \text{ W} \times 0.2}{12 \text{ V}} = 6.7 \text{ A} \quad (26)$$

The required inductance (L_{OUT}) is calculated in Equation 27 as:

$$L_{OUT} = \frac{V_{OUT} \times (1 - D_{TYP})}{\Delta I_{L_{OUT}} \times F_{SW}} = \frac{12 \text{ V} \times (1 - 65\%)}{6.7 \text{ A} \times 300 \text{ kHz}} = 2.1 \mu\text{H} \quad (27)$$

The RMS current of the output inductor ($I_{L_{OUT_RMS}}$) is calculated in Equation 28 as:

$$I_{L_{OUT_RMS}} = \sqrt{\left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + \left(\frac{\Delta I_{L_{OUT}}}{\sqrt{3}}\right)^2} = \sqrt{\left(\frac{400 \text{ W}}{12 \text{ V}}\right)^2 + \left(\frac{6.7 \text{ A}}{\sqrt{3}}\right)^2} = 33.6 \text{ A} \quad (28)$$

2.3.6 Output Capacitor Selection

The output capacitor is selected based on the required transient deviation with regards to a step change of the load current. A monolithic ceramic capacitor with a low equivalent series resistance (ESR) of 0.3 m Ω is selected. As a general rule, the bandwidth of the converter is estimated as shown in the following Equation 29:

$$f_{bw} = \frac{1}{10} \times F_{SW} = 30 \text{ kHz} \quad (29)$$

The output voltage deviation (ΔV_{OUT}) is targeted as shown in Equation 30:

$$\Delta V_{OUT} = V_{OUT} \times 3\% = 0.36 \text{ V} \quad (30)$$

The load step ($\Delta I_{loadstep}$) is considered to be the change from the maximum output current to zero. 15 ceramic capacitors are connected in parallel to minimize the ESR. As a result, the minimum required output capacitance is calculated in Equation 31 as:

$$C_{out_min} = \frac{1}{2\pi \times f_{bw}} \times \frac{1}{\frac{\Delta V_{OUT}}{\Delta I_{loadstep}} - ESR_{Cout}} = \frac{1}{2\pi \times 30 \text{ kHz}} \times \frac{1}{\frac{0.36 \text{ V}}{33.3 \text{ A}} - \frac{0.3 \text{ m}\Omega}{15}} = 246 \mu\text{F} \quad (31)$$

A total of 16 22- μF , 25-V X7R ceramic capacitors from Murata are selected and connected in parallel with an ESR of 0.3 m Ω .

2.3.7 Selection of Synchronous MOSFETs

Three MOSFETs are paralleled at the secondary side for each current freewheeling cycle to share the current and minimize the losses. To meet the power requirements, the 80-V, 100-A BSC057N08NS3 MOSFET from Infineon has been selected for synchronous rectification at the secondary side. Equation 32 and Equation 33 show the parameters of the MOSFET:

$$Q_{gs} = 13 \text{ nC} \quad (32)$$

$$R_{DS(on)} = 5.7 \text{ m}\Omega \quad (33)$$

The average output capacitance (C_{OSS_AVG}) is calculated based on the data sheet parameters for C_{OSS} , the drain-to-source voltage where C_{OSS_SPEC} is measured (V_{ds_SPEC}), and the maximum drain-to-source voltage in the design (V_{dsQE}) that is eventually applied to the MOSFET in the circuit. Equation 34 calculates the voltage across the MOSFET when switched off:

$$V_{dsQE} = \frac{V_{INMAX}}{a_1} = \frac{80 \text{ V}}{2.5} = 32 \text{ V} \quad (34)$$

Equation 35 is the voltage where MOSFET C_{OSS} is specified and tested in the data sheet.

$$V_{ds_spec} = 40 \text{ V} \quad (35)$$

Equation 36 is the output capacitance of the selected MOSFET.

$$C_{oss_spec} = 780 \text{ pF} \quad (36)$$

The average output capacitance is calculated in Equation 37 as:

$$C_{oss_avg} = C_{oss_spec} \times \sqrt{\frac{V_{dsQE}}{V_{ds_spec}}} = 780 \text{ pF} \times \sqrt{\frac{32 \text{ V}}{40 \text{ V}}} = 0.7 \text{ nF} \quad (37)$$

Equation 38 is the RMS current that flows into the MOSFETs.

$$I_{QE_RMS} = I_{SRMS} = 24 \text{ A} \quad (38)$$

The MOSFET data sheet provides the typical gate charge curve (see Figure 4). The gate charge at the beginning of the Miller plateau is determined in Equation 39 as:

$$QE_{MILLER_min} = 16 \text{ nC} \quad (39)$$

The gate charge at the end of the Miller plateau is determined in Equation 40 as:

$$QE_{MILLER_max} = 25 \text{ nC} \quad (40)$$

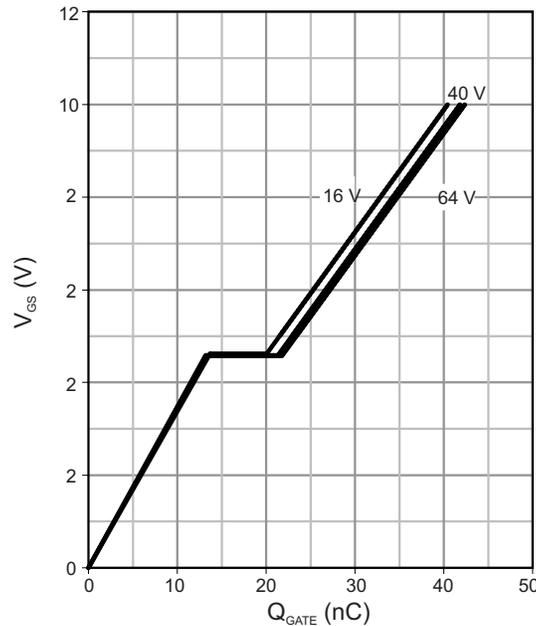


Figure 4. Gate Charge Curve of BSC057N08NS3

Equation 41 lists the gate driver (UCC27511A-Q1) peak source current:

$$I_p = 8 \text{ A} \quad (41)$$

Therefore, the MOSFET switching rise and fall times are estimated in Equation 42 as:

$$t_r \approx t_f = \frac{QE_{MILLER_max} - QE_{MILLER_min}}{\frac{I_p}{2}} = \frac{25 \text{ nC} - 16 \text{ nC}}{\frac{8 \text{ A}}{2}} = 2.3 \text{ ns} \quad (42)$$

Therefore, the total losses of the MOSFETs are calculated in Equation 43 as:

$$\begin{aligned}
 P_{QE} &= I_{QE_RMS}^2 \times R_{ds(on)} + \frac{P_{OUT}}{V_{OUT}} \times V_{dsQE} \times (t_r + t_f) \times \frac{F_{SW}}{2} + 2 \times C_{oss_avg} \times V_{dsQE}^2 \times \frac{F_{SW}}{2} + 2 \times Q_{gs} \times V_{gQE} \times \frac{F_{SW}}{2} \\
 &= 24 \text{ A}^2 \times 5.7 \text{ m}\Omega + \frac{400 \text{ W}}{12} \times 32 \text{ V} \times (2.3 \text{ ns} + 2.3 \text{ ns}) \times \frac{300 \text{ kHz}}{2} \\
 &= 2 \times 700 \text{ pF} \times 32 \text{ V}^2 \times \frac{300 \text{ kHz}}{2} + 2 \times 13 \text{ nC} \times 10 \text{ V} \times \frac{300 \text{ kHz}}{2} \\
 &= 3.28 \text{ W} + 4.9 \text{ mW} + 0.22 \text{ W} + 0.04 \text{ W} \\
 &= 3.55 \text{ W}
 \end{aligned}
 \tag{43}$$

2.3.8 Input Capacitor Selection

The input capacitance is selected according to the holdup and ripple current requirements. The resonant tank frequency of the transformer is calculated in Equation 44 as:

$$f_R \frac{1}{2 \times \pi \times \sqrt{L_S \times (2 \times C_{oss_QA_AVG})}} = \frac{1}{2 \times \pi \times \sqrt{0.33 \text{ }\mu\text{H} \times (2 \times 324 \text{ pF})}} = 11 \text{ MHz}
 \tag{44}$$

The time delay is defined in Equation 45 as:

$$t_{DELAY} = \frac{2}{f_R \times 4} = \frac{2}{11 \text{ MHz} \times 4} = 46 \text{ ns}
 \tag{45}$$

The effective duty cycle clamp (D_{clamp}) is calculated in Equation 46 as:

$$D_{clamp} = \left(\frac{1}{F_{SW}} - t_{DELAY} \right) \times F_{SW} = \left(\frac{1}{300 \text{ kHz}} - 46 \text{ ns} \right) \times 300 \text{ kHz} = 98\%
 \tag{46}$$

The capacitance must maintain the output regulation while the input voltage reaches the minimum (V_{drop}), which Equation 47 shows:

$$V_{drop} = 20 \text{ V}
 \tag{47}$$

The input capacitance is calculated in Equation 48 based on the holdup time of 150 μs :

$$C_{IN} \geq \frac{2 \times P_{OUT} \times 150 \text{ }\mu\text{s}}{(V_{IN}^2 - V_{drop}^2)} = \frac{2 \times 400 \text{ W} \times 150 \text{ }\mu\text{s}}{(36 \text{ V}^2 - 20 \text{ V}^2)} = 134 \text{ }\mu\text{F}
 \tag{48}$$

The high frequency RMS current delivered from the input capacitor is calculated in Equation 49 as:

$$I_{CINRMS} = \sqrt{I_{PRMS1}^2 - \left(\frac{P_{OUT}}{V_{INMIN} \times a_1} \right)^2} = \sqrt{13.2 \text{ A}^2 - \left(\frac{400 \text{ W}}{36 \text{ V} \times 2.5} \right)^2} = 13.2 \text{ A}
 \tag{49}$$

The input capacitors must be selected such that the total RMS current withstand rate is higher than 13.2 A.

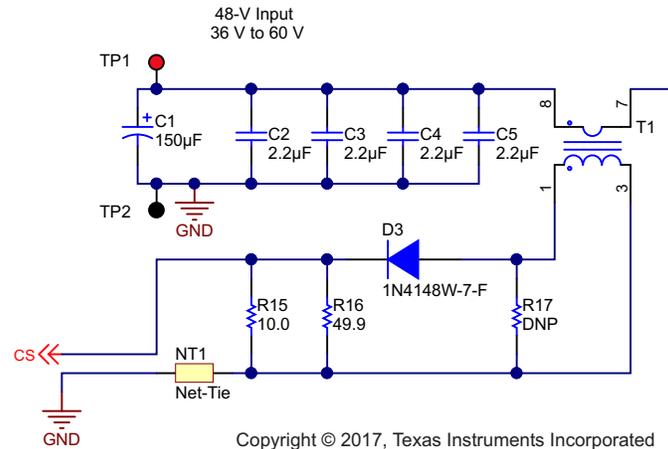


Figure 6. Current Sense Network

The maximum voltage across D3 (V_{DA}) is calculated in Equation 54 as:

$$V_{DA} = V_P \times \frac{D_{CLAMP}}{1 - D_{CLAMP}} = 2 \times \frac{98\%}{1 - 98\%} = 98 \text{ V} \quad (54)$$

This design uses a fast reverse-recovery diode (part number 1N4148W) with 100 V of breakdown voltage.

The power loss (P_{DA}) for D3 is calculated in Equation 55 as:

$$P_{DA} = \frac{P_{OUT} \times 1.3 \text{ V}}{V_{INMIN} \times 93\% \times a_2} = \frac{400 \text{ W} \times 1.3 \text{ V}}{36 \text{ V} \times 93\% \times 100} = 0.16 \text{ W} \quad (55)$$

The reset resistor R17 is placed to demagnetize the current transformer. The buildup voltage during the ON time of the current transformer is calculated in Equation 56 as:

$$V_{T1ON} = V_f + \left(\frac{I_{PRMS1}}{a_2} \right) \times R_S = 1.3 \text{ V} + \left(\frac{13.2 \text{ A}}{100} \right) \times 10 \Omega = 2.62 \text{ V} \quad (56)$$

The buildup voltage during the OFF time of the current transformer is calculated in Equation 57 as:

$$V_{T1OFF} = \left(\frac{I_{PRMS2}}{a_2} \right) \times R_{17} = \left(\frac{8.9 \text{ A}}{100} \right) \times R_{17} \quad (57)$$

Equation 58 and Equation 59 are used to calculate R17 as 1.45 kΩ:

$$V_{T1ON} \times T_{1ON} = V_{T1OFF} \times T_{1OFF} \quad (58)$$

$$\frac{T_{1ON}}{T_{1OFF}} = \frac{D_{MAX}}{1 - D_{MAX}} \quad (59)$$

Resistor R32 and capacitor C34 form a low-pass filter for the current sense signal pin 15 with Equation 60 calculating a cutoff frequency of:

$$f_L = \frac{1}{2 \times \pi \times R_{32} \times C_{34}} = \frac{1}{2 \times \pi \times 100 \times 820 \text{ pF}} = 2 \text{ MHz} \quad (60)$$

2.3.9.2 Voltage Amplifier

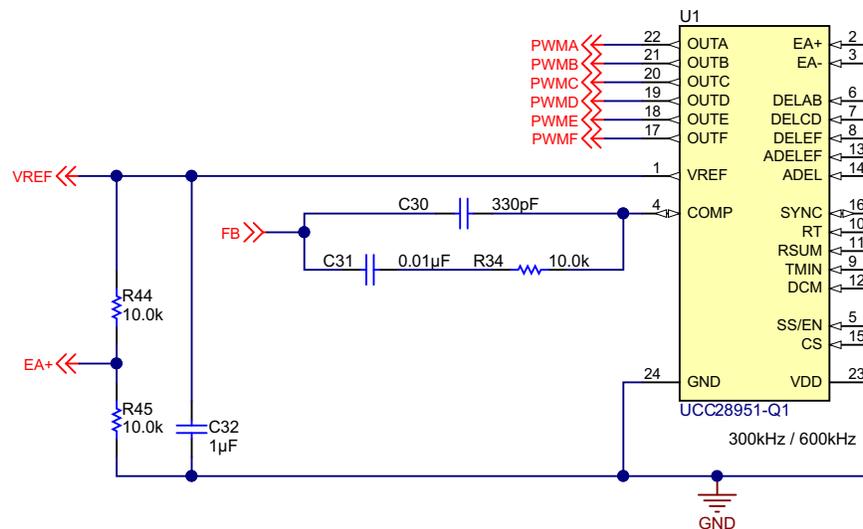
The voltage amplifier reference voltage (pin 2, EA+) is set by a voltage divider (R44 and R45 as the schematic in Figure 5 shows) from the internal reference pin (V_{REF}). R44 and R45 are both selected as 10 kΩ to set the reference to 2.5 V. A 1-μF decoupling capacitor is placed close to the V_{REF} pin to filter out the high-frequency noise.

The DC output voltage is set by the voltage divider R29 and R35 + R48. The feedback regulation voltage is set to 2.5 V according to Equation 61.

$$V_{EA-} = V_{OUT} \times \frac{R_{35} + R_{48}}{R_{29} + R_{35} + R_{48}} = 2.5 \text{ V} \tag{61}$$

2.3.9.3 Compensation Network

The compensation network comprises the feedback components C30, C31, and R34, as Figure 7 shows. The components must be placed as close as possible to pin 3 and pin 4.



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Figure 7. Compensation Network

The load impedance (R_{LOAD}) is calculated in Equation 62 as:

$$R_{LOAD} = \frac{V_{OUT}^2}{P_{OUT}} = \frac{12 \text{ V}^2}{400 \text{ W}} = 0.36 \Omega \tag{62}$$

The compensator gain (G_{gain}) in Equation 63 is set to:

$$G_{gain} = \frac{R_{34}}{R_{29}} = \frac{10 \text{ k}}{13.3 \text{ k}} \approx 0.75 \tag{63}$$

The compensation zero in Equation 64 is set at the pole frequency formed by the load and output capacitors:

$$\frac{1}{2 \times \pi \times C_{31} \times R_{34}} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} \tag{64}$$

where,

- C_{OUT} is the total output capacitance,
- R_{LOAD} is the load impedance.

The compensation pole in Equation 65 is set at the ESR frequency of the output capacitors:

$$\frac{1}{2 \times \pi \times C_{30} \times R_{34}} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR} \quad (65)$$

where,

- ESR is the equivalent series resistance of the output capacitor.

C30 and C31 have been selected as 330 pF and 0.01 μF per the standard values.

2.3.9.4 Soft-Start Capacitor

The UCC28951-Q1 implements a soft-start function to limit the inrush current during start-up. The soft-start time is selected as 5.7 ms. C_{SS} is calculated in Equation 66 as:

$$C_{SS} = \frac{t_{ss} \times 25 \mu A}{V_{EA-} + 0.55} = 48 \text{ nF} \quad (66)$$

2.3.9.5 Adaptive Delay DELAB, DELCD, and ADEL

The UCC28951-Q1 offers two different adaptive delay management techniques which improve the efficiency over a wide load current range:

1. ADEL – This technique sets and optimizes the dead-time control for the primary switches over a wide load current range. The technique also sets the delay between one of the outputs (OUTA or OUTB) going low and the other output going high.
2. ADELEF – This technique sets and optimizes the delay-time control between the primary side switch OUTA or OUTB going low and the secondary side switch OUTF or OUTE going low.

The resistor R51 connected from DELAB pin to GND, along with the resistor divider R41 and R53 connected from CS pin to GND, sets the delay time between the PWM outputs to the MOSFETs at the same bridge, pin OUTA or OUTB going low, and the other output going high, which is represented as T_{ABSET1} or T_{ABSET2} in Figure 8.

The CS signal fed into the ADEL pin settles and the dead-time control for the primary side switches dependent of the load current change. The delay time varies reversely proportional to the CS signal amplitude. The delay time gradually increases from T_{ABSET1} , which is measured at $V_{cs} = 1.5 \text{ V}$, to T_{ABSET2} , which is measured at $V_{cs} = 0.2 \text{ V}$. The delay time is fixed, independent of the load, when a fixed voltage is applied to the ADEL pin.

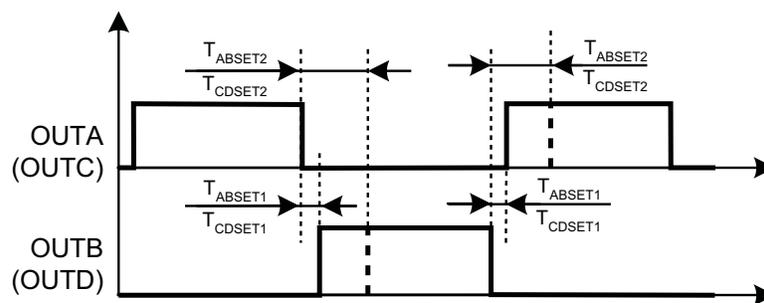


Figure 8. Delay Definitions Between OUTA and OUTB, OUTC, and OUTD

The turnon delay of primary MOSFETs Q9 (PWM signal OUTB) after Q2 (PWM signal OUTA) is initially set based on the interaction of leakage inductance L_S and the theoretical switch node capacitance. The resonant tank frequency is calculated in Equation 67 as:

$$f_R = \frac{1}{2 \times \pi \times \sqrt{L_S \times (2 \times C_{OSS_QA_AVG})}} = \frac{1}{2 \times \pi \times \sqrt{0.33 \mu H \times (2 \times 324 \text{ pF})}} = 11 \text{ MHz} \quad (67)$$

The initial t_{ABSET} is calculated in Equation 68 as:

$$t_{ABSET} = \frac{2.25}{f_R \times 4} = 52 \text{ ns} \quad (68)$$

The coefficient K_A defines how significantly the delay time depends on the CS voltage. K_A varies from 0, where the ADEL pin is shorted to ground ($R_{53} = 0$) and the delay does not depend on CS voltage, to 1, where ADEL is tied to CS ($R_{41} = 0$). In this design K_A is set as shown in the following Equation 69:

$$K_A = \frac{R_{53}}{R_{53} + R_{40}} = 1 \quad (69)$$

Therefore, the resistor from DELAB to GND R_{51} is calculated in Equation 70 as:

$$R_{51} = \frac{T_{ABSET} \times (0.26 \text{ V} + V_{CS} \times K_A \times 1.3)}{5} = 13 \text{ k}\Omega \quad (70)$$

where,

- V_{CS} is the voltage seen from pin CS when ZVS is expected to occur.

The turnon delays of OUTC and OUTD are set the same as T_{ABSET} ; therefore, R_{50} is selected as 13 k Ω , as well. The reflected output current is present in the primary of the transformer during the switching transient of MOSFETs Q3 and Q10.

2.3.9.6 Adaptive Delay DELEF, ADELEF

The resistor R_{49} from DELEF pin to GND, along with the resistor divider R_{42} and R_{43} from CS pin to GND, sets the delay time between the PWM outputs to the MOSFETs at the primary side, pin OUTA or OUTB going low, and the related output OUTF or OUTE going low, which is represented as T_{AFSET1} or T_{AFSET2} in Figure 9.

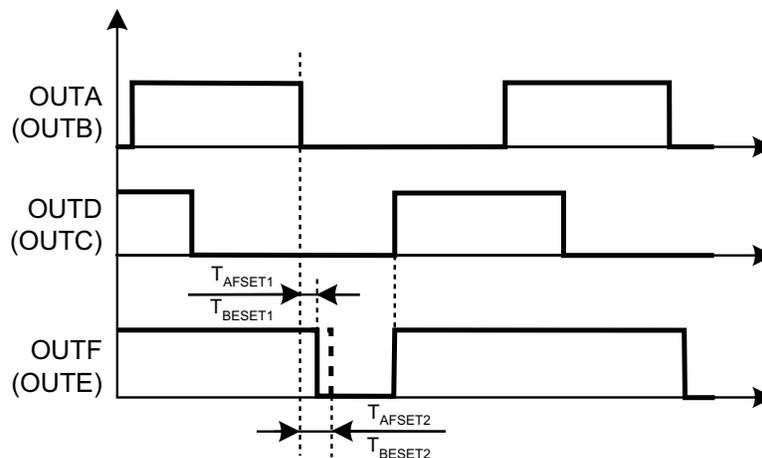


Figure 9. Delay Definitions Between OUTA and OUTF, OUTB, and OUTE

The turnoff delay of synchronous MOSFET Q1, Q4, and Q5 (PWM signal OUTE) after the turnoff of primary MOSFET Q9 (PWM signal OUTB) is set as 80 ns.

The CS voltage influence of T_{AFSET} has the same implied adaptive delay mechanism as the ADEL circuitry. In this design, the voltage fed into the ADELEF pin is tied to ground through a 10-k resistor; therefore, the coefficient K_{EF} is defined in Equation 71 as:

$$K_{EF} = \frac{R_{54}}{R_{54} + R_{42}} = 0 \quad (71)$$

The resistor from DELEF to GND R_{49} is calculated in Equation 72 as:

$$R_{49} = \frac{(T_{AFSET} - 4 \text{ ns}) \times (2.65 \text{ V} - V_{CS} \times K_{EF} \times 1.32)}{5} = 13 \text{ k}\Omega \quad (72)$$

Figure 10 shows an overview of the PWM switching and output waveforms of the phase-shifted full-bridge converter.

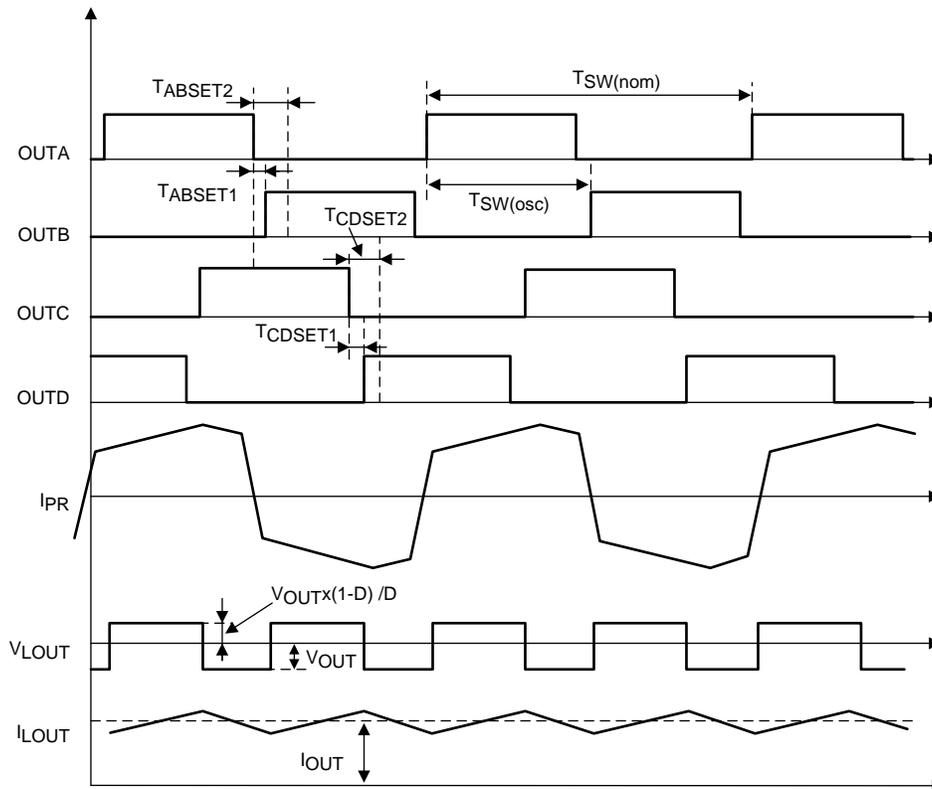


Figure 10. PWM Control and Output Waveforms of Phase-Shifted Full-Bridge Converter

2.3.9.7 Minimum Pulse (T_{MIN})

To enable ZVS at a light load, place resistor R_{TMIN} between the T_{MIN} pin to GND to set a fixed minimum pulse width. If the output PWM pulse that the feedback loop demands is shorter than T_{MIN}, the converter enters burst mode where an even number of T_{MIN} pulses are followed by the OFF time dictated by the feedback loop. The T_{MIN} duration must be selected such that it is sufficient for raising the magnetizing current in the power transformer to maintain ZVS. Figure 11 shows the typical start-up waveform and burst mode operation of the UCC28951-Q1.

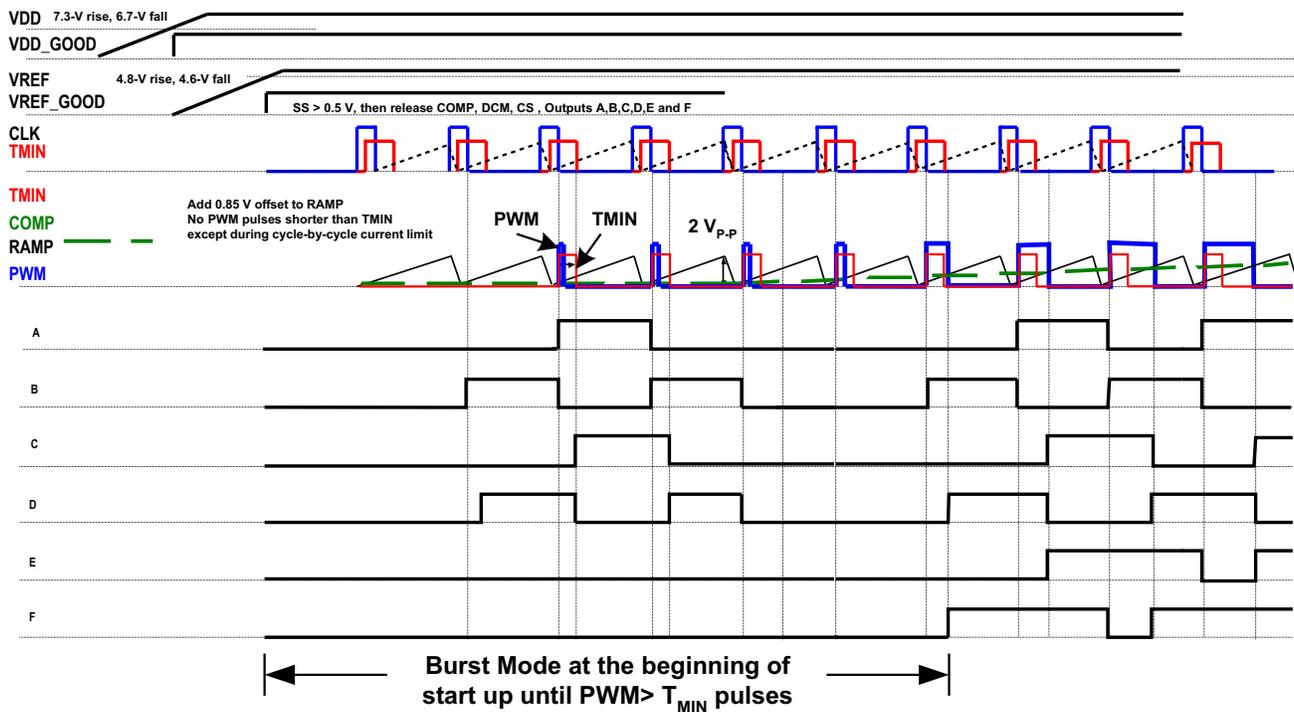


Figure 11. UCC28951-Q1 Start-Up Waveform and Burst Mode Operation

The minimum ON time for this design is set to 350 ns. R_{TMIN} is calculated in [Equation 73](#) as:

$$R_{TMIN} = \frac{t_{MIN}}{5.92} = 60 \text{ k}\Omega \quad (73)$$

2.3.9.8 Switching Frequency

The external resistor R_T , which is connected from the RT pin to the VREF pin, sets the switching frequency of the UCC28951-Q1. A switching frequency of 300 kHz is selected as a compromise between component size and efficiency. The value of R_T is calculated in [Equation 74](#) as:

$$R_T = \left(\frac{2.5 \times 10^6}{F_{SW}} - 1 \right) \times (V_{REF} - 2.5 \text{ V}) = 18.3 \text{ k}\Omega \quad (74)$$

2.3.9.9 Slope Compensation

Slope compensation is required to prevent a sub-harmonic oscillation in the peak current-mode control [\[4\]](#). Implement slope compensation by setting R_{SUM} with the following equations. The inductor current-ramp downslope as seen at the CS pin input is calculated in [Equation 75](#) as:

$$m_0 = \frac{V_{OUT}}{L_{OUT}} \times \frac{R_S}{a_1 \times a_2} = \frac{12}{2.1 \mu\text{H}} \times \frac{10}{2.5 \times 100} = 0.23 \frac{\text{V}}{\mu\text{s}} \quad (75)$$

where,

- L_{OUT} is the output inductance,
- R_S is the current sense resistor,
- a_1 is the turns ratio of the power transformer from the primary side to the secondary side (N_P / N_S),
- a_2 is the turns ratio of the current transformer from the secondary side to the primary side (I_P / I_S).

The slope of the additional ramp (m_e), which is added to the CS signal, is obtained by placing the resistor (R_{SUM}) to ground. The value for m_e is calculated in [Equation 76](#) as:

$$m_e = \left(\frac{2.5}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \quad (76)$$

The next step is to allow m_e to equalize m_0 ; therefore, R_{SUM} is calculated in [Equation 77](#) as:

$$R_{SUM} = \left(\frac{2.5 \times 2}{0.23} \right) k\Omega = 21.7 k\Omega \quad (77)$$

A 20-k Ω resistor (R47) is chosen.

2.3.9.10 Dynamic SR ON/OFF Control

The voltage at the DCM pin, which is provided by the resistor divider R_{DCMHI} (R39) between the VREF pin and DCM and the R_{DCM} (R52) from the DCM pin to GND. This voltage at the DCM pin sets the percentage of the 2-V current limit threshold for the current sense pin (CS). If the CS pin voltage falls below the DCM pin threshold voltage, then the controller initiates the light-load power-saving mode and shuts down the synchronous rectifiers, OUTE and OUTF. If the CS pin voltage is higher than the DCM pin threshold voltage, then the controller runs in CCM mode.

This design sets the percentage to approximately 10% of the load current. The threshold is calculated in [Equation 78](#) as:

$$V_{RS} = \frac{\left(\frac{P_{OUT} \times 0.15}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} \right) \times R_S}{a_1 \times a_2} = \frac{\left(\frac{400 \times 0.15}{12} + \frac{6.7 A}{2} \right) \times 8.3 \Omega}{2.5 \times 100} = 0.27 V \quad (78)$$

Set a standard resistor value for R_{DCM} ([Equation 79](#)):

$$R_{DCM} = 1 k\Omega \quad (79)$$

The resistor value of R_{DCMHI} is calculated in [Equation 80](#) as:

$$R_{DCMHI} = \frac{R_{DCM} \times (V_{REF} - V_{RS})}{V_{RS}} = \frac{1 k \times (5 - 0.27 V)}{0.27 V} = 17.5 k\Omega \quad (80)$$

The resistor value of R_{DCMHI} is finally tuned to be 19.1 k Ω .

3 Getting Started Hardware

3.1 Hardware

Figure 12 and Figure 13 show the PCB board image of TIDA-01407 from the top side and bottom side, respectively. These board images show the input and output connectors, power transformer, gate drivers, and the PCB area of the RC snubber.

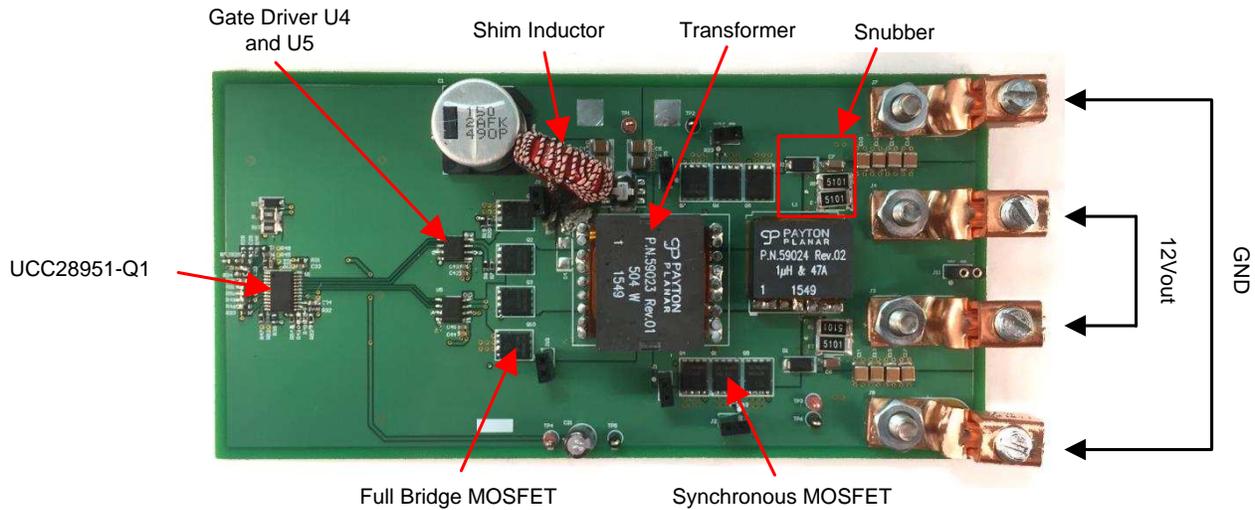


Figure 12. TIDA-01407 PCB Board—Top Side

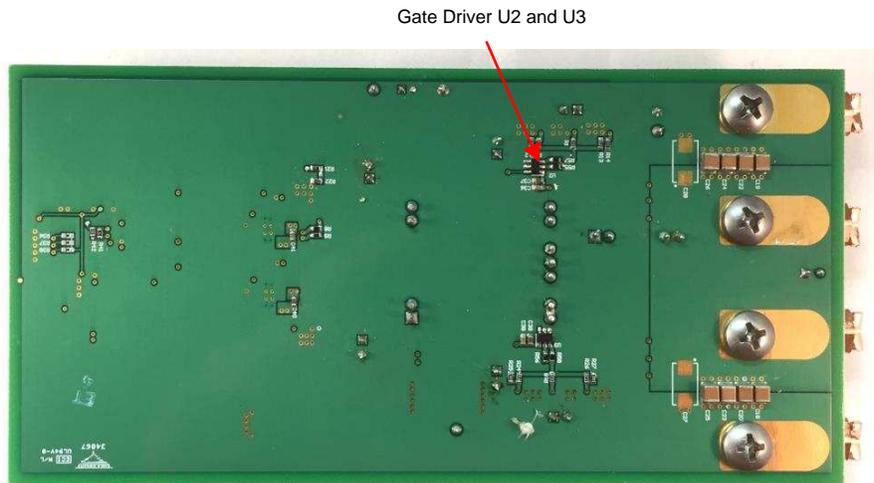


Figure 13. TIDA-01407 PCB Board—Bottom Side

4 Testing and Results

4.1 Start-Up and Power Down

Figure 14 shows the start-up waveform of the converter. As the waveform shows, the converter is powered up with a duration of 5.7 ms. Figure 15 shows the power down of the converter, where a duration of approximately 370 μ s has been observed.

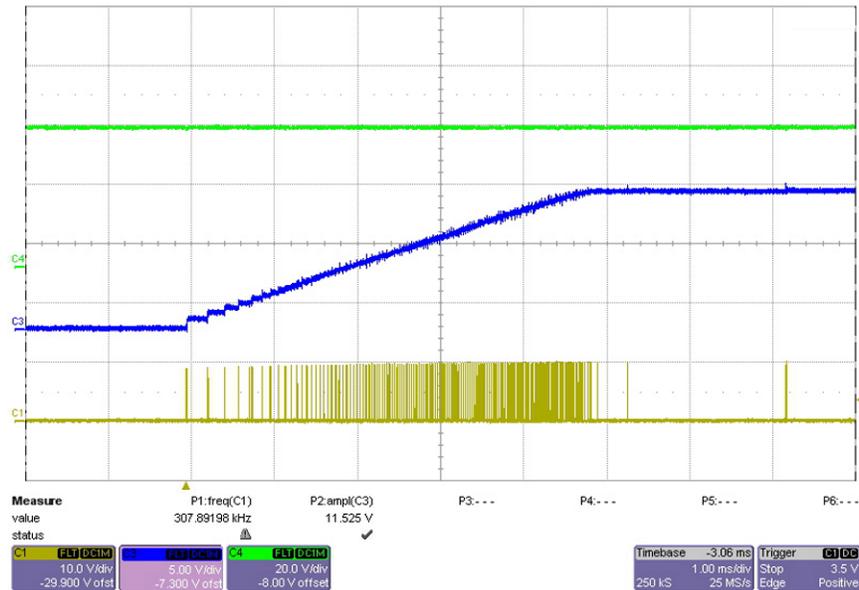


Figure 14. Start-Up Waveforms of TIDA-01407

NOTE: From top to bottom: CH4 – Input voltage, CH3 – Output voltage, CH1 – Gate drive B

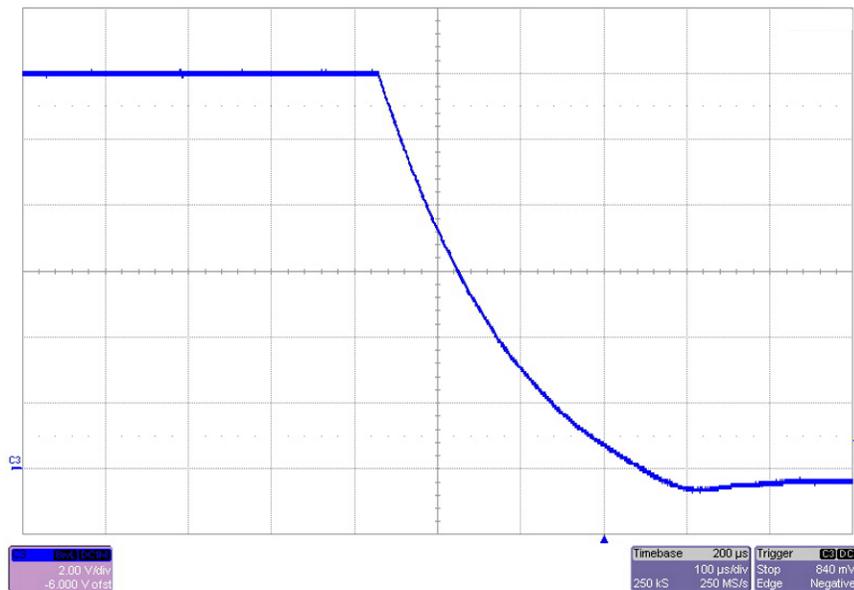


Figure 15. Power Down Waveform of TIDA-01407

NOTE: CH3: Output voltage

4.2 Output Voltage Ripple

The output voltage ripple of TIDA-01407 is measured under light-load and full-load conditions, respectively. The input voltage is kept constant as 48 V. Figure 16, Figure 17, and Figure 18 show the waveforms. As the waveforms show, less than 20 mV of peak-to-peak ripple voltage is obtained at a 33.3-A full load.

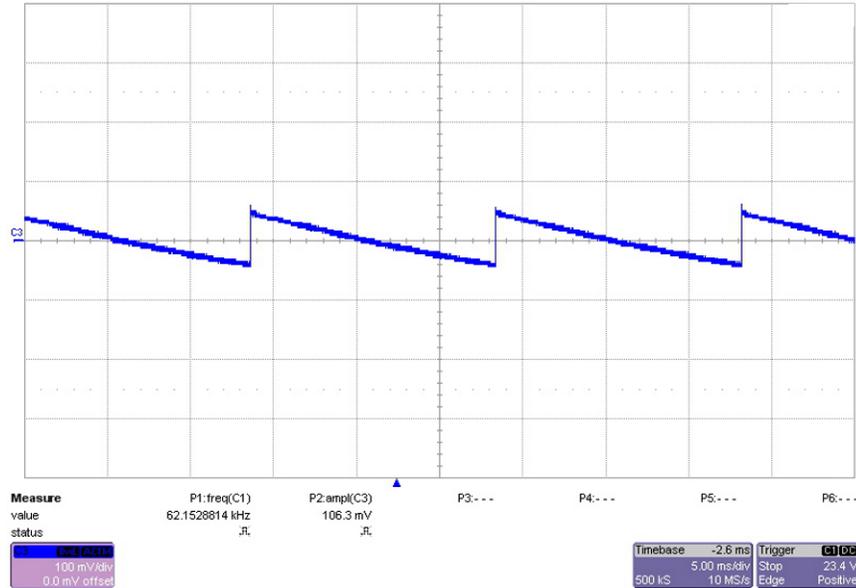


Figure 16. Output Voltage Ripple of TIDA-01407 With $V_{IN} = 48$ A and No Load

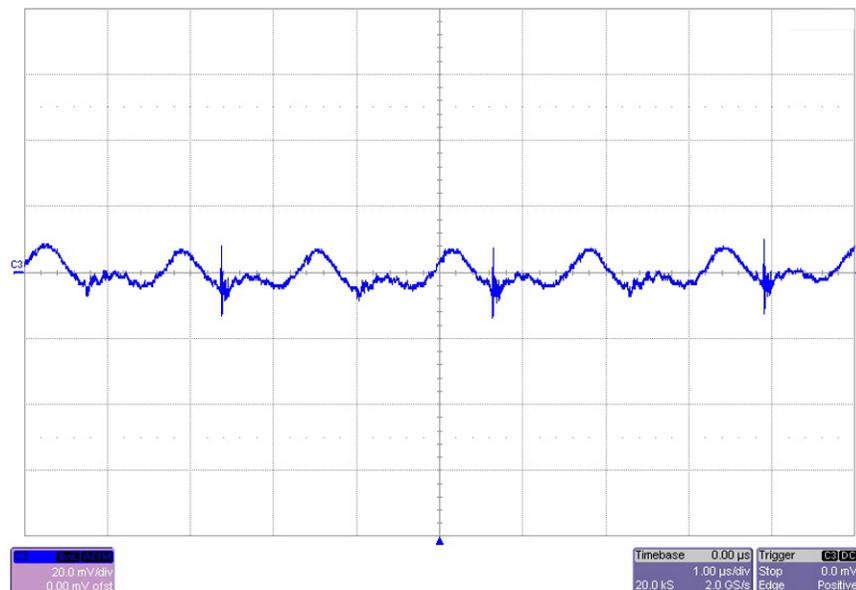


Figure 17. Output Voltage Ripple of TIDA-01407 With $V_{IN} = 48$ V and $I_{OUT} = 15$ A

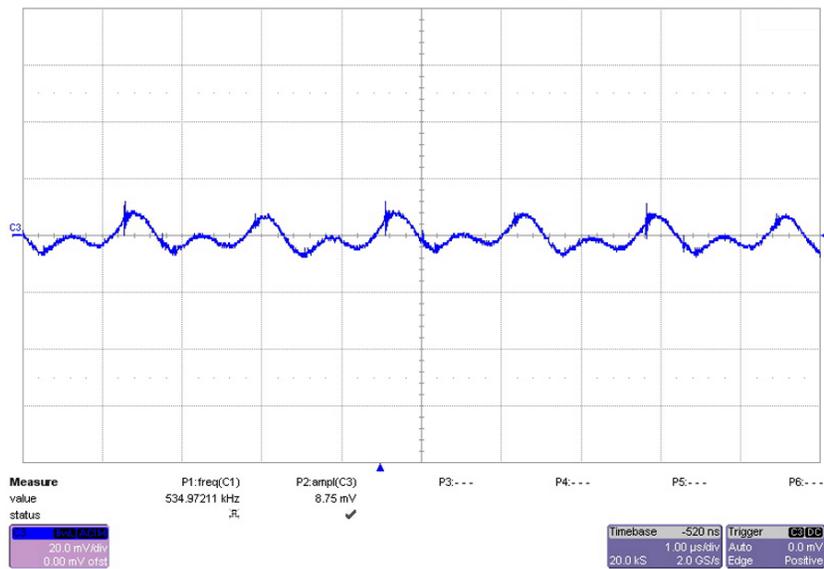


Figure 18. Output Voltage Ripple of TIDA-01407 With $V_{IN} = 48$ A and $I_{OUT} = 33.3$ A

4.3 Full Bridge Gate Drives and Primary Switch Node Voltages

The gate drive signals versus the switch node voltages of the primary side switches are measured under various load conditions (see Figure 19 to Figure 24). As the waveforms show, the ZVS resonance occurs earlier when the load current increases.

4.3.1 Under 5-A Load

Figure 19 and Figure 20 show the gate drive signals versus the switch node voltages of the primary side switches under a 5-A load.

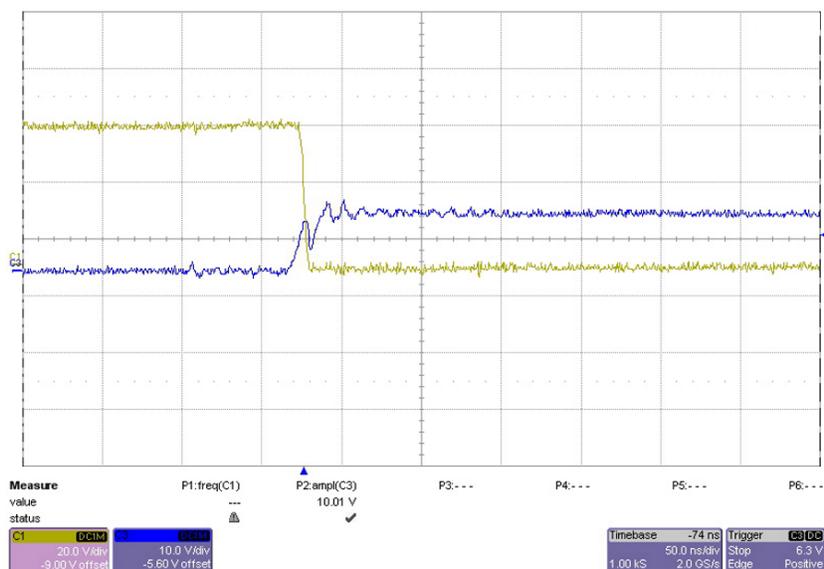


Figure 19. Switch Node AB (SW_AB) and Gate Drive B

NOTE: From top to bottom: CH1 – Drain-to-emitter voltage of Q9, CH3 – Gate drive voltage of Q9

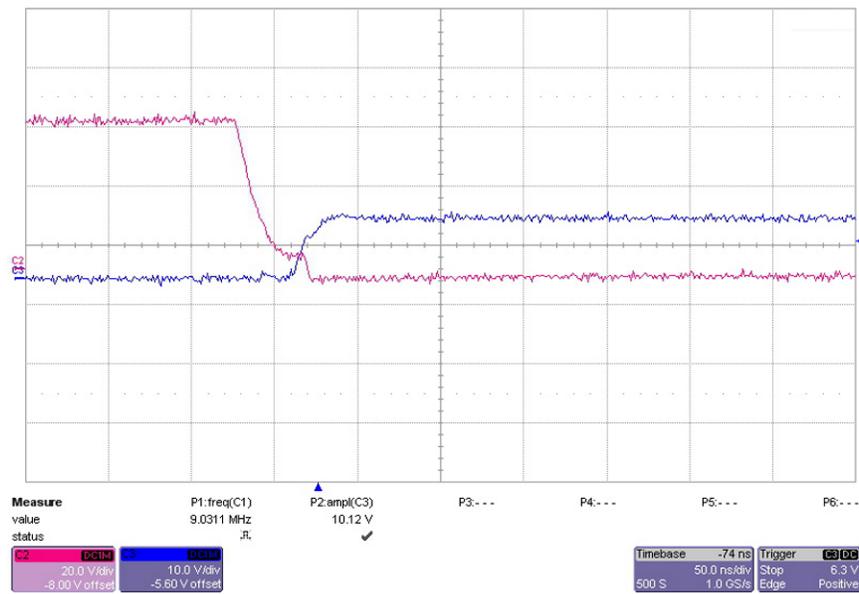


Figure 20. Switch Node CD (SW_CD) and Gate Drive D

NOTE: From top to bottom: CH2 – Drain-to-emitter voltage of Q10, CH3 – Gate drive voltage of Q10

4.3.2 Under 15-A Load

Figure 21 and Figure 22 show the gate drive signals versus the switch node voltages of the primary side switches under a 15-A load.

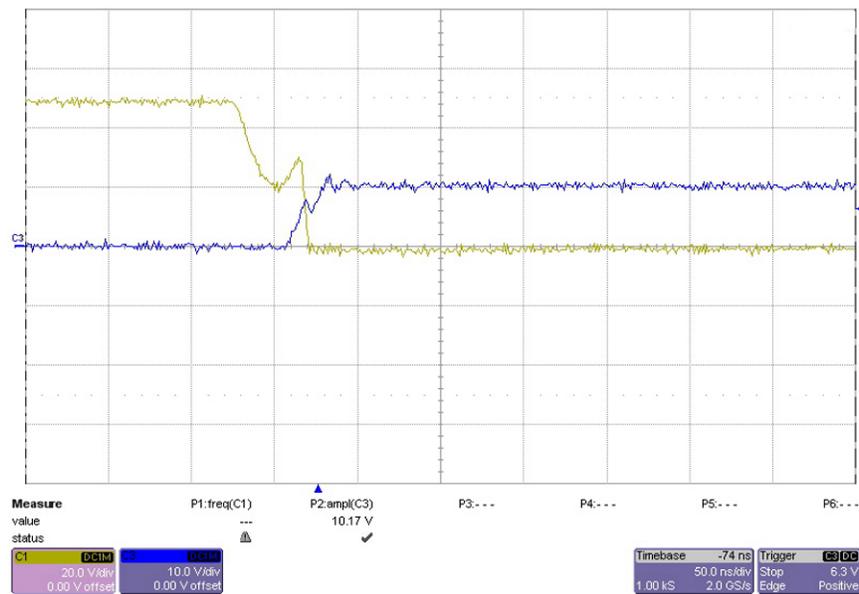


Figure 21. Switch Node AB (SW_AB) and Gate Drive B

NOTE: From top to bottom: CH1 – Drain-to-emitter voltage of Q9, CH3 – Gate drive voltage of Q9

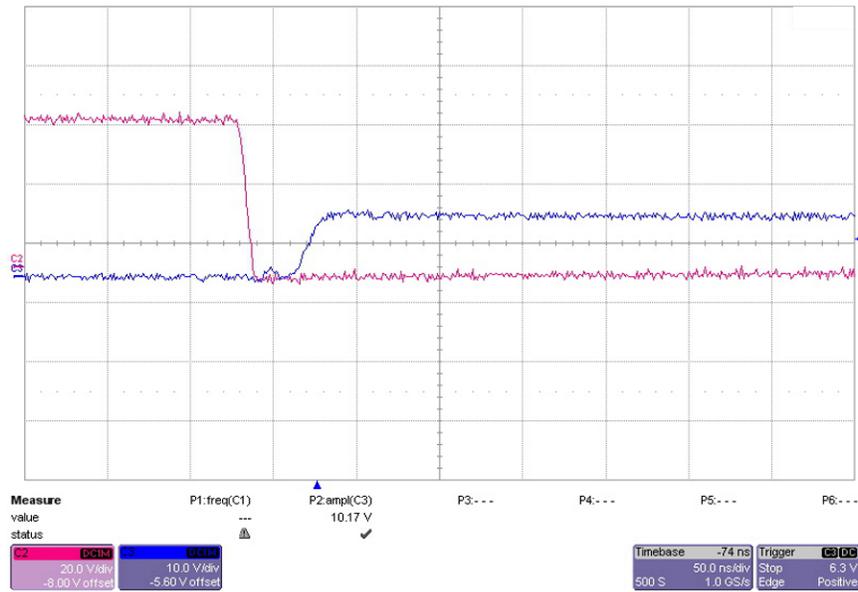


Figure 22. Switch Node CD (SW_CD) and Gate Drive D

NOTE: From top to bottom: CH2 – Drain-to-emitter voltage of Q10, CH3 – Gate drive voltage of Q10

4.3.3 Under 33.3-A Load

Figure 23 and Figure 24 show the gate drive signals versus the switch node voltages of the primary side switches under a 33.3-A load.

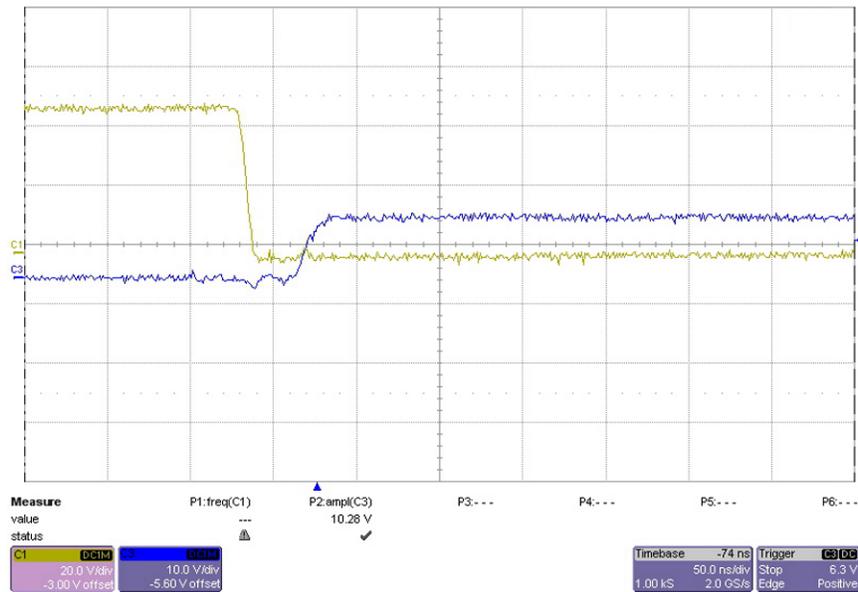


Figure 23. Switch Node AB (SW_AB) and Gate Drive B

NOTE: From top to bottom: CH1 – Drain-to-emitter voltage of Q9, CH3 – Gate drive voltage of Q9

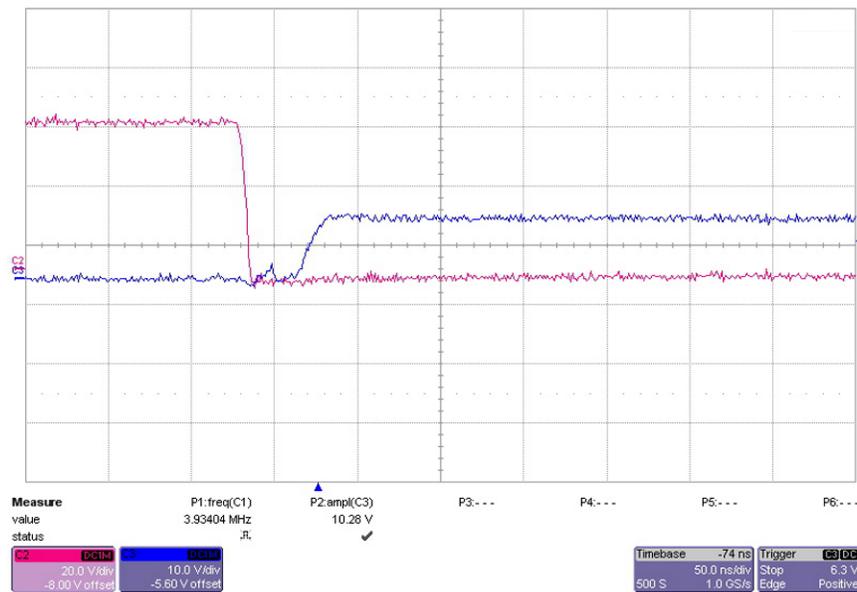


Figure 24. Switch Node CD (SW_CD) and Gate Drive D

NOTE: From top to bottom: CH2 – Drain-to-emitter voltage of Q10, CH3 – Gate drive voltage of Q10

4.4 Transition of SR From DCM to CCM

The synchronous rectifier (SR) MOSFETs at the secondary side are switched on when the converter runs from discontinuous conduction mode (DCM) into continuous conduction mode (CCM), during which the current flow path changes from the secondary side of the field-effect transistor (FET) body diode to the MOSFET channel. A comparison of Figure 25 and Figure 26 shows that there is a 730-mV voltage drop across the MOSFET body diode when the converter is running in DCM.

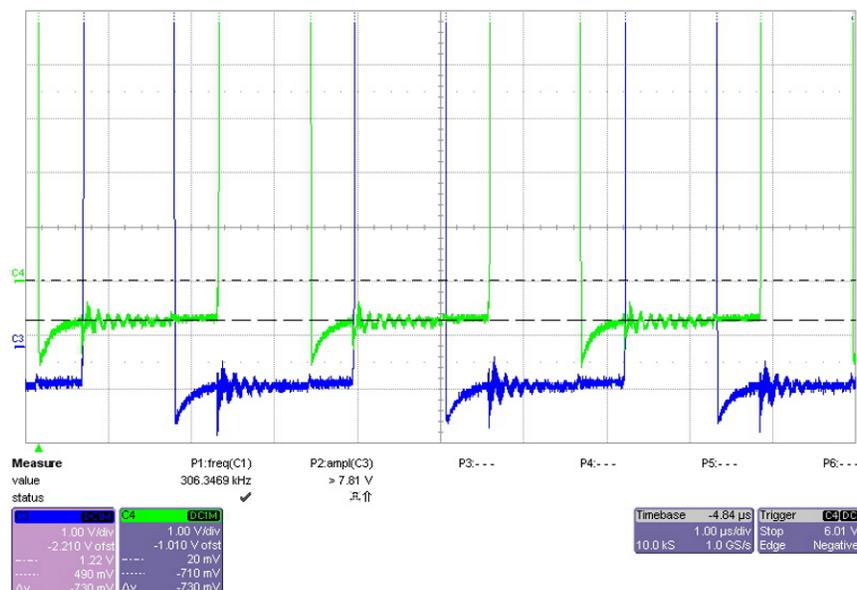


Figure 25. Switch Node Voltages of Synchronous Rectification MOSFETs When Converter Runs in DCM

NOTE: From top to bottom: CH4 – Switch node voltage of Q6, CH3 – Switch node voltage of Q1

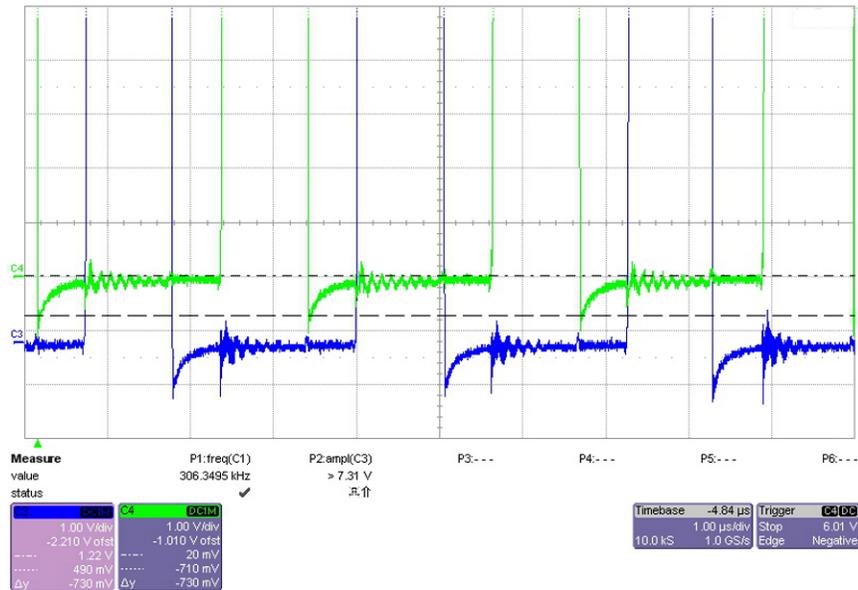
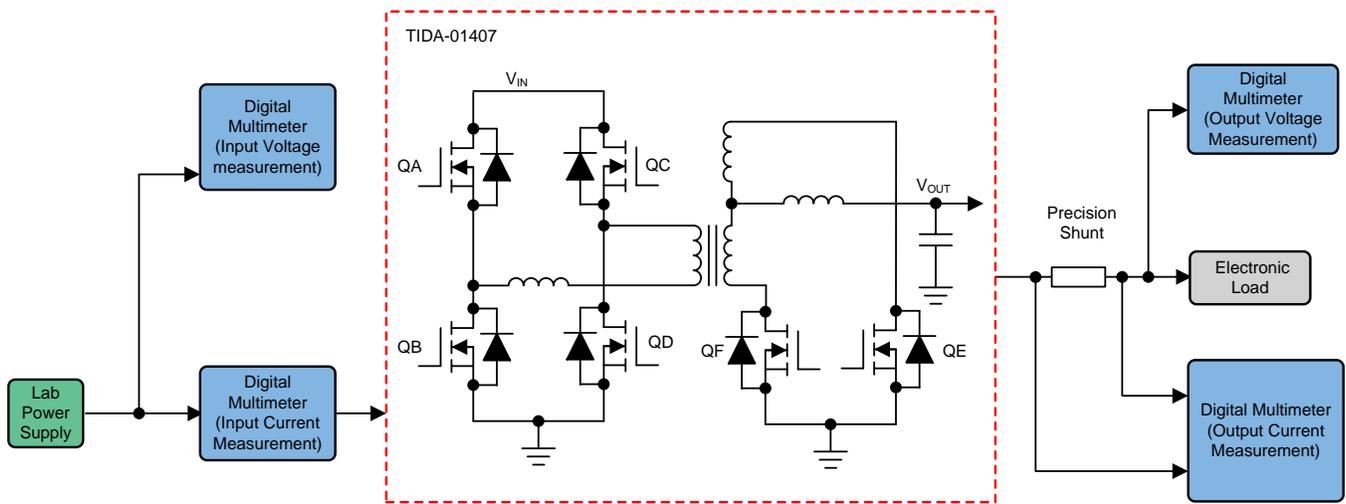


Figure 26. Switch Node Voltages of Synchronous Rectification MOSFETs When Converter Runs in CCM

NOTE: From top to bottom: CH4 – Switch node voltage of Q6, CH3 – Switch node voltage of Q1

4.5 Efficiency

The efficiency of TIDA-01407 is measured under conditions of varying input voltages. **Figure 27** shows the measurement setup. Two precision digital multimeters are placed at the input for measuring the input voltage and input current, respectively. One multimeter is placed at the output for measuring the output voltage. The output current is indirectly measured by the voltage drop from a precision shunt resistor.



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Figure 27. Experiment Setup of Efficiency Measurement

Figure 28 shows the measured efficiency of TIDA-01407. As the graph shows, a peak efficiency of 95.5% is achieved at a 36-V input voltage and 22-A load.

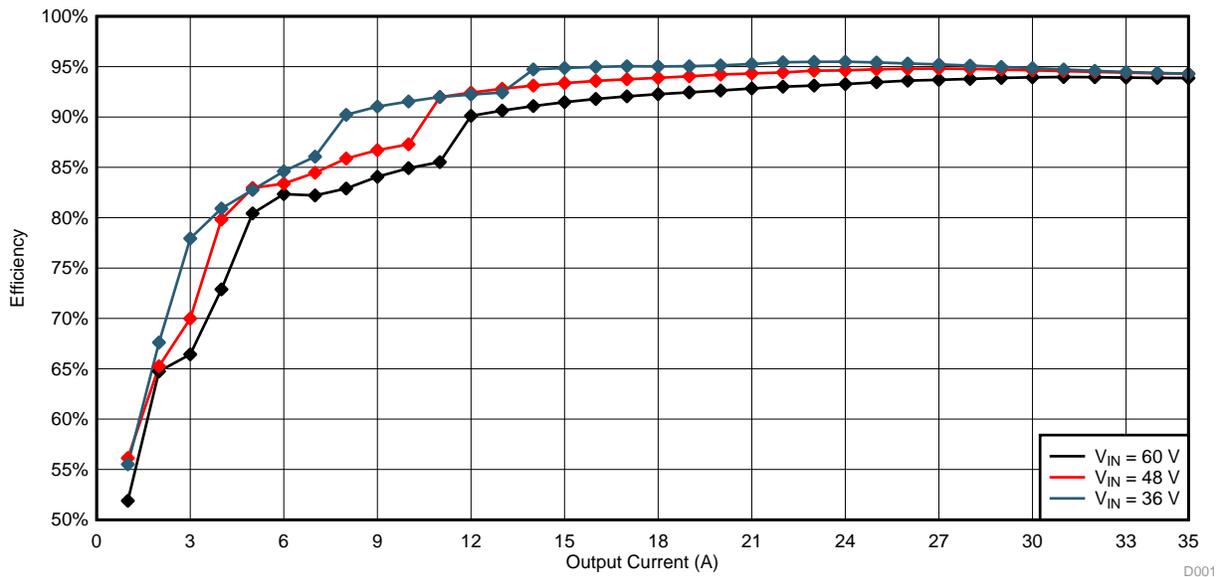


Figure 28. Measured Efficiency Under Input Voltages of 36 V, 48 V, and 60 V

4.6 Switch Node Waveforms of Synchronous Rectifier

Figure 29 shows the switch node voltage of the synchronous rectifier at the secondary side. The resistor-capacitor-diode (RCD) clamping circuit must be fine-tuned to protect the MOSFETs from overvoltage. The RCD clamp is formed by diodes D1, D2; resistors R2, R3, R4, and R5; and capacitors C6 and C7. As the waveform shows, the ringing peak is mitigated below 61 V.

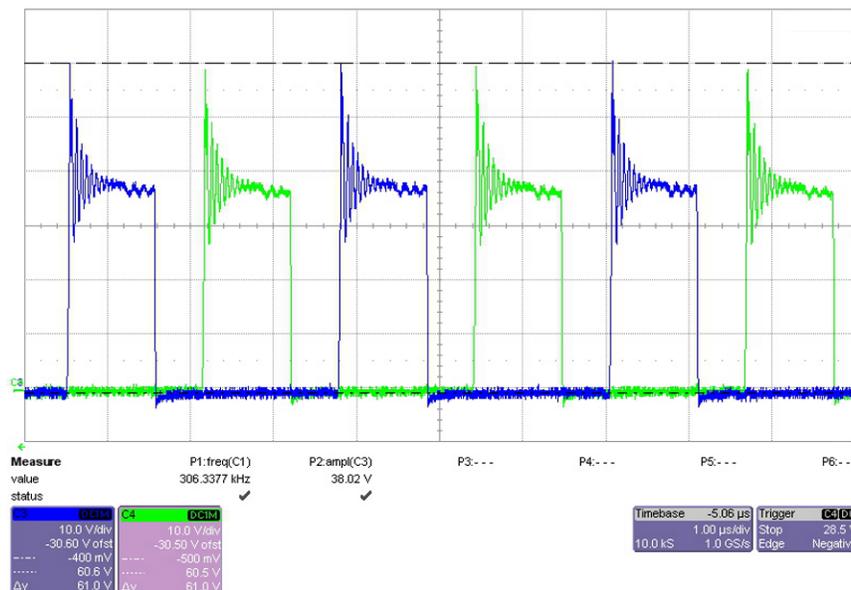


Figure 29. Switch Node Voltage of Synchronous Rectifier Under $V_{IN} = 48\text{ V}$, $I_{OUT} = 33\text{ A}$

NOTE: From top to bottom: CH3 – Switch node voltage of Q1, CH4 – Switch node voltage of Q6

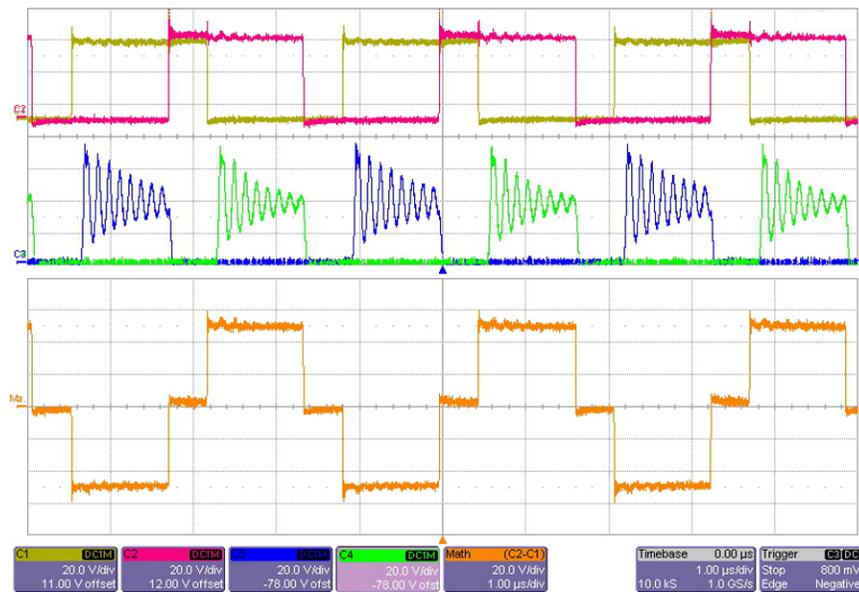


Figure 30. Switch Node Voltages and Voltage Across Transformer Primary Winding Under $V_{IN} = 48\text{ V}$, $I_{OUT} = 33\text{ A}$

NOTE: From top to bottom: CH1 – Switch node voltage of Q9, CH2 – Switch node voltage of Q10, CH3 – Switch node voltage of Q1, CH4 – Switch node voltage of Q6, Ma – Voltage across transformer primary winding

4.7 Load Regulation

Load regulation measurements show the percent of deviation from the nominal output voltage as a function of output current. The experiment setup is the same as that of the efficiency measurement shown in Figure 27. Figure 31 shows the measured results with 48-V and 60-V input voltages.

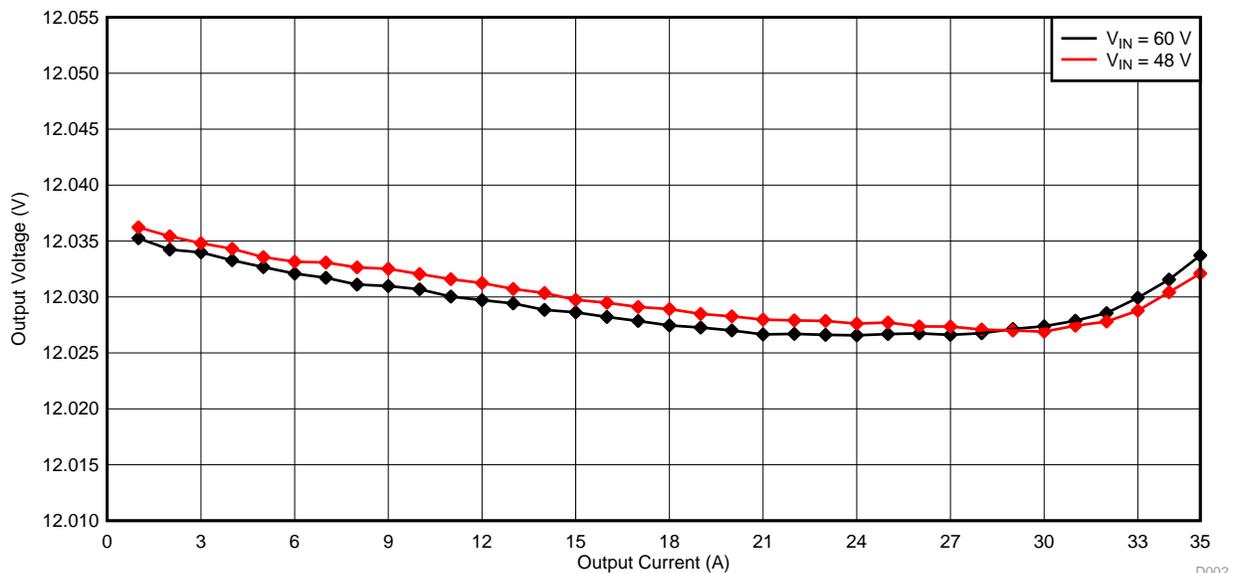


Figure 31. Load Regulation With $V_{IN} = 48\text{ V}$ and $V_{IN} = 60\text{ V}$

4.8 Load Transient Response

The load transient response presents how well a power supply copes with the changes in the load current demand. Figure 32 shows the load transient response of TIDA-01407. The load is switching from 16.5 A to 33 A with a period of 5 ms and a 50% duty cycle. The input voltage is set to 60 V.

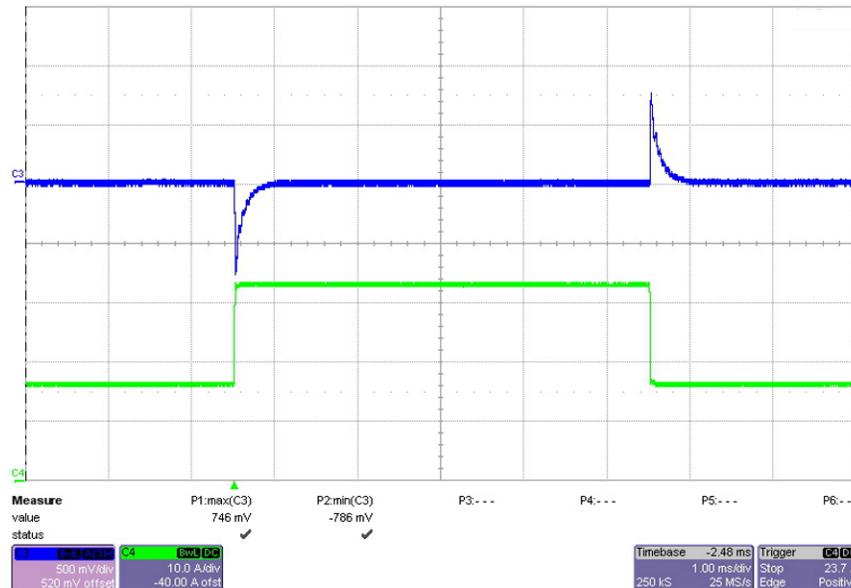


Figure 32. Load Transient Response With $V_{IN} = 60\text{ V}$ and I_{OUT} Switching Between 33 A and 16.5 A

NOTE: From top to bottom: CH3 – Output voltage ripple, CH4 – Load current

Figure 33 shows the load transient response when the input voltage is 48 V. The load is switching from 33 A to 16.5 A with a period of 5 ms and a 50% duty cycle.

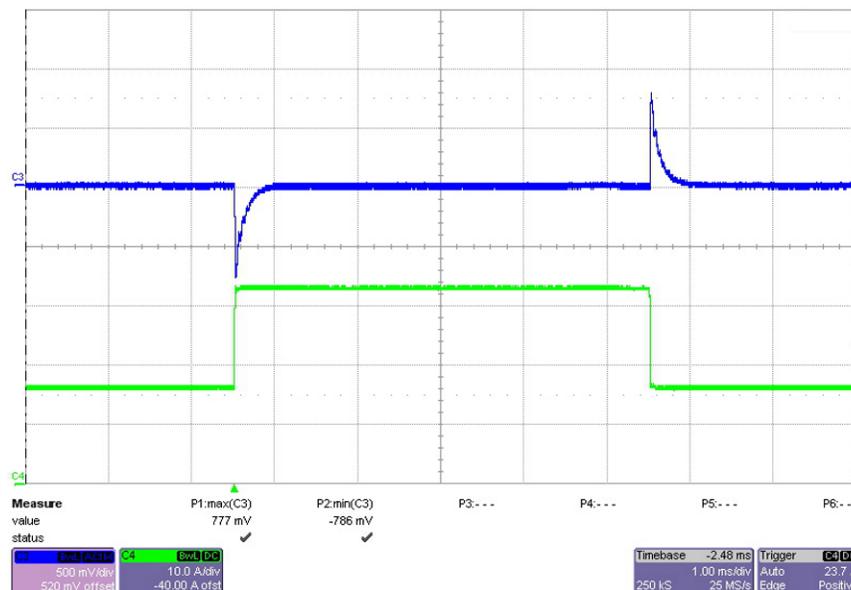


Figure 33. Load Transient Response With $V_{IN} = 48\text{ V}$ and I_{OUT} Switching Between 33 A and 16.5 A

NOTE: From top to bottom: CH3 – Output voltage ripple, CH4 – Load current

4.9 Thermal Images

The thermal images show the design board measurements under full load conditions. The circuit runs at room temperature for 15 minutes. A 48-V nominal voltage is applied. The converter is loaded with 33 A and the output power is 400 W. Figure 34 shows the temperature of the primary side switches Q2, Q9, Q3, and Q10. As the thermal image shows, the peak temperature is 81.2°C.

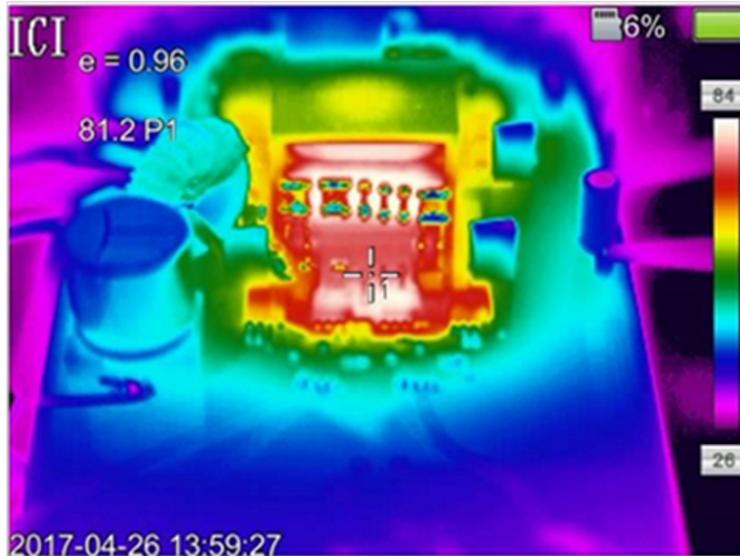


Figure 34. Thermal Image of Primary Side Switches (Q2, Q9, Q3, and Q10)

NOTE: $V_{IN} = 48\text{ V}$, $P_{OUT} = 400\text{ W}$

Figure 35 shows the temperature of the power transformer T2. As the thermal image shows, the peak temperature is 63.4°C.

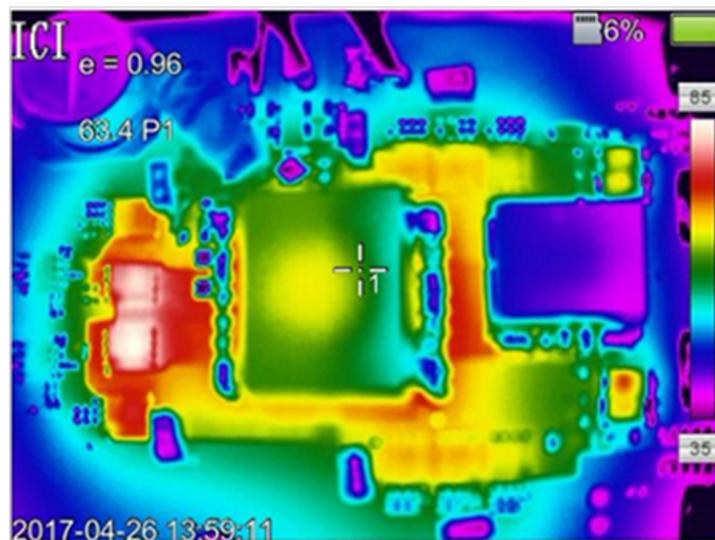


Figure 35. Thermal Image of Power Transformer T2

NOTE: $V_{IN} = 48\text{ V}$, $P_{OUT} = 400\text{ W}$

Figure 36 shows the temperature of the synchronous MOSFETs at the secondary side. As the thermal image shows, the peak temperature is 76°C.

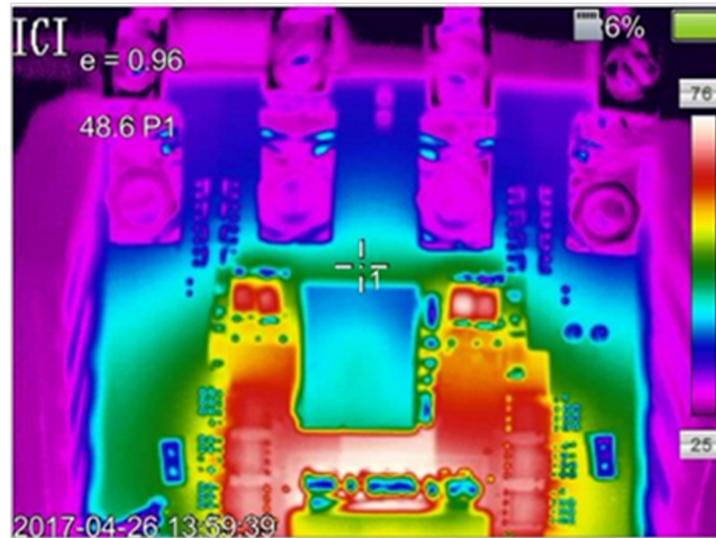


Figure 36. Thermal Image of Secondary Side Synchronous Rectifier (Q1, Q4, Q5, Q6, Q7, and Q8)

NOTE: $V_{IN} = 48\text{ V}$, $P_{OUT} = 400\text{ W}$

Figure 37 shows the temperature of the output inductor L1. As the thermal image shows, the peak temperature is 41.7°C.



Figure 37. Thermal Image of Output Inductor (L1)

NOTE: $V_{IN} = 48\text{ V}$, $P_{OUT} = 400\text{ W}$

4.10 Control Loop Frequency Response

The control loop frequency response represents the stability of the power supply system. The TIDA-01407 loop frequency response is measured under various loads and input voltages, respectively. Figure 38 shows the loop frequency response with a 48-V input voltage, 16.5-A load, and 33-A load, respectively. As the graph shows, phase margins of 59.54° and 63.46° are achieved, respectively.

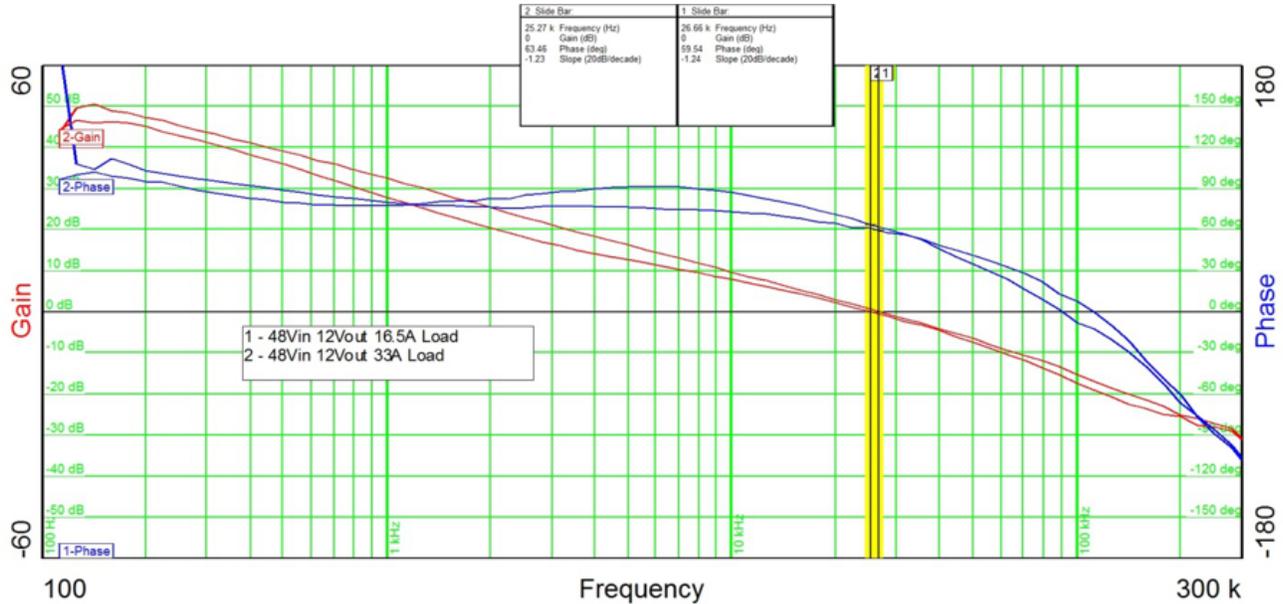


Figure 38. Loop Frequency Response of TIDA-01407 With $V_{IN} = 48\text{ V}$ and 16.5-A Load and 33-A Load

Figure 39 shows the loop frequency response with a 60-V input voltage, 16.5-A load, and 33-A load, respectively. As the graph show, phase margins of 57.63° and 58.35° are achieved, respectively.

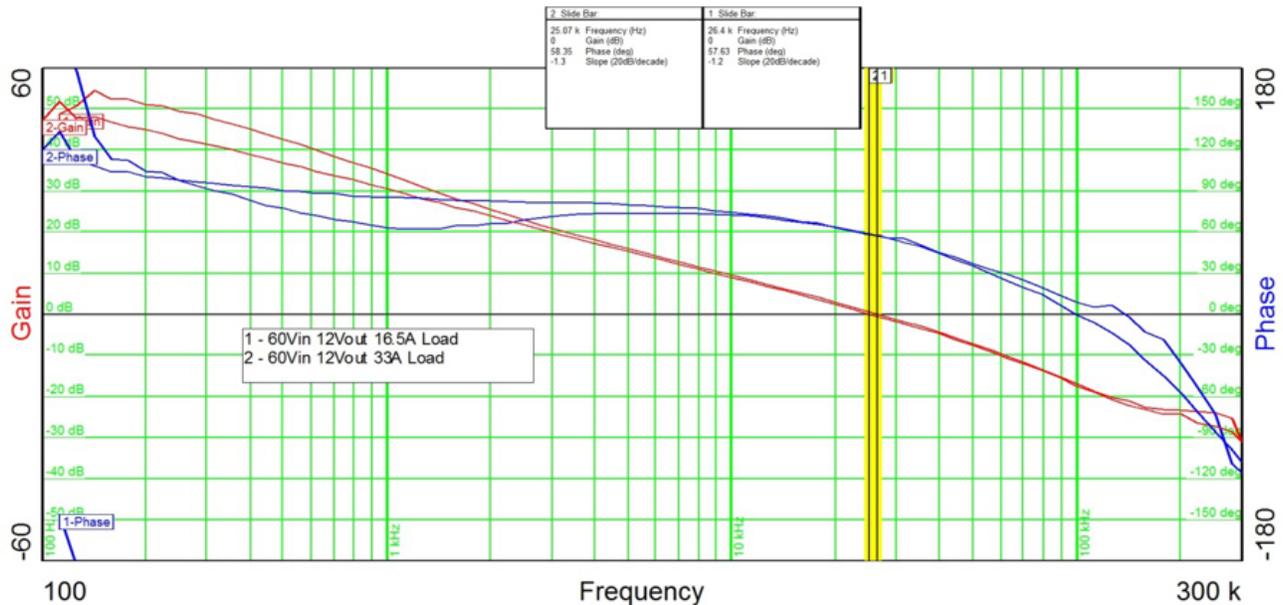


Figure 39. Loop Frequency Response of TIDA-01407 With $V_{IN} = 60\text{ V}$

5 Design Files

5.1 Schematics

To download the schematics, see the design files at [TIDA-01407](#).

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01407](#).

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01407](#).

5.3.2 Layout Guidelines

The TIDA-01407 design implements a four-layer PCB. [Figure 40](#) lists the board material, copper thickness, and the dielectric distance in between the layers.

Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Cov...	Surface Material	0.01016	Solder Resist	3.5			0
Top Layer	Signal	Copper	0.03556				Top	
Dielectric1	Dielectric	Core	1.50368	FR-4	4.8			
Signal Layer 1	Signal	Copper	0.03599				Not Allowed	
Dielectric 3	Dielectric	Prepreg	0.127		4.2			
Signal Layer 2	Signal	Copper	0.03599				Not Allowed	
Dielectric 2	Dielectric	Core	0.254		4.2			
Bottom Layer	Signal	Copper	0.03556				Bottom	
Bottom Solder	Solder Mask/Cov...	Surface Material	0.01016	Solder Resist	3.5			0
Bottom Overlay	Overlay							

Figure 40. Layer Stack of TIDA-01407

[Figure 41](#) shows the placement of the input capacitors. TI recommends to place the input capacitors as close as possible to the current transformer T1.

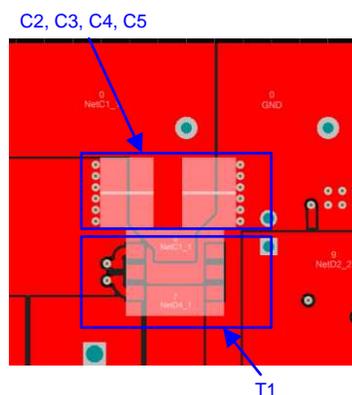


Figure 41. Placement of Input Capacitors and Current Transformer T1

Figure 42 shows the Kelvin connection from the current transformer T1 to the UCC29851-Q1 current sense pin. The two traces are kept close and identical to minimize the differential noise crosstalks.

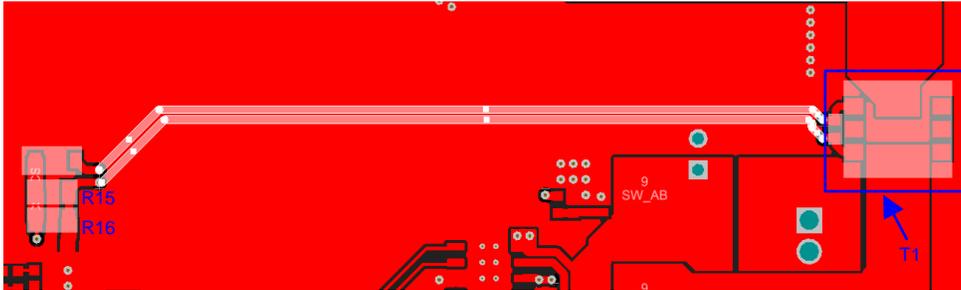


Figure 42. Placement of RC Filtering Network for Current Sense Pin (PCB Top Side)

Figure 43 shows the placement of synchronous rectification MOSFETs and the power transformer T2. The synchronous rectification MOSFETs Q1, Q4, Q5, Q6, Q7, and Q8 are placed as close as possible to the transformer secondary winding to minimize the current loop.

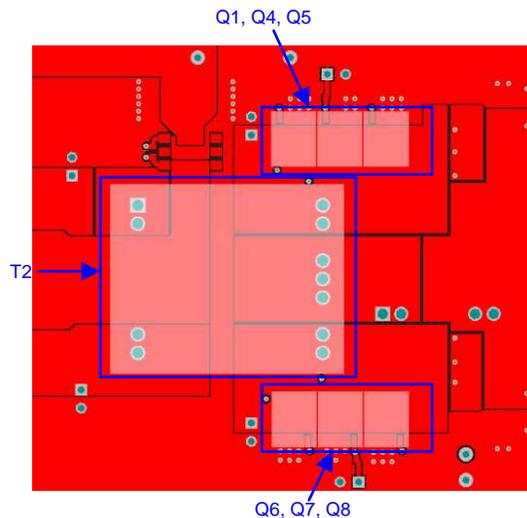


Figure 43. Synchronous Rectification MOSFETs and Power Transformer T2

Figure 44 shows the placement of the synchronous rectification MOSFETs at the transformer secondary side and the RC snubber circuit. The snubber circuit is placed close to the MOSFETs to keep the current-flowing loop tight.

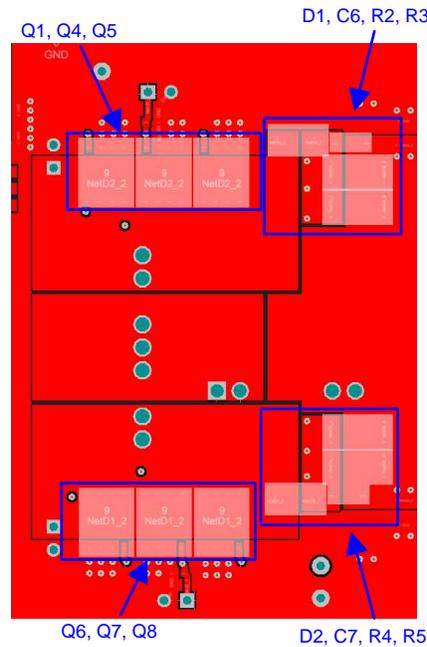


Figure 44. Placement of Synchronous Rectification MOSFETs and Snubber Circuit

Figure 45 shows the placement of the gate driver and the MOSFETs at the converter primary side. These components are placed closely to minimize the gate-drive current-flowing loop. The gate-drive current-flowing loop starts from the bootstrap capacitor C40, controller IC, gate resistor, MOSFET Q2, and then circles back to the capacitor C40.

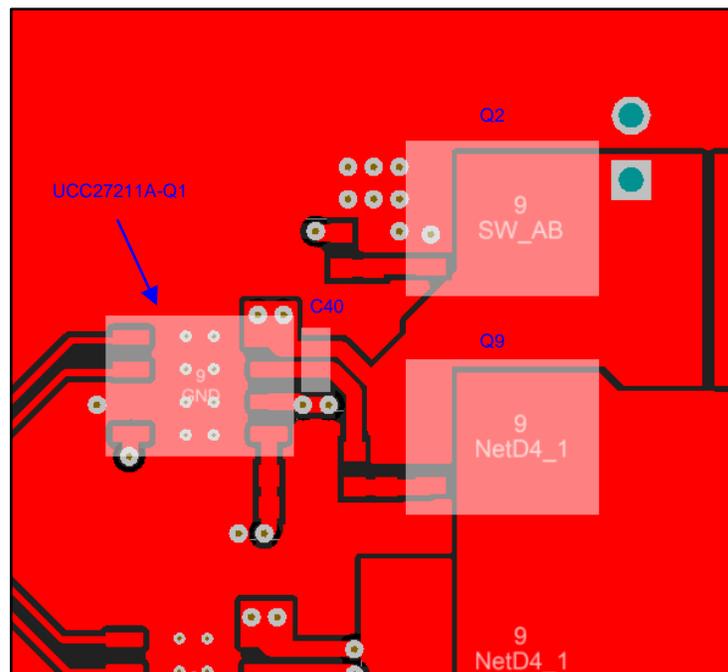


Figure 45. Placement of Gate Driver and MOSFETs at Converter Primary Side

Figure 46 shows the placement of the UCC28951-Q1 controller and components surrounding it for configuration. The components are placed as close as possible to the IC to avoid any noise coupling. See the *Layout Guidelines* section in the [UCC28951-Q1 data sheet](#) for more details [5].

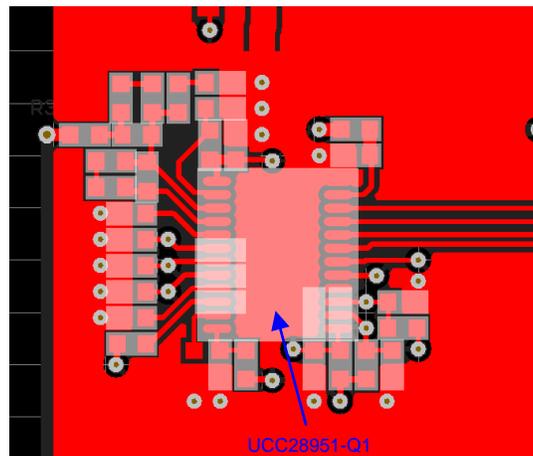


Figure 46. Placement of UCC28951 Controller and Components for Configuration

Figure 47 shows the placement of compensation network components. These components are placed on the same side of the controller and as close as possible to the controller.

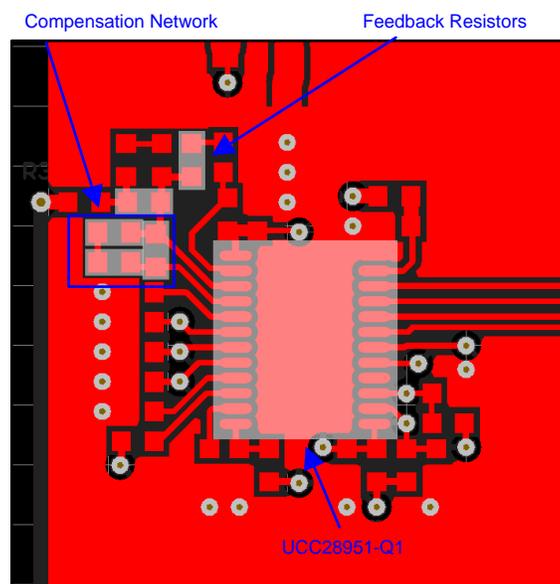


Figure 47. Placement of Compensation Network

5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01407](#).

5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01407](#).

5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01407](#).

6 Related Documentation

1. Texas Instruments, [Automotive Wide \$V_{IN}\$ Front-End Power Reference Design With Cold Crank Operation and Transient Protections](#), TIDA-01179 Reference Design (TIDUC53)
2. Texas Instruments, [A Design Review of a Full-Featured 350-W Offline Power Converter](#), PMP5568 Test Results (TIDU186)
3. Texas Instruments, [UCC28950 600-W Phase-Shifted, Full Bridge Application Report](#), Application Report (SLUA560)
4. Texas Instruments, [Modeling, Analysis and Compensation of the Current-Mode Converter](#), Application Note (SLUA101)
5. Texas Instruments, [UCC28951-Q1 Phase-Shifted Full-Bridge Controller for Wide Input-Voltage Range Applications](#), UCC28951-Q1 Data Sheet (SLUSCK4)

6.1 Trademarks

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7 Terminology

AFE— Analog front end

AEC— Automotive Electronics Council

ESR— Equivalent series resistance

EMI— Electromagnetic interference

EMC— Electromagnetic compatibility

DM— Differential mode

CM— Common mode

DCM— Discontinuous conduction mode

CCM— Continuous conduction mode

UVLO— Undervoltage lockout

MOSFET— Metal-oxide-semiconductor field-effect transistor

CISPR— International Special Committee on Radio Interference

PE— Protective earth

RMS— Root mean square

SR— Synchronous rectifier

BOM— Bill of material

OEM— Original equipment manufacturer

PCB— Printed-circuit board

HEV— Hybrid electric vehicle

EV— Electric vehicle

8 About the Author

XUN GONG is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the automotive segment in HEV/EV Power Train applications. Xun brings to this role expertise in the field of IGBT and SiC (Silicon Carbide) power transistors, EMI and EMC in motor drives, non-isolated and isolated DC-DC converters up to several hundred Watt. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, Netherlands. Xun Gong won the FirstPrize Paper Award of the IEEE Journal Transactions on Power Electronics in the year of 2014.

RYAN MANACK is the Power Design Services Manager for Automotive, Communications and Enterprise Compute markets. He is responsible for delivering over 350 custom power supply designs a year for global customers in these verticals. Ryan brings to this role expertise in the fields of point of load DC-DC, multiphase DC-DC and isolated DC-DC converters, including half-bridge, full-bridge, and phase-shifted full-bridge converters. He also has five years of experience as a Field Applications Engineer supporting major Consumer Electronic and Enterprise Compute accounts in Silicon Valley. Ryan has a Bachelor's of Science in Electrical Engineering degree from the University of Texas at Austin.

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