TI Designs: TIDA-01471
IEPE Vibration Sensor Interface Reference Design for PLC Analog Input

Description

Industrial vibration sensing is a crucial process in condition monitoring, which is necessary for predictive maintenance. An integrated electronic piezoelectric (IEPE) sensor is the most common vibration sensor used in the industrial environment. The TIDA-01471 design is a full analog front end for the IEPE sensor interface and demonstrates how to achieve flexible high-resolution, high-speed conversion with low-power and small-footprint implementation.

Resources

TIDA-01471	Design Folder
ADS127L01	Product Folder
THS4551	Product Folder
XTR111	Product Folder
LMV751	Product Folder
LP2901	Product Folder
DAC5311	Product Folder
TS3A5017	Product Folder
REF6025	Product Folder
SN74HC595	Product Folder

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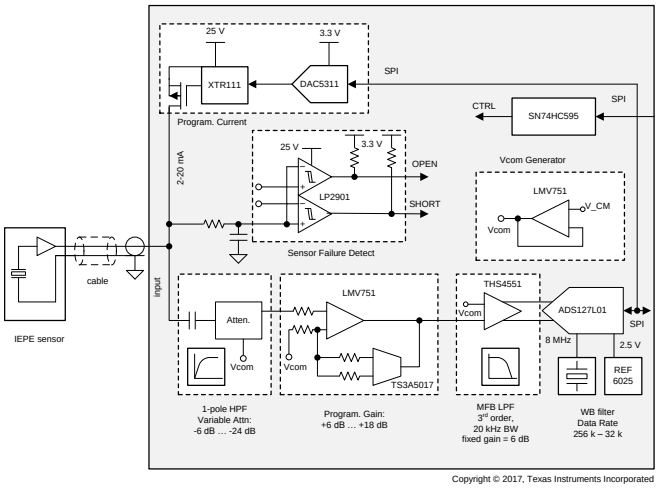
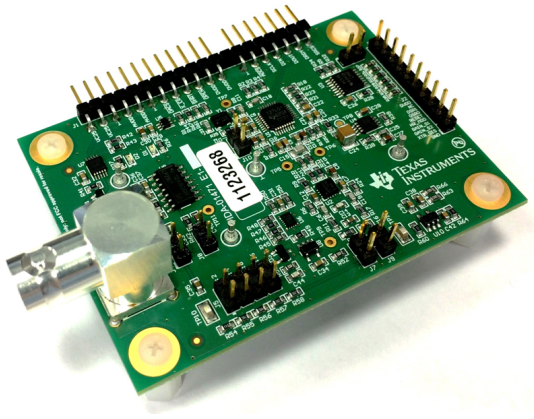
Features

- Single-Channel IEPE Sensor Analog Input
- 24-Bit Conversion Resolution
- 20-kHz Signal Bandwidth
- Programmable Data Rate: 265 kSPS to 32 kSPS
- Adjustable Gain: –12 dB to 18 dB
- Programmable Excitation Current: 2 mA to 20 mA
- ±10-V AC Input, 250-kΩ Input Impedance
- –40°C to 85°C Operating Temperature Range
- Diagnostics: Wire-Break, Short-Circuit Detection, and Short-Circuit Protection

Applications

- PLC, DCS Analog, and Mixed Input Module
- Analog Signal Conditioner/Transmitter
- Vibration Switch
- Data Acquisition and Measurement Systems





1 System Description

IEPE vibration sensor interface circuits are high-resolution, high-speed-specialized sensor interface circuits used in a range of industrial control products, including high-end measurement and data acquisition (DAQ) systems, vibration switches, conditioners, and transmitters, as well as dedicated analog input modules for programmable logic controllers (PLCs). The IEPE vibration sensor interface is an essential part of the condition monitoring platforms offered by top PLC and distributed control systems (DCSs) manufacturers. The range of existing IEPE sensor interface products extend from single channel to 12 or more channels for high-end systems. The bandwidth ranges from 1 kHZ up to 100 kHz with 20 kHz as the most common bandwidth setting. The sampling frequency ranges from 25 kSPS up to 100 kSPS, with a resolution of 16 bits to 24 bits.

1.1 Key System Specifications

This design is intended for use with a high-end single-channel IEPE sensor interface. A 24-bit conversion at maximum sampling speeds reaching up to 256 KSPS establishes this design at the leading edge of the existing product range. The design targets an input bandwidth of 20 kHZ and a programmable gain between –12 dB to 18 dB. A programmable excitation current of 2 mA to 20 mA as well as a programmable sampling speed down to 32 kSPS means that this design can accommodate different sensor cable distances and different back-end DAQ capabilities. Wire-break and short-circuit detection ensure safe and reliable operation of the sensor interface. Factors such as power consumption and design footprint have been considered to allow an affordable system that can be adjusted for a larger number of channels with a low-cost powering solution.

Table 1 lists the key system specifications.

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	1
Input range	±10 V
Resolution	24 bits
Accuracy	±0.5% FS
Bandwidth	0.6 Hz to 20 kHz
Sampling rate	256 kSPS, 128 KSPS, 64 kSPS, and 32 kSPS
SNR	100 dB
Gain	Programmable: –12 dB to 18 dB
Input impedance	250 kΩ
Excitation current	0 mA to 20 mA (8 bits of resolution)
Excitation voltage	23 V (minimum)
Operation temperature	–40°C to 85°C
Diagnostic features	Wire-break and short circuit
Form factor	55 mm × 75 mm

2 System Overview

Machine failure is very costly in a production environment. One way of mitigating the downtime of machines is to rely on scheduled preventive maintenance. However, regularly-scheduled maintenance can not completely prevent random failures. At the time of this writing, the industry actively transitioning toward predictive maintenance, which is the process of predicting a machine failure before it happens. This kind of maintenance is typically done through condition monitoring. Condition monitoring refers to the act of continuously monitoring machine temperature, vibration, and power consumption during normal operation. Several theoretical and empirical models can be applied to link these condition parameters to the health status of a machine, thus effectively indicating whether a component is due for replacement. This process greatly optimizes maintenance cost and decreases machine downtime.

Misalignment, defect bearing, loose machine foot, defective gears, defect pumps, and defect motors are some of the faults that are readily detectable through vibration monitoring.

Figure 1 details the components included in the vibration monitoring system.

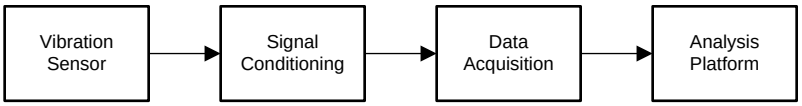


Figure 1. Vibration Monitoring System Components

1. Vibration sensor – Several sensor types are available for different applications. An integrated electronics piezoelectric (IEPE) sensor is the mainstream sensor used for industrial vibration monitoring.
2. Signal conditioning – A vibration sensor requires power and its output requires either attenuation or amplification, as well as level shifting. Low-pass filtering, high-pass filtering, and conditioning the signal to match the subsequent ADC input is also a requirement. All of these functions are implemented by the signal conditioning block.
3. Data acquisition – This component is typically a high-speed, high-resolution data converter with an integrated digital filter.
4. Analysis platform – The high-speed data generated by the DAQ block must be analyzed or converted to the frequency domain, where the vibration profile is compared to a standard healthy machine profile and failure modes are detected.

This design shows the implementation of the signal conditioning and the DAQ parts for an IEPE vibration sensor.

2.1 Block Diagram

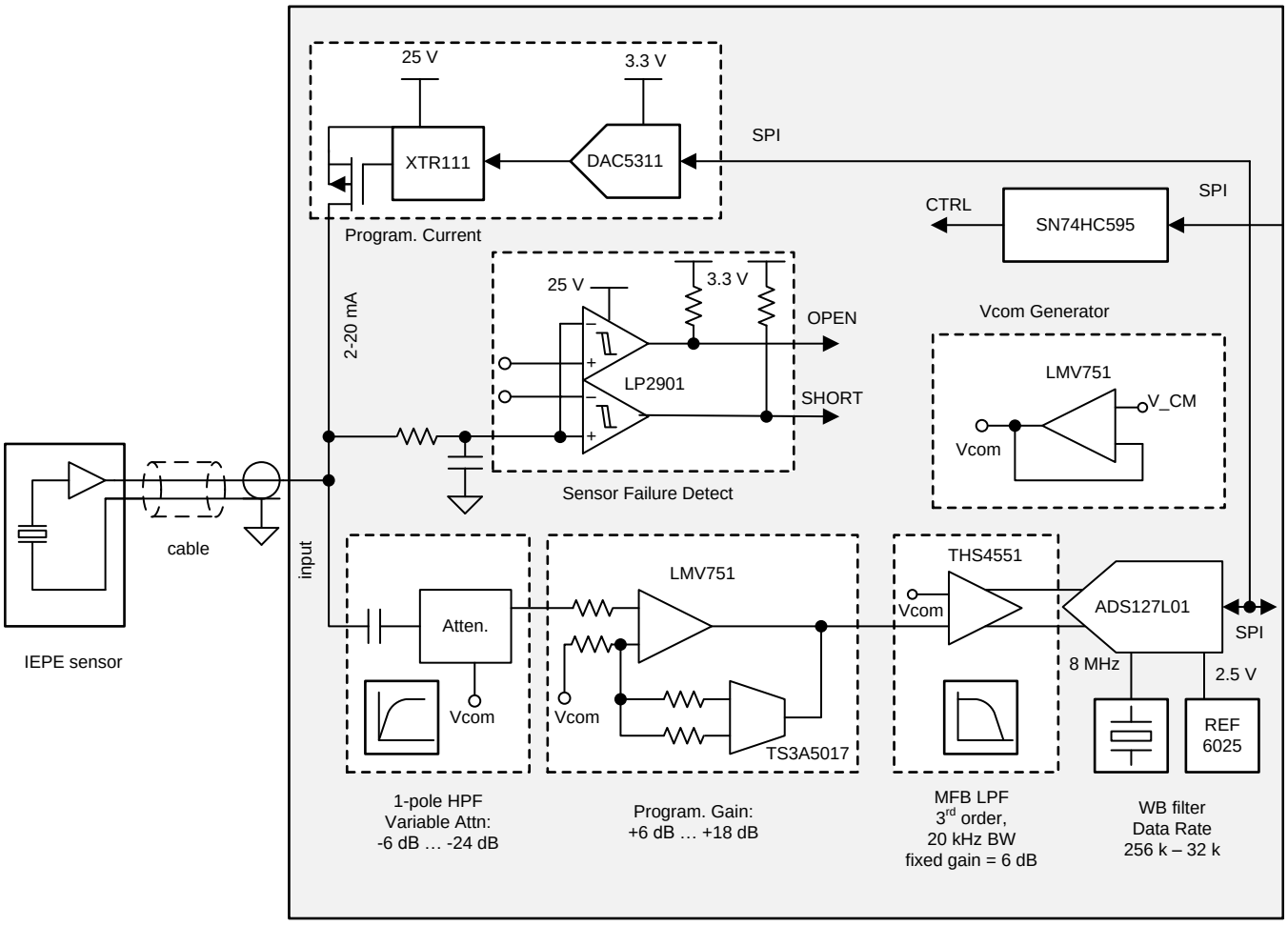


Figure 2. TIDA-01471 Block Diagram

The IEPE sensor interface of the TIDA-01471 block diagram shows three main sections of the design: the current source, the fault detection circuit, and the signal chain, which is the main section. A signal chain is composed of a variable attenuator, a programmable gain stage, a differential low pass filter stage, and high-speed analog-to-digital converter (ADC).

The current source powers the sensor and draws its own power from a voltage supply higher than 24 V to accommodate for the large ±10-V input signal. The input signal is AC coupled, amplified, or attenuated using a variable gain amplifier and then low-pass filtered before going to the ADC. A sampling frequency above 50 kHz is required for a typical bandwidth equal to 20 kHz. This design aims for 100 kSPS or more at 24 bits of resolution. An auxiliary circuit for detecting open- or short-circuit conditions is connected to the input before the coupling cap.

Section 2.2 details the component selection and Section 2.3.3 provides the detailed design procedure of the different blocks.

2.2 Highlighted Products

2.2.1 ADS127L01

The ADS127L01 is a 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with data rates up to 512 kSPS (see Figure 3). This device offers a unique combination of excellent DC accuracy and outstanding AC performance. The high-order, chopper-stabilized modulator achieves very-low drift with low in-band noise. The integrated decimation filter suppresses modulator out-of-band noise. In addition to al low-latency filter, the ADS127L01 provides multiple wideband filters with less than ±0.00004 dB of ripple and an option for –116-dB stop-band attenuation at the Nyquist rate.

Traditionally, industrial ΔΣ ADCs that offer good drift performance use digital filters with large passband droop. As a result, industrial ΔΣ ADCs have limited signal bandwidth and are mostly suited for DC measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than industrial counterparts. The ADS127L01 combines these converters, providing high-precision industrial measurement with excellent DC and AC specifications over an extended industrial temperature range of –40°C to +125°C.

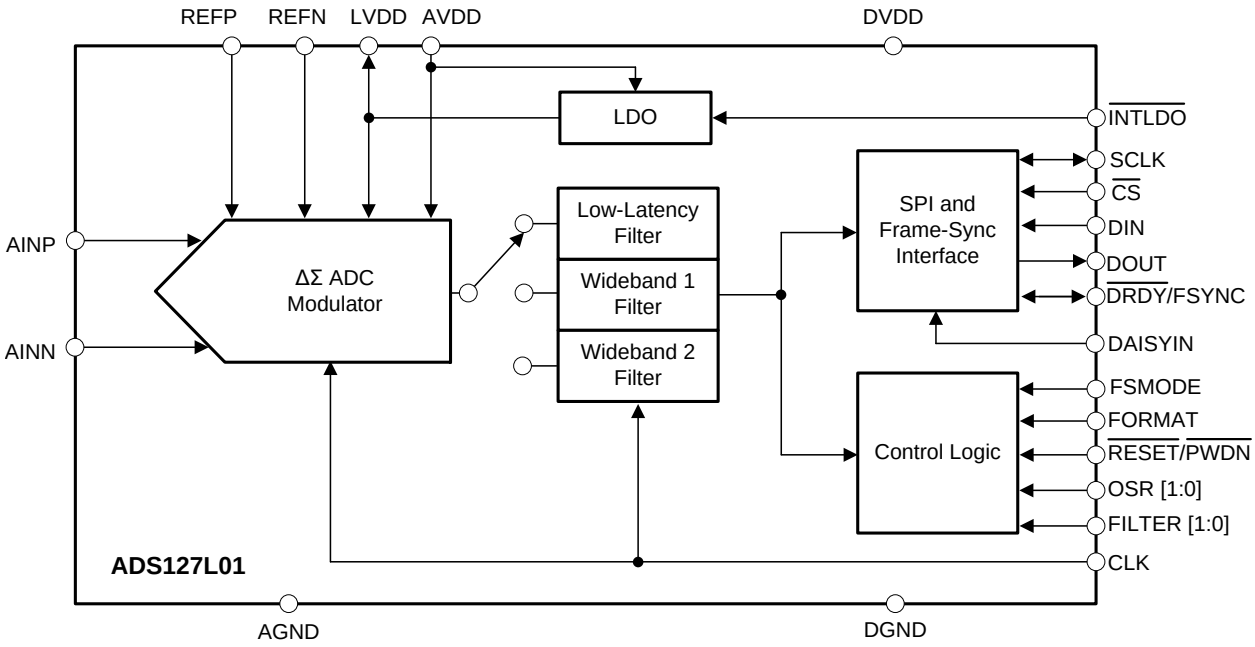


Figure 3. ADS127L01 Block Diagram

2.2.2 REF6025

The REF60xx family of voltage references have an integrated, low-output impedance buffer that enable the user to directly drive the REF pin of precision data converters while preserving linearity, distortion, and noise performance (see Figure 4). Most precision SAR and ΔΣ ADCs switch binary-weighted capacitors onto the REF pin during the conversion process. The REF6000 family devices are well suited to drive the REF pin of the ADS127xx family of ΔΣ ADCs. The REF60xx family variant specifies a maximum temperature drift of just 5 ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low output impedance buffer combined.

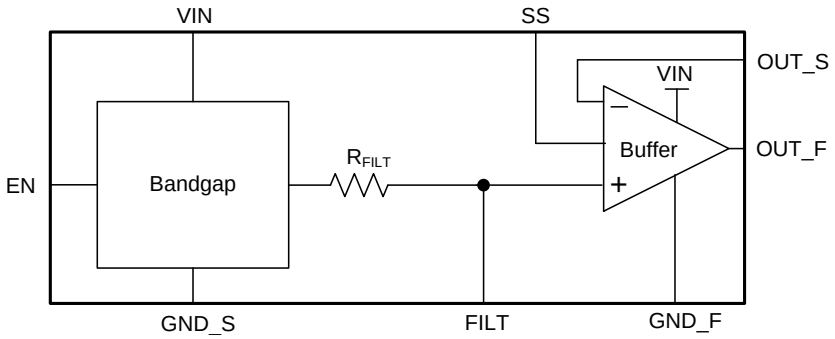


Figure 4. REF6025 Block Diagram

2.2.3 TS3A5017

The TS3A5017 is a dual single-pole, quadruple-throw (4:1) analog switch that is designed to operate from 2.3 V to 3.6 V. This device can handle both digital and analog signals and signals up to supply voltage can be transmitted in either direction. TS3A5017 switch features low on-resistance, low charge injection, and low total harmonic distortion (THD).

2.2.4 LP2901

The LP2901 is low-power quadruple differential comparator. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw 60-µA drain current over a wide range of voltages. Operation from split power supplies is also possible and the ultra-low-power supply drain current is independent of the power supply voltage.

The LP2901 is specifically designed to interface with the CMOS logic family. The ultra-low power supply current makes these products desirable in low-power applications. The LP2901 is characterized for operation from –40°C to 85°C.

2.2.5 XTR111

The XTR111 is a precision voltage-to-current converter for the standard 4-mA to 20-mA current loops. The device is designed to drive an external P-MOSFET to ensure high output resistance and broad compliance voltage range with only 2 V of headroom below the supply voltage, while still keeping MOSFET heat dissipation away from the converter chip that helps to achieve target high precision. The device in Figure 5 shows consists mainly of a high impedance input buffer and a current mirror with an external reference resistor that drives the external P-MOSFET gate through an output buffer. An auxiliary adjustable regulator is available for additional circuitry, along with an output disable pin (enabled by default) and an output failure status pin. The device can work with a supply in the range of 8 V to 40 V. An input voltage up to 12 V is possible.

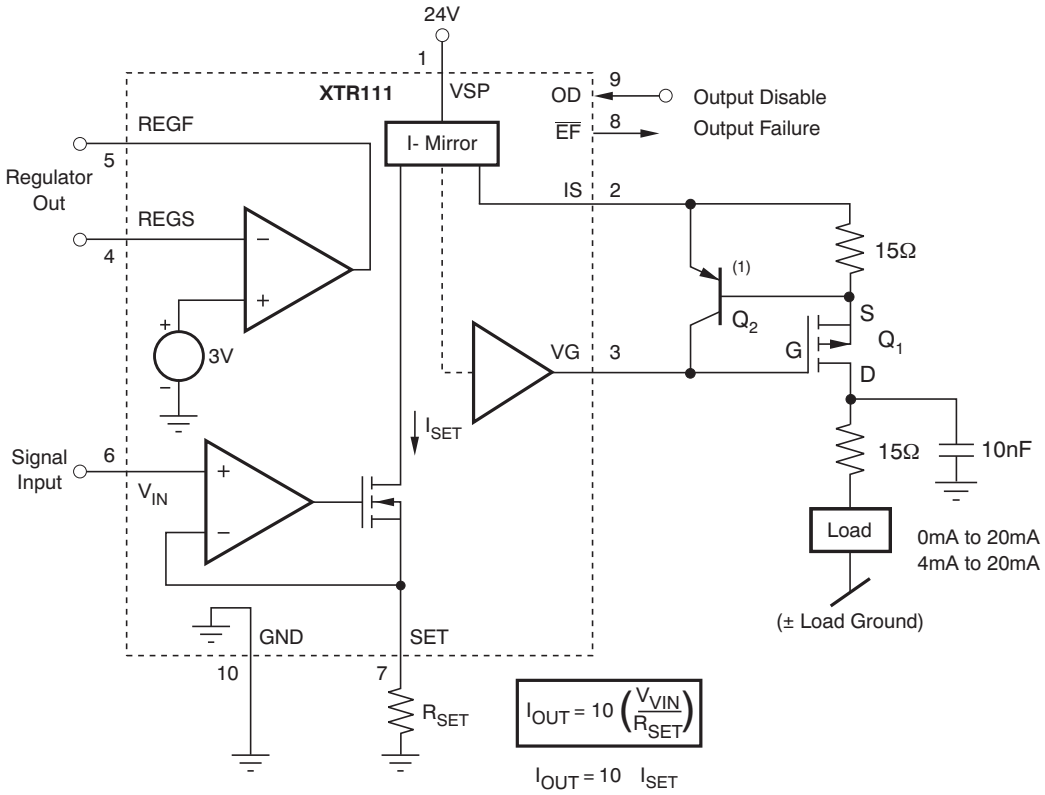


Figure 5. XTR111 Block Diagram

2.2.6 DAC5311

The block diagram in Figure 6 shows the DAC5311 (8-bit), which is a low-power, single-channel, voltage output digital-to-analog converter (DAC). The low power consumption of this device in normal operation (0.55 mW at 5 V, reducing to 2.5 µW in power-down mode) makes it ideally suited for low-power applications.

This device is monotonic by design, provides excellent linearity, and minimizes undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. DAC5311 uses a versatile, three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with the standard serial peripheral interface (SPI), quad serial peripheral interface (QSPI), Microwire, and digital signal processor (DSP) interface.

The device uses an external power supply as a reference voltage to set the output range. The devices incorporate a power-on reset (POR) circuit that ensures the DAC output powers up at 0 V and remains there until a valid write to the device occurs.

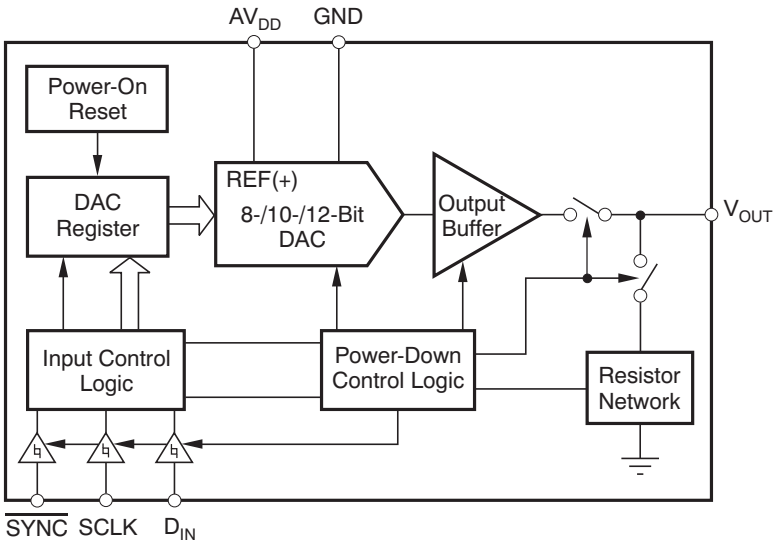


Figure 6. DAC5311 Block Diagram

2.2.7 LMV751

The LMV751 is a high-performance CMOS operational amplifier intended for applications requiring low noise and low input offset voltage. This amplifier offers modest bandwidth of 4.5 MHz for a very-low supply current and is unity gain stable.

The output stage is able to drive high capacitance (up to 1000 pF) and source or sink 8 mA of output current. The device is supplied in the space-saving SOT-23-5 tiny package.

The LMV751 is designed to meet the demands of small-size, low-power, and high-performance requirements.

2.2.8 THS4551

The THS4551 fully differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive-load driving, this device is well suited for DAQs where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination. The THS4551 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very-low DC error and drift terms support the 24-bit $\Delta\Sigma$ ADCs input requirements. A wide-range output common-mode control supports the ADC running from 1.8-V to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V. The THS4551 is commonly used in high-precision ADC driver circuits.

2.3 System Design Theory

2.3.1 IEPE Sensor

The integrated electronic piezoelectric (IEPE) sensor is a piezoelectric vibration transducer with integrated charge amplifier and impedance converter (see Figure 7). integrating the amplifier close to the sensor greatly reduces the sensor noise. One major advantage of the IEPE sensor is that it is interchangeable.

The IEPE sensor is also commercially known as an Integrated Circuit Piezoelectric (ICP®), Constant Current Line Drive (CCLD), Isotron®, DeltaTron®, and Piezotron®.

Uniaxial, biaxial, and triaxial IEPE accelerometers are available in the market typically with a two-wire connector per axis. Sensors with an output proportional to acceleration is more common (accelerometer), although a velocity-proportional output is also available.

Constant current is applied to the two-wire connection from which the IEPE sensor is drawing power and establishing a constant DC offset around 10 V. A vibration-sensing value is superimposed of this DC signal at the output of the sensor, which is typically AC-coupled to the sensor interface circuit.

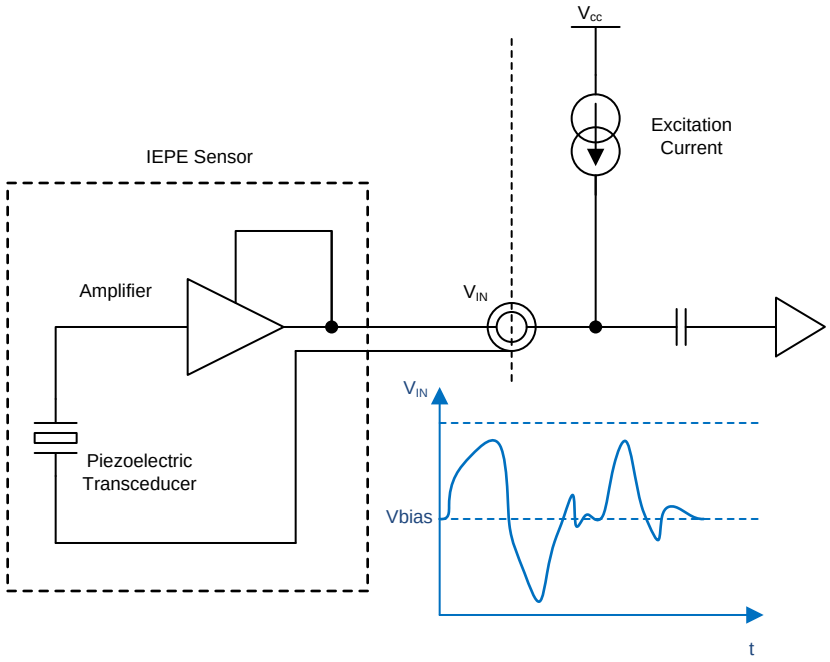


Figure 7. IEPE Sensor Conceptual Circuit

2.3.2 IEPE Accelerometer Parameters

IEPE accelerometer sensors are available with a wide range of performance parameters for different applications. Understanding those parameters and their relation to the sensor interface circuit performance is important. The following subsections describe these parameters and addresses their relevance.

2.3.2.1 Sensitivity and Measurement Range

Sensitivity is the output voltage change corresponding to a specific mechanical acceleration input. This parameter is commonly measured in *mV/g*, where g is the gravity of earth. Accelerometer data sheets typically report a single nominal sensitivity value. However, note that sensitivity changes with temperature, input frequency, and input acceleration level, which is why sensitivity tolerance is also stated in to ensure a bounded variation of sensitivity over the aforementioned variables.

IEPE accelerometer sensitivity falls in the range of tens of mV/g to a few thousands of mV/g, with a tolerance of 5% or 10%.

The measurement range is the minimum and maximum of acceleration inputs that can be converted by the sensor to a voltage output without saturation or clipping, which is what determines the maximum output voltage (see Equation 1).

$$\text{Output Voltage Range} = \text{Measurement Range} \times \text{Sensitivity} \quad (1)$$

For a measurement range of 10 g and sensitivity of 100 mV/g, the output range is ±5 V. The sensor output voltage range is typically 5 V or 10 V, maximum.

2.3.2.2 Excitation, Output Bias Voltage, and Output Impedance

As previously mentioned, the output voltage of the IEPE sensor can be as large as ±10 V. To avoid the requirement of a dual supply, the AC output of the IEPE sensor is shifted with a certain constant voltage called *output bias voltage*, which is typically in the range of 9 V to 12 V. Having the AC signal superimposed on the DC output bias voltage dictates a minimum compliance voltage from the current source supplying the sensor not to have signal clipping. This compliance voltage is also called *excitation voltage*. Excitation voltage is simply the maximum possible output bias voltage added to the maximum AC voltage output.

$$\text{Excitation Voltage}_{MIN} = \text{Bias Voltage}_{MAX} + \text{Sensitivity}_{MAX} \times \text{Input}_{MAX} \quad (2)$$

A value of 18 V to 22 V is typical for excitation voltage. An upper maximum also exists for the excitation voltage that must not be exceeded to avoid damaging the sensor electronics.

Output impedance is the effective AC output impedance seen by the interface circuit. Typical values are 300 Ω down to below 100 Ω. A lower impedance means less error in measurement when considering the finite input impedance of the interface circuit.

2.3.2.3 Linearity and Temperature Variance

As previously mentioned, sensitivity varies with input level and temperature.

Variation with input level is measured by the linearity (or non-linearity) of the sensor. Temperature variation is also measured by using the sensitivity deviation from the nominal sensitivity over the operating temperature range. The operating temperature range extends from 120°C to 280°C.

Both linearity and temperature variance are expressed as a percentage of the full-scale input range. A 10-g range sensor with a nominal sensitivity of 100 mV/g and 1% linearity has a maximum error of 0.1 g for the voltage reading.

2.3.2.4 Frequency Response

The sensitivity of the sensor changes with the frequency of the acceleration excitation. The sensitivity is generally considered as being constant over a certain frequency range as defined by the minimum and maximum 3-dB frequencies. Beyond the maximum frequency, the sensor has a mechanical resonance frequency that should be avoided in application. The usual frequency range is sub-Hz to 10 kHz, 20 kHz, or 30 kHz. The sensor interface circuit must have the same bandwidth of the targeted sensor and the ADC converter sampling frequency must be more than twice this bandwidth.

Note that the designer can extend the frequency range for some sensors by increasing the excitation current. For this reason, a variable current source is required for a versatile IEPE sensor interface circuit.

2.3.2.5 Noise and Dynamic Range

The IEPE sensor has intrinsic mechanical and electrical noise, which must be considered if detecting low-level signals. Output noise is represented as root-mean square (RMS) noise voltage.

This ratio of the maximum output range to the noise level constitutes the effective dynamic range of the sensor.

2.3.3 IEPE Sensor Interface Design Procedure

2.3.3.1 ADC Circuit

The ADC configuration is as follows:

- SPI mode communication
- Wideband filter 2, which has a passband at a 0.4 data rate to allow more noise suppression
- High resolution (HR) mode to obtain the highest SNR possible
- Internal LDO is enabled to avoid the requirement for an external 1.8-V supply
- 2.5-V voltage reference
- 8-MHz clock with OSR = 46 by default, resulting in a 125-kSPS data rate; measurement is done with OSR = 128 and 62.5 kSPS

The ADS127L01 is used in SPI mode; the *SCLK* and *DIN* pins are connected directly to the shared SPI bus. The *START* pin is pulled low to rely on the start command. The wideband filter 2 is used by setting *FILTER[1,0]* to "01". An internal low-dropout regulator (LDO) is enabled by pulling *INTLDO* low.

The oversampling ratio (OSR) is set by the *OSR[1,0]* pins; LP mode can be entered by pulling *HR_mode* low. The default values of *OSR[1,0]* = "01", that is, OSR =64 and *HR_mode* = "1" if not overwritten by the shift register.

REF6025 is used as voltage reference for the ADC, which means the full scale (FS) of the ADC is 2.5 V. REF6025 is powered by a 3.3-V supply. The ADC is powered by digital and analog supplies.

The ADC is clocked by an 8-MHz crystal, which results in a 62.5-kSPS output data rate given the default OSR value of 128 (see Equation 3).

$$\text{OUT Data Rate} = \frac{\text{Sampling Clock}}{\text{OSR}} \tag{3}$$

Note that SPI speed is also dependent on the output format set by the length of output word, which is set by *CS_ENB* (register 01h, bit 1). If *CS_ENB* = "1", the status word is disabled and the output is 24 bits of data. If *CS_ENB* = "0", the status word is enabled and the output word is 32 bits of data and status. In the process of disabling the status word, the minimum SPI clock is given by Equation 4:

$$\text{SPI Clk}_{\text{MIN}} = 24 \times \text{OUT Data Rate} + \text{Overhead} \tag{4}$$

At a data rate of 64 kSPS, a SPI clock of approximately 2 MHz suffices. At the top output rate of 256 kSPS, a clock rate of at least 8 MHz is required. The overhead term accounts for the delays in detecting the *DRDY* signal and starts to read the data.

The effective differential input impedance of the ADC is 10 kΩ, while the effective voltage reference input is 3.4 kΩ, both at the 8-MHz clock input.

Note that the ADS127L01 device continuously samples the input, generates the *DRDY* signal, and delivers the output when the clock signal is available. No register reading is required. Figure 8 shows an example of SPI signaling for the ADS127L01. Note that the most significant bit (MSB) is delivered first with the SCLK rising-edge.

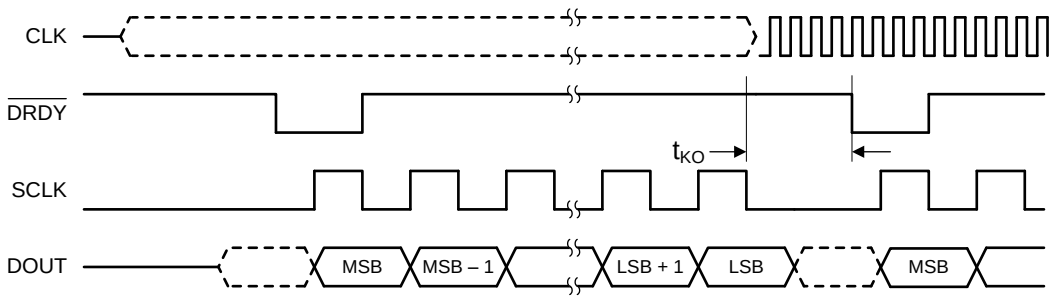


Figure 8. Example SPI Waveform for ADS127L01

2.3.3.2 Low-Pass Filter

The low-pass filter in front of the ADC offers several functions. This component filters the high-frequency noise from both the sensor and active electronics of the front end. Most importantly, the filter attenuates the images around the ADC clock of 8 MHz. It ensures low impedance drive for the ADC. The filter also delivers a balanced differential input to the ADC for achieving the best SNR by converting the single-ended input to differential signal and adjusting the output to the FS range of the ADC.

The single-ended (SE) input means that a minimum gain of 2 V/V is required by the filter to reach the FS of the ADC. A value of 20 kHz is the target 3-dB bandwidth for the sensor interface. A targeted image rejection of 110 dB at 8 MHz dictates a third-order filter. Multi-feedback topology has been chosen for this filter to use a single amplifier. A second-order multiple feedback (MFB) filter followed by a passive RC filter is used to synthesize the third-order filter.

The TI FilterPro™software is used to design the differential MFB filter with a 24-kHz bandwidth to accommodate for the additional third pole. Minor adjustments to the results are made such as adding a series resistor to the output to improve stability.

Figure 9 shows the result of FilterPro design wizard.

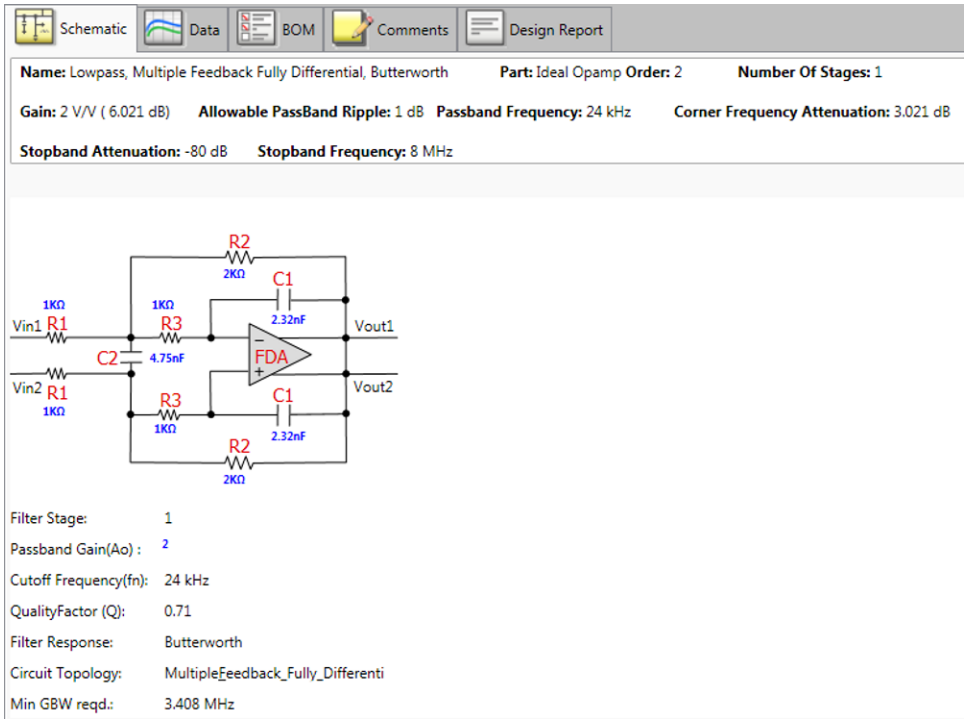


Figure 9. Filter Design Using TI FilterPro™ Tool

The maximum output swing must be limited to ±2.5 V, hence the input amplitude is limited to 2.5 V over the 1.65-V DC common-mode level. The second input of the filter circuit is connected to the common mode as well to convert the DC-shifted SE signal into a differential signal.

E192 0.1% (or E96 1% resistors) and C0G/NP0 E24 5% capacitors are used for the filter passives.

A circuit simulation using the TINA-TI™ software shows an accurate 20.4-kHz to 20.7-kHz bandwidth with Monte-Carlo analysis and a minimum of –110-dB image rejection at 8 MHz. The output impedance of 20 Ω to 30 Ω, input impedance of approximately 1.3 kΩ, and a minimum –100 dB of supply rejection are validated by simulation.

2.3.3.3 Gain Stage

A gain stage is required to allow programmable gain. A non-inverting operational-amplifier (op amp) gain stage is selected to have constant input impedance as well as to allow an easy DC shift. The gain stage must have high input impedance so as not to affect the attenuator impedance. A programmable gain (2, 4, 6, and 8 V/V) is made possible through a low impedance switch. The dual 4:1 switch is used in parallel to give 7-Ω to 10-Ω maximum resistance per branch. This property has the side effect of increasing the parasitic capacitance and the common pole is connected to the op-amp output to decrease the parasitic capacitance effect. Gain selection is done through the *GAIN_SEL[2:1]* bits going to the 4:1 switch. A high impedance of 1.1 MΩ is added in parallel to the switch to avoid the case of an open switch.

The input to the gain stage is a zero-centered AC signal, which originates from the resistive attenuator and may exceed the supply limits in the case of a wrong attenuator setting or input overvoltage. Schottky diodes are placed at the input to the supply rails to protect the gain stage. Choose optimal resistor values to reduce the power consumption in addition to reducing noise contribution from the gain stage. This design uses E96 1% resistors.

The maximum output swing must be limited to 2.5 V over the 1.65-V DC common-mode level, hence the input amplitude is limited to 1/gain. In the case of gain = 2, the input peak-to-peak voltage must be limited to 1.25 V, or 1.65 ± 0.625 V.

A TINA-TI circuit simulation shows accurate gain with only ±0.1-dB error over all gain settings. The input impedance is quite high (above 50 MΩ at 1 kHz) and above 3 MΩ within the 20 kHz. The power-supply rejection ratio (PSRR) = –6 dB up to 500 kHz due to the single-ended structure. A good-quality supply must be provided to the gain stage. The output impedance is below 3 Ω in the 20-kHz bandwidth and reaches 400 Ω at 2 MHz—this translates to a lower gain for high frequencies, which is desirable anyway. The output swing is between 70 mV and 3.1 V. Protection diodes clip the inputs at 3.52 V and –0.22 V, which is the safe operating range of the LMV751 device, as Figure 10 shows.

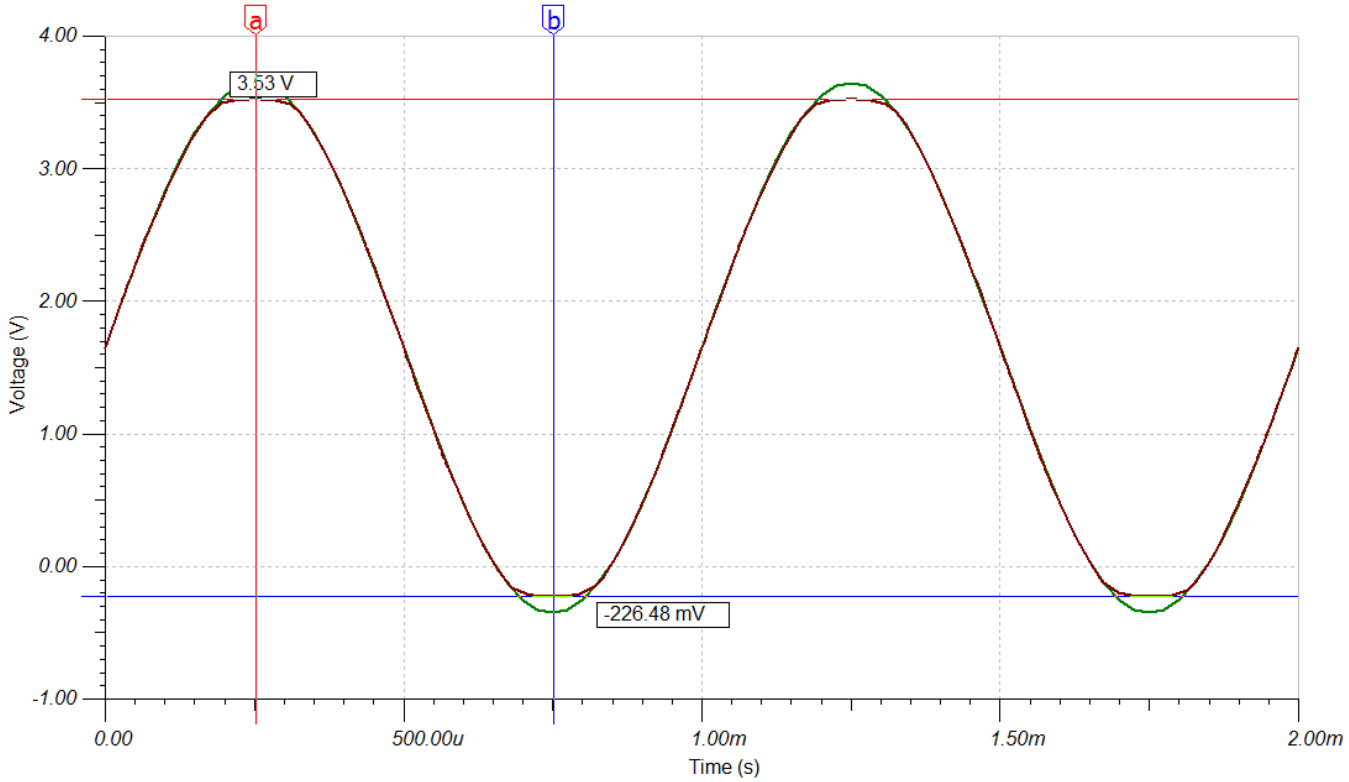


Figure 10. Overvoltage Clipping by Input Protection Diodes

2.3.3.4 High Pass filter

The IEPE sensor signal is AC-coupled to the interface circuit. A high-pass filter (HPF) is formed from the coupling capacitor and a series resistor. At high frequencies, the capacitor impedance is negligible and the series resistor represents the input impedance of the interface circuit. The HPF cutoff frequency (sub 1 Hz) dictates the RC constant. In general, a high input impedance is desirable to reduce the measurement error. A higher resistance, though, results in higher noise at the input. A value of 250 kΩ is chosen as a compromise. Most IEPE sensors with less than 200-Ω output impedance have less than 0.1% error and can be easily compensated.

The sensor signal can be as large as ±10 V and output of the filter should be limited to ± 0.625 V. Attenuation is simple to achieve through the use of a resistive potential divider. Multiple taps across the 250 kΩ allows for different attenuation ratios: 1/2, 1/4, 1/8, and 1/16. Use the 1/16 setting for a 10-V sensor signal. Use the 1/8 setting for the 5-V sensor signal. Note that, in the case of overvoltage, the gain stage is protected through the diodes with a 2-kΩ series resistor. In the worst-case scenario, where 5 V is applied directly (1/2 setting with 10-V input) to the gain stage, the diode current is limited to 2.5 mA, which is within the acceptable current limits of the op-amp clamping circuit. The output of the attenuator is attached to a small parallel capacitor. This capacitor helps to remove the high-frequency noise in an unwanted band.

The AC signal after the coupling capacitor is centered around 0 V. This signal must be shifted by the common-mode voltage before reaching the single-supply LMV751 amplifier. This shifting is easily accomplished by attaching the second terminal of the HPF series resistor to the common-mode voltage instead of ground.

The HPF also determines the settling time in the case of an abrupt, large-signal input like start-up, during which time the output should be discarded. The lower the cutoff frequency, the larger the settling time.

The TINA-TI circuit simulation shows an accurate 3-dB cutoff frequency of 0.6 Hz to 0.7 Hz with component tolerance. A gain error over the bandwidth and over different attenuation settings is below 0.1 dB for lower attenuation and reaches 0.5 dB for higher attenuation settings (1/16). The input impedance is stable at 250 kΩ over the whole bandwidth. In a lower attenuation (1/2) case, the impedance starts to drop around 200 kHz and reaches half of its rated value around 8 MHz. The settling time is less than 2 seconds.

2.3.3.5 Current Source

A constant current source is required for driving the IEPE sensor. A minimum of 2 mA to 4 mA is required; however, a higher current is required for longer cables and higher cable capacitance. A current range of 2 mA to 20 mA covers all application cases. The current source should work from a supply higher than 24 V. The XTR111 with an external MOSFET is used to generate a constant current between 2 mA and 20 mA. The XTR111 device provides protection against short circuit as well as disable functions. A small capacitor (100 pF) is placed at the transistor drain to reduce noise. This capacitor must be kept low because it provides the AC low-impedance path at higher frequencies, which affect the overall interface input impedance.

According to Equation 5, the XTR111 device converts input voltage to current for a V_{IN} between 0 V and 3 V and R_{SET} = 1.47 k (0.1%).

$$I_{OUT} = 10\frac{V_{VIN}}{R_{SET}} \tag{5}$$

A value of 2 mA requires an input voltage of 0.3 V, 4 mA requires 0.6 V, and 3 V results in a 20-mA output current.

The low-cost 8-bit DAC5311 is used to generate the input voltage to the XTR111 device. The DAC5311 device is powered by a 3.3-V supply, which also acts as a reference, and is programmed through a SPI bus, which is shared with the ADC. The DAC conversion follows Equation 6:

The codes corresponding to 2-mA, 4-mA, and 20-mA outputs are 0x17, 0x2E, and 0xE8, respectively.

$$V_{OUT} = AV_{DD} \times \frac{Code}{2^8} \tag{6}$$

10 kΩ is placed between the DAC5311 output and the XTR111 input to protect it from excessive current in case the DAC is powered while the XTR is not. The configuration data word for the DAC5311 is 16 bits, with the SYNC input acting as chip select (CS). Figure 11 shows an example of the SPI configuration waveform for a 1-MHz SPI.

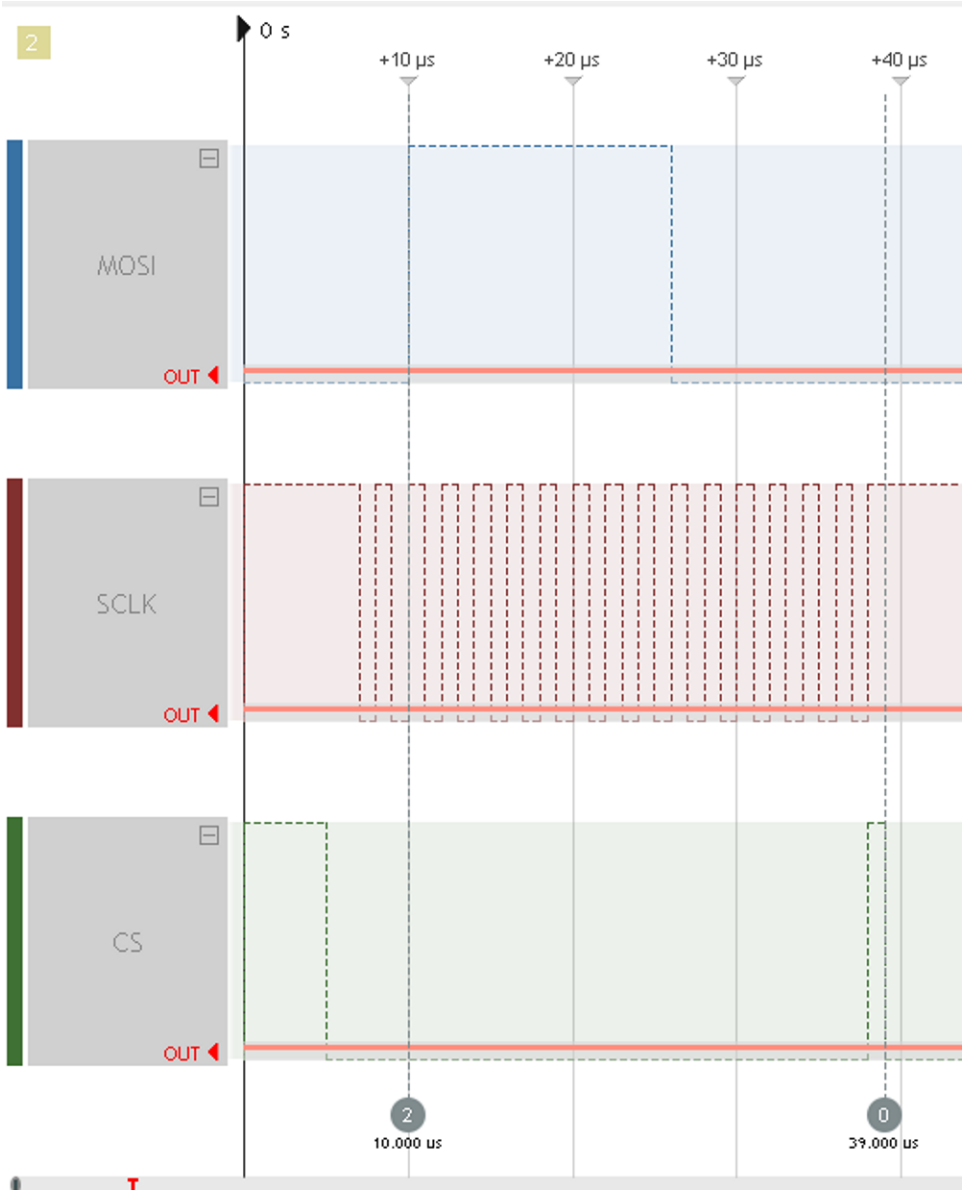


Figure 11. Example SPI Waveform for DAC5311 Programming

2.3.3.6 Common-Mode Supply

HPF, gain stage, and differential low-pass filter (LPF) all require common-mode voltage. The exact common-mode voltage is not critical as long as it is not 100 seconds of mV away from mid-supply. A simple resistive supply divider is used to generate mid-supply, followed by a unity-gain buffer. A simple RC filter is placed in between the simple resistive supply divider and unity-gain buffer to reduce resistor noise.

The TINA-TI circuit simulation shows less than 20-mV variation of VCOM with component variation and less than 2-uV RMS noise over the useful bandwidth of 20 kHz. The output impedance is less than 2 Ω over the band of interest. A current sink or source up to 10 mA results in less than 0.25 mV of VCOM voltage change.

2.3.3.7 Fault Detection Circuit

To detect an open circuit and short circuit while supporting the large signal of ±10 V, a DC signal must be extracted from the input signal. This extraction can be performed with a low-cutoff LPF; however, this LPF must maintain the high input impedance of the input stage, which mandates the use of a high-value resistor. A value of 5 MΩ is selected, which ensures the effect on the impedance is negligible. The LPF cutoff frequency must not be too low because a low-cutoff frequency results in a very slow response, that is, a long delay in detecting the fault condition. A cutoff of 1.4 Hz is chosen as a trade-off.

Given that low frequency inputs like 1.4 Hz are still permissible signal inputs, the designer must accommodate for extra AC signals in the threshold selection. Another important point is the effect of the input bias current of the comparators: The sum of the input bias current is equivalent to a series 10-MΩ resistor. This fact means that a ratio of 2:3 exists between the filtered DC value and the actual input DC.

The threshold levels of 1.8 V (short circuit) and 11.1 V (open circuit) work sufficiently in normal operation even with the full-scale inputs at low frequency. Threshold levels are generated using a resistor ladder with noise-filtering capacitors. The two comparators of the LP290 quad comparator device are used for open- and short-circuit detection. LP290 comparators are powered by the same high-voltage supply just like the XTR111 and feature open-collector output; therefore, the comparator outputs are pulled high to the 3.3-V digital supply and the error signal is indicated by the logic-low state.

The TINA-TI circuit simulation shows less than 200 mV of variation in the threshold voltages: 11.1 V for open detection and 1.8 V for short detection. The delay cannot be accurately simulated because the input bias current is not accurately modeled. If detection delays are unacceptable for a certain application, the bandwidth of the LPF can be increased. Be careful not to interpret the AC signal as a fault. If a very-short detection time is required, digital methods can be used with a wider-band LPF to filter the oscillating fault signal as non-fault.

2.3.3.8 Shift Register

Multiple control signals are required for different components: *GAIN_SEL[2:1]* for the gain-stage MUX control inputs, *XTR_DIS* for disabling the XTR111, *OSR[1:0]* for setting the OSR ratio of the ADC, and *HR_mode* and *RESET* for the ADC, as well. A serial-to-parallel shift register is used to reduce the overall number of required general-purpose input/output (GPIOs) pins or isolation channels. This serial-to-parallel shift register is driven by the same SPI bus shared with the ADC and DAC. The CS signal for the shift register is active-high while the CS for both ADC and DAC are active-low.

The board allows the user to disable the shift register. In the case of this design, the default settings for the control signals are set through 100-kΩ pullup and pulldown resistors.

One important thing to note is that, when driving the SN74HC595 device with a SPI bus, DIN is connected to the SER pin, SCLK to SRCLK, and CS to RCLK. The SRCLK pin is sensitive to the clock rising-edge in contrast to DAC5311 and ADS127L01, which are both clock falling-edge sensitive. Moreover, while an early rising-edge of CS would invalidate the data write in both the DAC and the ADS, in the case of the SN shift register, a rising-edge of RCLK would load the input data incorrectly. Figure 12 shows an example of the SPI write for the SN74HC595.

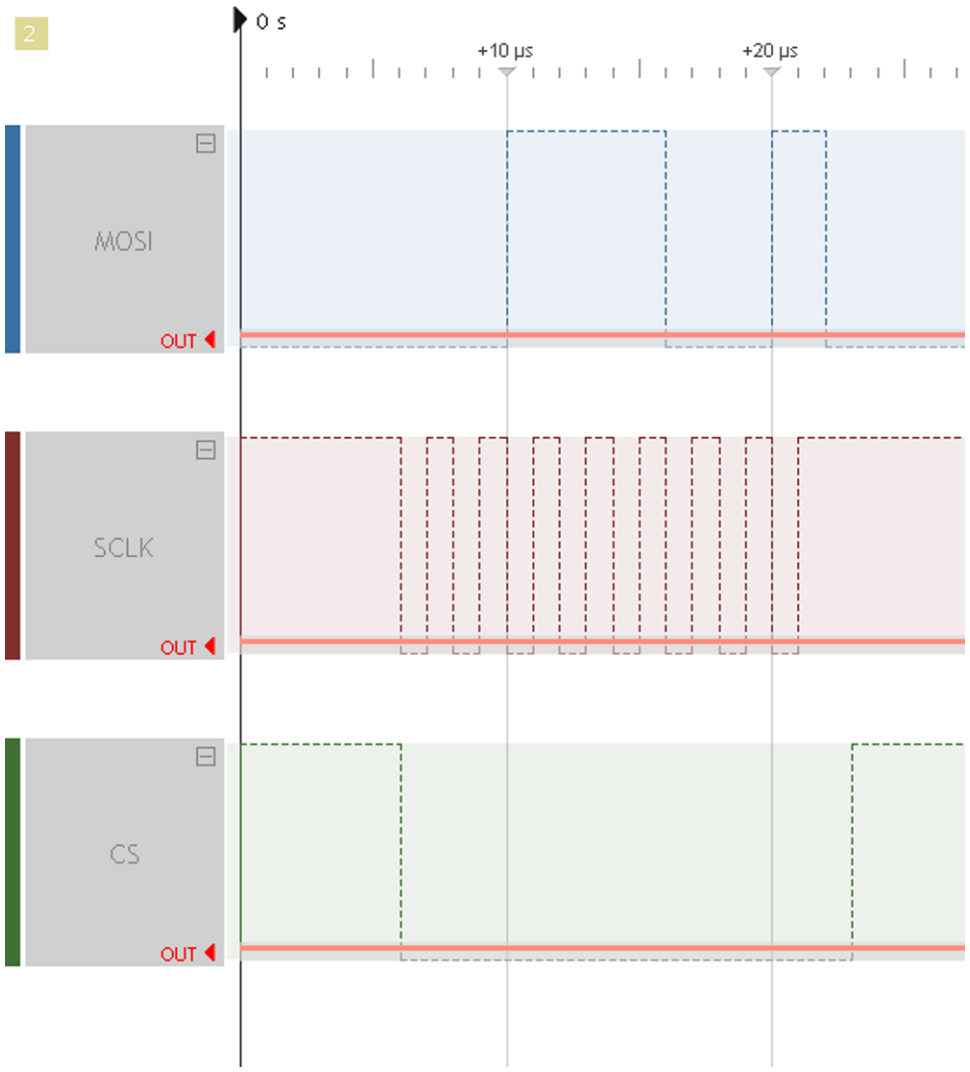


Figure 12. Example SPI Waveform for SN74HC595 Programming

2.3.3.9 Full Signal Path Verification

A TINA-TI simulation for the full signal path is conducted to evaluate the gain, bandwidth, and noise performance of the full path.

Figure 13 shows the overall AC transfer characteristics of the full path.

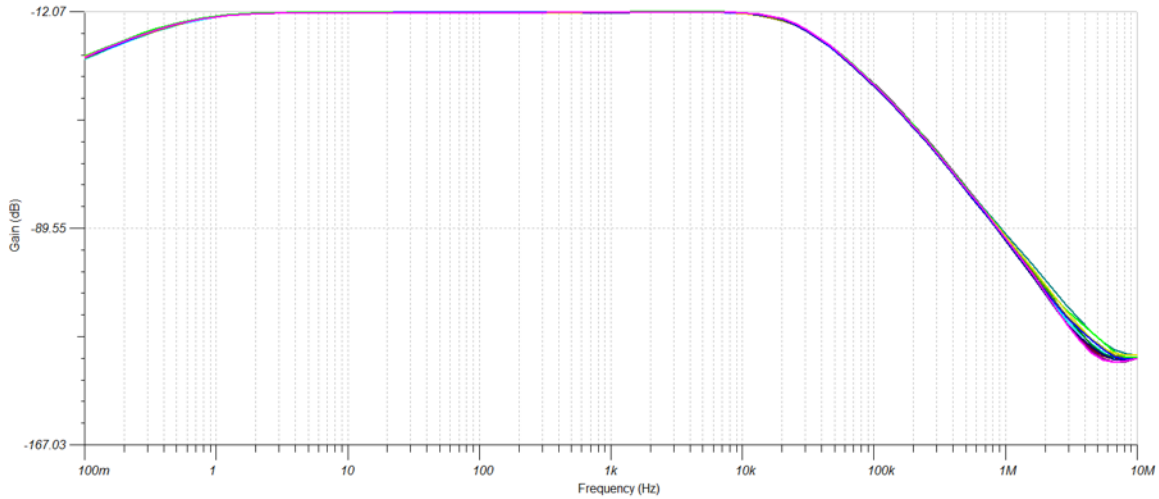


Figure 13. AC Transfer Characteristics of Signal Chain

Figure 14 and Figure 15 show the signal path passband in both –12-dB and +18-dB total gain cases. The 0.7-kHz to 20-kHz bandwidth is clearly guaranteed even with component tolerance. The gain variation over the passband is 0.3 dB. A gain offset of 0.5 dB is also observed, which is easily calibrated.

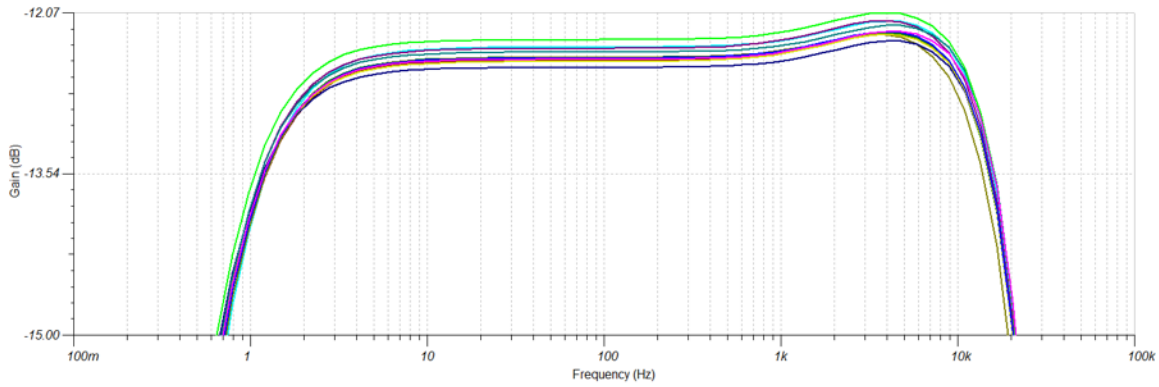


Figure 14. Signal Chain Passband at –12-dB Gain Setting

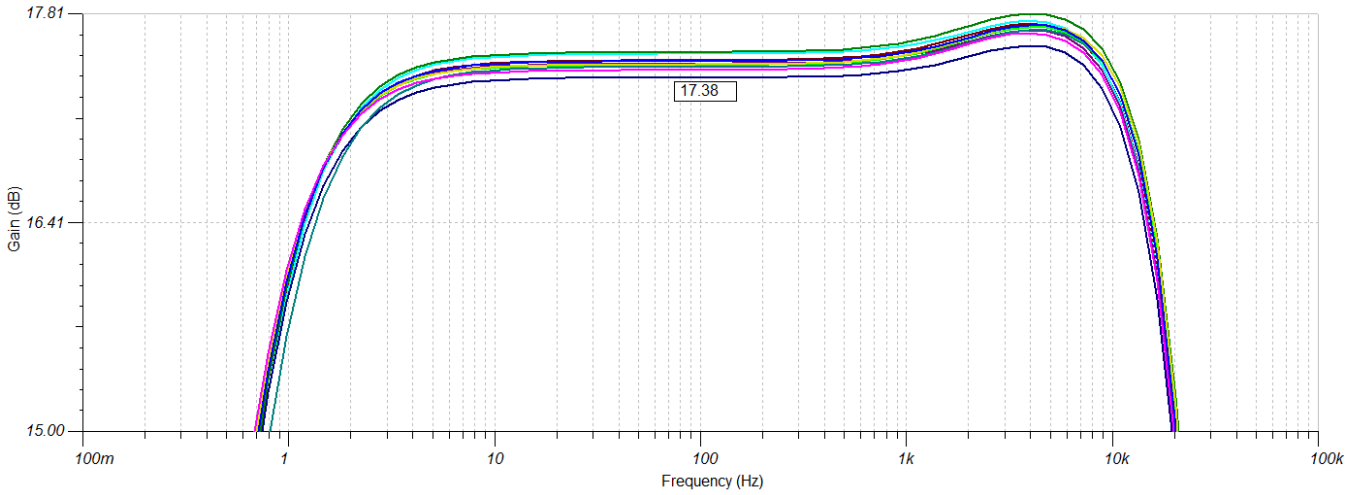


Figure 15. Signal Chain Passband at +12-dB Gain Setting

Figure 16 shows that the total integrated noise for the whole chain is 12 uV_{RMS} for the –12-dB gain setting.

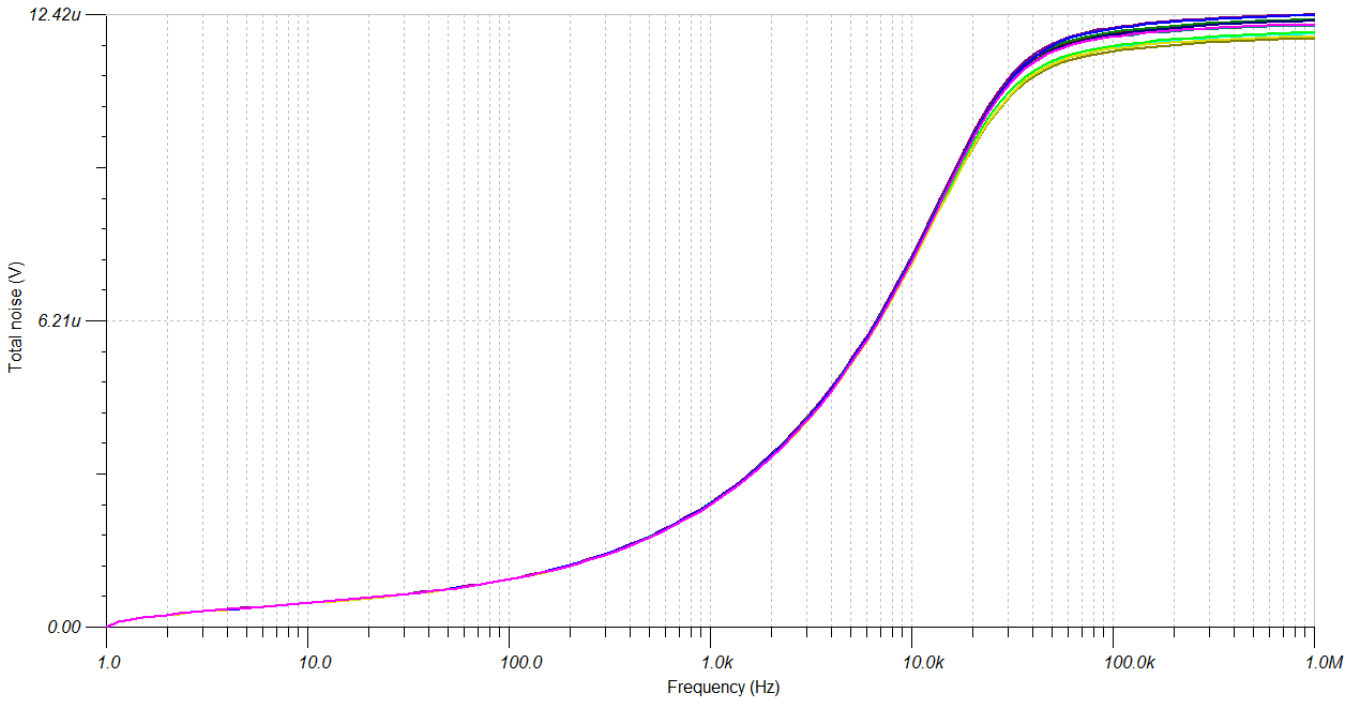


Figure 16. Total Output Noise of Signal Chain

Transient simulations at both –12-dB and 18-dB settings show no sign of distortion at the output level close to the full scale.

The current consumption is also estimated by monitoring the current through VCC. A maximum of 5 mA to 6 mA is drawn for a full-scale 5-kHz input, with an average of approximately 4.2 mA. The power consumption is dependent on the input level as well as the input frequency. A value from 4 mA to 5 mA can be used as a very conservative estimate of the power consumption of the signal path, including the VCOM supply. The VCOM current is below ±0.8 mA and decreases with increased input frequency.

Figure 17 and Figure 18 show the current consumption simulation results for the whole chain and VCOM reference, respectively.

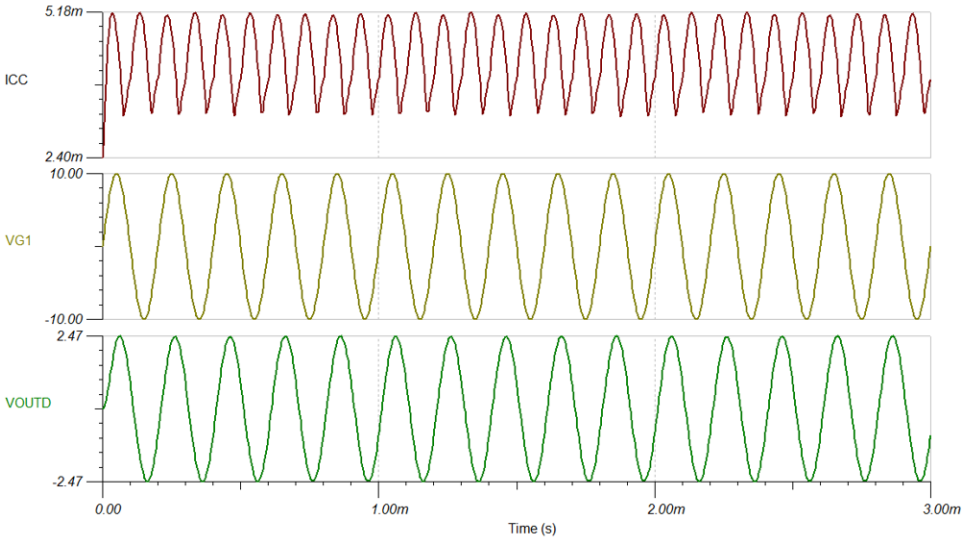


Figure 17. ICC Current Consumption for Whole Chain

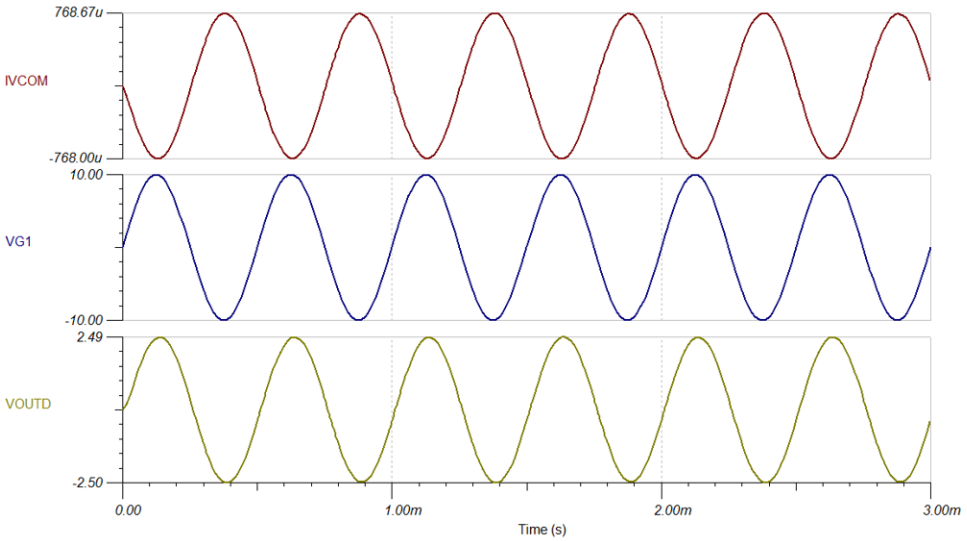


Figure 18. Output Current of VCOM Reference

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The TIDA-01471 printed-circuit board (PCB) is four-layer, single-sided board. Several jumpers are placed on the small form-factor board to make validation and measurements more flexible. Figure 19 shows the component side with all connectors and jumpers indicated.

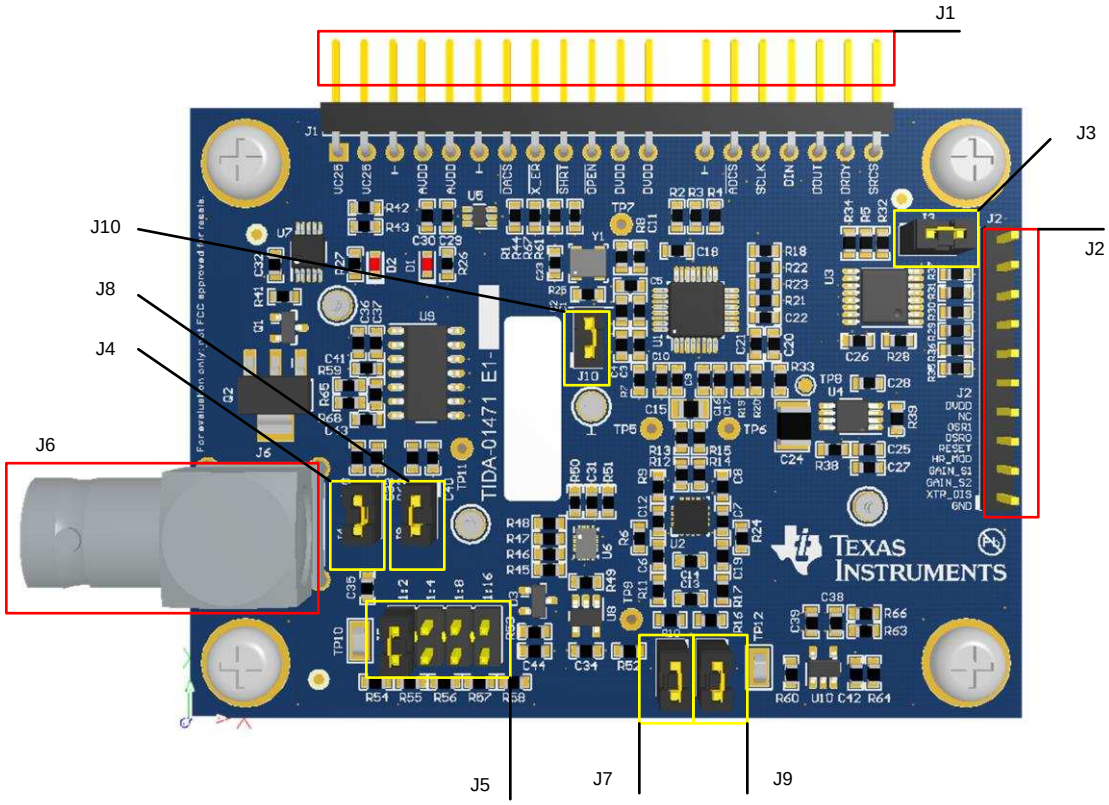


Figure 19. TIDA-01471 PCB Hardware—Top View

Table 2 provides a description of each jumper or connector and its usage.

Table 2. Jumper or Connectors

JUMPER OR CONNECTOR	DESCRIPTION OR USE
J1	Connector for power (AVDD 3.3 V, DVDD 3.3 V, and VCC 25 V), SPI bus, and output of detection circuit (SHORT, OPEN); connect before operating the board
J5	Attenuation setting jumper, select attenuation level (1/2 down to 1/16) based on the maximum input level
J6	Input BNC connector; connect to IEPE sensor, note the attenuation level (J5) before attaching (maximum ±10 V)
J3	Disable the shift register output; leave it open in case control signals are provided externally through J2—note that when disabled, the output of the SR takes on default values
J2	Control signal jumper; used to provide control signals externally (must short J2 to use)
J8	Fault detection circuit disable; remove this to disconnect the detection circuit; connect to GND to avoid floating input
J4	Current source disconnect; remove this to disconnect the current source from the input; an external source is required in case a sensor is used; in this disconnect mode, the intrinsic noise of the signal chain can be measured

Table 2. Jumper or Connectors (continued)

JUMPER OR CONNECTOR	DESCRIPTION OR USE
J7	VCOM disconnect from input attenuator; remove ths if the external source is to be used for input attenuator VCOM
J9	VCOM disconnect from signal chain; remove this and connect to external source if the effect of the VCOM is to be measured
J10	Clock disable jumper; short in the case where an external clock is to be used through TP7

3.1.2 Software

In this design, 10-MHz SPI communication is implemented through the AM437x IDK. See the TIDEP0033 tool folder for more details on coding the programmable real-time unit (PRU) for high-speed SPI.

3.1.3 Testing and Results

3.1.3.1 Test Setup

The TIDA-01471 PCB was tested using the test setup shown in Figure 20.

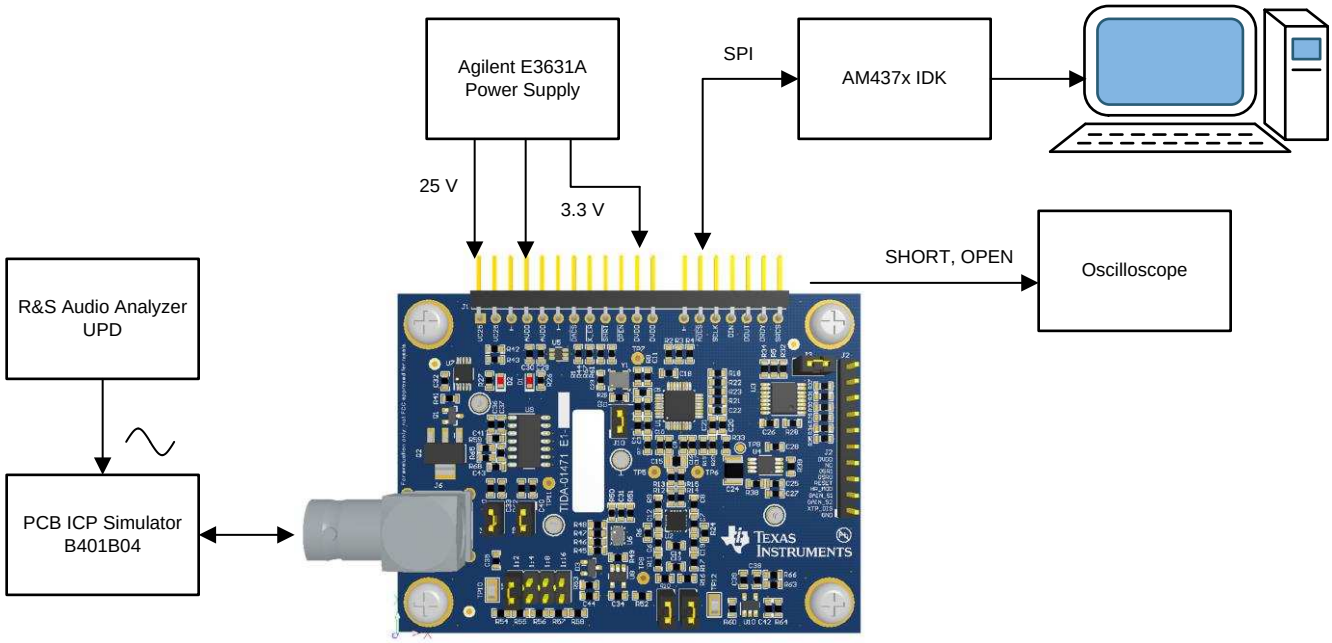


Figure 20. TIDA-01471 Test Setup

An E3631A Agilent® power source powers the board, providing 25 V and 3.3 V. The 3.3 V is used for both AVDD and DVDD pins.

A high-quality input source (R&S Audio Analyzer UPD with THD < –100 dB) excites the PCB ICP Simulator (B401B04), which acts as an IEPE sensor with unity gain buffer for the excitation signal. The PCB ICP Simulator is connected to the input BNC connector, which also provides the required excitation current to the sensor simulator.

SPI and control lines are connected to the AM437x IDK, which in turn is connected to the PC through a USB debugger. The Code Composer Studio™ (CCS) integrated development environment (IDE) is used to run the SPI and capture the ADC output data at the 10-MHz maximum SPI speed. The 64-k points data capture is stored in DDR memory and later transferred to a file using CCS debugging tools. The data is then processed to generate the power spectral density plot and calculate the SNR of the interface circuit.

In some tests, fault detection bits (SHORT and OPEN) are connected to a scope to measure some delay or input threshold parameters.

In all the remaining tests and results of this section, the data rate is set to 62.5 kSPS (CLK = 8 MHz, OSR = 128), even though sampling rates up to 256 kSPS are possible; however, the user can obtain a higher SNR by reducing the data rate, especially with a bandwidth of only 20 kHz.

Moreover, 64-k samples are collected for each measurement and the power spectral density (PSD) is calculated using a fast Fourier transform (FFT) periodogram after windowing with a Hanning window. All time graphs featured in this section are normalized with FS = 1 and with the offset removed. All frequency domain PSD is normalized so that the peak-to-peak FS input results in –3-dB power, that is, normalized to input RMS value according to the ITU-T G.100 standard. So when the input peak-to-peak is equal to FS, this level is reported as –3 dBFS according to its RMS value.

3.1.3.2 Gain and Input Range

The audio analyzer (UDP) source is connected directly to the BNC input connector of TIDA-01471, with the input level adjusted to ±10-V peak-to-peak. The chain gain is set to –12 dB, with the attenuator set to 1/16. The inputs at 100 Hz, 3.9 kHz, and 18 kHz are injected with the output examined for the minimum and maximum. The following Figure 21 and Figure 22 show that no clipping occurs and the chain gain is very close to the expected gain with less than 0.3 dB of error. The power consumption at the FS input is 32 mA from a 3.3-V supply, including the digital and analog circuit sections setting the power consumption close to 0.1 W per channel.

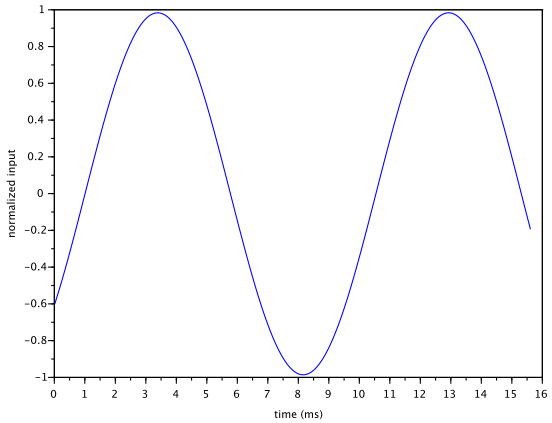


Figure 21. Sampled Input at 0.1 kHz

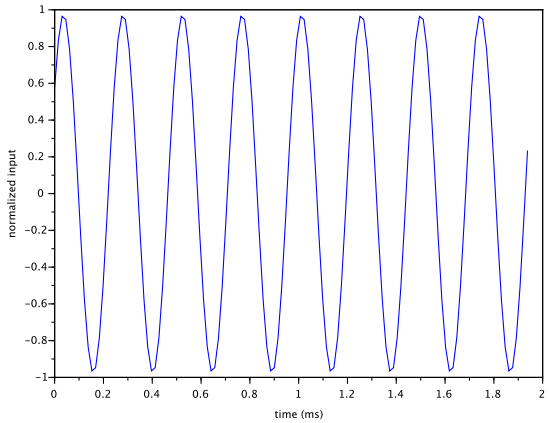


Figure 22. Sampled Input at 3.9 kHz

Table 3. Gain for Different Frequency Inputs

FREQUENCY (kHz)	GAIN (dB)
0.1	–0.14
3.9	–0.31
18	–2.5

3.1.3.3 Noise Floor and Signal-to-Noise Ratio (SNR)

The audio analyzer (UDP) source is connected directly to the BNC input connector of TIDA-01471 with the XTR current source disabled. Figure 23 and Figure 24 show the noise floor for attenuation in 1/16 and 1/2 cases.

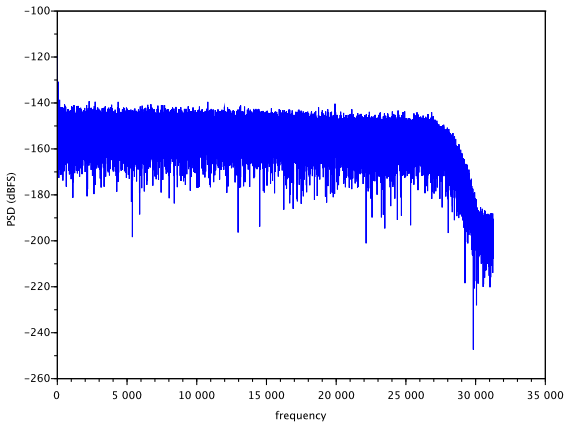


Figure 23. Noise Floor for Attenuation = 1/16

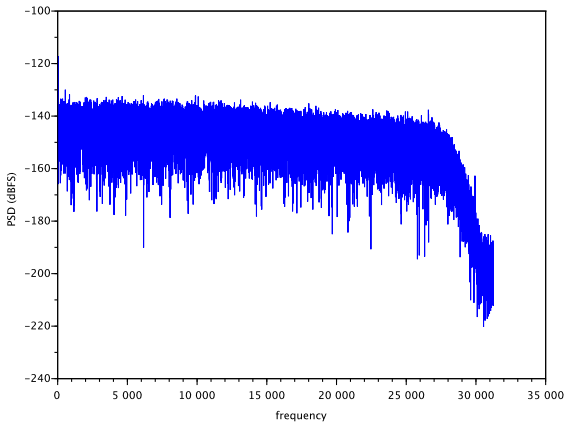


Figure 24. Noise Floor for Attenuation = 1/2

Table 4 shows the SNR and the ENOB for the various attenuation settings.

Table 4. Maximum SNR Achieved for Different Attenuation Settings

ATTENUATION	NOISE (μV_{RMS})	MAX SNR (dB)	ENOB (BITS)
1/16	12.9	102.7	17.0
1/8	16.1	100.8	16.7
1/4	21.5	98.3	16.3
1/2	29.5	95.5	15.8

Note here that, to a great extent, the integrated noise matches the simulated integrated noise of the signal path, as the previous Figure 16 shows. The ADC data sheet states approximately 4.8 μV_{RMS} as the ADC noise in the given settings of the OSR, filter, and clock frequency. The 12.9 μV_{RMS} is exactly the RMS noise summation of 12 μV_{RMS} and 4.8 μV_{RMS}.

As an experiment to break down the noise contribution, the circuit is measured without the gain MUX and with only a single 2-kΩ feedback resistor. The noise measured was at the 10.77 μV_{RMS} level, which is equivalent to an SNR = 107 dB, which translates to ENOB = 17.7. So if the programmable gain is not essential in an application, TI recommends to use a simple gain stage.

3.1.3.4 Clock Image Rejection

A high-frequency source is connected to the input directly with fin = 8.01 MHz and –16 dBFS. The highest spur is monitored in the noise spectrum and image rejection is calculated as the image spur referred to the input level, as Figure 25 shows. The image rejection is measured at –95 dB.

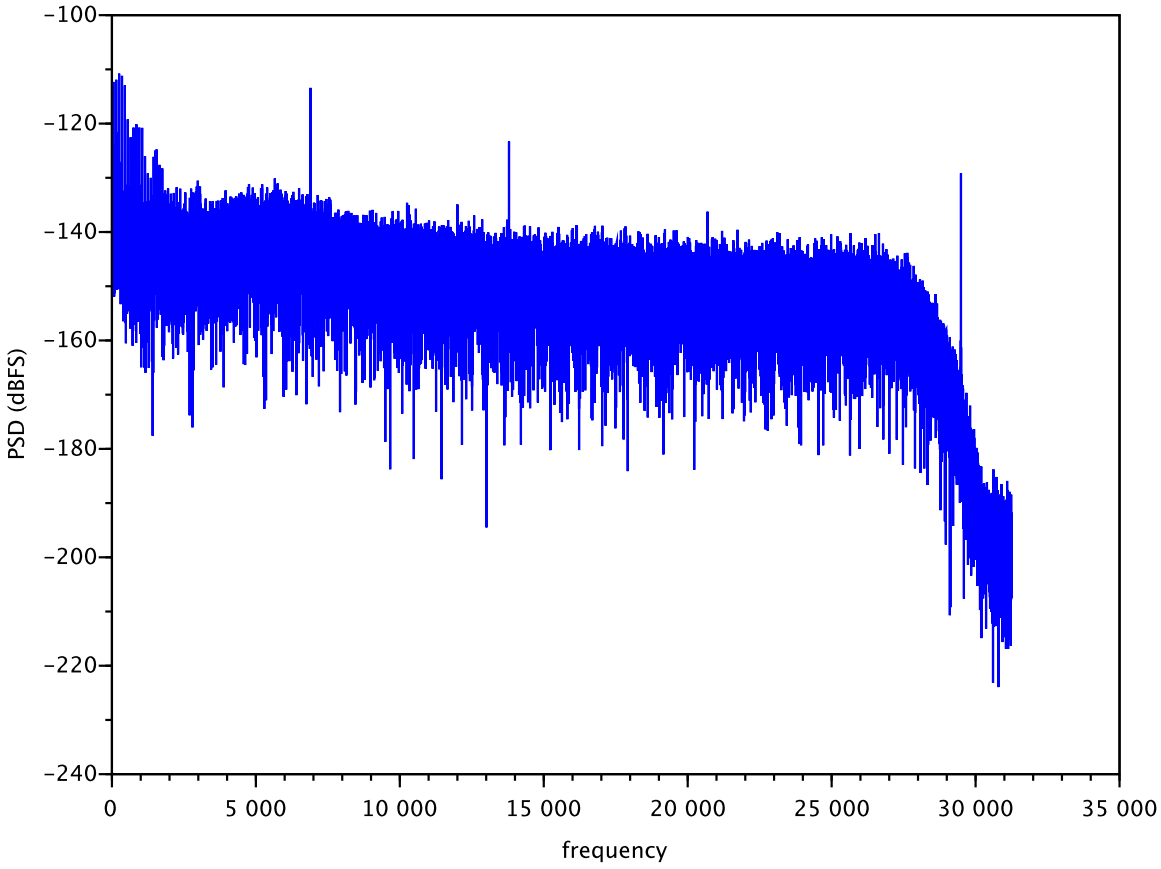


Figure 25. Noise in Presence of Image Frequency at 8.01 MHz

3.1.3.5 Sensor Simulator Noise Floor

Before using the sensor simulator in active setup, the user must evaluate the noise by powering the simulator with an external 4 mA from an accurate source and leaving the input simulator open. Figure 26 shows the power spectral density of the sensor. The integrated noise is 28.9 μV_{RMS}, which shows that simulator noise is much higher than the typical noise of the signal chain. This is a limitation of the sensor simulator that prevents the measurement of very-high SNR when the simulator is part of the setup.

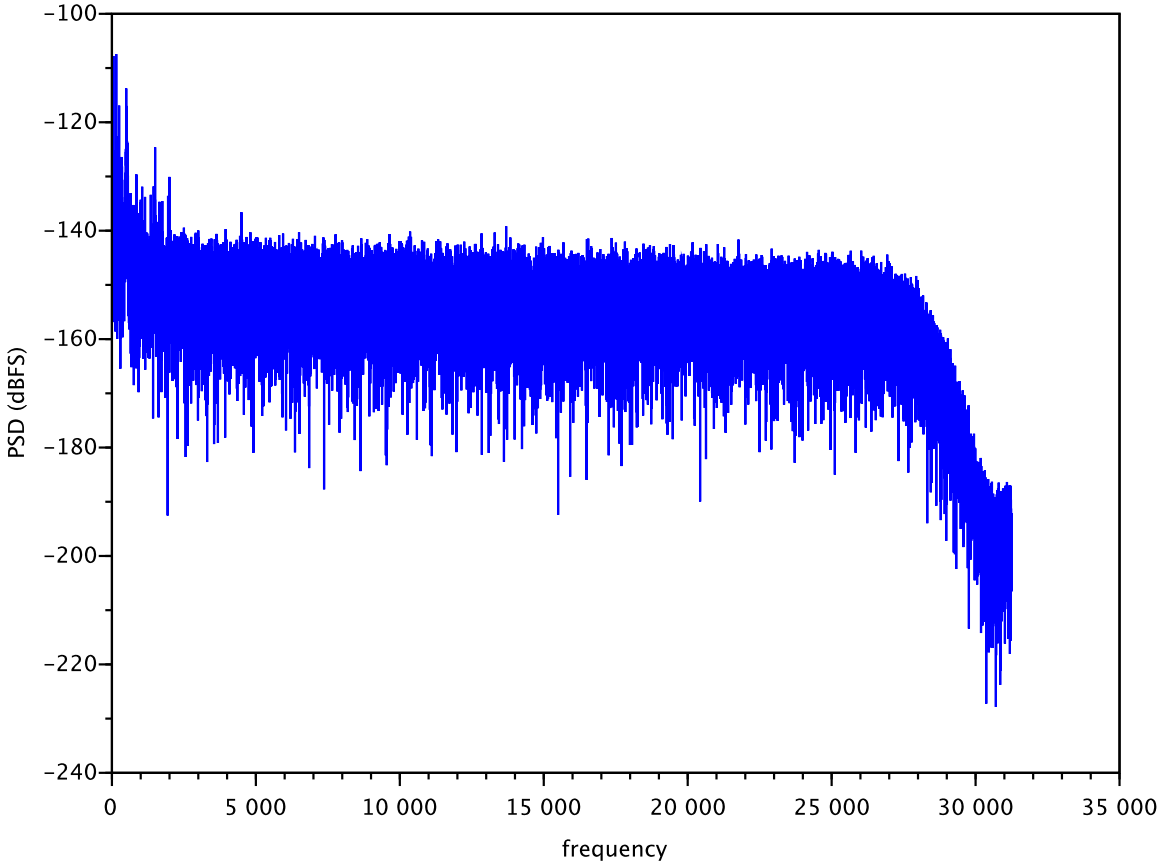


Figure 26. Noise Floor With External Sensor Simulator Connected

3.1.3.5.1 XTR111 Noise Contribution

The XTR is evaluated by enabling the current source without a sensor attached and leaving the input open. The resulting integrated noise is 43.3 μV_{RMS}, which is quite high for the target resolution. Figure 27 shows the noise floor when XTR is enabled without any load attached.

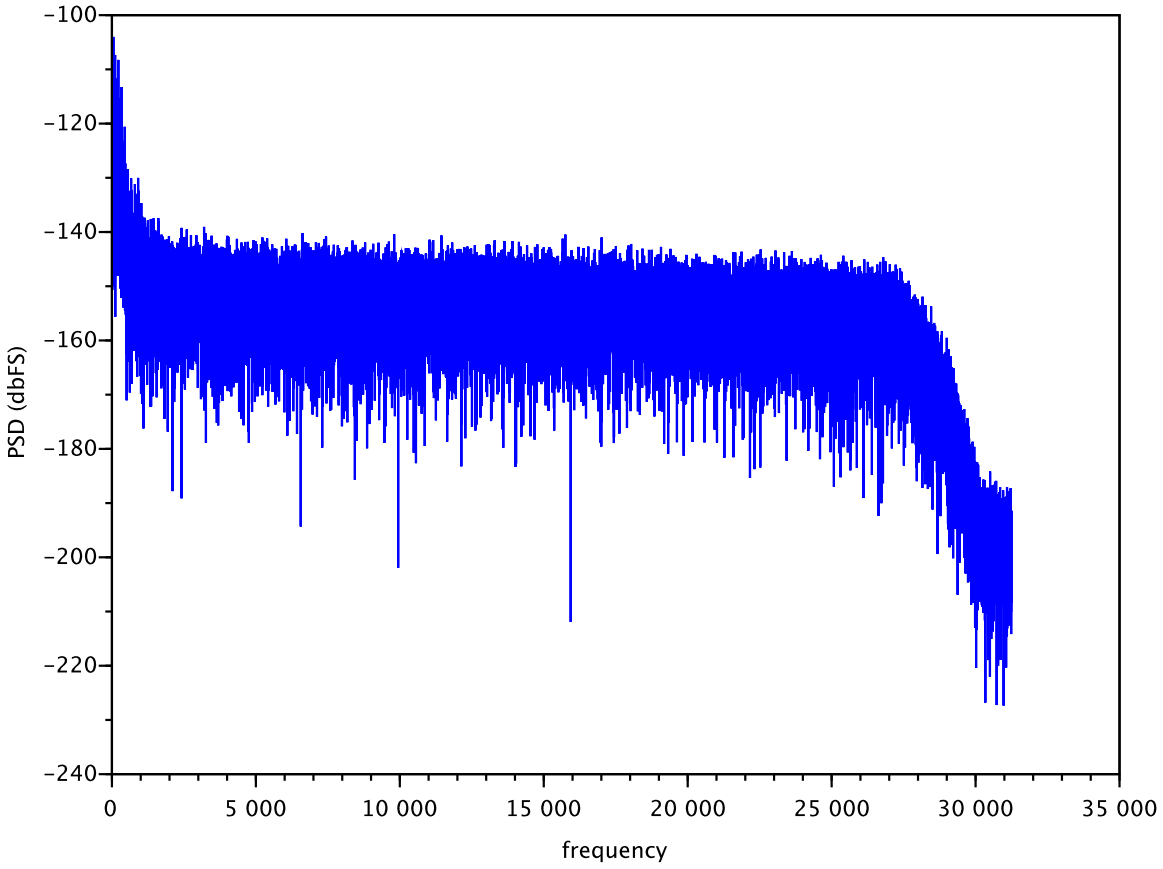


Figure 27. Noise Floor With XTR111 Enabled

3.1.3.5.2 Total Harmonic Distortion

With the UDP source connected directly to the input and providing an input power level of –37 dBFS at a frequency of 3.9 kHz, the total harmonic distortion (THD) is measured as –92 dB. In the case of an input level of –23 dBFS, the THD is measured as –90.8 dB. Figure 28 and Figure 29 show the spectrum including harmonics for both -37-dBFS and -23-dBFS inputs.

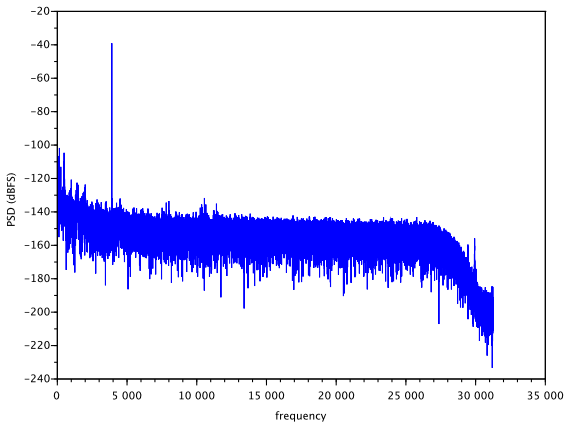


Figure 28. PSD for –37-dBFS Input at 3.9 kHz

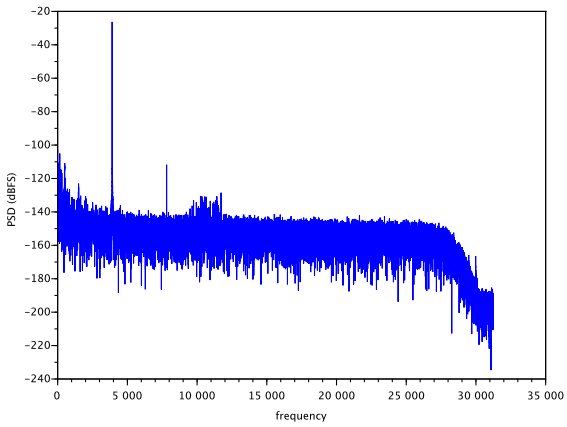


Figure 29. PSD for –23-dBFS Input at 3.9 kHz

3.1.3.5.3 Fault Detection Delay

Measurement of OPEN and SHORT fault outputs (both active low) is performed with a step input; 0 V to 23 V in the case of an open detection and 10 V to 0 V in the case of a short detection. Figure 30 and Figure 31 show an observable delay time of 113 ms and 106 ms.

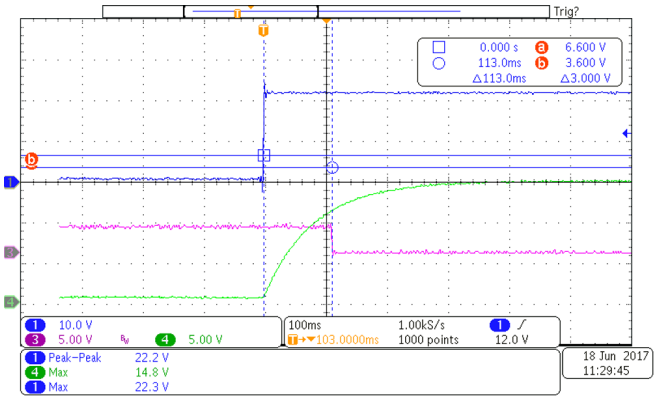


Figure 30. Open-Circuit Detection Delay

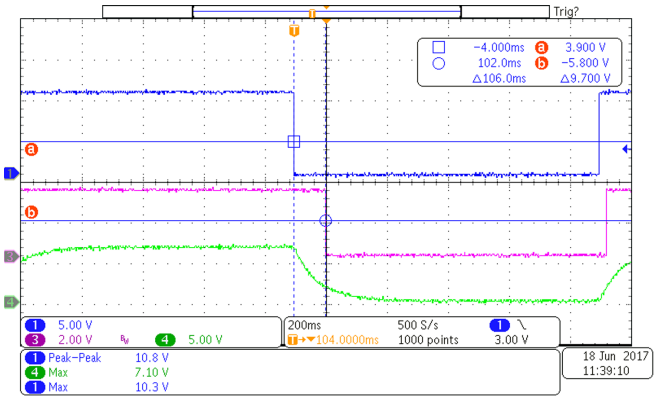


Figure 31. Short-Circuit Detection Delay

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01471.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01471.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01471.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01471.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01471.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01471.

5 Trademarks

6 About the Author

AHMED NOEMAN is a system engineer at Texas Instruments Germany where he is responsible for developing reference design solutions for industrial applications. Ahmed has many years of experience in analog and RF design, AMS modeling, and verification, as well as application and system engineering in a wide range of fields including RF transceivers, clocks and PLLs, memory systems, and others. Ahmed received his BSC and MSEE from Ain Shams University, Egypt.

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