TI Designs

Advanced Dimming Capable Buck LED Driver Reference Design for Industrial IR LED Applications

Description

This TI Design showcases a TPS92515 small-form factor LED driver optimized to drive up to five Infrared (IR) LEDs for an industrial camera design. The buck topology is implemented as a secondary-stage LED driver to offer a simple high-performance and cost-effective lighting solution. Additional design flexibility includes analog and PWM dimming (including shunt FET dimming) support as well as cycle-by-cycle current limit and integrated thermal shutdown protection. EMI filtering has been included and designed to meet FCC part 15 class B conduction requirements.

Resources

PMP15022	Design Folder
TPS92515	Product Folder
TPS92515HV-Q1 Buck LED Driver EVM	Product Folder

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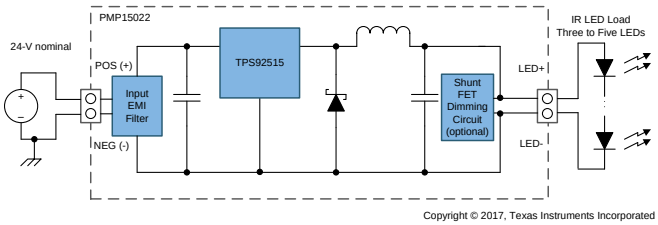
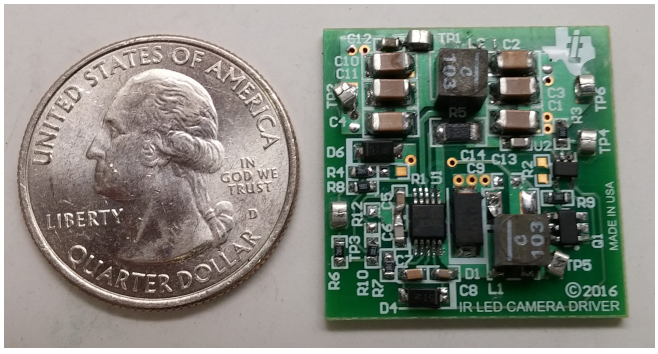
Features

- Optimized for Infrared LEDs and Other Small-Form Factor LED Lighting Applications
- Small Inductor Size (4 mm × 4 mm)
- FCC Part Class B 15 Tested EMI
- Deep Analog and PWM Dimming
  - 13:1 Analog Dimming Only
  - 500:1 PWM Pin or Shunt FET Dimming
  - 2000:1 Analog and PWM Combination Dimming
- Supports High-Speed Shunt FET PWM Dimming
- Fast Transient Response With No Loop Compensation Required
- Cycle-by-Cycle Current Limit, Integrated Thermal Shutdown Protection, and Input Undervoltage Lockout
- Capable of Wide Dimming Ranges

Applications

- Industrial Cameras
- Machine Vision
- Bar Code Readers
- Low- to Medium-Wattage Luminaires





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1 System Overview

1.1 System Description

Energy efficiency, longevity, and precise dimming control are all factors that are causing widespread adoption of LEDs in industrial camera applications. Infrared light-emitting diodes (IR LEDs) offer clear performance and reliability advantages over traditional light sources while enhancing longevity and dimming performance. However, short development cycles and intense competition puts pressure on product vendors to reduce their time to market while still offering high-quality lighting solutions in terms of low electromagnetic interference (EMI), thermal efficiency, and light quality.

The PMP15022 reference design is a small-form factor, easy-to-adopt LED driver implementation that can be used in a broad range of applications. This TI Design uses the TPS92515 LED driver, which has an integrated N-channel field-effect transistor (FET), contributing to a very streamlined design with a minimized printed-circuit board (PCB) footprint. The efficient buck topology accepts an input voltage range of 21 to 27 V (24-V nominal input) and has been optimized for driving up to five IR LEDs in series while meeting FCC part 15 class B conducted EMI standards. Onboard analog and pulse-width modulation (PWM) dimming enables user-configured LED lighting calibration and precision dimming capability.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
VIN input voltage	—	21	24	27	V
VIN input voltage (maximum)	—	—	—	42	V
OUTPUT CHARACTERISTICS					
LED forward voltage	—	—	1.65	1.9	V
No. of LED in series	—	—	—	5	—
VLED output voltage	LED+ to LED–	—	—	9.5	V
ILED output current	—	—	1	—	A
Output power	—	—	—	9.5	W
Analog dimming range	V_{IADJ} = 0 to 2.4 V (minimum on-time limited), five LEDs	10:1	13:1	—	—
PWM dimming range	PDIM dimming, 1.5 kHz, five LEDs	100:1	500:1	—	—
PWM dimming range	Shunt FET dimming, 30 kHz, five LEDs	100:1	500:1	—	—
Analog plus PWM dimming range	Analog dimmed to 13:1 first then further reduced with a 1.5-kHz PWM signal on the PWM pin, five LEDs	1000:1	2000:1	—	—
SYSTEM CHARACTERISTICS					
ΔIL-PP inductor current ripple	—	—	1000	—	mA
ΔVIN-PP input voltage ripple	—	—	—	10	mV
f_{SW} switching frequency	V_{IN} = 24 V, five LEDs	—	520	—	kHz
Efficiency	V_{IN} = 24 V, five LEDs	—	88	—	%
EMI (conducted)	—	FCC part 15 class B			
BASE BOARD CHARACTERISTICS					
Form factor	—	1 in × 1 in (25.4 mm × 25.4 mm)			
Number of layers	—	2			
Height	—	0.26 in (6.6 mm)			

1.3 Block Diagram

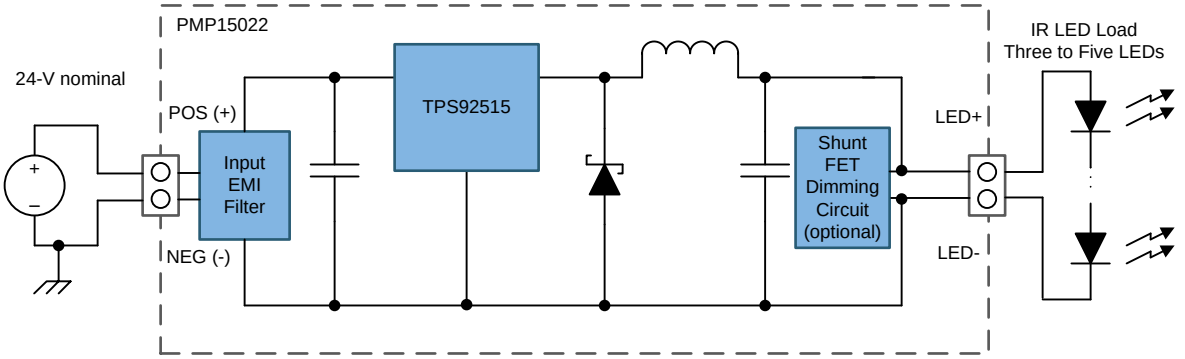

Figure 1. PMP15022 Block Diagram

1.4 Highlighted Products

1.4.1 TPS92515

The TPS92515 is a compact, monolithic-switching regulator integrating a low-resistance N-Channel MOSFET (see Figure 2). The device is intended for high-brightness LED lighting applications where efficiency, high bandwidth, small size, PWM, or analog dimming (or both) are important.

The regulator operates using a constant off-time, peak current control. The operation is simple: after an off-time based on the output voltage, an on-time begins. The on-time ends when the inductor peak current threshold has been reached. The TPS92515 device can be configured to maintain a constant peak-to-peak ripple during the ON and OFF periods of a shunt FET dimming cycle. This configuration is ideal for maintaining a linear response across the entire shunt FET dimming range.

Steady-state accuracy is aided by the inclusion of a low-offset, high-side comparator. LED current can be modulated using either analog dimming, PWM dimming, or both simultaneously. Other features include undervoltage lockout (UVLO), wide input voltage operation, open and overvoltage protection (OVP) operation, and wide-operating temperature range with thermal shutdown.

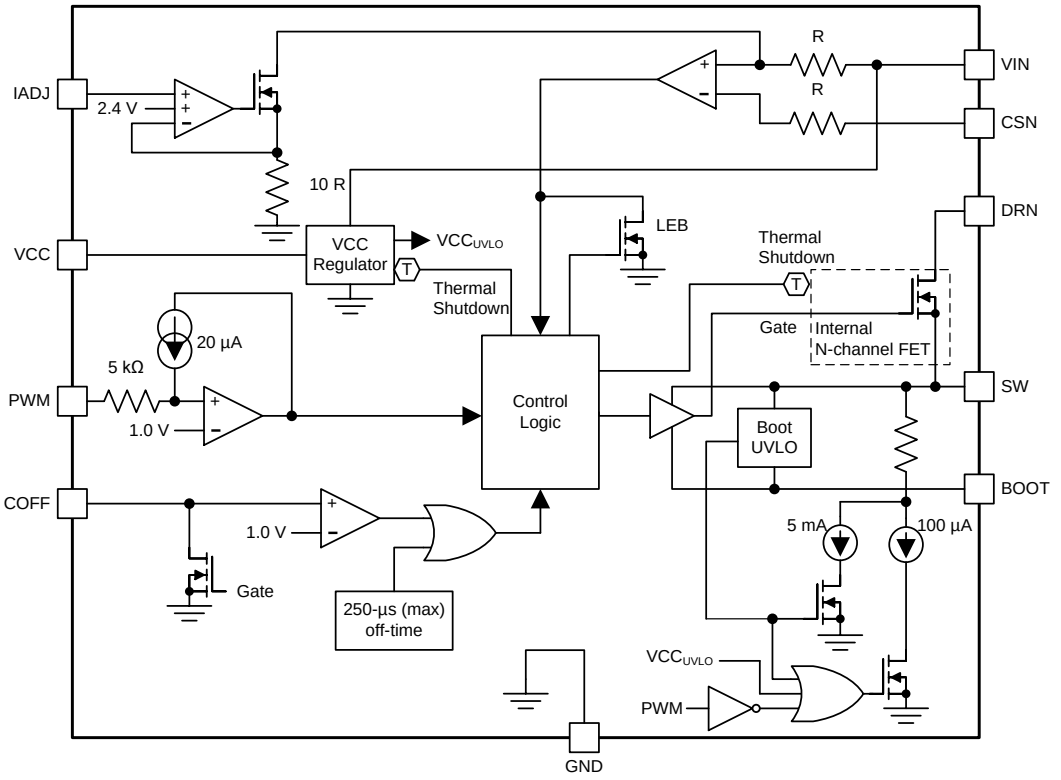

Figure 2. TPS92515 Block Diagram

The TPS92515 device has an operational input range up to 42 V. The TPS92515HV is a high-voltage option with an input range up to 65 V. Each device is available in a thermally enhanced 10-pin HVSSOP package.

Features:

- Integrated 290-mΩ (typ) internal N-channel FET
- Input voltage range:
  - TPS92515x: 5.5 to 42 V
  - TPS92515HVx: 5.5 to 65 V
- Operation down to 5.15 V after start-up
- Low-offset, high-side peak current comparator
- Constant average current, up to 2 A
- Inherent cycle-by-cycle current limit
- Multiple dimming methods
- Simple constant off-time control
- No loop compensation
- Fast transient response
- Thermally-enhanced HVSSOP package
- Integrated thermal protection

2 System Design Theory

This TI Design consists of a high-performance LED controller integrated circuit (IC) with an integrated FET configured in a buck (step-down) topology with EMI filtering at the input (see Figure 3). The input voltage range is 21 to 27 V, which makes this LED driver compatible for standard second stage industrial configurations. This design supports 1 A of output current and an output power rating of just under 10 W maximum. The design has been optimized to drive up to five IR LEDs in series (assuming an LED forward voltage of 1.65 V) from a typical voltage supply of 24 V. However, multiple combinations of input supplies and LED loads can easily be created using this TI Design as a starting point.

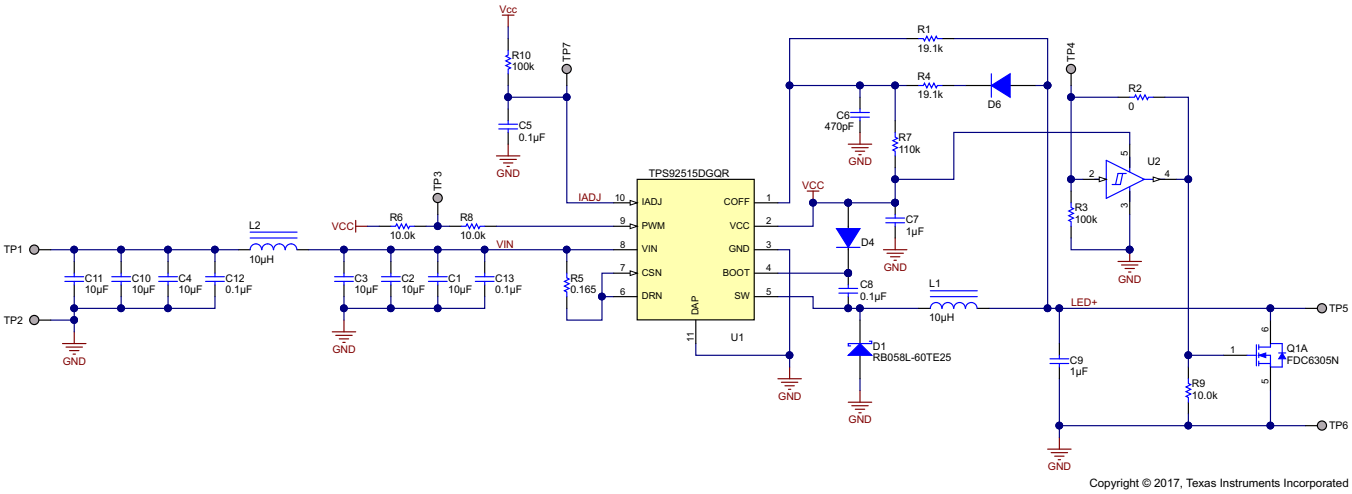

Figure 3. PMP15022 Schematic

2.1 Analog Adjust Input (IADJ) and Analog Dimming

The analog adjust pin (IADJ) provides the reference for the peak inductor current trip point. This threshold is then used to establish the default output current level for this design, which is 1 A. The IADJ voltage is tied to VCC through resistor R10, which results in the V_{IADJ} voltage being clamped internally to 2.4 V. Connecting the IADJ pin directly to VCC is the simplest configuration and the most accurate standalone implementation.

Other configurations using the IADJ pin include thermal foldback, interfacing with a microcontroller (MCU), implementing a soft-start sequence, and so forth. Refer to the product data sheet for further details on these options.

If analog dimming is required, an external voltage between 0 and 2.4 V can be applied directly to the IADJ pin to provide an analog dimming function. An analog dimming range of over 10:1 is attainable with this TI Design. Increased analog dimming range can be achieved with lower switching frequencies or lower input voltages (increased duty cycles) since this particular design is minimum on-time (minimum duty cycle) limited due to a higher switching frequency chosen.

2.2 PWM Dimming

The default PWM pin voltage for this design is approximately 2.5 V as set up by the resistor divider (consisting of R6 and R8), from VCC to GND. This default voltage ensures that the TPS92515 starts up and operates properly when input power has been applied.

Additionally, PWM dimming can be implemented by applying a signal above 1 V (typical) and below 900 mV (typical) at test point TP3. This TI Design has been tested with a PWM frequency of 1.5 kHz. When using higher frequencies (greater than 5 kHz), the delays from PWM to gate turnon and turnoff can begin to limit the achievable duty cycle. In this situation, TI recommends the designer consider using a shunt FET PWM solution with the TPS92515 (described in further detail in the product datasheet). This TI Design incorporates optional shunt FET dimming components and has been tested at 30 kHz. This circuitry is not populated for standard analog dimming or PWM pin dimming.

2.3 Switching Frequency and Off-Time

For a fixed LED load, the switching frequency of the TPS92515 increases as the input voltage, V_{IN}, increases, as Figure 4 shows.

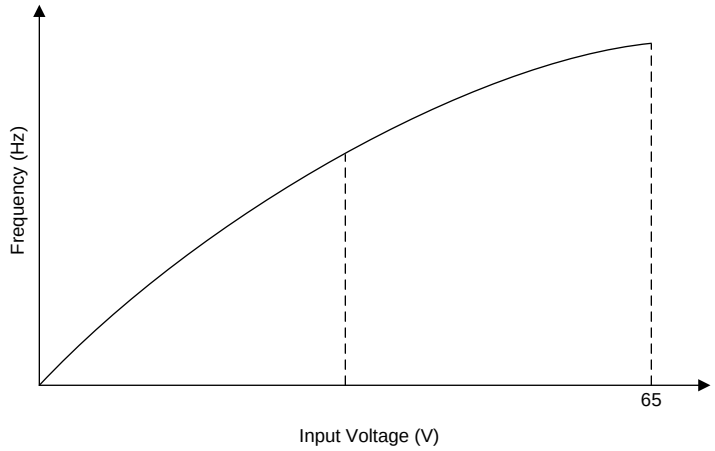

Figure 4. Frequency versus Input Voltage V_{IN} (Fixed LED Voltage)

To prevent this TI Design from operating above 600 kHz to limit thermal heating in such a small form factor, the maximum specified V_{IN} and switching frequency are used to calculate the off-time, t_{OFF}, and associated component values.

Using the following Equation 1, Equation 2, and Equation 3 (found in the product datasheet), duty cycle (D) and off-time (t_{OFF}) can be calculated. Component values can then be selected to meet the design criteria for this LED driver.

$$D = \frac{V_{LED}}{V_{IN} \times n} \quad (1)$$

$$t_{OFF} = \left(\frac{1}{f_{SW}}\right) \times (1 - D) \quad (2)$$

$$R_{OFF} = \frac{t_{OFF}}{-C_{OFF}\left(\ln\left(1 - \frac{V_{OFT}}{V_{LED}}\right)\right)} \quad (3)$$

From Equation 1 and using an output voltage (V_{LED}) of 8.395 V (bench measurement at 1 A), input voltage (V_{IN}) of 24 V, and a target efficiency (n) of 90%, the duty cycle (D) is calculated as 38.8%. With a maximum frequency (f_{SW}) of 540 kHz for some margin, the OFF time is calculated to be 1.13 µs using Equation 2. The typical off-time threshold (V_{OFT}) is 1 V, and by using the datasheet recommended 470 pF for the off-time capacitor C_{OFF} (C6), the OFF-time resistor R_{OFF} (R1) is calculated to be 19.0 kΩ using Equation 3.

For this TI Design, a resistor value of 19.1 kΩ has been chosen for R1.

2.4 Inductor Selection and Current Ripple

Choosing an inductor requires a balance between inductor current ripple, efficiency, physical size, and thermal considerations. A higher inductance value reduces current ripple but may require a physically larger inductor to handle a specific inductor current and maintain acceptable efficiency (with a lower-winding resistance DCR) and thermal dissipation. However, implementing a physically larger inductor then impacts the overall PCB footprint, headroom, and the overall potential design cost.

The inductor and the current ripple specification have been carefully chosen to provide an optimized balance of LED regulation performance, physical size, PCB footprint, and thermal dissipation. With the 1-A LED current and 1-A peak-to-peak inductor current ripple ($\Delta I_{L\text{-}PP}$) inductance can be calculated. Using Equation 4, the calculated inductance is 9.5 µH.

$$L = \frac{V_{LED} \times t_{OFF}}{\Delta I_{L-PP}} \tag{4}$$

For this LED driver, a 10-µH inductor has been chosen for L1.

2.5 Calculating Sense Resistor

The sense resistor R5 in now calculated using Equation 5. Because the IADJ pin is tied to V_{CC}, the V_{IADJ} reference voltage is clamped at 2.4 V.

$$R_{SENSE} = \frac{\left(\frac{V_{IADJ}}{10}\right)}{I_{LED} + \frac{\left(\Delta I_{L-PP}\right)}{2}} \tag{5}$$

The calculated sense resistance is 0.16 Ω. For this TI Design, a 0.165-Ω resistor has been chosen for R5.

2.6 Verify Peak Current for Inductor Selection

Using the selected sense resistor and Equation 6, the peak inductor current is calculated as 1.45 A. Inductor L1 has been selected to meet this minimum peak current rating.

$$IL_{PEAK} = \frac{\left(\frac{V_{IADJ}}{10}\right)}{R_{SENSE}} \tag{6}$$

2.7 Input Capacitance

Per the product datasheet, the voltage ripple ($\Delta V_{IN\text{-}PP}$) must not exceed 10% of the input voltage (V_{IN}) or 2 V, whichever is lower. Because this TI Design can operate up to an input voltage of 27 V, the maximum voltage ripple is 2 V. However, the minimum capacitance must also be based on the lowest-operating switching frequency, which occurs at an input voltage of 21 V for this design. Using Equation 1 and Equation 2 with the previously calculated off-time of 1.13 µs and an input voltage of 21 V results in a frequency of 480 kHz. Using this information with Equation 7, the minimum input capacitance is calculated as 0.4 µF.

$$C_{IN-MIN} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF}\right)}{\Delta V_{IN-PP}} \tag{7}$$

If using PWM dimming, then a larger input capacitor is required to supply the initial current required for the LED driver to reach the current regulation set-point. A general rule for PWM dimming applications is to use a capacitance value that is ten times greater than the value calculated for non-PWM dimming designs.

For this particular design, an EMI input filter is required to pass FCC 15 limits. The input capacitor is therefore designed in conjunction with the EMI filter and the result is an input capacitance much greater than the minimum value calculated in the preceding Equation 7 and is also able to support PWM dimming requirements.

2.8 Output Capacitance

A capacitor placed in parallel with the LED load can be used to reduce ΔI_{LED-PP} while keeping the same average current through both the inductor and the LED load. With an output capacitor, the inductance can be lowered, making the magnetic smaller and less expensive. Alternatively, the circuit can be run at a lower frequency with the same inductor value, improving the efficiency and increasing the maximum allowable average output voltage. A parallel output capacitor is also useful in applications where the inductor or input voltage tolerance is poor. Adding a capacitor that reduces ΔI_{LED-PP} to well below the target provides headroom for changes in inductance or V_{IN} that might otherwise push the maximum ΔI_{LED-PP} too high.

Because the inductor value of this design has been chosen to meet the inductor current ripple specification, a minimum amount of output capacitance (1 µF) has been added for the analog dimming and analog plus PWM pin dimming circuits. It is omitted for shunt FET dimming (large charging and discharging currents could damage the shunt FET) and for standalone PWM pin dimming tests for this design. It may be used for PWM pin dimming if desired but linear dimming may be impacted at very low duty cycles.

Alternatively, because current is being regulated and is continuous, no output capacitance is required to supply the load and maintain output voltage. This feature is advantageous when designing for high-frequency PWM dimming on the LED load (that is, PWM shunt FET), which requires fast dimming edges.

2.9 Thermal Protection

Internal thermal protection circuitry protects the controller in the event of exceeding the maximum junction temperature. At 175°C the converter typically shuts down, thus protecting all the circuitry in the reference design. The maximum junction temperature is a function of the system operating points (that is, efficiency, ambient temperature, and thermal management), component choices, and switching frequency.

3 Designing for Low EMI

3.1 EMI Performance

Figure 5 shows the conducted EMI scan for this design at a nominal 24-V input voltage and driving a 8.25-V LED load (that is five IR LEDs in series) at 1 A of LED current. The blue trace is the peak scan and the line labeled "QP.LIN" denotes the peak limits for FCC part 15 class B. The black trace is the average scan with the line labeled "A.LIN" denoting average limits for FCC part 15 class B. The scan covers the entire conducted frequency range of 150 kHz to 30 MHz. This is a pre-compliance test scan used for engineering development and evaluation and not a certified EMI test result. It is the responsibility of the end-user to submit any design based on this TI Design to a certified EMI lab if an official EMI test result is required.

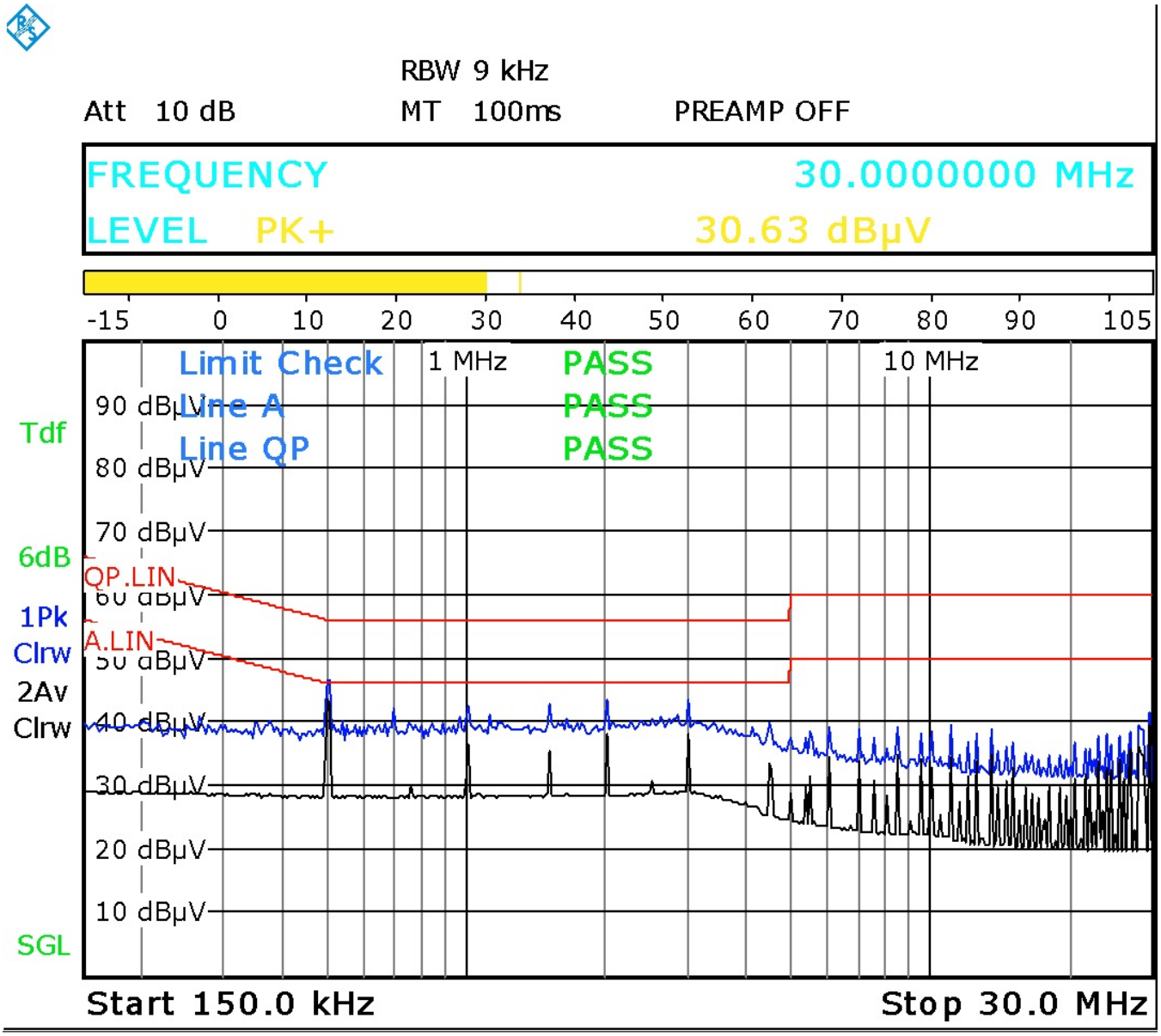

Figure 5. FCC Part 15 Class B Conducted EMI Scan (QP.LIN: Peak Limits, A.LIN: Average Limits) V_{IN} = 24 V, Five LEDs, I_{LED} = 1 A (Pre-Compliance Data)

3.2 EMI Filter Design

The input EMI filter consists of a differential mode PI filter formed by the input capacitors (C1 through C4, C10 through C13) and the input inductor (L2). The primary purpose of the filter is to minimize EMI conducted from the circuit to prevent it from interfering with the electrical network supplying power to the LED driver. Frequencies in and around the LED driver switching frequency (that is, fundamental and harmonics) are primarily addressed with this filter and the filter cutoff frequency is determined by the inductor and capacitor resonance.

Sufficient differential mode noise filtering on the output if required is generally provided by the output capacitor assuming low equivalent-series-resistance (ESR) ceramics are used as in the design for FCC part 15 class B conducted limits. This LED driver has been designed with the assumption that a connection to chassis ground is not available.

For more information on EMI filter design, see the application notes *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* and *Input Filter Design for Switching Power Supplies*.

3.2.1 Additional EMI Considerations

Higher power levels may likely require increased EMI filtering to pass FCC part 15 class B limits. Options include increasing input capacitance, or output capacitance (or both), adding ferrite bead resistance to mitigate high frequency EMI, or adding output choke inductance for common-mode noise reduction.

4 Testing and Results

4.1 Test Setup

Figure 6 shows the test setup. The input voltage was supplied by a DC power supply connected to the onboard test points TP1 and TP2. The LED load was connected to the board using test points TP6 and TP5. Four digital multimeters (DMMs) were used to measure input voltage, input current, output voltage, and output current. To enable PWM dimming, an external signal generator was connected to the PWM using test point TP3. For analog adjustment and dimming measurements, an external voltage supply was connected to the IADJ pin at TP7.

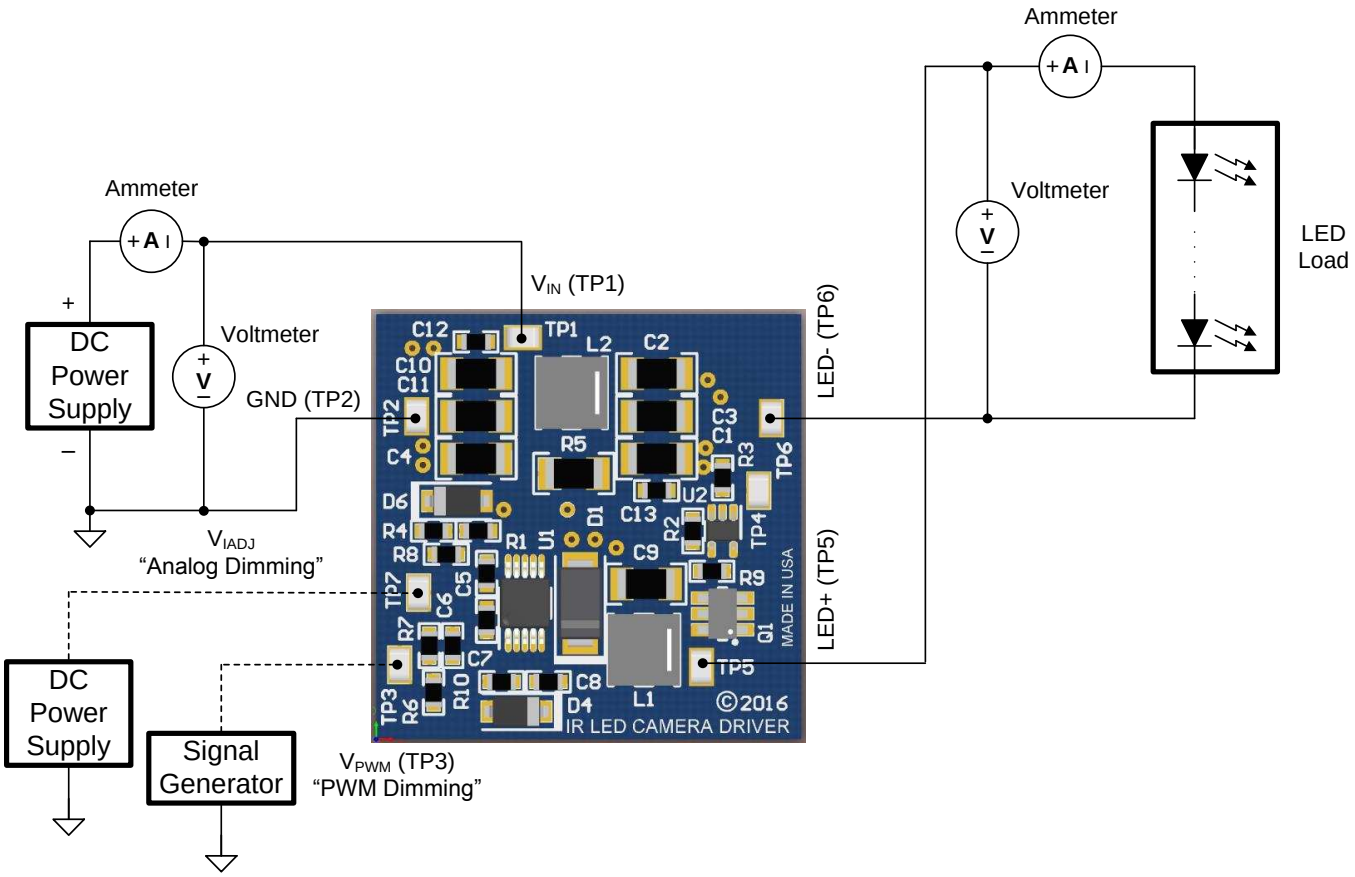

Figure 6. Test Setup Connections

4.2 Test Results

The test setup described in Figure 6 was used to generate the following data for analog dimming and PWM dimming measurements. All graphs and oscilloscope shots are with an input of 24 V, five IR LEDs in series, and a nominal LED current of 1 A.

4.2.1 Nominal Operation Waveform

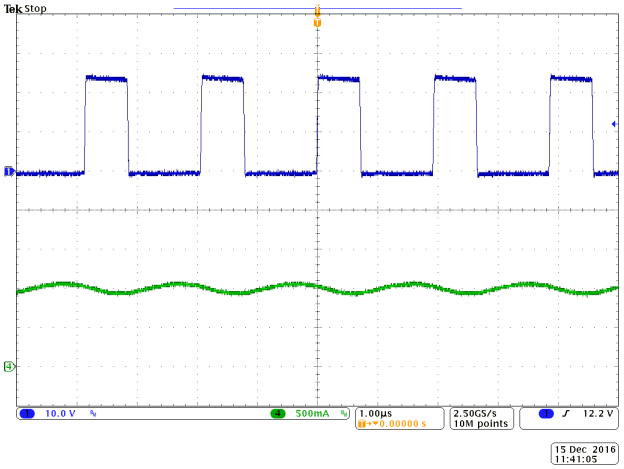

Figure 7. CH 1: Switch Node (DRN) Voltage and CH4: LED Current

4.2.2 Analog Dimming

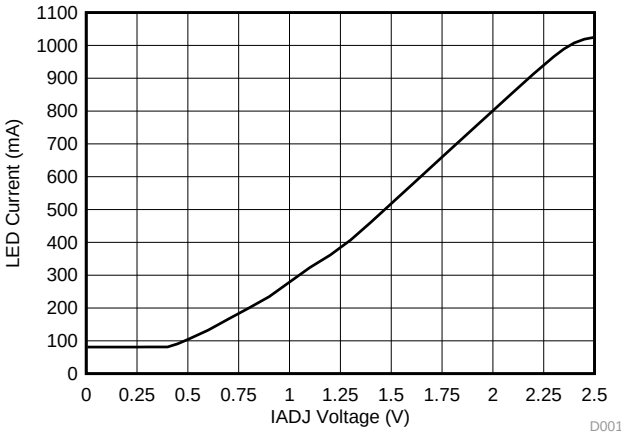

Figure 8. LED Current versus IADJ Voltage (13:1, Minimum Duty Cycle Limited)

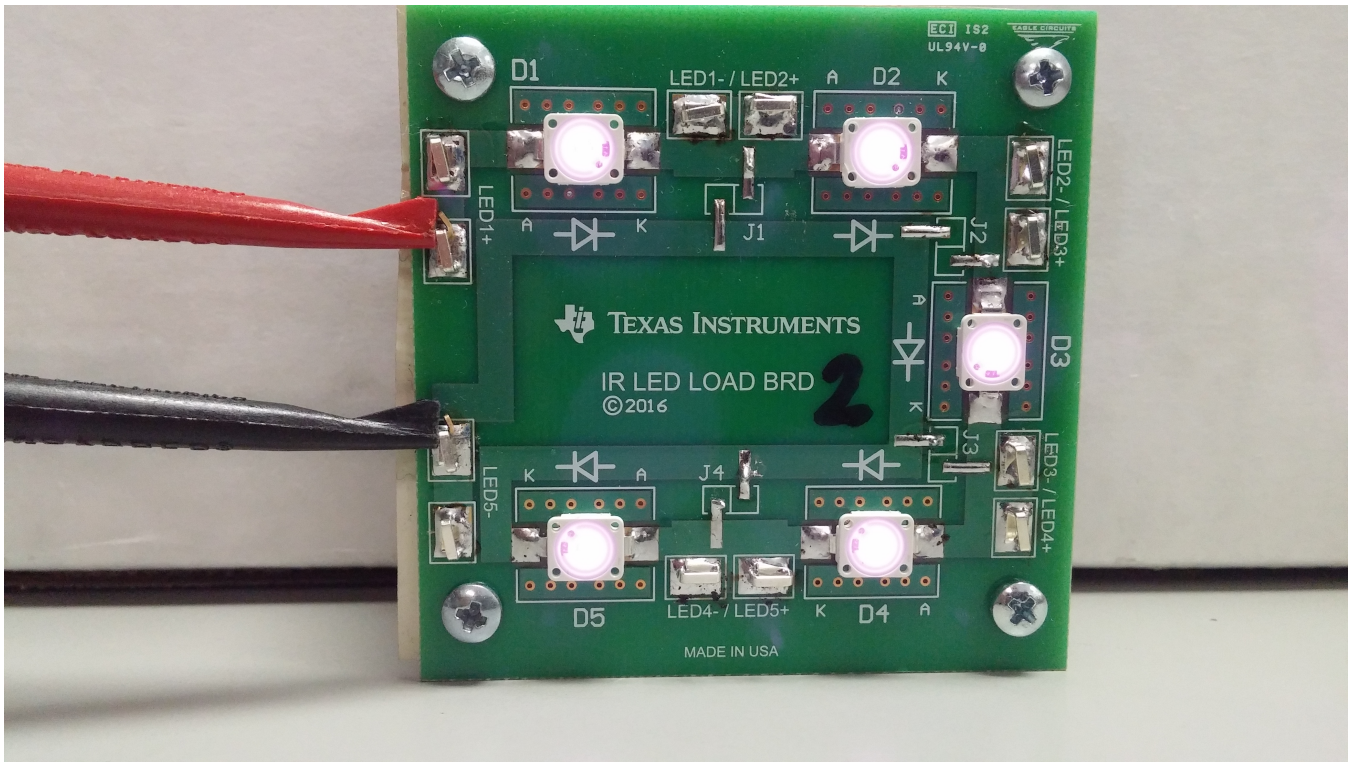

Figure 9. IR LEDs at Full Current

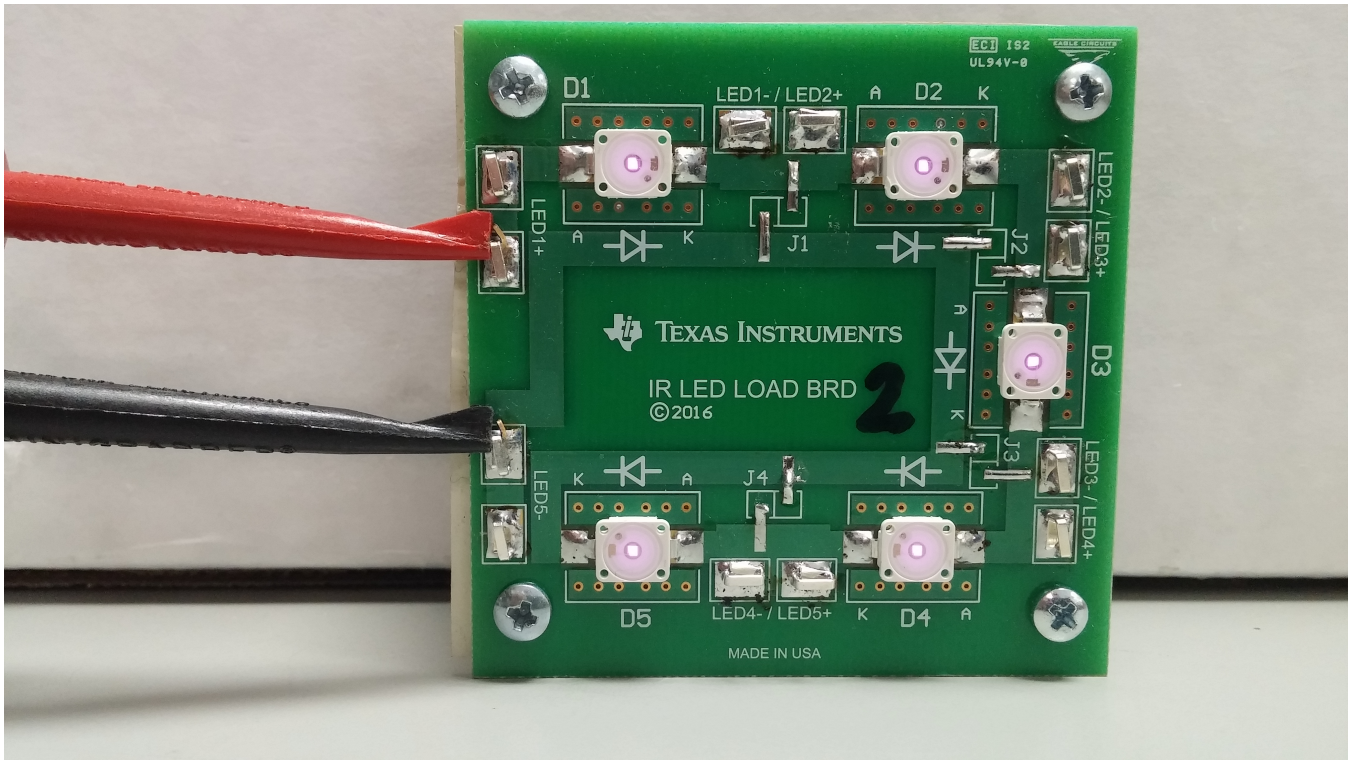

Figure 10. IR LEDs Dimmed to 13:1

4.2.3 Combination of Analog and PWM Pin Dimming

To extend the dimming range, a combination of analog and PWM dimming may be used. For this data, analog dimming is used to achieve 13:1 dimming down to 77 mA (Figure 11), and a 1.5-kHz PWM pin dimming is used to further reduce LED current down to 0.48 mA at 1% duty cycle (Figure 12). For this setup, the following components are not populated:

1. R2, R3, R4, R7, R9
2. U2, Q1A, D6

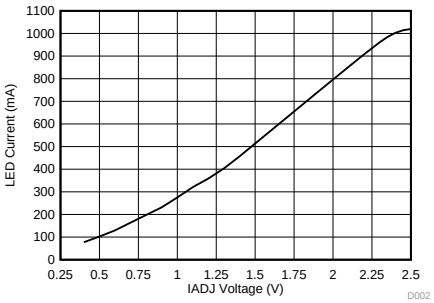

Figure 11. LED Current versus IADJ Voltage (IADJ = 0.4 to 2.5 V)

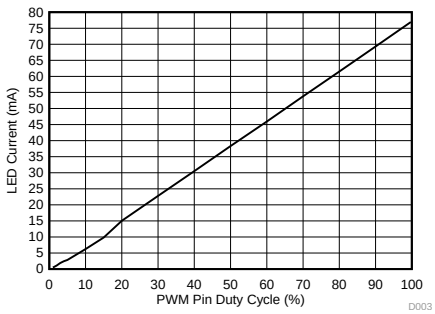

Figure 12. LED Current versus PWM Pin Duty Cycle

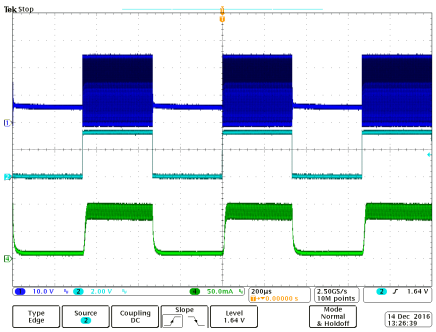

Figure 13. 50% Duty Cycle (IADJ = 0.4 V); Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (50 mA/div)

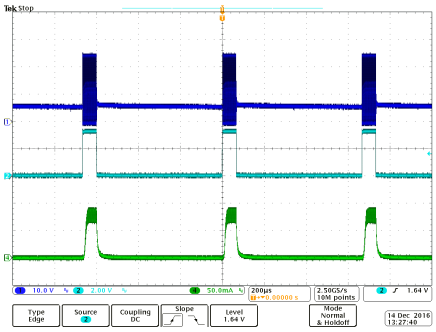

Figure 14. 10% Duty Cycle (IADJ = 0.4 V); Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (50 mA/div)

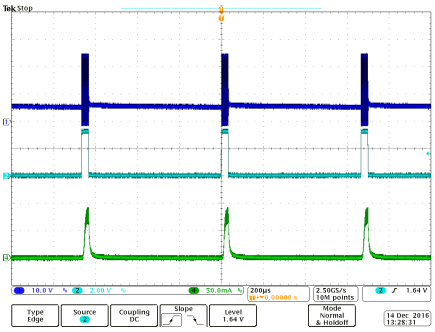

Figure 15. 5% Duty Cycle (IADJ = 0.4 V); Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (50 mA/div)

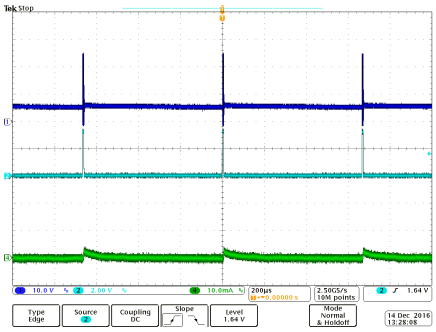

Figure 16. 1% Duty Cycle (IADJ = 0.4 V); Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (10 mA/div)

4.2.4 PWM Pin Dimming

For a wide dimming range without analog dimming PWM, dimming alone may be used. For this TI Design, a PWM frequency of 1.5 kHz is used. For this data to obtain maximum linearity at low duty cycles, the output capacitor has been removed for the fastest rise and fall times possible in the LED current. For this setup, the following components are not populated:

1. R2, R3, R4, R7, R9
2. U2, Q1A, D6
3. C9

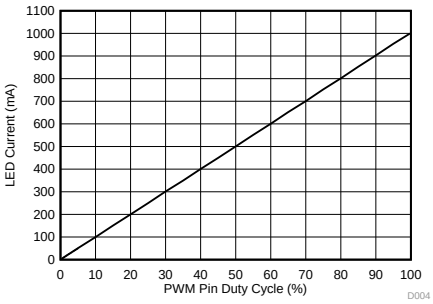

Figure 17. LED Current versus PWM Duty Cycle (0% to 100%)

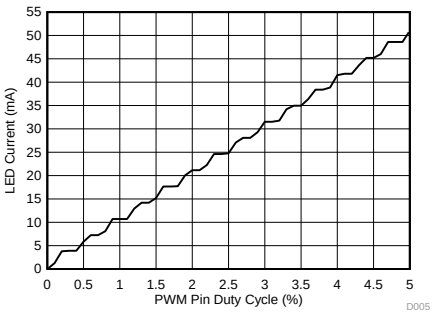

Figure 18. LED Current versus PWM Duty Cycle (0% to 5%)

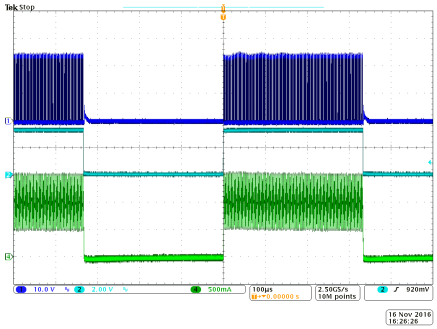

Figure 19. 50% Duty Cycle; Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (500 mA/div)

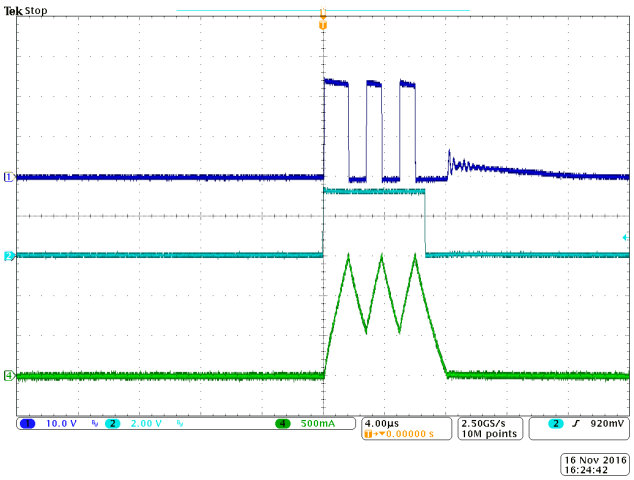

Figure 20. 1% Duty Cycle; Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (500 mA/div)

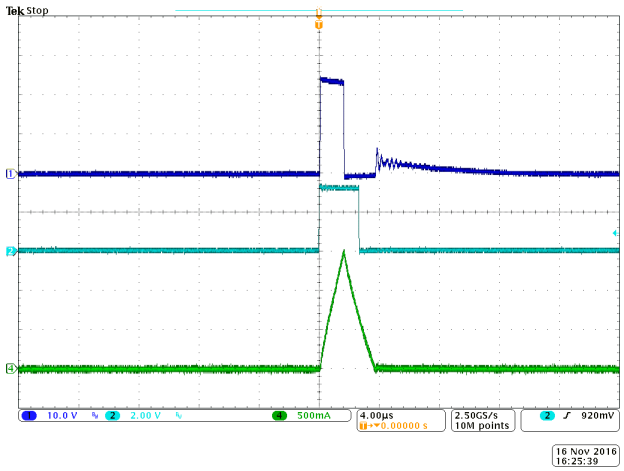

Figure 21. 0.4% Duty Cycle; Ch1: V_{DRN}, Ch2: V_{PWM} Ch4: I_{LED} (500 mA/div)

4.2.5 Shunt FET PWM Dimming

For a wide dimming range at high PWM frequencies, shunt FET dimming may be used. For this TI Design, a PWM frequency of 30 kHz is used. For this data, the output capacitor has been removed to avoid shunt FET damage due to the high charge and discharge currents caused by the capacitor (very high dv/dt). For this setup, the following components are not populated:

1. R1, R2
2. C9

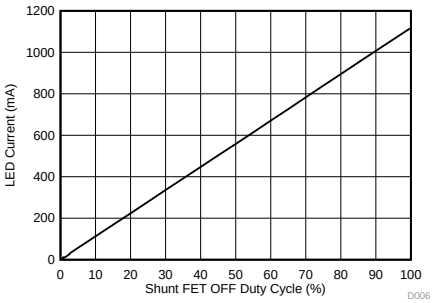

Figure 22. LED Current versus Shunt FET OFF Duty Cycle

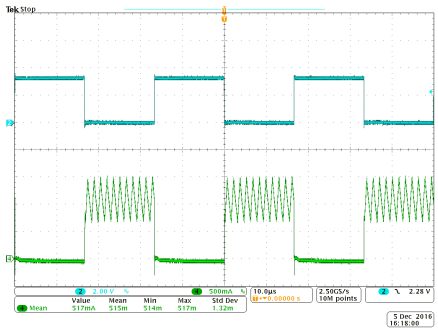

Figure 23. 50% Duty Cycle; Ch2: V_{TP4} Ch4: I_{LED} (500 mA/div)

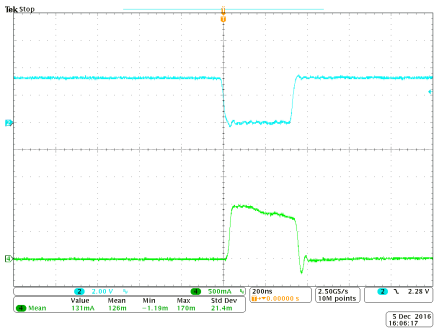

Figure 24. 1% Duty Cycle; Ch2: V_{TP4} Ch4: I_{LED} (500 mA/div)

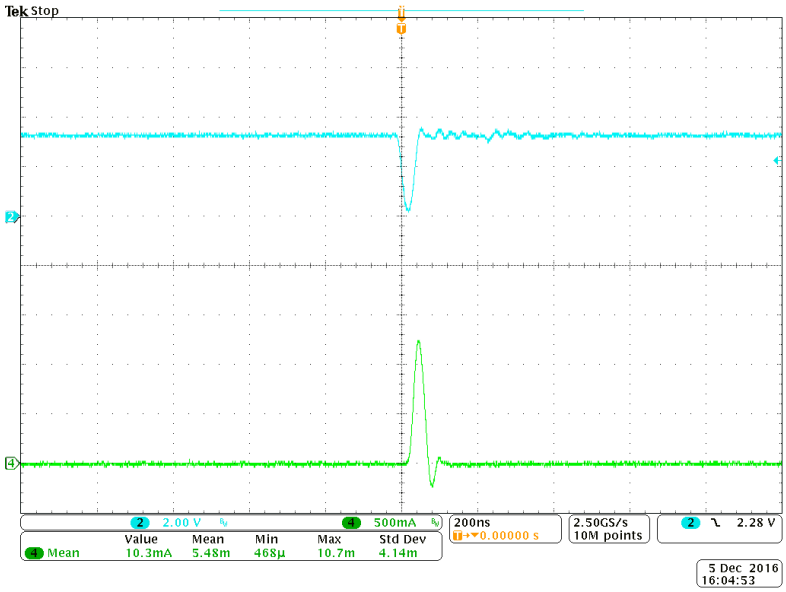

Figure 25. 0.1% Duty Cycle; Ch2: V_{TP4} Ch4: I_{LED} (500 mA/div)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at PMP15022.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP15022.

5.3 PCB Layout Recommendations

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. By carefully considering the PCB layout requirements, a designer can avoid noise issues, device misbehavior, as well as reducing EMI. Figure 26 shows a generic layout and the associated current loops.

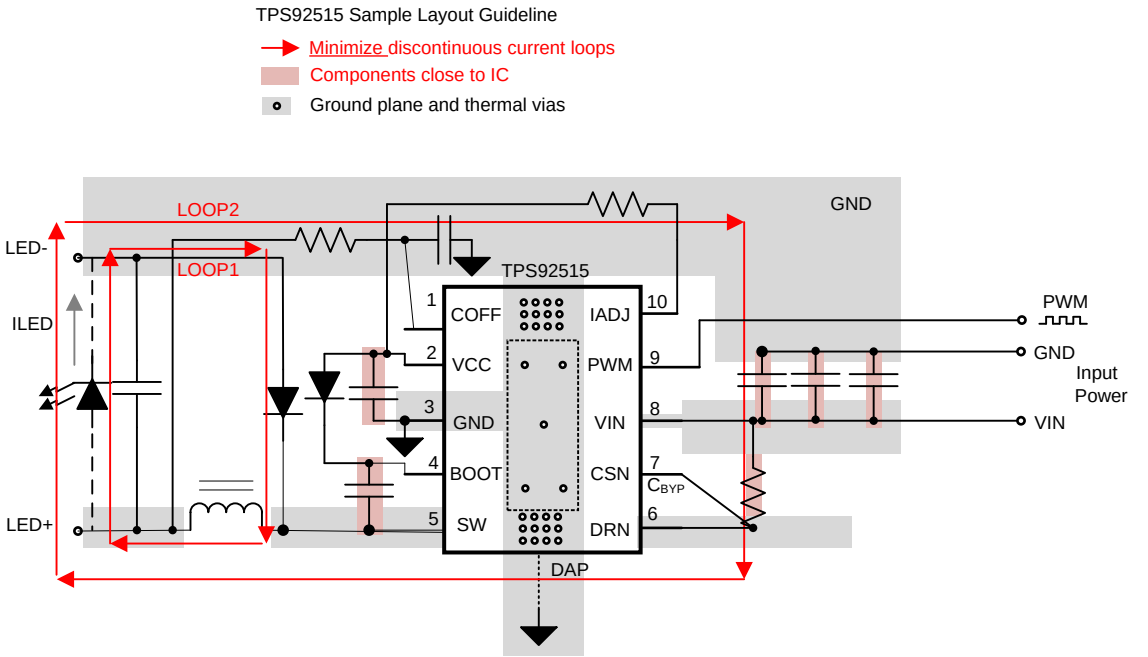

Figure 26. PCB Layout Example

Follow these simple guidelines to maximize noise rejection and minimize the generation of EMI within this TI Design:

- Discontinuous currents are the type of current most likely to generate EMI; therefore, ensure to take care when routing these paths:
  - The main path for discontinuous current contains the input capacitor (C1, C2, C3), the recirculating diode (D1), the internal MOSFET (DRN pin to SW pin), and the sense resistor (R5) shown as LOOP2. Make LOOP2 as small as possible.
  - Make the connections between all three components short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1, and the SW pin connect, as LOOP1 shows) must only be large enough to connect the components without excessive heating from the current it carries.

- The IADJ, COFF, CSN, and VIN pins are all high-impedance control inputs; therefore, minimize the loops containing these high impedance nodes. The most sensitive loop contains the sense resistor (R5). Place the sense resistor as close as possible to the CSN and VIN pins to maximize noise rejection.
- Place the off-time capacitor (C6) close to the COFF and GND pins to maximize noise rejection.
- If external resistors are used to bias the IADJ pin, these resistors should also be placed close to the IADJ and GND pins and can then be decoupled with a small capacitor.
- In some applications the LED load can be far away from the device, several inches or more, or on a separate PCB connected by a wiring harness. When an output capacitor is used (such as C9) and the LED load is large or separated from the main converter, the output capacitor must be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
- The TPS92515 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction-to-ambient thermal resistance varies with application. The most significant variables are the area of copper in the PCB and the number of vias under the exposed pad. The integrity of the solder connection from the device exposed pad to the PCB is critical. Excessive voids greatly decrease the thermal dissipation capacity.

5.3.1 Thermal Scan

Figure 27 shows a thermal scan of the board running at a room temperature (≈25°C) with no air-flow. Table 2 lists measured temperatures of key components.

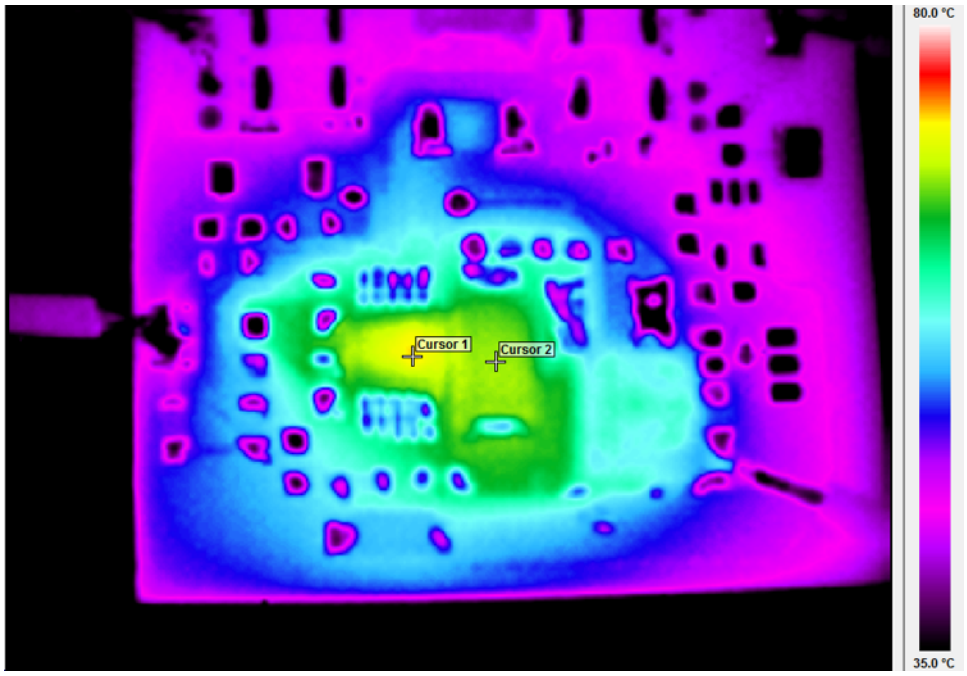

Figure 27. Thermal Scan—Top-View: V_{IN} = 24 V, Five LEDs, I_{LED} = 1 A

Table 2. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	U1	73.2
2	D1	69.1

5.3.2 Layout Prints

To download the layer plots, see the design files at PMP15022.

5.4 Altium Project

To download the Altium project files, see the design files at PMP15022.

5.5 Gerber Files

To download the Gerber files, see the design files at PMP15022.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP15022.

6 References

1. Texas Instruments, *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability*, TPS92515/TPS92515-Q1 and TPS92515HV/TPS92515HV-Q1 Datasheet (SLUSBZ6)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265