TI Designs

Automotive Off-Battery Processor Power Reference Design for ADAS and Infotainment

Description

The TIDA-00805 reference design is an off-battery automotive power solution targeting processors in advanced driver assistance systems (ADAS) like surround view, front camera and driver monitoring, as well as infotainment systems such as cluster and head unit. The design operates directly from a 3.9 to 40V car battery input and provides all supply rails for the application processor, Controller Area Network (CAN), input/output interfaces and double data rate (DDR) memory.

Resources

TIDA-00805	Design Folder
LM53635-Q1	Product Folder
TPS22965-Q1	Product Folder
TPS52100-Q1	Product Folder
TPS61240-Q1	Product Folder
TPS65917-Q1	Product Folder

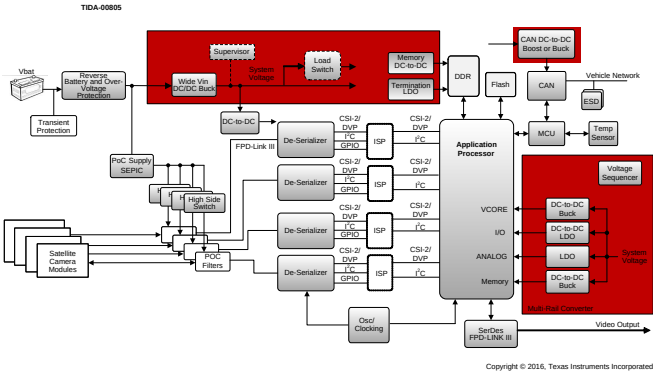
TI E2E™ Community — ASK Our E2E Experts

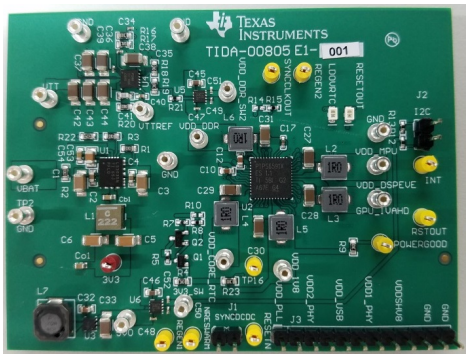
Features

- Supports Start-Stop, Cold and Warm Cranking Down to 3.9 V
- Supports Modern Processors Sequencing Needs Without Further Logic
- Provides all power supply rails for TDA2x/TDA2Ex and DRA72x/DRA74x/DRA75x application processors
- Supports Power for Peripherals
- Small Form Factor
- Small Solution Size
- Low System-Cost Solution

Applications

- Advanced Driver Assistance Systems (ADAS)
  - Front Camera
  - Driver Monitoring
  - Surround View
- Infotainment and Cluster





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Overview

1.1 System Description

This reference design is an automotive off-battery processor power solution for Advanced Driver Assistant Systems (ADAS) or infotainment systems such as cluster and head unit. It takes an input connected to the car battery and provides output supplies to the application processor. The design uses the LM53635-Q1 synchronous buck converter to regulate a stable 3.3 V output from the car battery. The LM53635-Q1 supports a wide range of input voltages from 3.9 V to 40 V, allowing support of start-stop, cold and warm cranking conditions down to 3.9 V. An integrated power management device, TPS65917-Q1, integrates five SMPSs and five LDOs to provide supply voltages for system functions and supplies point-of-load power to the application processor (such as TDA2x/TDA2Ex and DRA72x/DRA74x/DRA75x), DDR memory and other system components. Included in the design is a 4 A load switch (TPS22965-Q1) to provide a sequenced 3.3 V to the processor. Also included is a linear voltage regulator (TPS51200-Q1) for active DDR memory termination.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Preregulator	Provides a regulated 3.3-V rail at 3.0 A maximum from a battery input between 3.9 V and 40 V	See section Section 1.4.1
Load Switch	Turns on to provide I/O voltage upon a signal from the PMIC (up to 4 A)	See section Section 1.4.2
DDR Termination	Provides appropriate termination voltage for the selected DDR-voltage (SMPS5 of PMIC) at 1 A	See section Section 1.4.3
Boost Converter	Provides a regulated 5-V rail at 250 mA for USB and CAN operations	See section Section 1.4.4
Power Management IC (PMIC)	Provides various output voltages and digital signals in the correct order with the correct timing	See section Section 1.4.5

1.3 Block Diagram

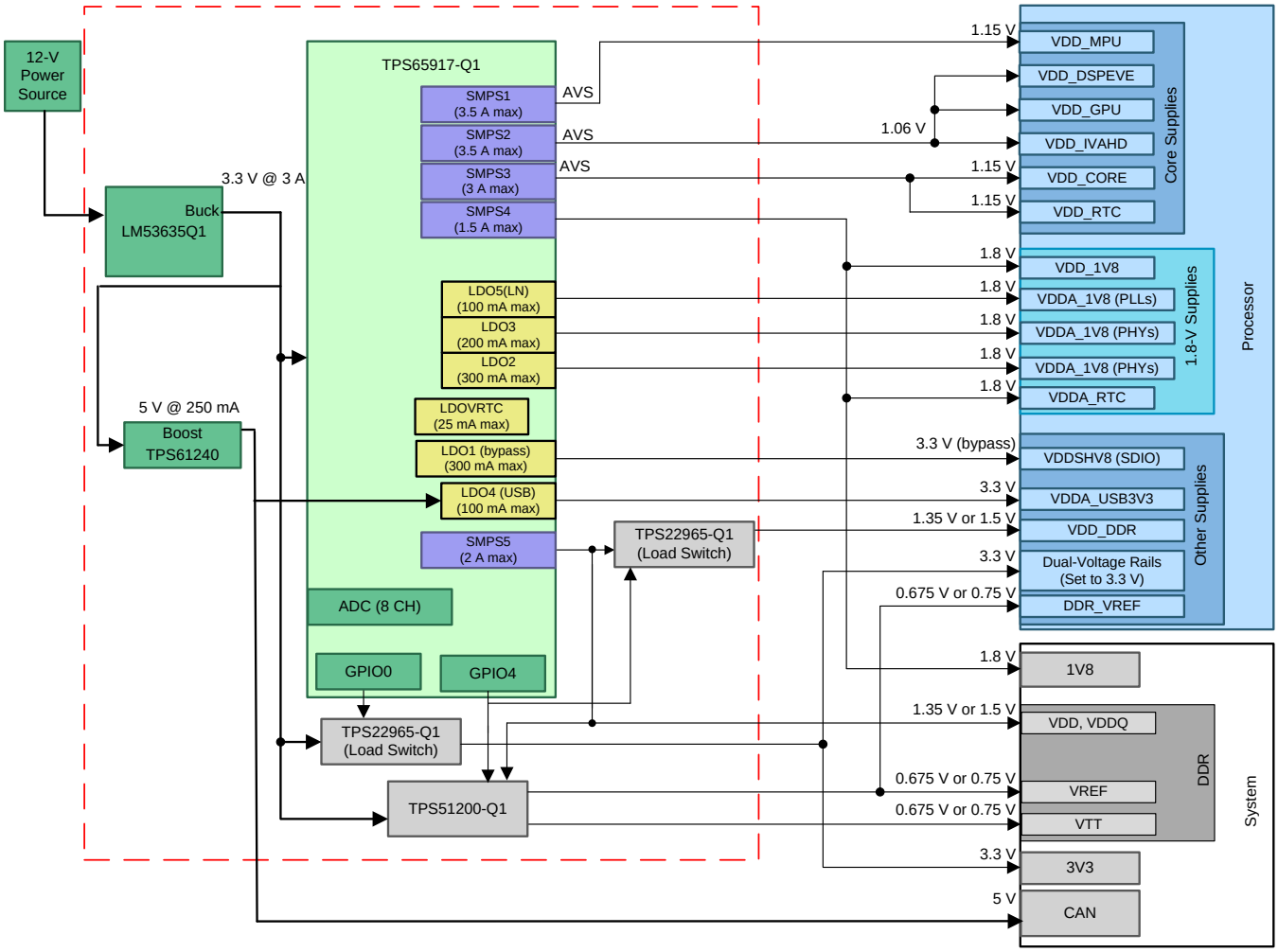


Figure 1. Block Diagram

1.4 Highlighted Products

This reference design features the following devices, see corresponding datasheets for additional information:

- LM53635-Q1
- TPS22965-Q1
- TPS51200-Q1
- TPS61240-Q1
- TPS65917-Q1

For more information on each of these devices, see the respective product folders at www.ti.com.

1.4.1 LM53635-Q1 3.5 A, 36 V Synchronous Step-Down DC-to-DC Converter

The LM53635-Q1 is the preregulator for this design to provide a stable 3.3-V output from the nominal 12-V battery input (Figure 2).

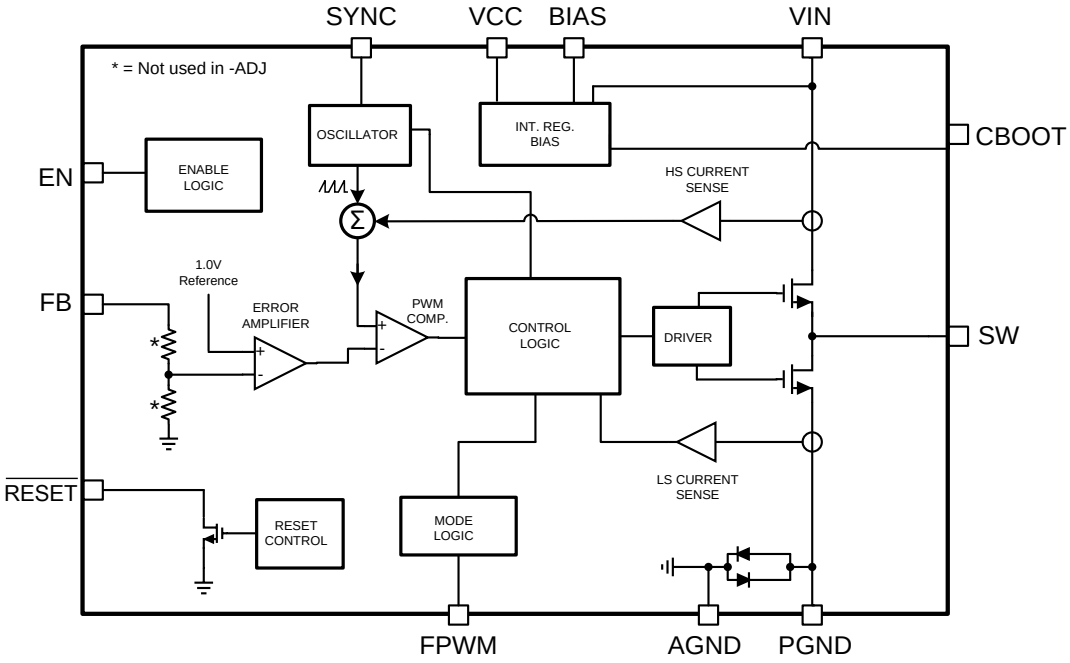


Figure 2. LM53635-Q1 Block Diagram

- AEC-Q100 automotive qualified
- 15-μA quiescent current at no load (typical) with 3.3-V output
- Low EMI and switch noise
- Spread spectrum option
- External frequency synchronization
- $\overline{\text{RESET}}$ output with internal filter and 3-ms release timer
- Pin-selectable forced PWM mode
- Built-in compensation, soft start, current limit, thermal shutdown, and UVLO
- 0.6-V dropout at 3.5 A at 105°C T_A
- ±1% output voltage tolerance (–40°C to 125°C T_J)
- Available with fixed 5-V, 3.3-V, or adjustable output

1.4.2 TPS22965-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch

The TPS22965-Q1 is a small, ultra-low RON, single-channel load switch with controlled turnon (Figure 3).

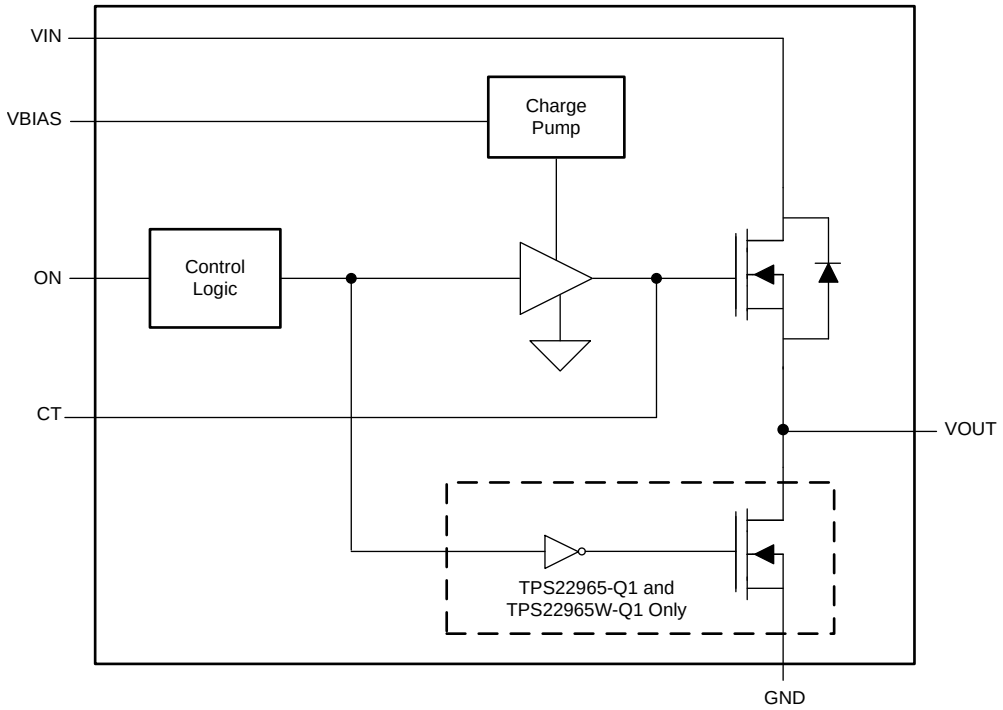


Figure 3. TPS22965-Q1 Block Diagram

- AEC-Q100 qualified
- Integrated single-channel load switch
- Input voltage range: 0.8 V to 5.5 V
- Ultra-low on resistance (RON)
- 4-A maximum continuous switch current
- Low quiescent current (50 µA)
- Low control input threshold enables use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Configurable rise time
- Quick output discharge (QOD)

1.4.3 TPS51200-Q1 Sink and Source DDR Termination Regulator

The TPS51200-Q1 device is a sink and source DDR-termination regulator specifically designed for low-input voltage, low-cost, low-noise systems where space is a key consideration. Figure 4 shows a simplified schematic of the TPS51200-Q1 device.

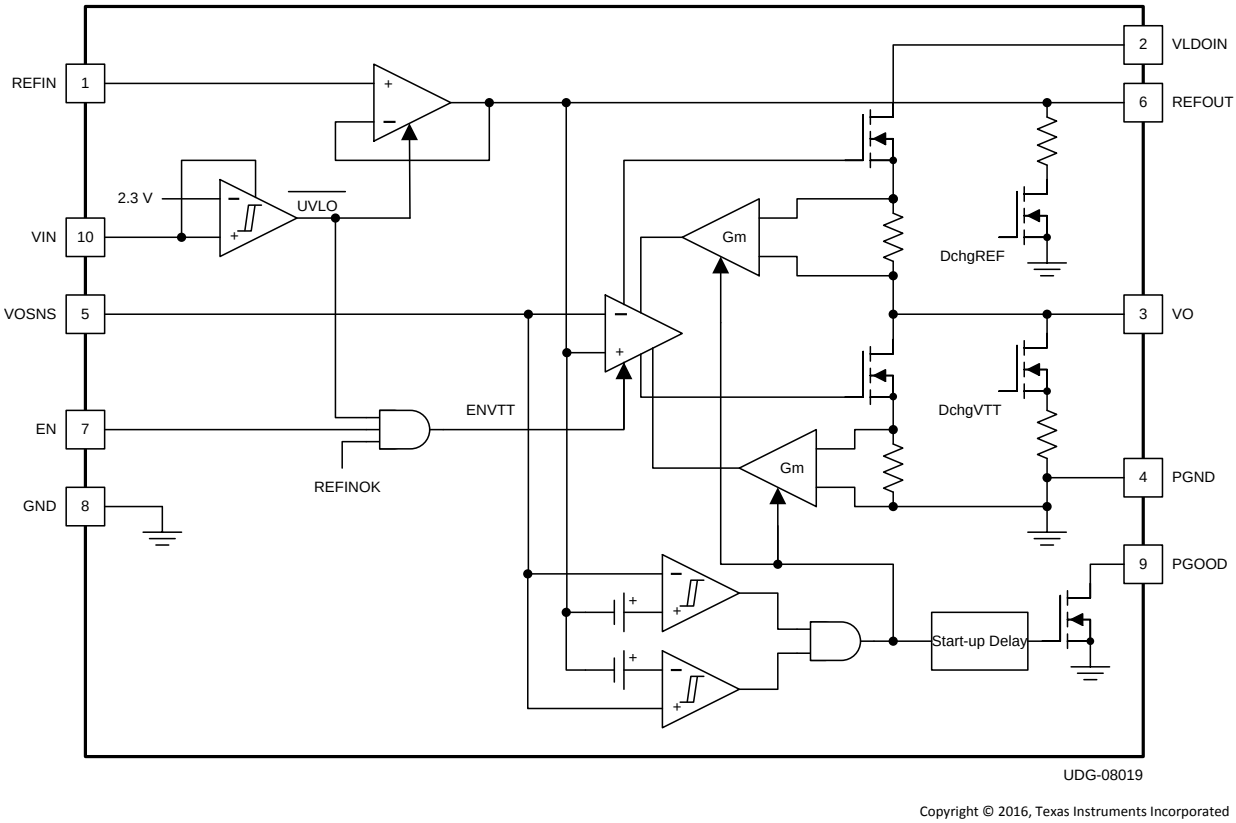


Figure 4. TPS51200-Q1 Block Diagram

- AEC-Q100 qualified
- Input voltage: supports 2.5-V and 3.3-V rails
- VLDOIN voltage range: 1.1 V to 3.5 V
- Sink/Source termination regulator includes droop compensation
- Requires minimum output capacitance of 20 µF (typically 3 × 10-µF MLCCs) for memory termination applications (DDR)
- PGOOD to monitor output regulation
- EN input
- REFIN input allows for flexible input tracking either directly or through resistor-divider
- Remote sensing (VOSNS)
- ±10-mA buffered reference (REFOUT)
- Built-in soft start, UVLO and OCL
- Thermal Shutdown
- Meets DDR and DDR2 JEDEC specifications; supports DDR3 and low-power DDR3 and DDR4 VTT applications

1.4.4 TPS61240-Q1 3.5-MHz Synchronous Boost Converter

The TPS61240-Q1 is a high-efficiency synchronous step-up DC-to-DC converter has a high-switching frequency, 3.5MHz, and is able to support output currents up to 450 mA (Figure 5).

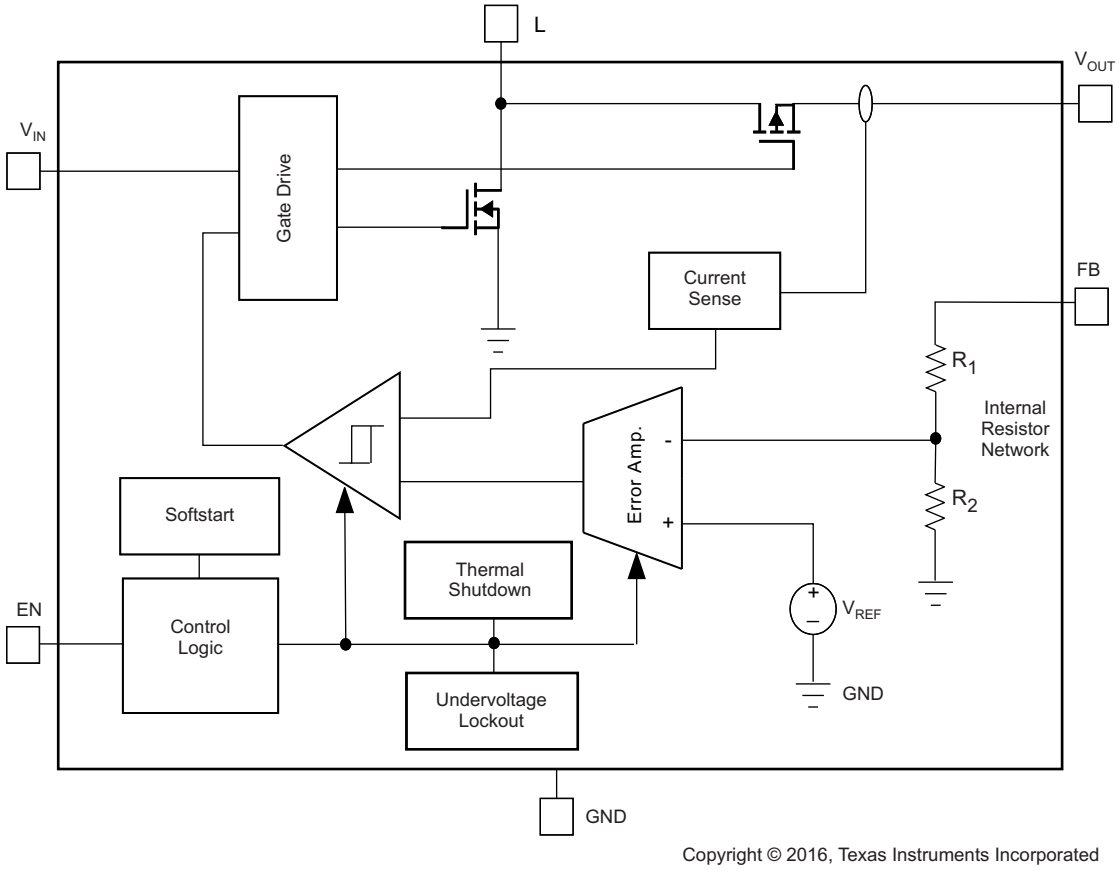


Figure 5. TPS61240-Q1 Block Diagram

- Qualified for automotive applications
- Efficiency > 90% at nominal operating conditions
- Total DC-output voltage accuracy 5.0 V ±2%
- Typical 30-µA quiescent current
- Wide V_{IN} range from 2.3 V to 5.5 V
- Output current up to 450 mA
- Automatic PFM and PWM mode transition
- Low-ripple power save mode for improved efficiency at light loads
- Internal soft start, 250-µs typical start-up time
- 3.5-MHz typical operating frequency
- Load disconnect during shutdown
- Current overload and thermal shutdown protection
- Only three surface-mount external components required (one MLCC inductor, two ceramic capacitors)

1.4.5 TPS65917-Q1 Power Management Unit for ADAS and Infotainment Application Processor

The TPS65917-Q1 device is an integrated power-management integrated circuit (PMIC) for automotive applications optimized for the TDA2x/TDA2Ex processors, see Figure 6.

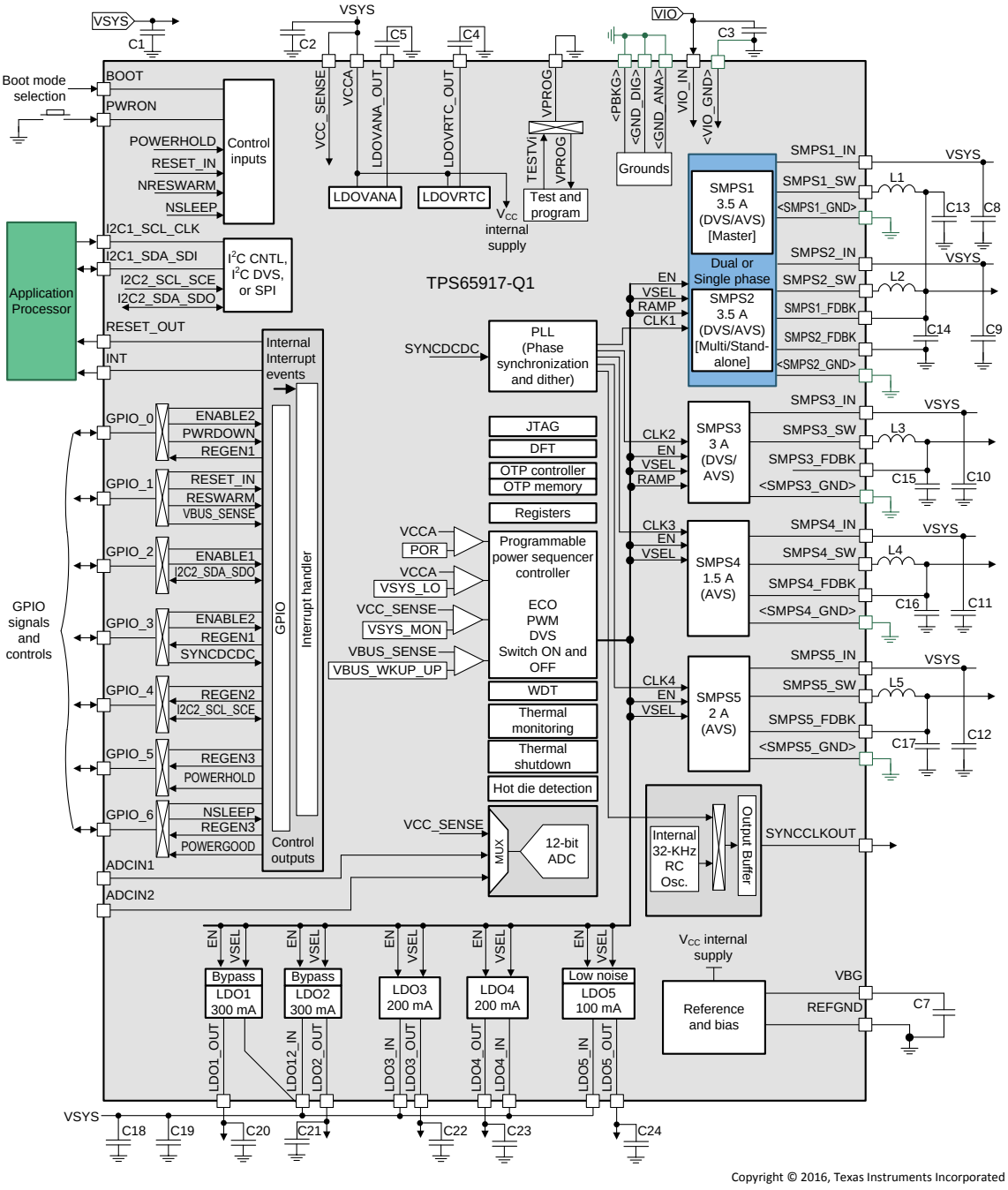


Figure 6. TPS65917-Q1 Block Diagram

- AEC-Q100 automotive qualified
- System voltage range from 3.135 V to 5.25 V
- Five step-down switched-mode power supply (SMPS) regulators
  - Two 0.7 V to 3.3 V at 3.5 A (10-mV or 20-mV steps)
    - Dynamic voltage scaling (DVS) control
    - Ability to combine regulators into a 7-A dual-phase regulator

    - Differential remote sensing (output and ground) in dual-phase configuration
  - One 0.7 V to 3.3 V at 3 A (10-mV or 20-mV steps)
    - Dynamic voltage scaling (DVS) control
  - One 0.7 V to 3.3 V at 2 A (10-mV or 20-mV steps)
  - One 0.7 V to 3.3 V at 1.5 A (10-mV or 20-mV steps)
  - Output current measurement in 3.5-A and 3-A SMPS regulators
  - Hardware- and software-controlled Eco-mode™ up to 5 mA with 15-uA quiescent current
  - 100% Duty Cycle for Lowest Dropout
  - Short-circuit protection
  - Power-good indication (voltage and overcurrent indication)
  - Internal soft-start for in-rush current limitation
  - Ability to synchronize SMPS to external clock with phase synchronization
- Five low-dropout (LDO) linear regulators (50-mV steps)
  - Two 0.9 V to 3.3 V at 300 mA with a pre-regulated supply
    - With bypass mode for load switch functionality
  - One low-noise LDO 0.9 V to 3.3 V at up to 100 mA (Low-noise performance up to 50 mA)
  - Two 0.9 V to 3.3 V at 200 mA
  - Two additional LDOs for Power-management Integrated Circuit (PMIC) internal use
  - Short-circuit protection
- Overcurrent alarm with programmable time window and current thresholds 12-Bit sigma-delta general-purpose ADC (GPADC) with 8 input channels (2 external)
- Low-power consumption
- Thermal monitoring
  - High temperature warning
  - Thermal shutdown
- Configurable power-up and power-down sequences (OTP)
- Three digital output signals mulitplexed with GPIO that can be Included in the startup sequence

2 System Design Theory

2.1 Pre-Regulation with LM53635-Q1 3.5A Step-Down DC-to-DC Converter

The LM53635-Q1 was chosen as the pre-regulator for this design to provide a stable 3.3-V output from the nominal 12-V battery input (Figure 2). Its wide input voltage range makes it a good fit for automotive applications as battery voltage can dip low during start-stop, cold or warm cranking conditions faced in automotive applications. The device has low IQ requirements and can survive supply drops due to cranking events down to 3.9V making it suitable as a pre-regulator. The innovative architecture allows this device to regulate a 3.3-V output from an input voltage of only 3.55 V at lower current requirements. An input voltage range up to 36 V, with transient tolerance up to 42 V, eases input surge protection design. An open-drain reset output, with built-in filtering and delay, provides a true indication of system status. This feature negates the requirement for an additional supervisory component, saving cost and board space.

2.2 Power Management Unit for TDA2x/TDA2Ex and DRA72x/DRA74x/DRA75x Processors

The TPS65917-Q1 device is an integrated power-management integrated circuit (PMIC) for automotive applications optimized for the TDA2x/TDA2Ex and DRA72x/DRA74x/DRA75x processors, see Figure 6. The device was chosen because it integrates five configurable step-down converters with up to 3.5 A of output current for memory, processor core, input-output (I/O), or pre-regulation of LDOs suitable for the application processor. All of these step-down converters can synchronize to an external clock source between 1.7 Mhz and 2.7 MHz, or an internal fall back clock at 2.2 MHz. The TPS65917-Q1 device

contains five low dropout (LDO) regulators for external use. All LDOs and switched-mode power supply (SMPS) converters can be controlled by the I^2C interface, or by power request signals. In addition, SMPS1, SMPS2 and SMPS3 support dynamic voltage scaling through the I^2C interface. General-purpose input-output (GPIO) functionality is available and three GPIOs can be configured as part of the power-up sequence to control external resources. Power request signals enable power mode control for power optimization.

2.3 Load Switch Rail with TPS22965-Q1

The TPS22965-Q1 is a small, ultra-low RON, single channel load switch with controlled turnon (Figure 3). The device contains an N-channel MOSFET that can operate over an input-voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 4 A. The VOUT rise time is configurable so that inrush current may be reduced. For quick output discharge when the switch is turned off, the TPS22965-Q1 includes a 225-Ω on-chip load resistor. This device has been selected for its size, cost, and performance. Selection of the device is also because it matches the following key criteria:

- Soft-start feature to limit inrush-currents
- Active discharge to maintain the power-down sequence demanded by the controller
- Low RDSon for the highest efficiency and lowest-voltage drop

2.4 DDR-Termination with TPS51200-Q1

The TPS51200-Q1 device is a sink and source DDR-termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration. The device supports a remote-sensing function and all power requirements for DDR3, and Low Power DDR3 VTT bus termination. In this design, the options are predefined by the PMIC, which supports DDR3 and DDR3LV. The part was chosen for cost and space reasons and because it is easy-to-use. Figure 4 shows a simplified schematic of the TPS51200-Q1 device.

2.5 TPS61240-Q1 for USB and CAN System Operations

The TPS61240-Q1 is a high-efficiency synchronous step-up DC-to-DC converter has a high-switching frequency, 3.5MHz, and is able to support output currents up to 450 mA (Figure 5). The high-switching frequency avoids frequency bands in which noise would be disruptive (for example, AM broadcast and vehicle motion and position monitors). With an input voltage range of 2.3 V to 5.5 V the device can regulate a steady 5-V output, which this design uses to power LDO4 for USB and system CAN operations. During light loads, the device automatically pulse skips allowing maximum efficiency at lowest-quiescent currents. In shutdown mode, the current consumption is reduced to less than 1 µA. The operating temperature range of the TPS61240-Q1 boost converter used in this design is –40ºC to 85 ºC. If application is out of this temperature range, the design must use a different boost converter.

3 Getting Started

3.1 Hardware

TIDA-00805 was optimized for size by packing the automotive battery to point-of-load power solution in a 1.99 in. by 3 in. printed circuit board with necessary power rails and signals broken out for proper evaluation. See Figure 7 for the respective connections. Additional test points are labeled on the board.

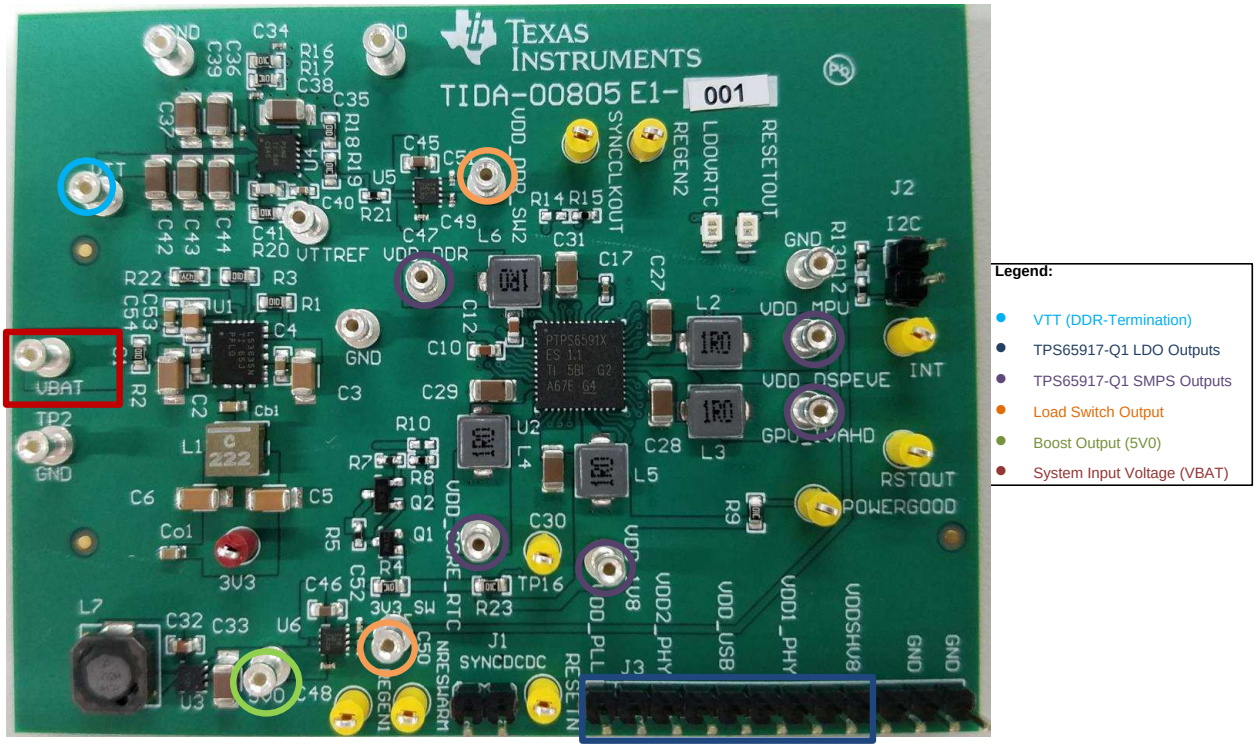


Figure 7. Hardware Connectors and Test Points

3.2 Hardware Setup

To begin using the hardware, a power supply with sufficient output power is required across the input of the preregulator (LM53635-Q1), TP1 (VBAT), and TP2 (GND). A load can be applied to the PMIC switch-mode power supplies or LDOs using the turrets and headers available on the board. A summary of the important outputs are outlined in Table 2. The pre regulator is configured for 3.3-V output voltage and 3-A maximum-load current. The output rails of the PMIC are configured at different voltages outlined in Table 2.

Table 2. Vout Configuration Descriptions

Designator	Vout (V)	Description
3V3	3.3	Pre Regulator output
VDD_MPU	1.15	TP23. SMPS1
VDD DSPEVE,GPU,IVAHD	1.06	TP24, SMPS2
VDD CORE RTC	1.15	TP25, SMPS3
VDD 1V8	1.8	TP26, SMPS4
VDD DDR	1.35	TP27, SMPS5
VDD SHV8	3.3	LDO1
VDD1 PHYs	1.8	LDO2
VDD2 PHYs	1.8	LDO3
VDD USB	3.3	LDO4

Table 2. Vout Configuration Descriptions (continued)

Designator	Vout (V)	Description
VDD PLL	1.8	LDO5
5V0	5	TP30
VDD DDR SW2	1.35	TP33
3V3_SW(1)	3.3	TP34
VTT	0.75	TP32
VTTREF	0.65	TP31

(1) The 3V3_SW is the output of the load switch and is sequenced. Take care not to confuse 3V3_SW with the 3V3 test point at the output of the preregulator, which is always on.

3.3 Configurable Components

A summary of the configurable components are as follows:

- Change the DDR-Voltage from 1.35 V (for DDR3L) to 1.5 V for DDR3 by removing R15 and installing R14
- Change 3V3_SW supply to VIO_IN by removing R8 and installing R10

To further optimize this design for size, the 2.5 mm by 2.0 mm, TFM252012ALMA-1R0MT, TDK power inductor for automotive systems can be used for the TPS65917-Q1 SMPS output inductors.

3.4 Power Up

The design configuration powers up the pre-regulato, which supplies the PMIC, a load switch, DDR termination, and a boost converter. The system is enabled automatically when power is supplied.

To support Suspend-to-RAM, a switched version of the preregulators 3.3-V output that comes up before GPIO4 is provided by populating R8 and leaving R10 unpopulated. VCCA must be the first supply to the PMIC, and VIO_IN must come after VCCA is stable. Since GPIO4 is on the VIO domain, VIO_IN must be supplied before GPIO4 is enabled in the power sequence. Since VIO_IN is 3.3 V, then the switch configuration in Figure 8 enabled by SMPS4 sequences VIO_IN after VCCA, but before GPIO_4.

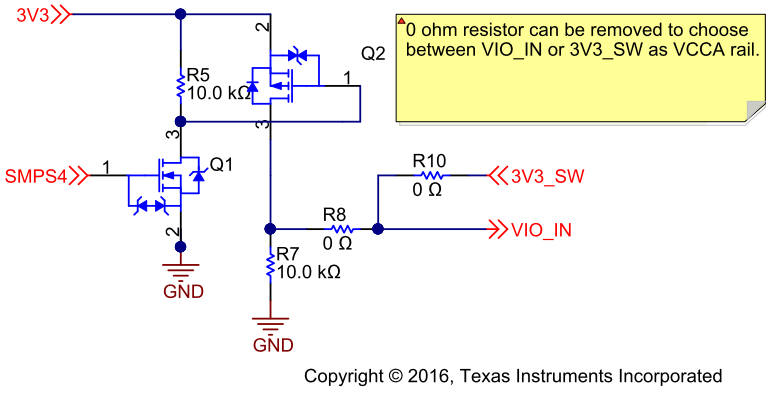


Figure 8. Power Up Switch Configuration

The BOOT pin on the TPS65917-Q1 PMIC can be configured using two R14 and R15 footprints depending on the voltage requirements (Table 3). Only one resistor should be populated at any given time. On the design, the boot pin is pulled low by R15 that sets the SMPS and LDO outputs.

Table 3. Boot Pin Configurations

	BOOT= 0	BOOT =1	UNIT
SMSP1	1.15		V
SMSP2	1.06		V
SMSP3	1.15		V
SMPS4	1.8		V
SMSP5	1.35	1.5	V

The boot sequence of the PMIC starts as soon as power is applied to the preregulator and the 3V3 output becomes stable. As soon the output voltage reaches 95% of its nominal value, the RESETN signal of the preregulator RESETN signal sets the GPIO_5 (POWERHOLD) signal of the PMIC high, which turns on the PMIC. All pre-configured rails come up in the correct order as outlined in TPS65917 Users Guide to Power DRA7xx and TDA2x/TDA2Ex (SLVUAJ1). The VTT, VDD_DDR_SW2, and 3V3_SW are also sequenced using REGEN outputs available via the GPIOs of the PMIC. At the end of the sequence, which takes about 10 ms, D1 or RESET_OUT LED illuminates. This pin on the PMIC has a signal that can be used to release the reset of the processor for proper operation since all rails have come up and are stable.

3.5 Power Down

The power-up and power-down controller is configurable and programmable through OTP memory. Refer to TPS65917 Users Guide to Power DRA7xx and TDA2x/TDA2Ex (SLVUAJ1) for a detailed description of the predefined power sequences (OFF2ACT, ACT2OFF, SLP2OFF, ACT2SLP, and SLP2ACT). When power is removed, GPIO_5 (POWERHOLD) is set low by the RESETN output of the preregulators starting the power down sequence. To ensure proper power-down sequencing, this sequence should be completed before the PMIC supply (VCCA) reaches 2.75 V.

3.6 PMIC Switching

The PMIC switches its SMPSs at 2.2 MHz, the frequency of the internal clock of the IC. An external clock in the range of 1.7 MHz and 2.7 MHz may be applied using the SYNCDCDC jumper available. If the clock signal has a high level of 1.8 V and is within the frequency range, the SMPSs will synchronize with the clock signal. Otherwise, it defaults to the 2.2-MHz clock.

All LDOs and SMPSs can be controlled by the I^2C interface available through the J2 jumper onboard. In addition, voltage scaling registers allow the SMPSs to transition to different voltages via the I^2C interface. Using either a proprietary solution or the USB2ANY-adapter (HPA665-001) and a graphical user interface (GUI), one can read or write to PMIC registers. This gives the designer flexibility to adjust voltages. For the default operation and power up, no software is required.

4 Testing and Results

4.1 Test Setup

The following sections show the test setups for the corresponding tests and test data.

4.1.1 Load Regulation

Figure 9 shows the test setup to test how well each voltage rail operates under loading. A DC-power supply set to 14 V is the input power to the TIDA-00805 board. Place a voltmeter across the output connecters of each output and the electronic load in use has an internal Ammeter to monitor the load current. Apply the electronic load at the output connectors of each voltage rail. Using an oscilloscope, capture VOUT, Load Current, and the Switching Node (PH) waveforms.

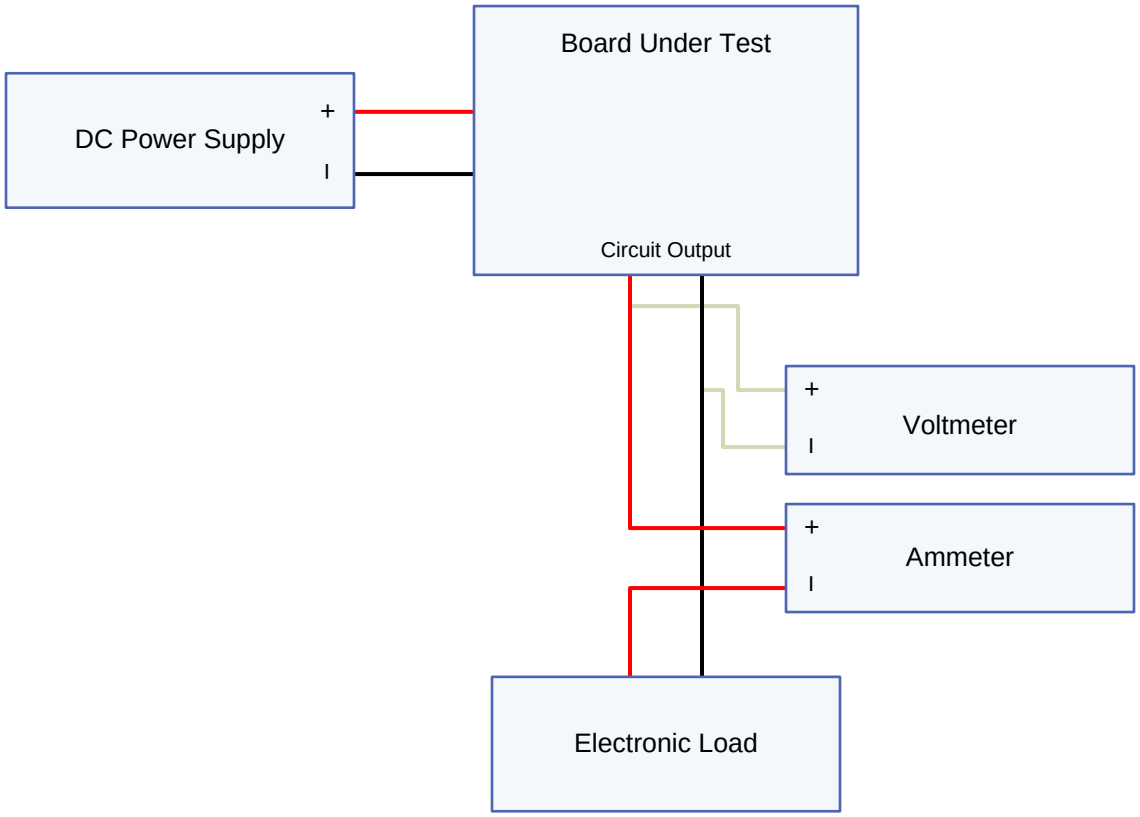


Figure 9. Load Regulation Test Setup

4.1.2 Load Transient

Using the setup in Figure 10, apply a load transient to each output to determine how well the voltage rail responds to drastic changes in load. Set a DC-power supply to 14 V for the input power to the TIDA-00805 board. Placed an AC-coupled oscilloscope probe with a short ground directly across the output capacitor of the respective voltage rail to capture the changes in VOUT due to the applied load step. To apply a fast-load transient, connect a power field-effect transistor (FET) across the output rail under test. Determine the FET-switching frequency by a square wave from a function generator. The load and frequency vary depending on the voltage rail under test. All load transient tests performed in this document had a ~200ns slew rate.

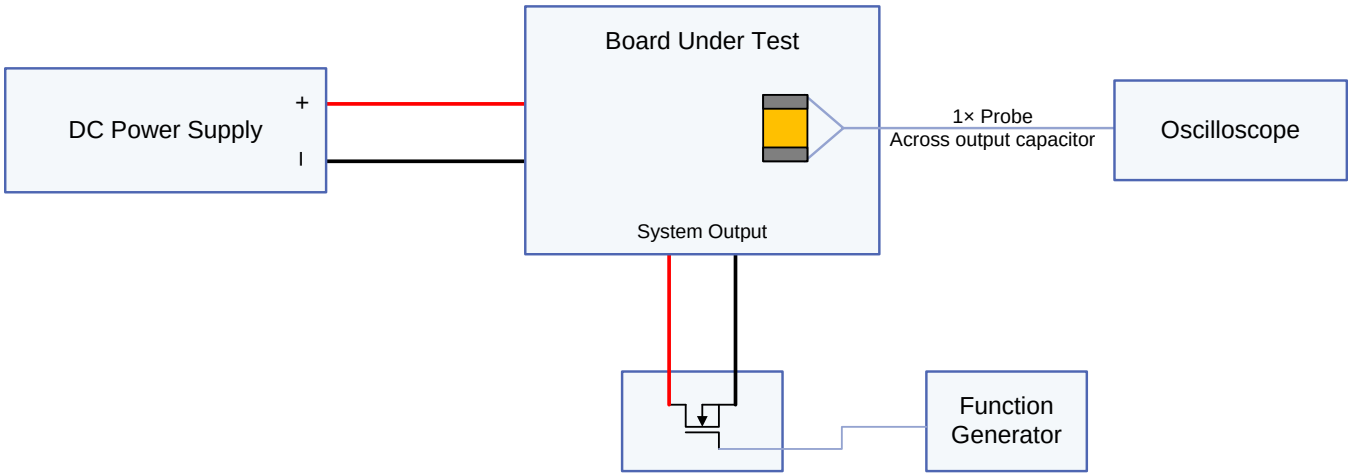


Figure 10. Load Transient Test Setup

4.1.3 Line Transient

Figure 11 shows the test setup to test a line-transient condition down to 3.9 V at the input of the preregulator. Use a function generator to create the line transient profile down to 3.9 V. Apply the electronic load at the output of the preregulator. Using an oscilloscope, capture the output voltage, load current, and input voltage waveforms.

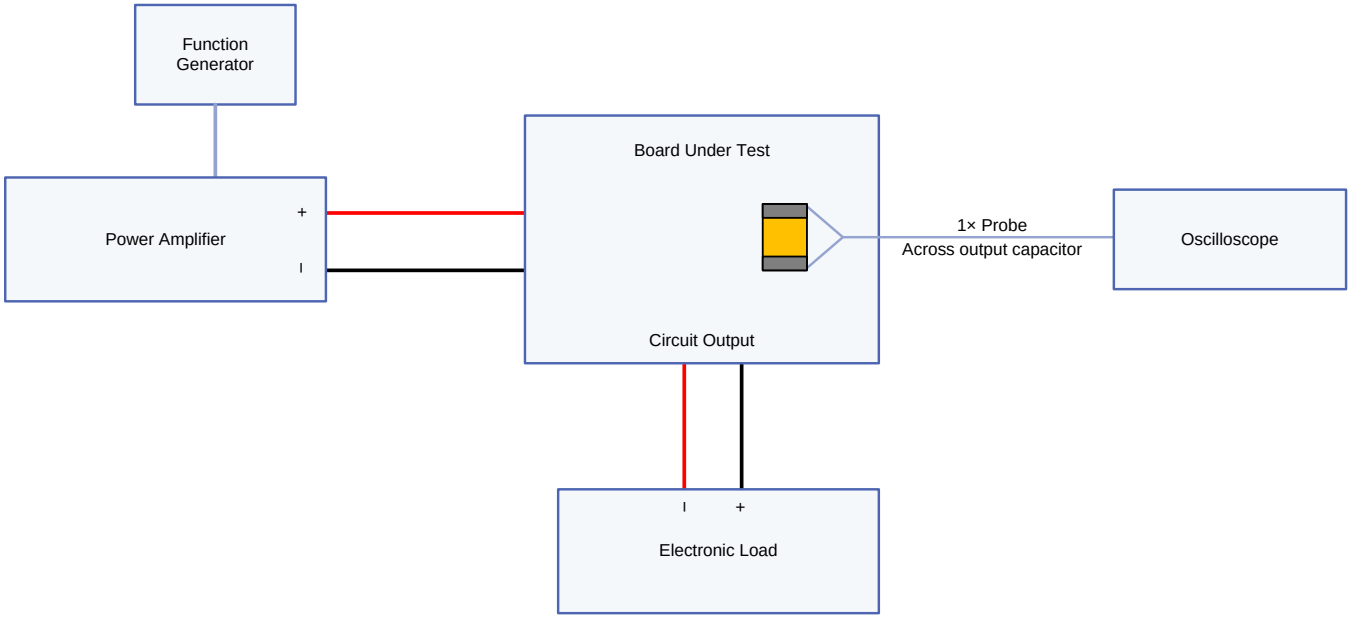


Figure 11. Line Transient Test Setup

4.2 Test Data

4.2.1 LM53635-Q1

4.2.1.1 Steady-State Load Regulation

The following plots are the test results for the preregulator at steady state using the following parameters:

- VBAT =3.9 V
- Load is specified for the corresponding figures at 3 A (Figure 12)

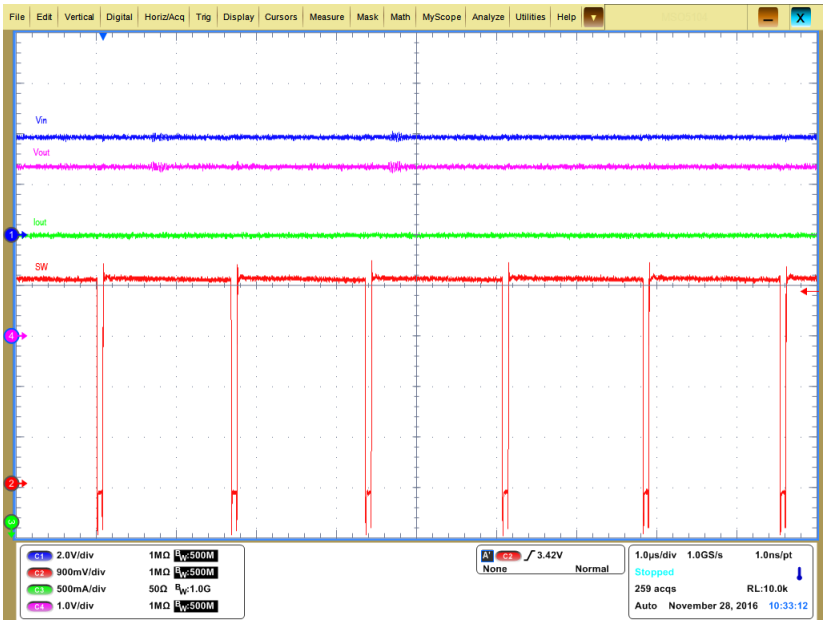


Figure 12. Steady State Load Regulation VBAT= 3.9 V, 3 A

- VBAT =14 V
- Load is specified for the corresponding figures at 3 A (Figure 13)

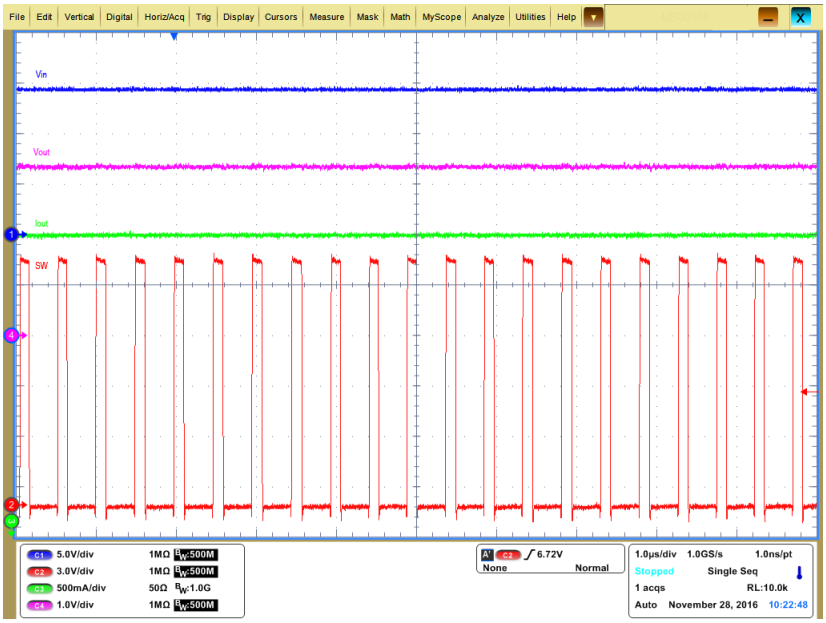


Figure 13. Steady State Load Regulation VBAT= 14 V, 3 A

4.2.1.2 Load Transient

The following plots are the test results for the preregulator load transient response.

- VBAT =3.9 V
- Load starts at 10 mA, goes to 2 A, then returns to 10 mA (Figure 14)

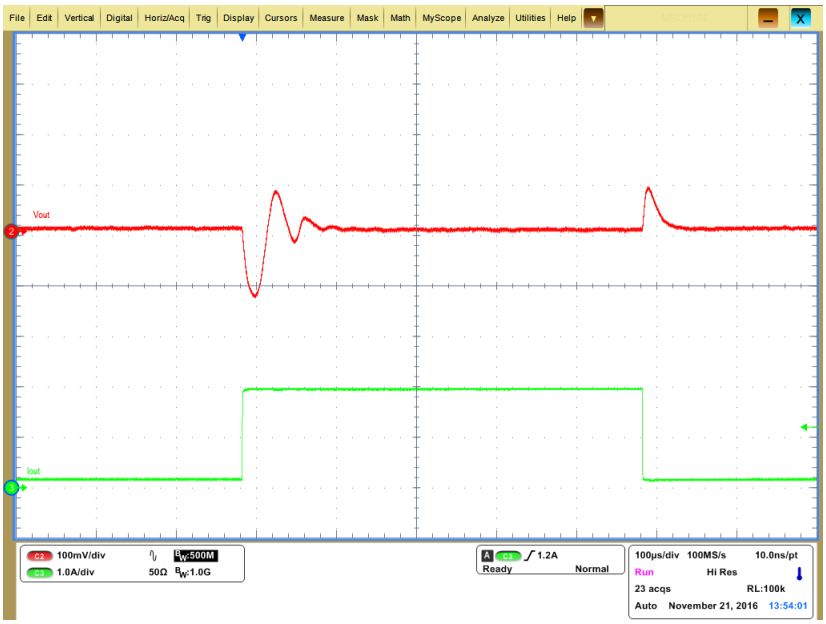


Figure 14. Load Transient Response, 3.9 V

- VBAT = 14 V
- Load starts at 10 mA, goes to 2 A, then returns to 10 mA (Figure 15)

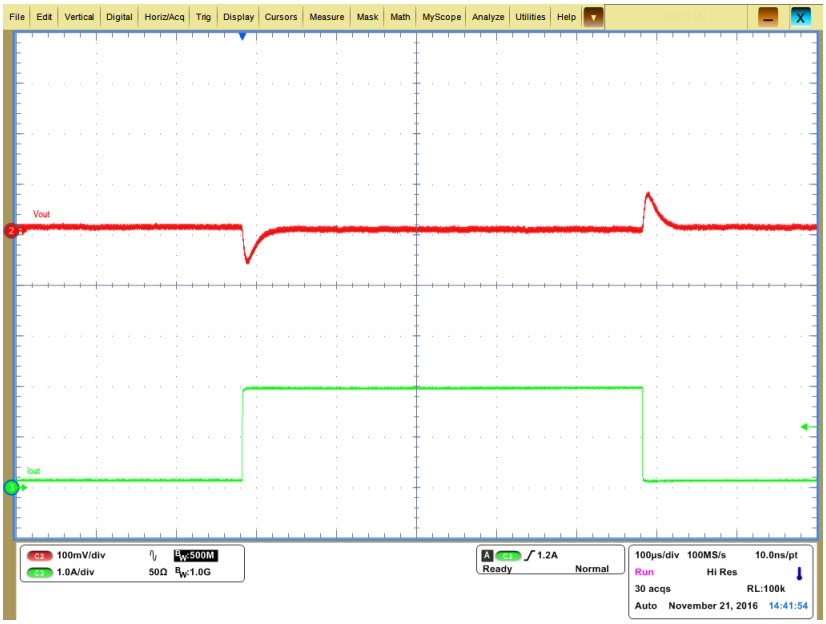


Figure 15. Load Transient Response, 14 V

4.2.1.3 Line Transient Down to 3.9 V

The following plot is the test results using the following parameters.

- Voltage for VBAT starts at 14 V, steps down to 3.9 V, and returns to 14 V (Figure 16)

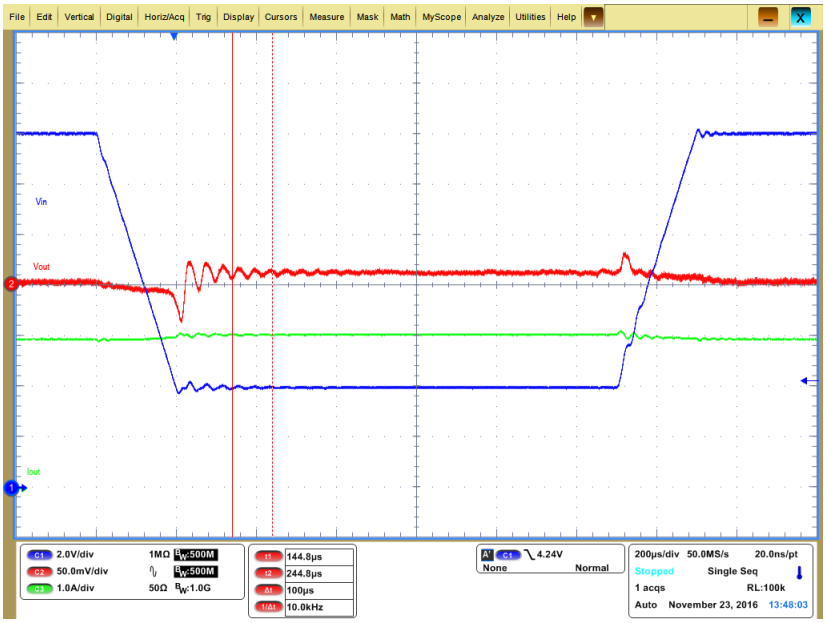


Figure 16. 3.2.1.3 Line Transient Down to 3.9 V

4.2.2 TPS65917-Q1

The following are test plots for the TPS65917Q1 using the following parameters:

- VBAT = 14 V
- VCCA = 3.3 V
- VIO_IN = 3.3 V

The plots show the transient response waveform of the PMIC for the respective SMPS and for the output of the preregulator.

4.2.2.1 SMPS1

- VOUT = 1.15 V
- Load starts at 800 mA, goes to 3.5 A, then returns to 800 mA (Figure 17)

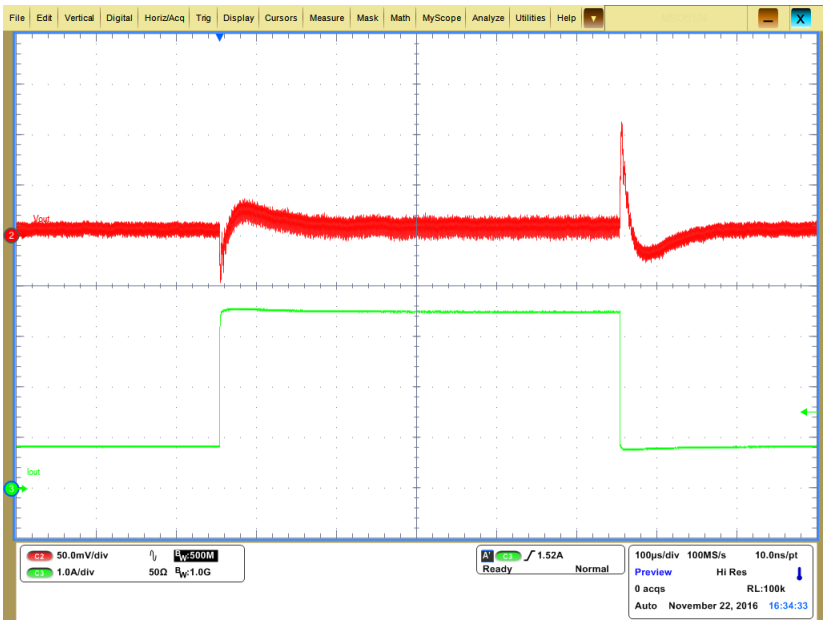


Figure 17. Transient Response Waveform, SMPS1

4.2.2.2 SMPS2

- VOUT = 1.06 V
- Load starts at 800 mA, goes to 3.5 A, then returns to 800 mA (Figure 18)

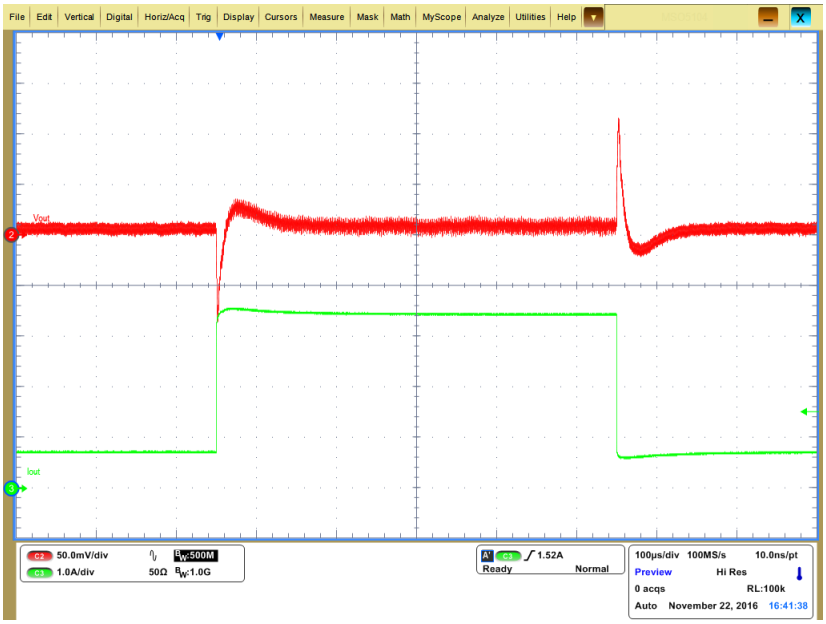


Figure 18. Transient Response Waveform, SMPS2

4.2.2.3 SMPS3

- VOUT = 1.15
- Load starts at 600 mA, goes to 3 A, then returns to 600 mA (Figure 19)

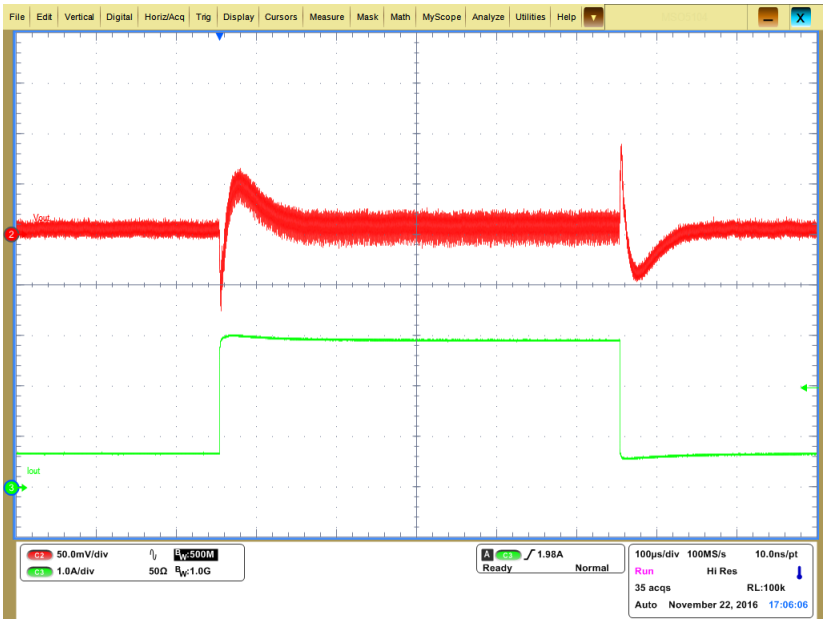


Figure 19. Transient Response Waveform, SMPS3

4.2.2.4 SMPS4

- VOUT = 1.8 V
- Load starts at 300 mA, goes to 1.5 A, then returns to 300 mA (Figure 20)

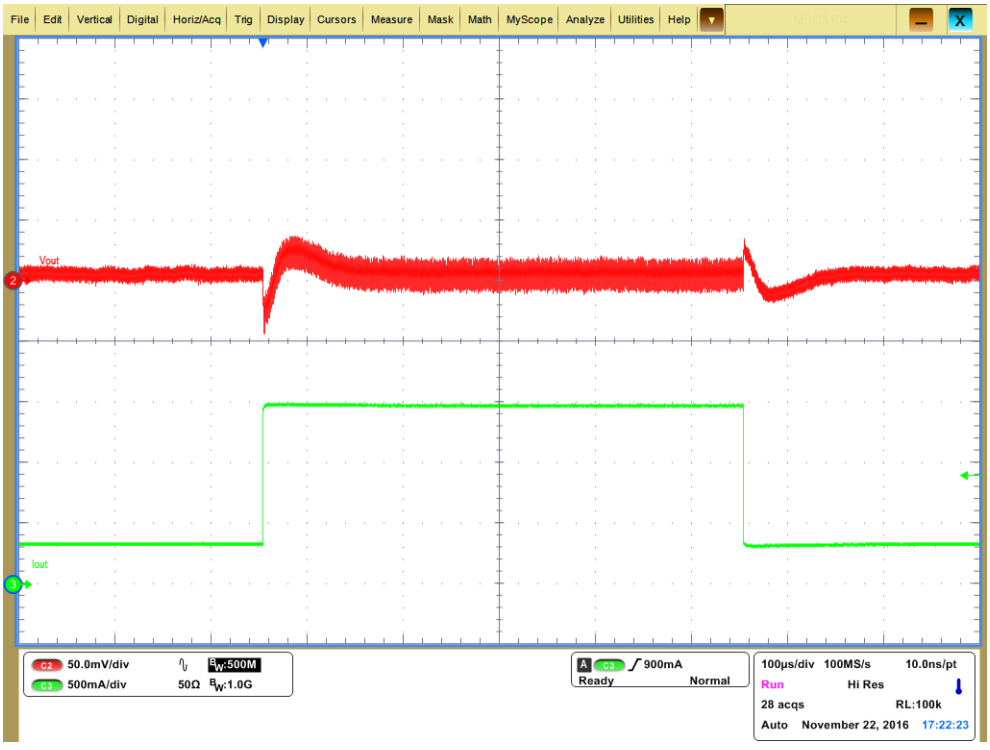


Figure 20. Transient Response Waveform, SMPS4

4.2.2.5 SMPS5

- VOUT = 1.35 V
- Load starts at 500 mA, goes to 2 A, then returns to 500 mA (Figure 21)

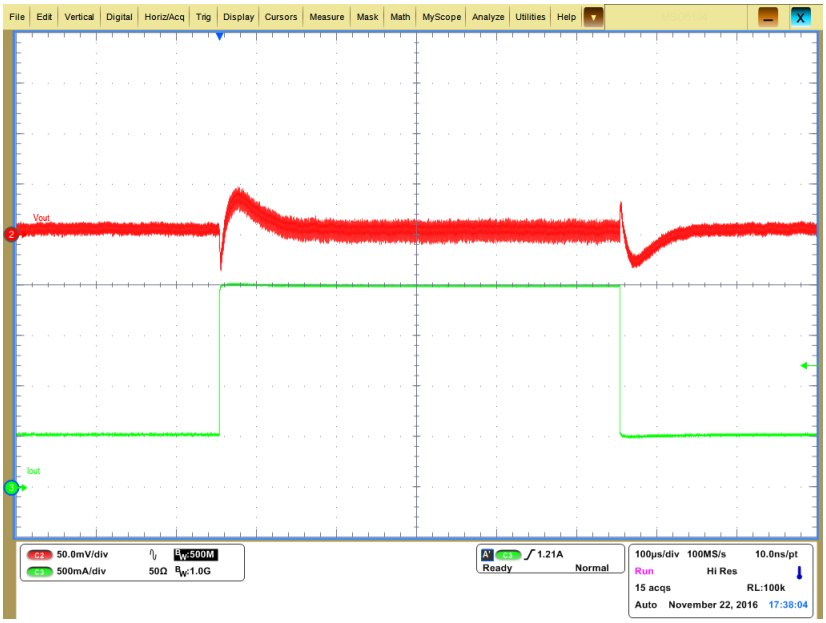


Figure 21. Transient Response Waveform, SMPS5

4.2.2.6 Sequencing

The following plot shows the test results for sequencing (Figure 22).

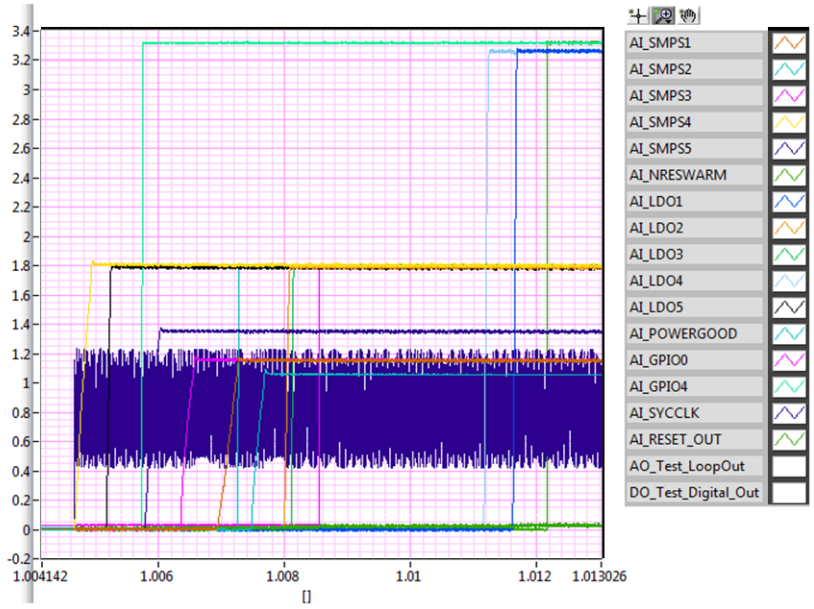


Figure 22. Sequencing

4.2.3 TPS61240-Q1

4.2.3.1 Load Transient

The following plots are the test results for the preregulator load transient response:

- VBAT = 14 V
- VIN = 3.3 V
- Load starts at 50 mA, goes to 210 mA, then returns to 50 mA (Figure 23)

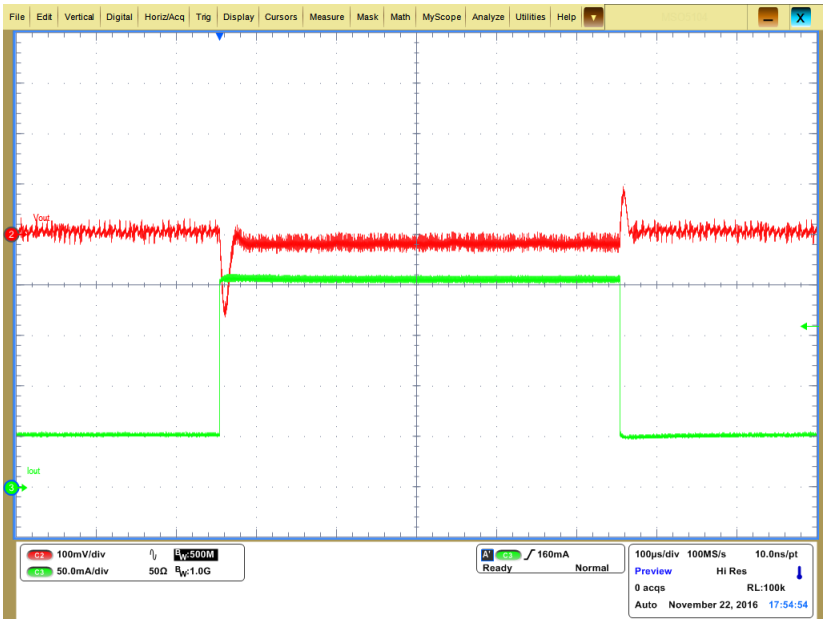


Figure 23. Load Transient Response, 14 V, 50 mA

4.2.4 TPS51200-Q1

The following plot shows the test results for the TPS51200-Q1 device using the following parameters:

- VSYS = 3.3 V
- VREF = 1.35 V
- VOUT = 0.675 V
- Iload goes from 100 mA to 1 A and then returns to 100 mA (Figure 24)

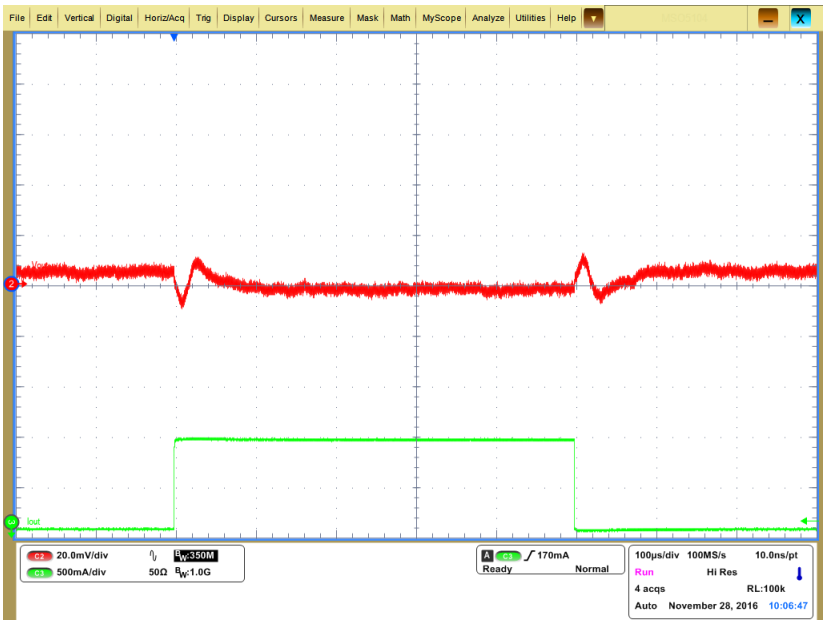


Figure 24. TPS51200-Q1 Test Plot

4.2.5 TPS22965-Q1

The following plots show the test results for the TPS22965-Q1 device using the following parameters.

4.2.5.1 Load Switch 1 (3V3_SW)

- VBIAS = 5 V
- Input Voltage = 3.3 V
- VBAT = 14 V
- Iload goes from 200 mA to 2 A and then returns to 200 mA

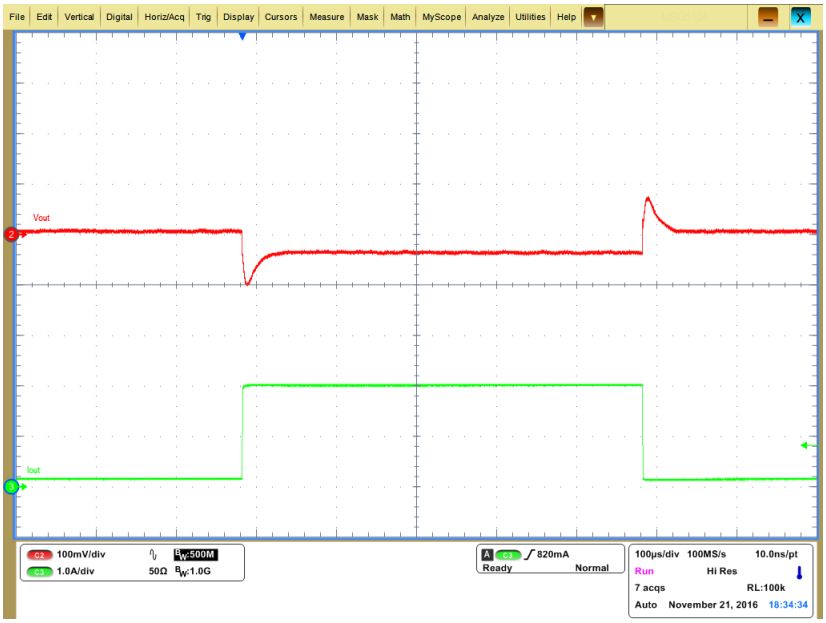


Figure 25. Load Switch 1 (3V3_SW)

4.2.5.2 Load Switch 2 (VDD DDR SW2)

- VBIAS = 5 V
- Input Voltage = 1.35 V
- VBAT = 14 V
- Iload goes from 500 mA to 2 A and then returns to 500 mA (Figure 26)

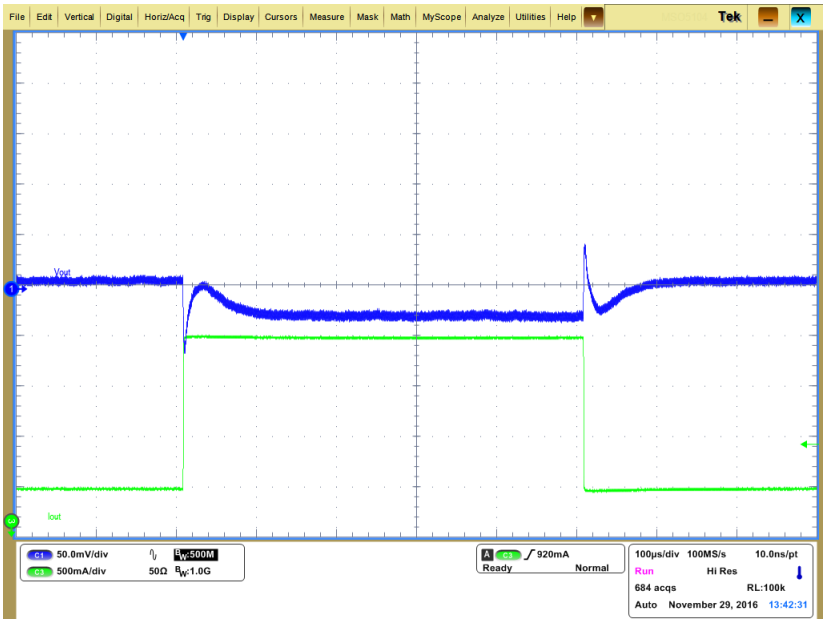


Figure 26. Load Switch 2 (VDD DDR SW2)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00805.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00805.

5.3 PCB Layout Recommendations

5.3.1 LM53635-Q1 Layout Recommendations

The IC uses two input loops in parallel IN1 and IN2 that cuts the parasitic input inductance in half. To get the minimum input loop area two small high frequency capacitors CIN1 and CIN2 are placed as close as possible. The output current loop is optimized as well by using two ceramic output caps COUT1 and COUT2 on each side. Having two parallel ground return paths can result in reduced “ground bouncing”. To further reduce inductance, an input current return path should be placed underneath the loops IN1 and IN2. Below are guidelines regarding placement of components.

1. Place two 0.047-µF, 50-V high-frequency input capacitors CIN1 and CIN2 as close as possible to the VIN1 and VIN2 and PGND1 and PGND2 pins to minimize switch node ringing.
2. Place bypass capacitors for VCC and BIAS close to their respective pins. Make sure AGND pin “sees” the CVCC and CBIAS capacitors first before connecting it to GND.
3. Place CBOOT capacitor with smallest parasitic loop. Shielding the CBOOT capacitor and switch node will have biggest impact to reduce common mode noise. Placing a small RBOOT resistor (less than 3 Ω is recommended) in series to CBOOT will slow down the dV/dt of the switch node and reduce EMI.
4. Use dedicated BIAS trace to avoid noise into feedback trace.
5. Minimize switch node and CBOOT area for lowest EMI common mode noise.

5.3.2 TPS65917-Q1 Layout Recommendations

As in every switch-mode-supply design, general layout rules apply:

1. Use a solid ground-plane for power-ground (PGND)
2. Use an independent ground for Logic, LDOs, and Analog (AGND)
3. Connect those grounds at a star-point that is ideally underneath the IC.
4. Place input capacitors as close as possible to the input pins of the IC. This placement is paramount and more important than the output-loop!
5. Place the inductor and output capacitor as close as possible to the phase node (or switch-node) of the IC.
6. Keep the loop-area formed by phase-node, inductor, output-capacitor, and PGND as small as possible.
7. For traces and vias on power lines, keep inductance and resistance as small as possible by using wide traces, avoid switching layers, but if needed, use plenty of vias.

The goal of the previously listed guidelines is a layout that minimizes emissions, maximizes EMI-immunity, and maintains a safe operating area for the IC. To minimize the spiking at the phase-node for both, high-side (VIN – SWx) as well as low-side (SWx – PGND), the decoupling of VIN is paramount. Appropriate decoupling and thorough layout should ensure that the spikes never exceed 9-V peak-to-peak at the IC.

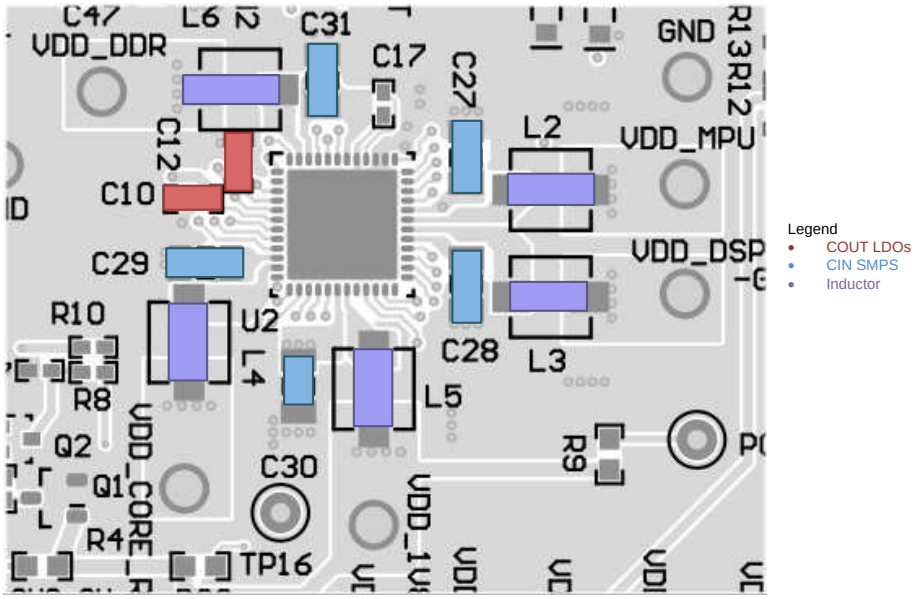


Figure 27. Top Layer Overview of Inductor and Capacitor Placement and Routing of SMPSs

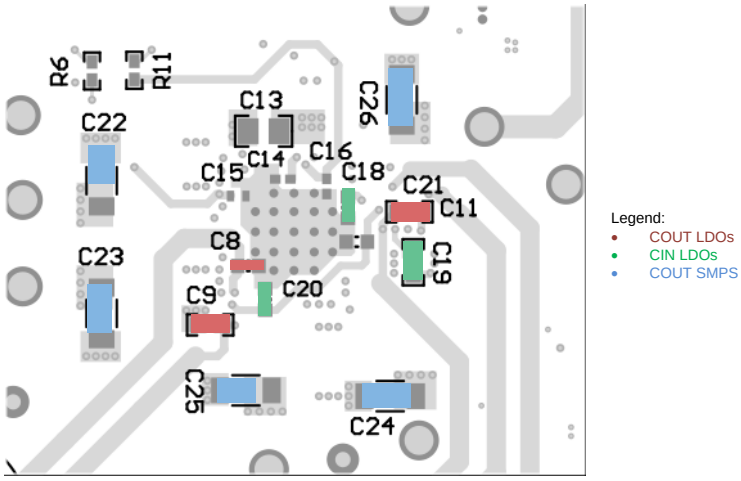


Figure 28. Bottom Layer Overview of Capacitor Placement and Routing of LDOs

5.3.3 TPS61240-Q1 Layout Recommendations

Use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

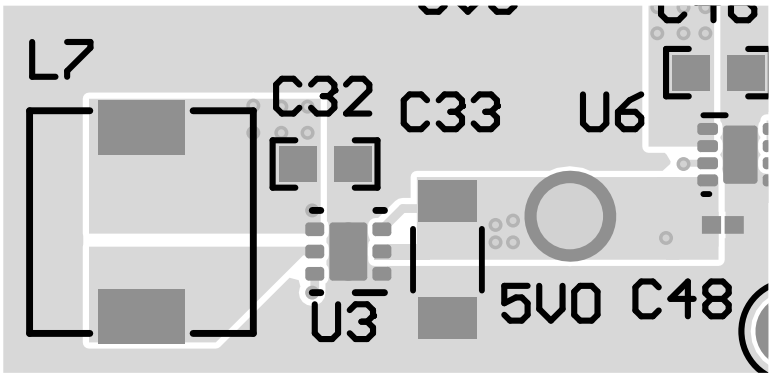


Figure 29. TPS61240-Q1 Top Layer Overview

5.3.4 TPS22965-Q1 Layout Recommendations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

5.3.5 TPS51200-Q1 Layout Recommendations

Consider the following points before starting the TPS51200-Q1 layout design.

1. The input bypass capacitor for VLDOIN must be placed as close as possible to the pin with short and wide connections.
2. The output capacitor for VO must be placed close to the pin with short and wide connection to avoid additional ESR or ESL trace inductance.
3. VOSNS must be connected to the positive node of VO output capacitors as a separate trace from the high current power line. This configuration is strongly recommended to avoid additional ESR, ESL, or both. If sensing the voltage at the point of the load is required, TI recommends to attach the output capacitors at that point. Also, it is recommended to minimize any additional ESR, ESL, or both of ground trace between the GND pin and the output capacitors.
4. Consider adding low-pass filter at VOSNS if the ESR of the VO output capacitors is larger than 2 mΩ.
5. REFIN can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of REFOUT. Avoid any noise-generating lines.
6. The negative node of the VO output capacitors and the REFOUT capacitor must be tied together by avoiding common impedance to the high current path of the VO source/sink current.
7. The GND and PGND pins must be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground planes (for better result, use at least two internal ground planes).Use as many vias as possible to reduce the impedance between PGND and GND and the system ground plane. Also, place bulk caps close to the DIMM load point, route the VOSNS to the DIMM load sense point.
8. To effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the thermal pad of the package. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0,33 mm in diameter connected from the thermal land to the internal/solder side ground planes must also be used to help dissipation.
9. See the TPS51200-EVM User's Guide (SLUU323) for detailed layout recommendations.

5.3.6 Layout Prints

To download the layer plots, see the design files at TIDA-00805.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00805.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00805.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00805.

6 Related Documentation

1. Texas Instruments, *Automotive Off-Battery Infotainment Processor Power Reference Design*, TIDA-00801 Reference Design (TIDUAX5)
2. Texas Instruments, *Automotive Power Design for Front Camera Systems using Single Core Voltage Application Processors*, TIDA-00803 Reference Design (TIDUBF7)
3. Texas Instruments, *ISR Input/Output Filters*, Application Report (SLTA013)
4. Texas Instruments, *LM53625/35-Q1, 2.5-A or 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter*, LM53625/35-Q1 Datasheet (SNVSAA7)
5. Texas Instruments, *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch*, TPS22965x-Q1 Datasheet (SLVSCI3)
6. Texas Instruments, *Using theTPS51200 EVM Sink/Source DDR Termination Regulator*, TPS51200 EVM User Guide (SLUU323)
7. Texas Instruments, *TPS51200-Q1 Sink and Source DDR Termination Regulator*, TPS51200-Q1 Datasheet (SLUS9894)
8. Texas Instruments, *TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter*, TPS61240-Q1 Datasheet (SLVSAO4)
9. Texas Instruments, *TPS65917-Q1 Power Management Unit (PMU) for Processor*, TPS65917-Q1 Datasheet (SLVSCO4)

6.1 Trademarks

7 About the Author

JULIO SANCHEZ joined Texas Instruments as an Applications Engineer in 2016 after earning his Bachelor of Science in Electrical Engineering from Texas Christian University. As a member of the Mixed Signal Automotive – Automotive Safety and Power team, Julio focuses on supporting automotive customers and creating valuable collateral.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (January 2017) to B Revision	Page
• Deleted preregulator output inductor from *Configurable Components* section	12

Changes from Original (December 2016) to A Revision	Page
• Changed part number to TFM252012ALMA-1R0MT	12

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265