TI Designs

High-Speed Multichannel ADC Clock Reference Design for Oscilloscopes, Wireless Testers and Radars

Description

This TI Design demonstrates the performance of a clocking solution for a high-speed multichannel system, analyzed by measuring the channel-to-channel skew for the entire input frequency range of the RF sampling ADC. Channel-to-channel skew is critical for phased array radar and oscilloscope applications. The ADC12J4000 is a low-power, 12-bit, 4-GSPS RF-sampling analog-to-digital converter (ADC) with a buffered analog input, integrated digital down converter, features a JESD204B interface, and captures signals up to 4 GHz. This design showcases the clocking solution using the LMK04828 to achieve the synchronization between multiple ADC12J4000 signal chains using synchronized SYSREF.

Features

- Synchronization of Multichannel High-Speed ADCs
- RF Sampling ADC Clocking Solution
- 4-GHz High-Frequency Input Signal Capture Capability
- Low-Phase Noise Clocking Solution for RF Sampling ADC

Applications

- Oscilloscope
- Wireless Communication Tester
- Phased Array Radar
- RF-Sampling Software Defined Radio

Resources

TIDA-01017	Design Folder
ADC12J4000EVM	Tool Folder
ADC12J4000	Product Folder
LMK04828	Product Folder
LMK04828EVM	Tool Folder

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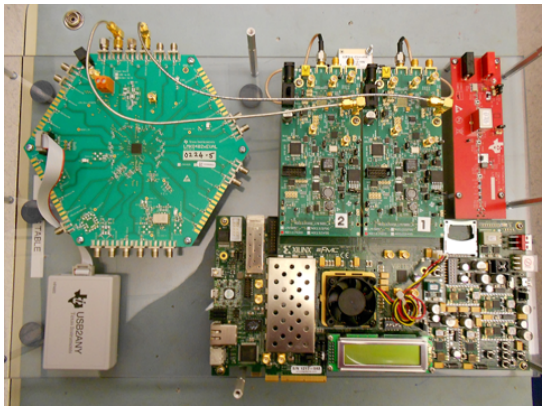

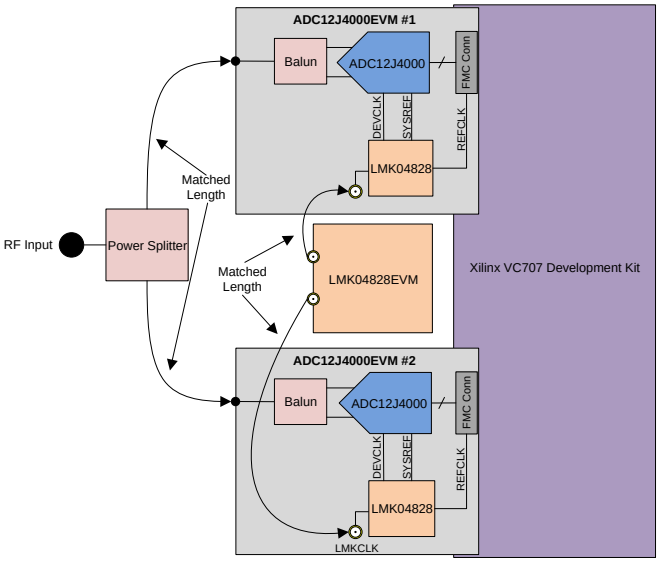

1 System Overview

1.1 System Description

The clocking solution in a high-speed multichannel system is extremely critical for synchronization of input data. This reference design demonstrates a clocking scheme for synchronization of high-speed ADCs using a Xilinx platform. The design focuses on the LMK04828 clock generator as an input clock source and the ADC12J4000 GSPS ADC for the applications of phased array radar and oscilloscopes using a RF sampling approach. The LMK04828 operates up to 3 GHz and provide very low clock jitter for GSPS ADCs.

In this solution, the LMK04828 in each channel receives a reference clock frequency from another LMK04828EVM for performing the synchronization between them and provides the device clock or sampling clock (DEVCLK) to the ADC12J4000. The LMK04828 clock jitter cleaner supplies the system reference low-frequency clock (SYSREF) to the ADC12J4000 and FPGA needed to properly operate the JESD204B SERDES.

Multichannel digital oscilloscopes require a wideband analog front-end and low channel-to-channel skew. The ADC12J4000 ADC is well suited for these requirements. The clocking solution described in this TI Design provides an optimum solution for clocking the ADC12J4000 ADCs to achieve wide bandwidth and low channel-to-channel skew.

Wireless tester equipment involves multi-channel receivers to test a MIMO device or equipment. Wireless testers require high dynamic range and wideband receivers to test 3G and later wireless standards compliant equipment. The ADC12J4000 is well suited for the multi-channel receiver requirements of the wireless testers. The clocking solution described in this TI Design provides a fitting solution for clocking the multiple ADC12J4000 devices to achieve a low-time skew between channels providing both high dynamic range and wide receiver bandwidth in wireless tester applications.

Phased array radar applications need a high dynamic range, wide receiver bandwidth, low latency, and good synchronization between the channels. The signal chain solution based on the ADC12J4000 and LMK04828 helps to achieve optimum performance for phased array radar applications.

RF-sampling software defined radio (SDR) technology also needs multichannel, high dynamic range, highly re-configurable receiver bandwidth, and wide input frequency range. This TI Design can meet the requirements of the high-performance SDRs in terms of multichannel, dynamic range, and re-configurability.

1.2 Key System Specifications

The objective of the TI Design is to demonstrate the synchronization scheme between two ADC12J4000 signal chains using an LMK04828EVM, which is key in high-speed multichannel systems. The data capture is done by the VC707 Xilinx EVM. The design focuses on measuring the time skew between the two ADC signal chains by feeding input signal frequency up to 3.7 GHz. The high-frequency input signals are fed to both ADC12J4000EVMs through a splitter and a set of matched cables. The input baluns on the ADC12J4000EVMs were modified to enhance the input frequency range up to 4 GHz. Table 1 lists the key system level specifications for the signal chain from the clocking solution perspective.

Table 1. Key System Level Specifications

PARAMETER	SPECIFICATIONS	CONDITIONS
Time skew	< 50 ps	350-MHz input signal
		600-MHz input signal
		900-MHz input signal
		1650-MHz input signal
		2400-MHz input signal
		2700-MHz input signal
		3700-MHz input signal

1.3 Block Diagram

Figure 1 shows the block diagram of the high-speed multichannel ADC clock solution along with the reference source (LMK04828EVM) and VC707 platform for capturing the data. Both ADC12J4000EVMs are interfaced with VC707 board through onboard FMC connectors. Reference signals and analog inputs are provided to both EVMs using length matched cables and 0-degree power splitters.

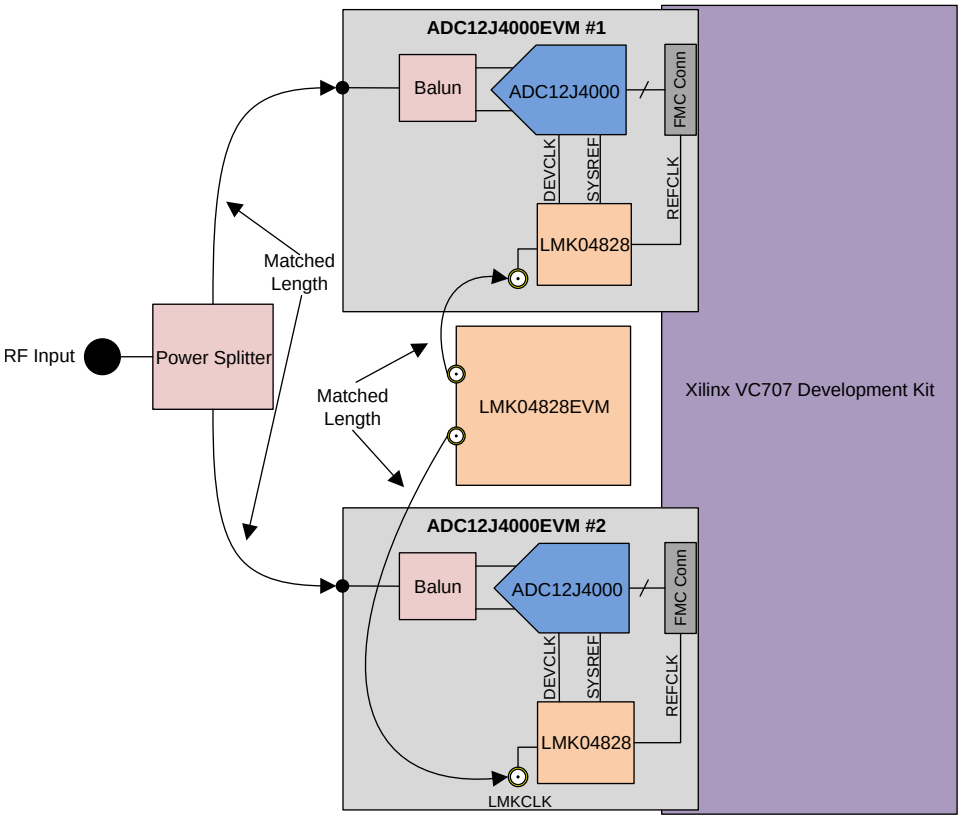

Figure 1. Block Diagram of Multichannel System With ADC12J4000EVMs, LMK04828EVM, and VC707 Platform

1.4 Highlighted Products

1.4.1 ADC12J4000

The ADC12J4000 is a wideband sampling high-speed ADC with a JESD204B interface. It includes a 12-bit, 4-GSPS ADC with an integrated digital down converter (DDC) with programmable NCO and decimation settings (including un-decimated, 12-bit ADC output). It has a 3-dB input bandwidth of 3.2 GHz and is usable up to 4 GHz. The device input is buffered with an on-chip differential termination of 100 Ω.

1.4.2 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator. The LMK04828 is set up in single PLL 0-delay mode, which phase locks the SYSREF signal of the ADC with the SYSREF reference signal. The LMK04828 supplies the SYSREF and DEVCLK to the ADC and other clocks for the JESD204B FPGA interface.

1.5 System Design Theory

This TI Design demonstrates synchronization of two high-speed ADCs, which is critical in multichannel systems like oscilloscopes and phased array radars. Synchronization performance is measured in terms of time skew between the analog inputs channels. Good phase synchronization of the sampling clock of ADCs should result in lower time skew. The time skew between the channels are calculating by the phase difference between signals captured from each ADC. The phase difference is measured by the comparing the phases of the signals using an FFT and converting the phase difference to a time value, which is the skew between the input channels.

Figure 2 shows the clocking solution for multichannel ADCs. The LMK04828EVM creates two phase-aligned 9.216-MHz SYSREF signals that are sent to each ADC12J4000EVM through matched-length cables to maintain phase alignment at the input of the LMK04828 on each ADC EVM. The LMK04828 clock IC onboard each ADC EVM is set up in single-loop 0-delay mode to create a SYSREF signal for each ADC, which is phase-aligned to the SYSREF input. This setting also generates phase-aligned DEVCLKs for each ADC. The LMK04828EVM acts as a frequency and phase reference for both ADC12J4000EVMs. Each ADC12J4000EVM generates its own clocks from this reference.

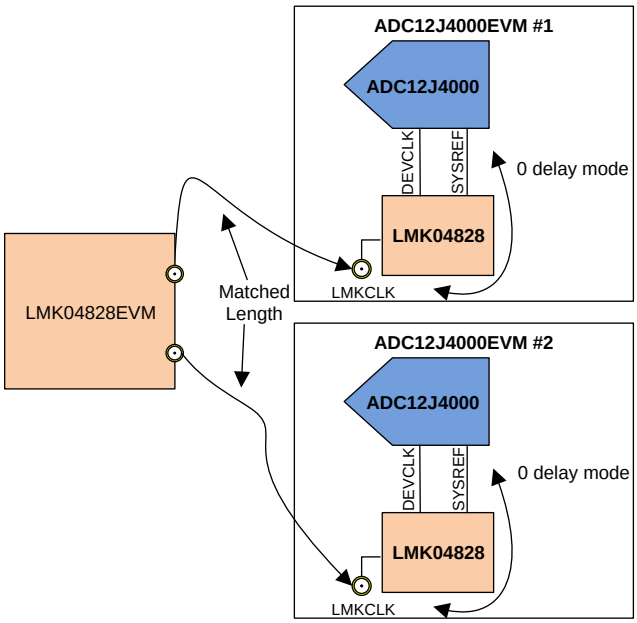

Figure 2. Block Diagram of Clocking Solution

Both the ADCs are setup in the following configurations:

- Fs = 2949.12 MHz
- JESD mode: Decimation-by-10, DDR = 1, P54 = 0, LMF = 2,2,2
- K = 16

The ADC12J4000 ADCs are in decimation-by-10 mode, so the Xilinx VC707 board works in low IF (70 MHz). NCO frequency is selected based on IF frequency and NCO frequency is the analog input signal subtracted by the IF frequency. NCO counter value also depends on the DEVCLK of ADC.

2 Getting Started Hardware and Software

2.1 Hardware Configuration

2.1.1 ADC12J4000EVM Setup

Figure 3 shows the block diagram for the setup of the ADC12J4000EVM. Follow the ADC12J4000EVM user's guide[1] (SLAU551) for the ADC12J4000EVM hardware setup procedure. The onboard LMK04828 device is set up in single PLL 0-delay mode, which phase-locks the SYSREF signal of the ADCs with the SYSREF reference signal provided to the LMKCLK connector. This mode creates a phase-locked SYSREF and DEVCLK for the two ADCs on the separate ADC12J4000EVMs.

The ADC12J4000EVM needs modification for this clocking scheme. Modify the ADC12J4000EVM by removing C32 and C33 and populating C262 and C263. For single-loop 0-delay mode, populate C85 and C86 to apply the reference SYSREF signal to the OSCin+ pin of the LMK04828. Due to the low-PFD frequency in this mode, modify the loop filter for PLL2 to stabilize the loop. Remove the installed components for LF1, LF2, and LF3. Populate 12 nF, 0.22 nF, and 1 kΩ, respectively. Place a jumper on KC705 JTAG for programming the VC707 development kit. Follow the TIDA-00432 design guide[2] (TIDU752) for a detailed modification on ADC12J4000EVM hardware.

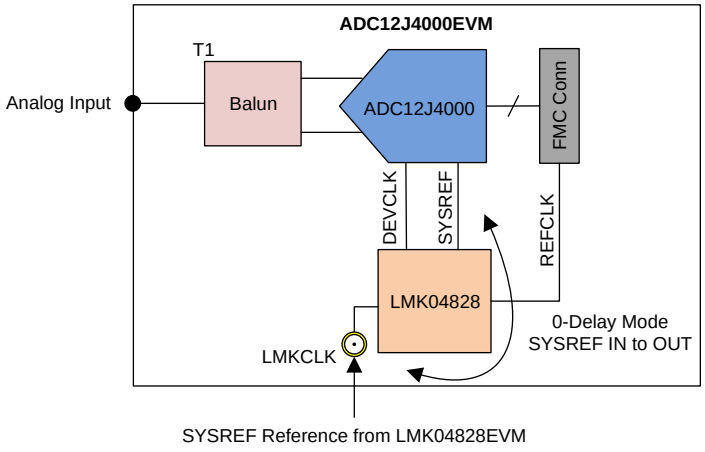

Figure 3. Block Diagram of Modified ADC12J4000EVM

On the original EVM the balun, T1 supports an input frequency up to 3 GHz. In this TI Design, the balun was replaced with the BD2040J50100AHF to support frequencies up to 4 GHz.

2.1.2 LMK04828EVM Setup

The LMK04828EVM must remain unmodified.

2.1.3 VC707 Development Kit

The VC707 development kit must remain unmodified.

2.2 Software Configuration

2.2.1 ADC12J4000EVM Configuration

The ADC12J4000 and LMK04828 devices are configured in the ADC12J4000EVM in this TI Design. For this test, the ADC12J4000EVM was set up for decimate-by-10 using two SerDes lanes (Decimate-by-10, DDR = 1, P54 = 0, LMF = 2,2,2). For synchronization, the SYSREF receiver was enabled. The SYSREF timing was adjusted using the dirty SYSREF capture bit to detect timing errors and then using the programmable delays to meet setup and hold times. Both ADC12J4000 ADCs were loaded with the same configuration.

The LMK04828 must be set up for single-loop 0-delay mode. In this mode, only PLL2 is used (PLL1 can be disabled). The reference signal provided to the OSCin pin is the SYSREF signal from the LMK04828EVM. Both R and N dividers are set to 1. By tracing the signal from the phase detector through the N divider, the VCO frequency is the reference frequency multiplied by the SYSREF divider. Because the output of the SYSREF divider is the feedback signal and both R and N dividers are set to 1, the phase detector forces the phase of the SYSREF divider output to match the phase of the reference signal.

The onboard LMK04828 also generates the device clock for the ADC12J4000. In this case, the device clock runs at 2949.12 MHz. The LMK04828 from one of the boards also sends a device clock and SYSREF signal back to the FPGA through the FMC connector and each ADC board sends a reference clock to the related FPGA transceiver blocks.

For configuring the ADC12J4000EVM, set the clock source as external and provide the sampling frequency of 2949.12 MHz in ADC12J4000EVM GUI as shown in Figure 4. Later in the process, load the modified LMK04828 configuration file, the ADC12J4000 configuration file and set the NCO frequency as per the analog input frequency.

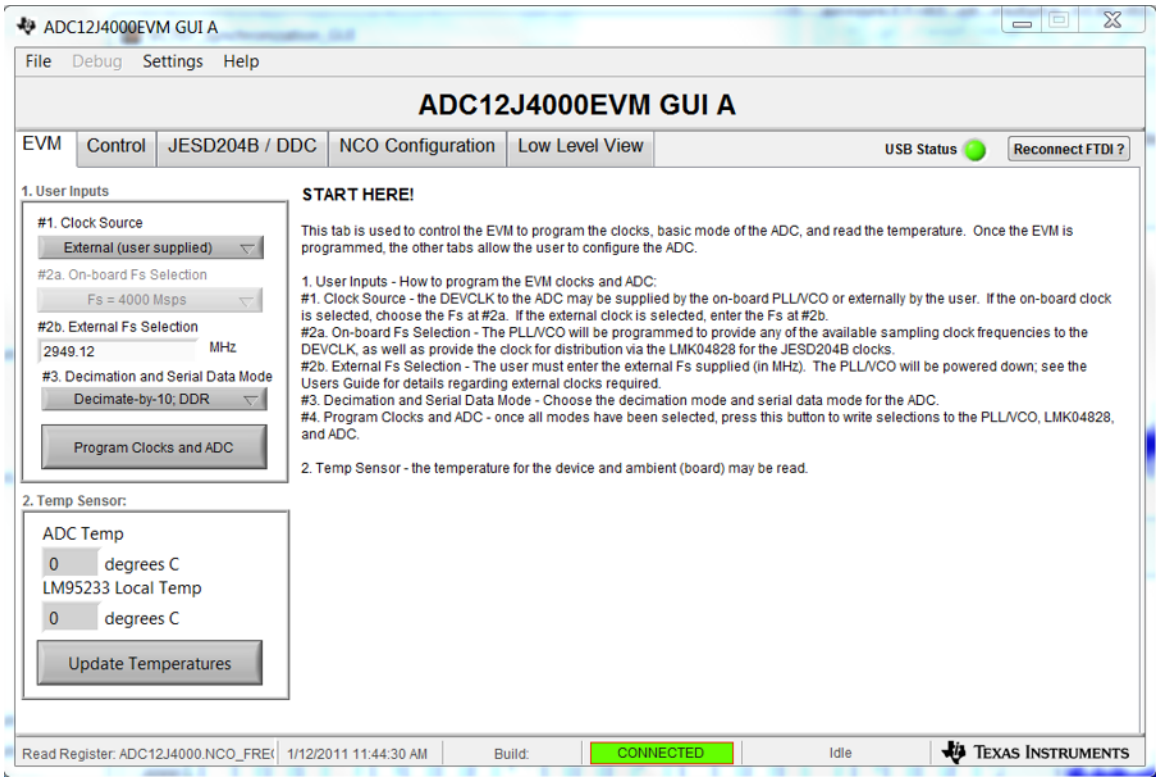

Figure 4. ADC12J4000EVM Programming

2.2.2 LMK04828EVM Configuration

The LMK04828EVM is configured for dual-loop mode. The only clocks required for this setup are two phase-matched SYSREF clocks used as references for the ADC12J4000EVM devices. Alternatively, a signal generator could provide these clocks through a phase-matched power splitter. Any phase error between these clocks results in skewed-sampling instances in the ADCs. Using the code loader, upload the configuration file for generating the SYSREF outputs.

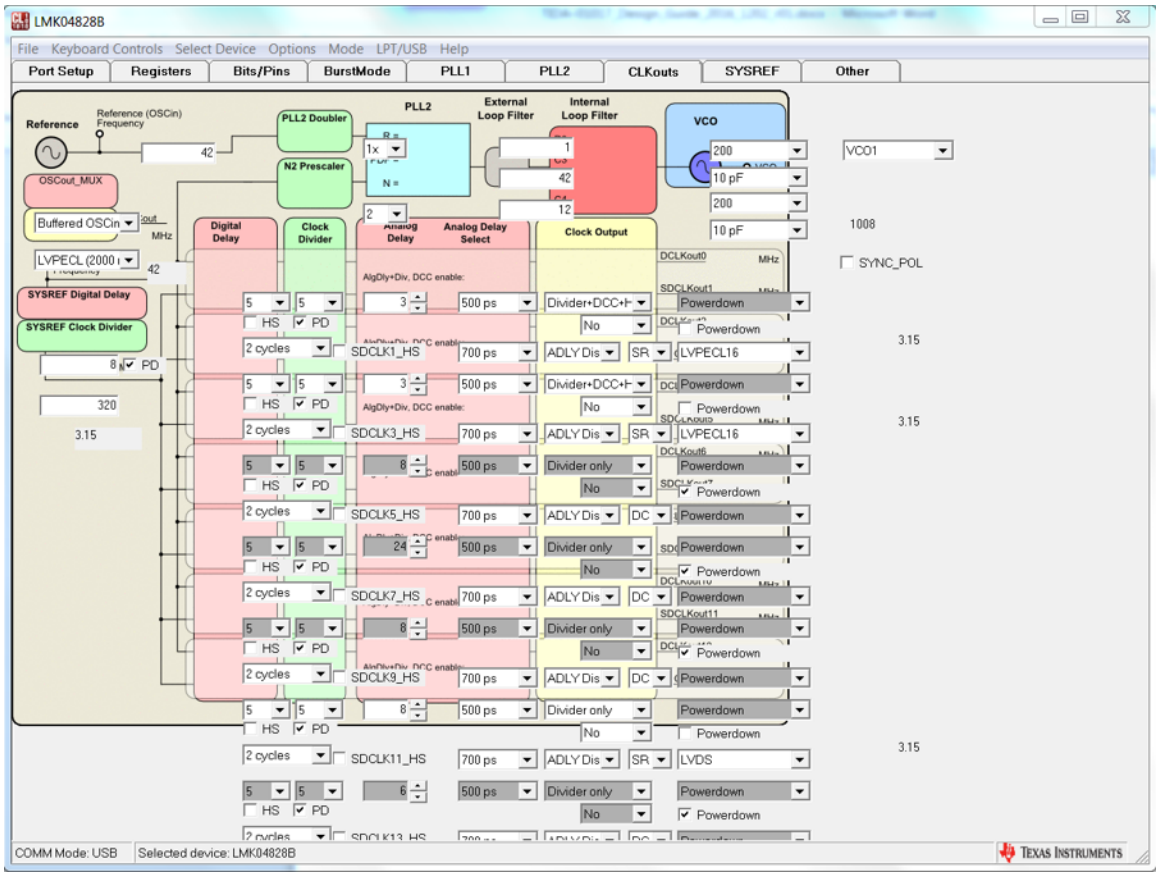

Figure 5. LMK04828EVM Programming

2.2.3 VC707 Programming

The firmware for the VC707 platform is responsible for the interface with the two ADC12J4000EVM devices and captures the data from them. Follow the TIDA-00432 design guide[2] (TIDU752) for VC707 firmware, pin assignments, JESD core implementations and transceiver setup.

3 Testing and Results

3.1 Test Setup

Figure 6 shows the test setup for time skew measurement. The analog input signal feeds into the 0-degree phase delay power splitter and is given to both ADC EVMs.

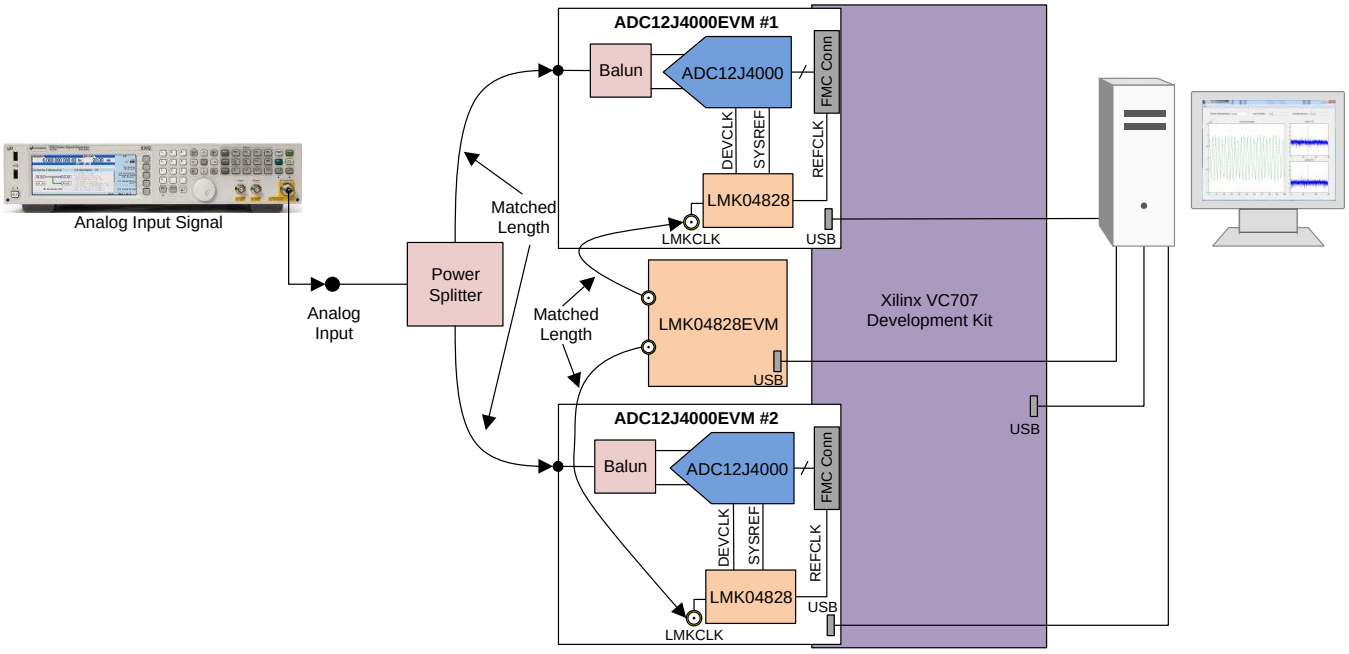

Figure 6. Test Setup for Skew Measurement

3.2 Results

The time skew is evaluated by calculating the phase difference between signals captured from each ADC. Table 2 shows the measured time skew between the two ADCs at different analog input frequencies. Using this technique, the measured time skew was < 50 ps for an input signal frequency up to 3.7 GHz.

Table 2. Measured Time Skew

INPUT FREQUENCY (MHz)	NCO FREQUENCY (MHz)	MEASURED TIME SKEW (PS)
350	280.00	11.01
600	530.00	13.91
900	830.00	0.50
1650	1580.00	7.85
2400	2330.00	–45.31
2700	2630.00	–28.90
3700	2268.24	40.59

Figure 7 shows the sampled signals of the two ADCs at a 350-MHz analog input signal.

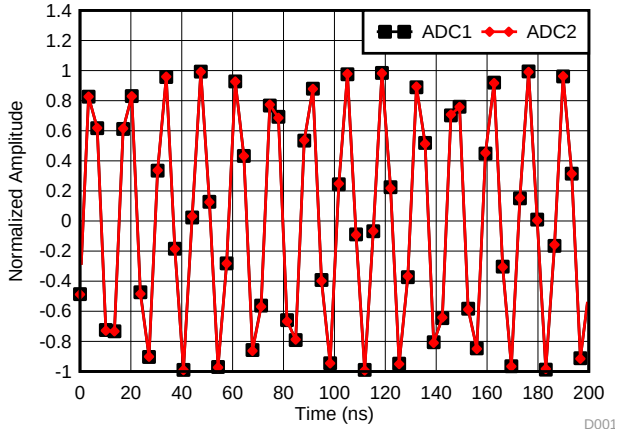

Figure 7. Sampled Signals of Two ADCs at 350-MHz Input

4 Summary and Conclusion

The TIDA-01017 is a clocking solution reference design for high-speed multichannel systems that can be used in oscilloscopes, wireless testers and radars. This TI Design demonstrates a synchronization scheme between two ADC EVMs using an LMK04828EVM to achieve low channel-to-channel skew for input frequencies up to 4 GHz. Test results show that it is possible to achieve skew better than 50 ps for input frequencies up to 4 GHz by carefully matching the RF input paths and the clock paths.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01017.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01017.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01017.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01017.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01017.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01017.

6 Software Files

To download the software files, see the design files at TIDA-01017.

7 Related Documentation

1. Texas Instruments, *ADC12J4000EVM User's Guide* (SLAU551)
2. Texas Instruments, *Synchronization of JESD204B Giga-Sample ADCs using Xilinx® Platform for Phased-Array Radar Systems Design Guide*, TIDA-00432 Design Guide (TIDU752)

7.1 Trademarks

8 About the Authors

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