TI Designs

Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters

Description

This TI Design aims to improve the integration, power consumption, performance, and clock distribution typically associated with 18-bit SAR data acquisition (DAQ) systems. The analog front-end optimization is usually the most critical part of the ADC system signal path design. The key aspect of this reference design is to explore the benefits and shortcomings of the two main ADC driver architectures—single-ended and differential—and provide a clear guidance on where each of them would yield a better performance. Another goal for this reference design is to develop a front-end ADC module for the multichannel simultaneous sampling systems. Special considerations are given for minimizing the channel to channel variations due to the reference voltage loading, clocking, and power distribution. All the key design steps are described in this document to guide users through the part selection and trade-off considerations during the design optimization process.

Resources

TIDA-01050	Design Folder
OPA827, OPA625, THS4551	Product Folder
ADS8910B, REF6041, OPA376	Product Folder
LMZ14201, LMZ14202, LMZ14203	Product Folder
TPS7A47, LM7705	Product Folder
LM5574, TPS7A3001	Product Folder
SN74AHC1G04, SN74AUP1G80	Product Folder
LMK61E2, LMK00804B	Product Folder
TIDA-00732, TIPD211	Design Folder
TINA-TI™	SPICE Simulator

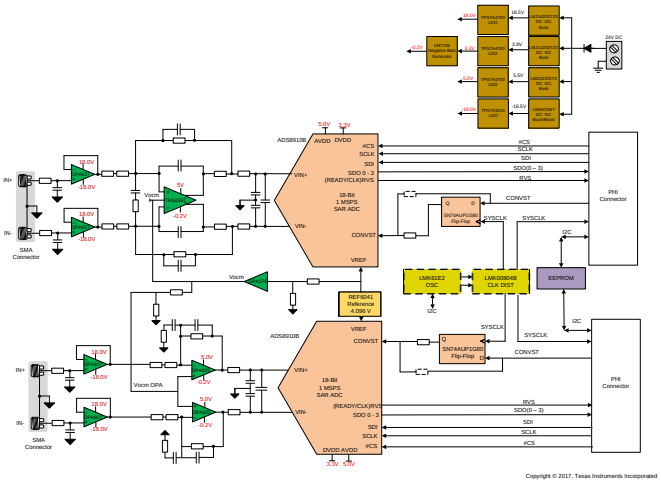
TI E2E™ Community — ASK Our E2E Experts

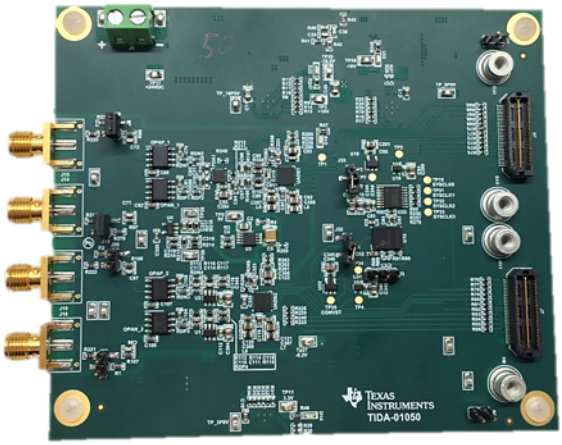
Features

- Two 18-Bit SAR ADC Channels
- Up to ±12-V Input Signal
- Modular Front-End Reference Design for High Channel Count Systems to Repeat
- Single-Supply Current: 84 mA

Applications

- Automatic Test Equipment
- Industrial Instrumentation
- Data Acquisition
- LCD Test Equipment
- Memory Test Equipment





1 System Overview

1.1 System Description

Multi-input systems requiring the simultaneous or parallel sampling of many data channels present many design challenges to engineers developing data acquisition (DAQ) modules and automatic testers for such applications as semiconductor tests, memory tests, LCD tests, and battery tests. In these systems, sometimes hundreds or even thousands of data channels are required and thus maximizing SNR performance while minimizing power, component count, and cost are all key design criteria. The analog front-end (AFE) signal chain often consists of a series of muxes, a scaling or programmable gain amplifier (PGA) followed by an antialiasing, noise limiting, low-pass filter (LPF), which is paired with the appropriate ADC driver prior to digitization. The ADC will convert the time varying analog input to either a serial or parallel binary bit stream, which is then passed to the embedded host controller (MCU or FPGA). Depending on the application, the ADC may contain the necessary reference or the associated buffer integrated as part of the ADC. Furthermore, portions or the entire AFE may also be integrated as a single device for specific applications, but this can also limit flexibility.

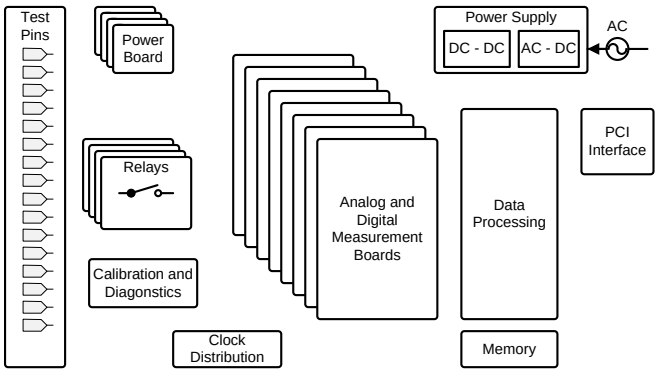


Figure 1. Multichannel Test System

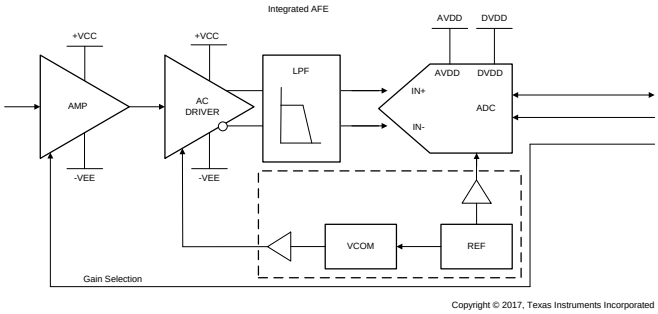


Figure 2. Generic AFE

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASURED
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	±24-V fully differential	±24-V fully differential
Resolution	18 bits	18 bits
SNR	> 95 dB	98.53 dB
THD	< –100 dB	–123.26 dB
ENOB	> 15.00	16.07
Power	< 2.5 W	2.3 W
Form factor (L × W)	120 × 100 mm	116.59 × 99.82 mm

1.3 Block Diagram

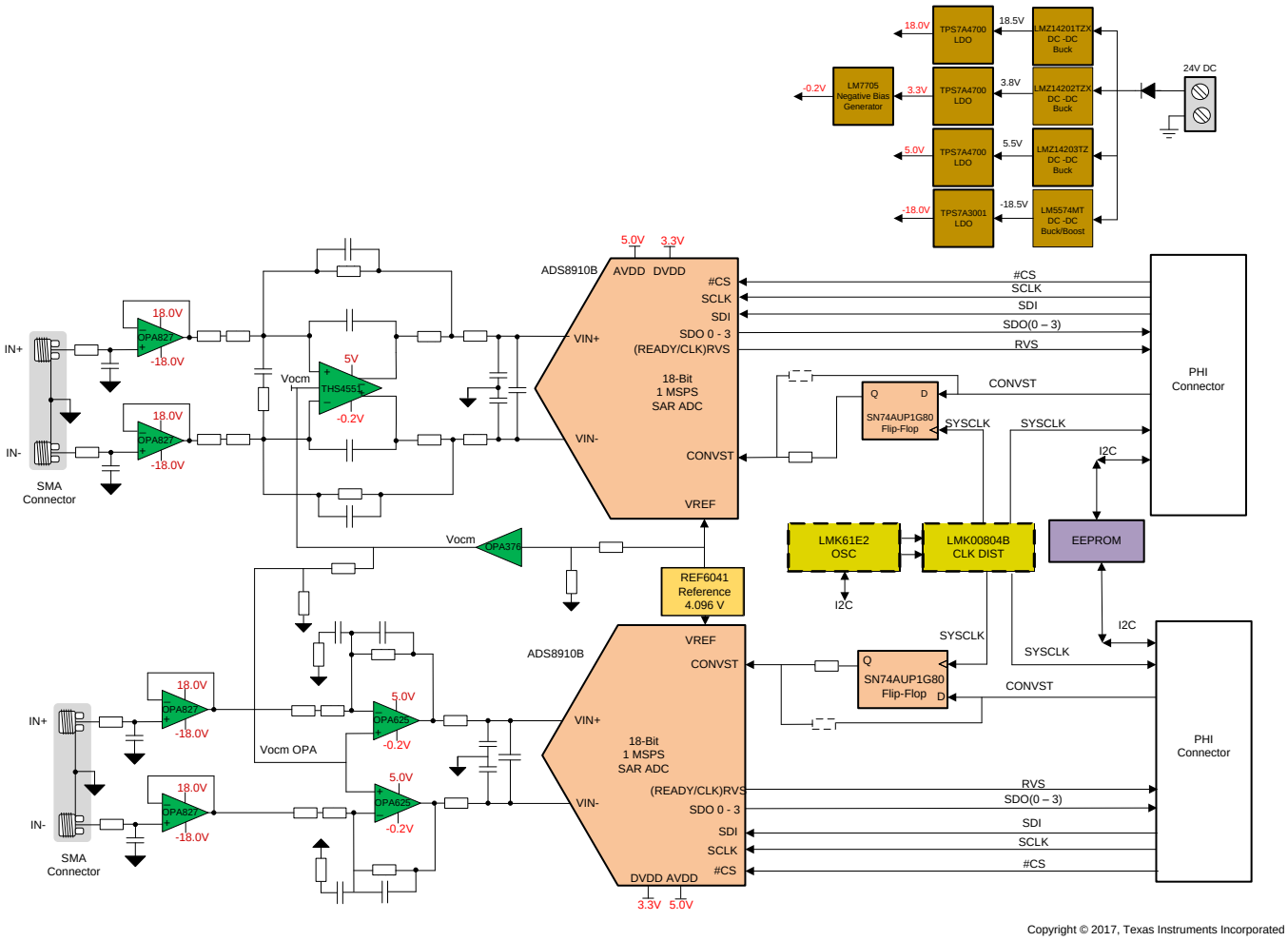


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Figure 3. TIDA-01050 Block Diagram

1.4 System Design Theory

The complexity of automatic test equipment (ATE) systems continues to grow as their application demands ever increasing input channels with some requiring more than 5000. In this reference design, a modular solution is proposed as to promote a design that will scale to the required number of inputs by the application. End equipment such as mixed signal SOC testers, memory testers, battery testers, LCD testers, high-density DAQ cards, high-density power cards, x-ray inspection, and so on require multiple, simultaneous-sampling channels with excellent DC and AC performance, while managing power in order to maximize PCB density. The AFE consists of the high-speed signal chain and the associated point-of-load (POL) power supplies it requires.

In order to optimize the different performance metrics of a modular multisampling ATE system, this TI Design uses two different front-ends to compare the performance and application when used to drive identical high-performance SAR ADCs. One front-end uses a fully differential amplifier (FDA) and the second uses two precision operational amplifiers. The resulting digital data from the ADC output is connected to the Texas Instruments precision host interface (PHI, available for purchase with ADS8910B evaluation board) where the data is analyzed for SNR, THD, and other performance parameters.

The following sections detail the design challenges presented by high channel count systems, including theory, calculations, component selection, simulations, PCB layout design, and measurement results. Unless otherwise noted, TI's SPICE and design developments tools, TINA-TI™ and WEBENCH® were used to aid in development.

1.4.1 OPA827 Buffer

The first stage of the input chain is a buffer stage consisting of two OPA827s. The purpose of this stage is to buffer the input signal at the ±18-V level and achieve very high input impedance. This amplifier was chosen due to its JFET input stage and 36-V capabilities. In addition, the OPA827 has a very good noise performance, which is crucial for this system.

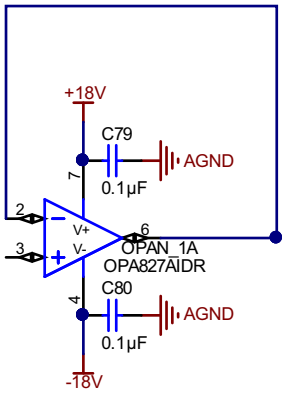

Figure 4. OPA827 Buffer Schematic

The 28-V/µs slew rate of the OPA827 can be used to calculate the maximum frequency that the input signal can be operated at without experiencing slew-induced distortion by re-arranging the full power bandwidth equation.

$$\frac{V_P}{\sqrt{2}} = \frac{SR}{2\pi f} \quad (1)$$

Therefore,

$$f = \frac{SR}{2\pi \frac{V_P}{\sqrt{2}}} \quad (2)$$

This results in:

$$525\ \text{kHz} = \frac{28\frac{\text{V}}{\mu\text{s}}}{2\pi \times \frac{12}{\sqrt{2}}}$$

Based on these equations, this part should be capable of buffering high input amplitude signals up to 525 kHz; however, the THD degradation starts to affect the whole system's performance at the frequency range of 2 kHz and above. This presents the challenge for designing high input swing, high input impedance, high frequency, and high resolution systems. There is always a trade-off between the highest signal amplitude and the frequency range that could be supported if the input signal needs to be buffered. The TI OPA827 was chosen for this TI Design due to its high-performance 36-V JFET input. For systems with the lower input voltage requirements, higher bandwidth parts could be used instead of the OPA827 to support frequencies above 2 kHz.

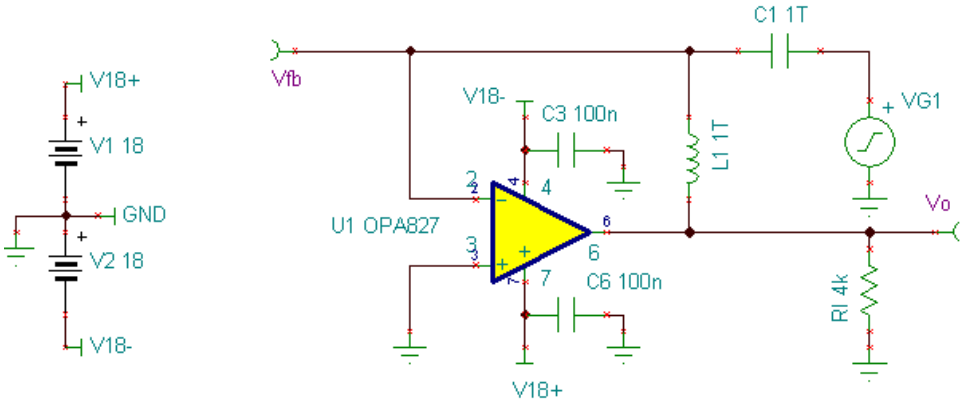

Figure 5. OPA827 TINA-TI Stability Schematic

Figure 5 highlights the schematic used to test the stability of the OPA827 buffer stage. When measuring the stability of an amplifier, it is important to look at the closed-loop noise gain, loaded open-loop gain, and loop gain. The phase margin of the circuit also needs to be sufficient for circuit stability and required settling. See TI's precision labs on op amps for more details on op amp design and amplifier stability.

The TINA-TI schematic in Figure 5 features a 1TF capacitor and 1TH inductor for simulation purposes. This is used to break the feedback loop as the capacitor will be an open at DC while the inductor is a short. At high frequencies, the inductor will be an open and the capacitor will be a short. The load the OPA827 will see by the next stage of the system was also added on the right side of the schematic. This allows for the proper simulation of the circuits stability.

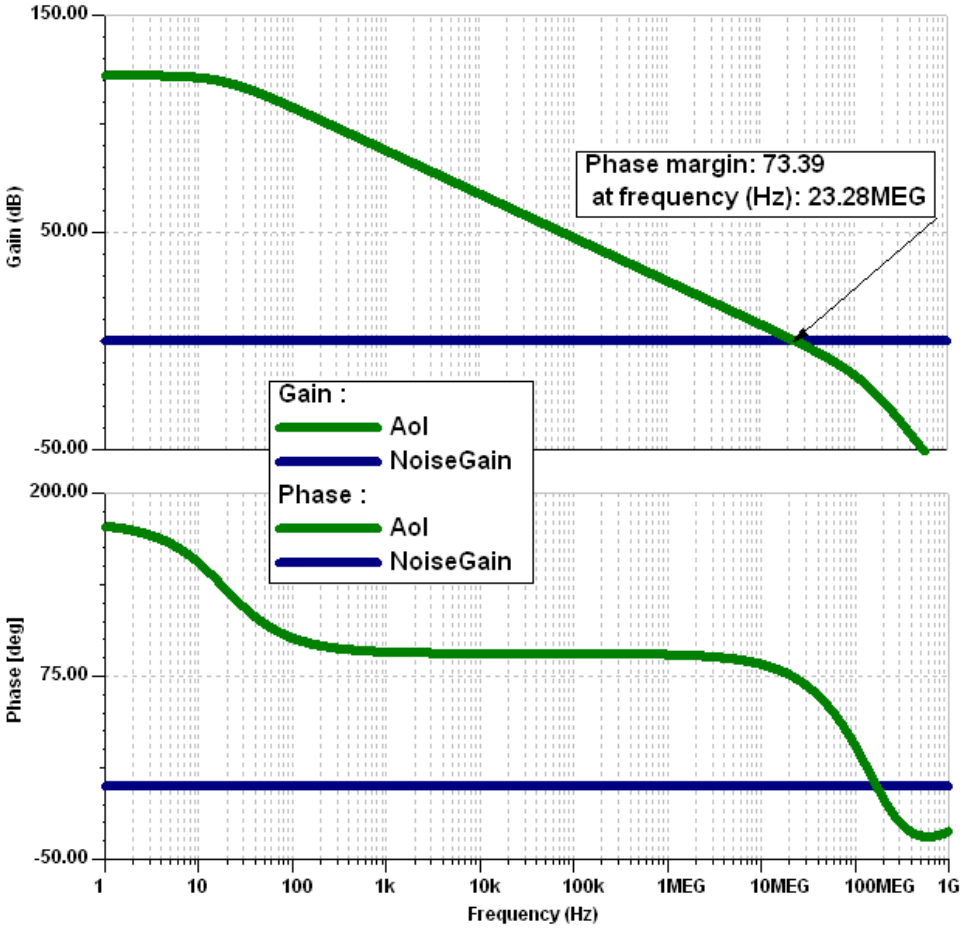

Figure 6. OPA827 TINA-TI Stability Simulation Results

Figure 6 highlights the results from the OPA827 stability simulation resulting in a phase margin of >73º implying stability. It is also important to consider the rate of closure between the loop gain and loaded open loop gain curves. The loaded open loop gain curve is decreasing at –20 dB/decade at the point of intersection with the noise gain curve. The noise gain curve is flat, meaning it is at 0 dB/decade. The rate of closure is thus 20 dB/decade. For a circuit to be considered stable, the rate of closure has to be less than 40 dB/decade. For more information about amplifier stability, see TI's Precision Labs.

To further confirm the functionality of the OPA827 buffer stage, transient simulations were completed to ensure the response is appropriate. Figure 7 illustrates the schematic used in TINA-TI to simulate the transient response of the OPA827 buffer stage. When simulating the transient response of an amplifier, it is important to input a signal with a sharp edge. In this simulation, a 50-mV amplitude 50-kHz square wave is applied to the input and the output response is observed over a 100-µs period.

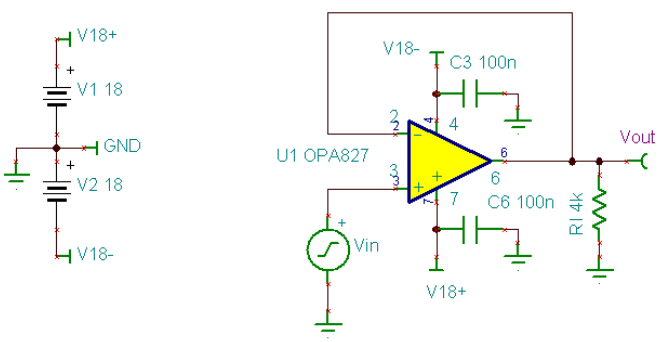

Figure 7. TINA-TI Transient Schematic

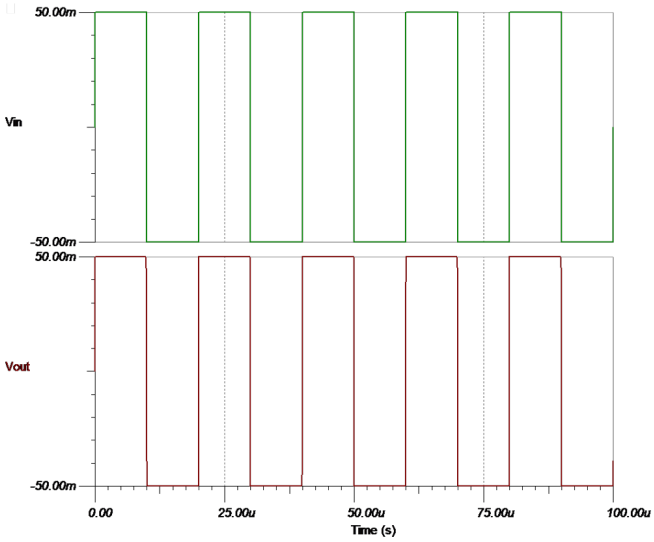

Figure 8. TINA-TI Transient Simulation

Figure 8 illustrates the results of the transient simulation. The output of the OPA827 buffer shows no ringing and only a slight slew limitation at the beginning and the end of each rising and falling edge. From these results, it is concluded that the OPA827 buffer is stable and will perform as expected.

In Figure 4, 0.1-µF decoupling capacitors are placed on both the positive and negative supplies of the OPA827. This is to help remove any noise present on the power supplies. This value is recommended on page 15 of the OPA827 datasheet.

1.4.2 THS4551 Attenuation Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a flywheel RC filter. The amplifier is used for signal conditioning of the input signal, and its low output impedance provides a buffer between the signal source and the ADC's switched capacitor inputs. The RC filter helps attenuate the sampling charge injection from the switched capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful front-end circuit design is required to meet the resolution, linearity, and noise performance of capabilities of ADS8910B. The input op amp must support following key specifications:

1. Rail-to-rail input and output (RRIO)
2. Low noise
3. High small-signal bandwidth with low distortion at high frequencies
4. Low power

For DC signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier datasheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, it is required to verify the settling behavior of the input driver within the simulators such as TINA-TI to help select the appropriate amplifier.

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum of interest known as aliasing. Therefore, an analog antialiasing filter must be used to remove the noise and harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass RC filter, where the 3-dB bandwidth is optimized based on specific application requirements.

For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the signal at the inputs of the ADC during the small acquisition time window.

For AC signals, keeping the filter bandwidth low is desirable to band-limit the noise fed into the input of the ADC and thereby increasing the system SNR. Besides filtering the noise from the front-end drive circuitry, the filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected from each input pin of the ADC to the ground (as shown in Equation 3 and Figure 9).

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 15 times the specified value of the ADC sampling capacitance. For the ADS8910B, it is recommended to keep C_{FLT} greater than 900 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (3)$$

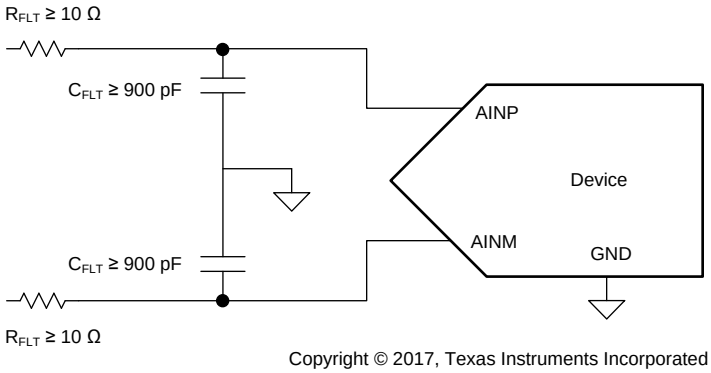

Figure 9. Antialiasing Filter Configuration Diagram

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT} or R_{ISO}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For the ADS8910B, limiting the value of R_{FLT} to a maximum of 10 Ω is recommended to avoid any significant degradation in linearity performance. The tolerance of the selected resistors must be kept less than 1% to keep the inputs balanced. The driver amplifier must be selected such that its closed-loop output impedance is at least five times lesser than the R_{FLT}.

Following the OPA827 is the THS4551 for one of the ADC drivers. The THS4551 is a fully differential amplifier specifically designed to be used with high performance SAR ADCs. In this TI Design, the THS4551 needed to be implemented as an attenuator in order to ensure the ADC input is between 0 and 4.096 V. The gain of this stage is configured to be 1/8. RDP1 and RDP2 in Figure 10 are connected in series to give 4.00 kΩ while R101 is 499 Ω. These values give a gain of 1/8. RDN1, RDN2, and R101 deliver the same gain for the negative input to the fully differential amplifier. Additionally, R99, C83, C87, C86, R211, R212, R103, R104, C89, C90, C315, C316, and C317 were added to ensure stability. The selection of these components is discussed in detail here. R211 and R212 are 0-Ω placeholder resistors for later study (for example, incase larger isolation is required). Capacitors C89, C90, and C315 are flywheel or "charge bucket" capacitors designed to quickly charge the sample and hold circuit inside the ADC. It is important to place the single ended capacitors C89 and C90 from each ADC input to GND in addition to the differential capacitor C315 to ensure the common-mode voltage is stable during the switching of the sample and hold circuit.

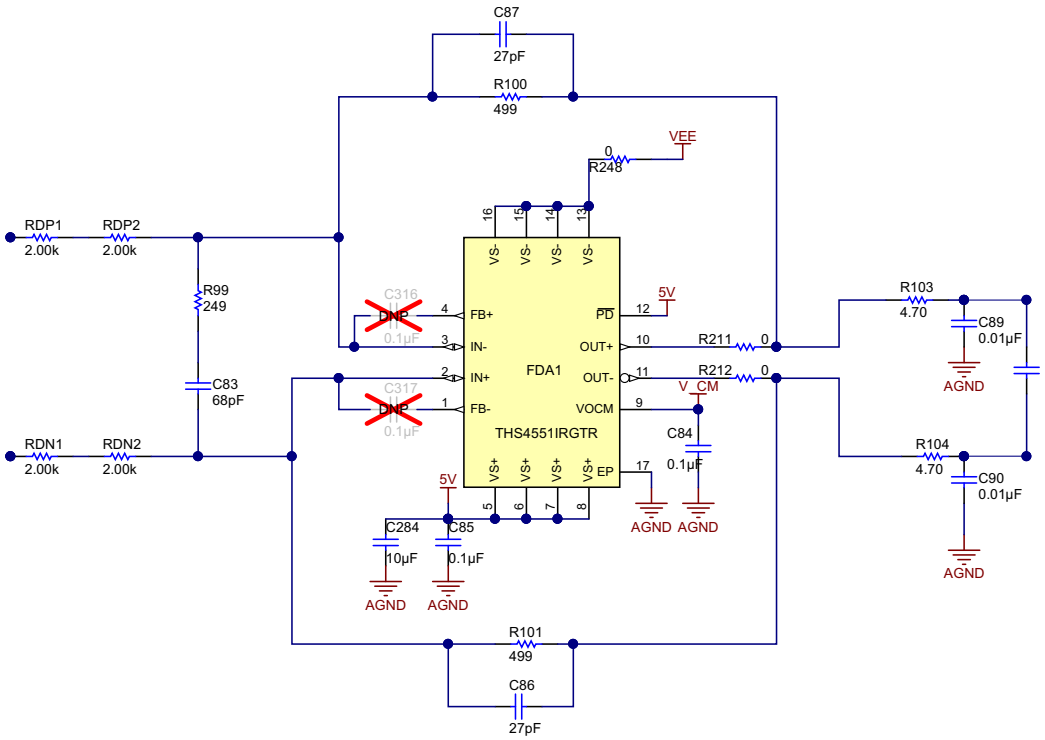

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Figure 10. THS4551 Stage Altium Schematic

First determining the values of R103 and R104 was done by comparing the THS4551 output impedance versus the ADC load impedance. The schematic used to simulate the output impedance is shown in Figure 11.

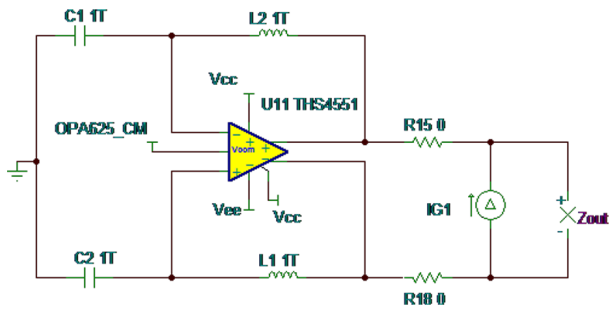

Figure 11. THS4551 Output Impedance Simulation

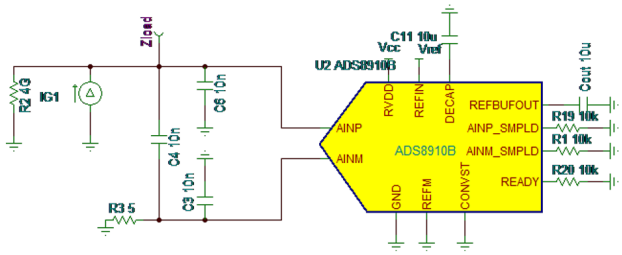

Figure 12. ADS8910B Load Impedance Simulation

The results of the two impedance calculations are compared in Figure 13.

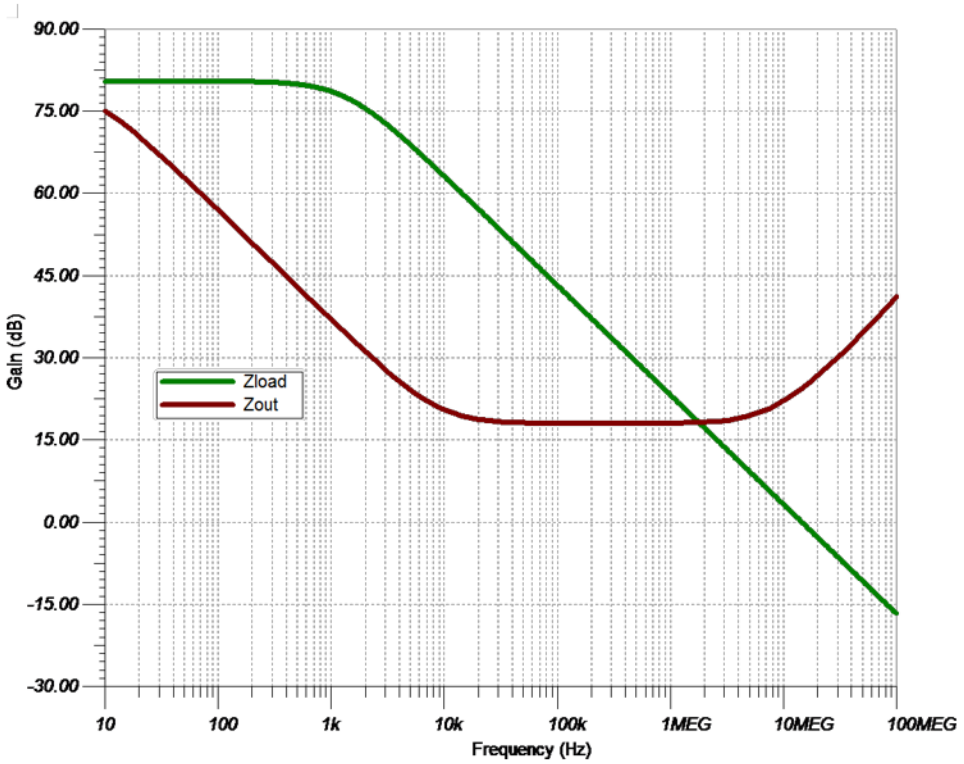

Figure 13. Zout versus Zload THS4551

As seen in the simulation results in Figure 13, the load impedance curve is falling while the output impedance curve is rising at the point of the intersection. In order to flatten the output impedance response to ensure stability, a series output isolation resistance of 4.7 Ω was added.

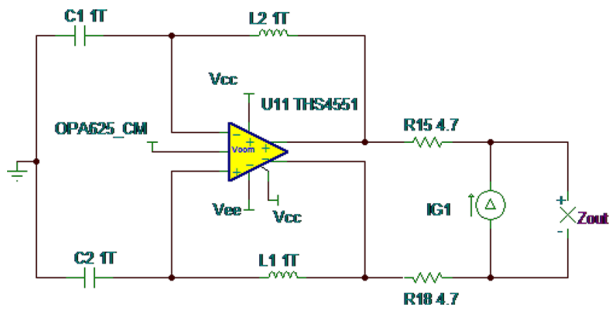

Figure 14. THS4551 R_{ISO}

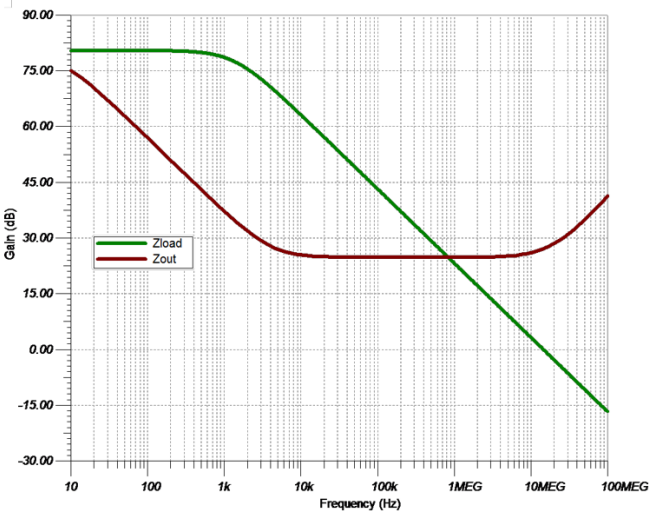

Figure 15. THS4551 With R_{ISO} Compensation

Figure 15 highlights the results of simulating the THS4551 output impedance after the isolation resistance was added. The load impedance curve crosses the output impedance curve at a frequency where the impedance is constant, improving robustness.

Next, the full driver-ADC subsystem stability simulations were performed as shown in Figure 16.

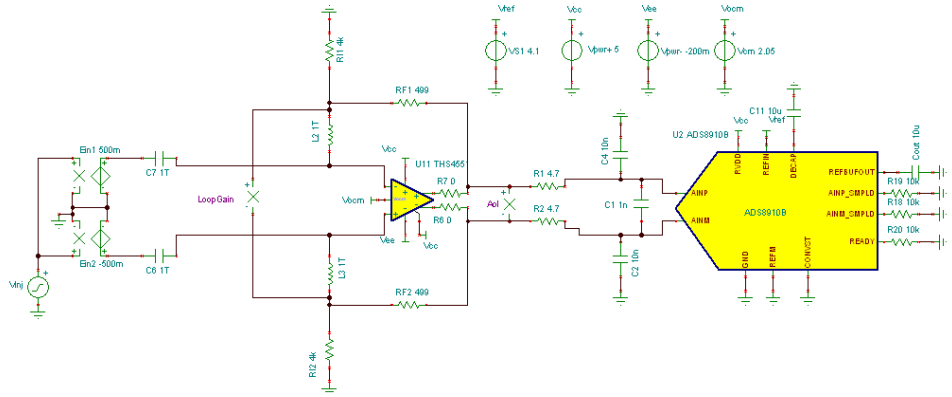

Figure 16. THS4551 Initial Stability Schematic

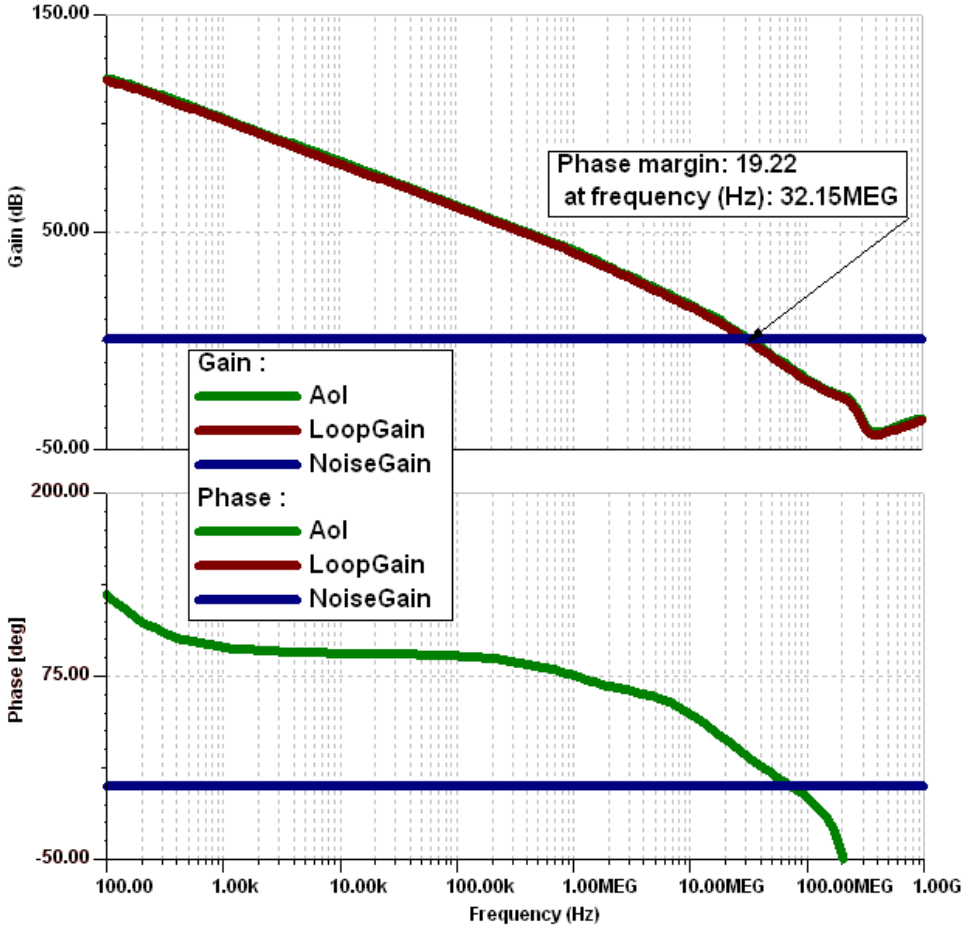

Figure 17. THS4551 Initial Stability Results

Figure 17 indicates a marginable stable circuit where the phase margin is less than 45° and thus prone to ringing and long transient settling characteristics. For a circuit to be stable it is desirable for the rate of closure between the open loop gain and the noise gain to be less than 40 dB/decade and the phase margin greater than 45° throughout the bandwidth. This is achieved from raising the noise gain by introducing a pole and zero with a capacitor and resistor between the two feedback loops.

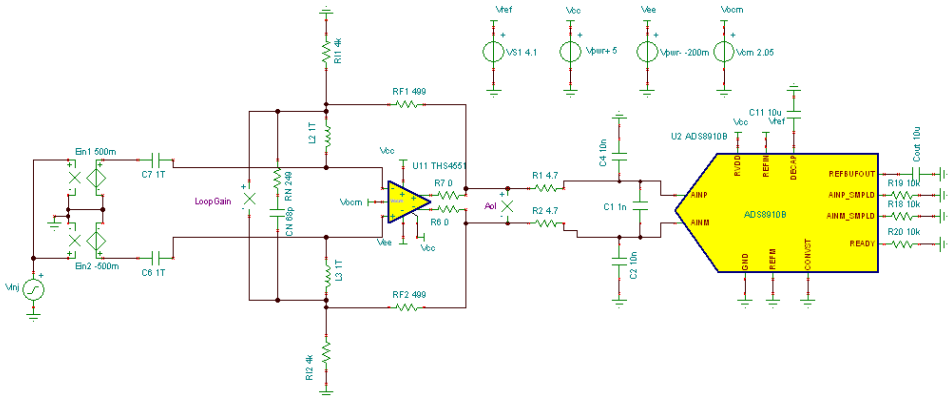

Figure 18. THS4551 Pole and Zero 1 Stability

As seen in Figure 18, a 249-Ω resistor (RN) and a 68-pF capacitor (CN) were added in between the two feedback loops of the THS4551. The intent of this is to raise the noise gain curve before the intersection with the open loop gain curve.

The zero value was calculated first. It needs to be one decade before the pole to achieve this goal. The formula for a zero in the noise gain curve is:

$$fz1 = \frac{1}{2\pi \times (RN\_eq + RI \,||\, RF) \times (CN\_eq)} \tag{4}$$

where:

- RN_eq = RN / 2
- CN_eq = CN × 2

$$fp1 = \frac{1}{2\pi \times RN \times CN} \tag{5}$$

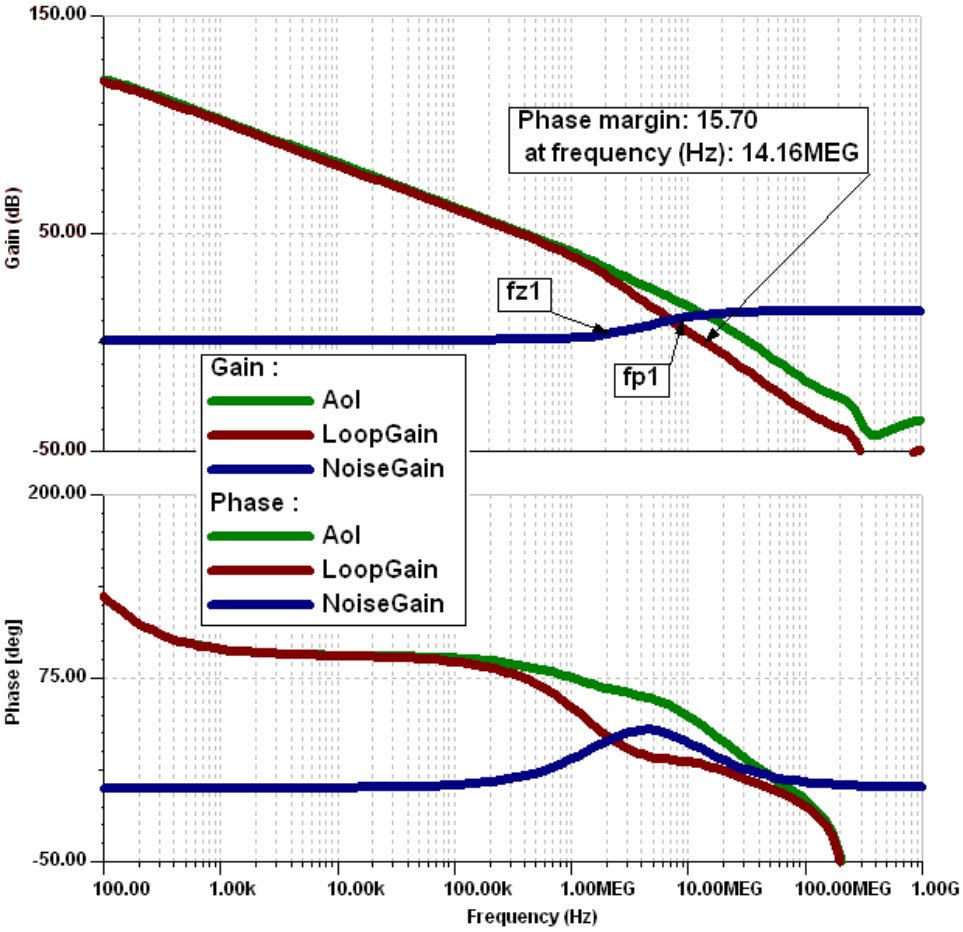

Figure 19. THS4551 Pole and Zero 1 Stability Results

As seen in Figure 19, the addition of the first pole and zero is not enough to make the circuit stable. The rate of closure is still 40 dB/decade and the phase margin is still below 45º. To further compensate for the stability, a second zero and a pole were added to the noise gain curve in an attempt to cross the noise gain curve with the loop gain curve at a rate of closure less than 40 dB/decade.

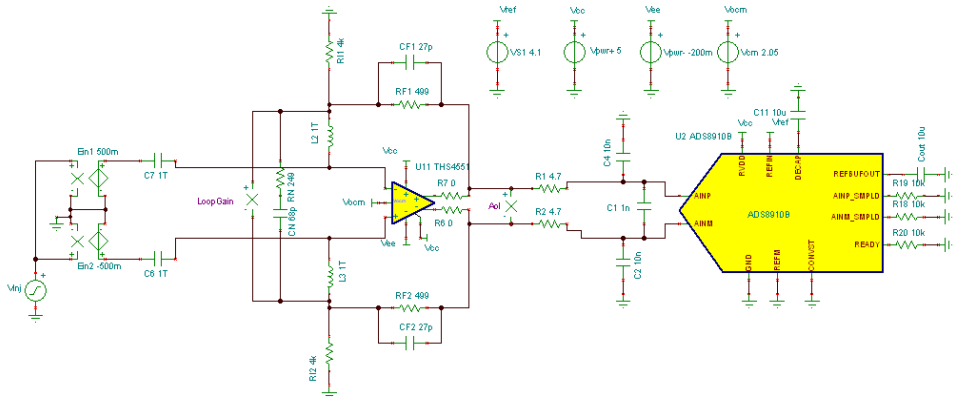

Figure 20. THS4551 Zero 2 Stability

Figure 20 shows the simulated schematic with the added 27-pF capacitor CF in the feedback loop of the THS4551. This capacitor will generate a second pole and a high-frequency zero in the noise gain curve, and the formula to compute the frequency of this pole is:

$$fp2 = \frac{1}{2\pi \times RF \times CF} \quad (6)$$

The same AC analysis test was then ran again and the results are shown in Figure 21:

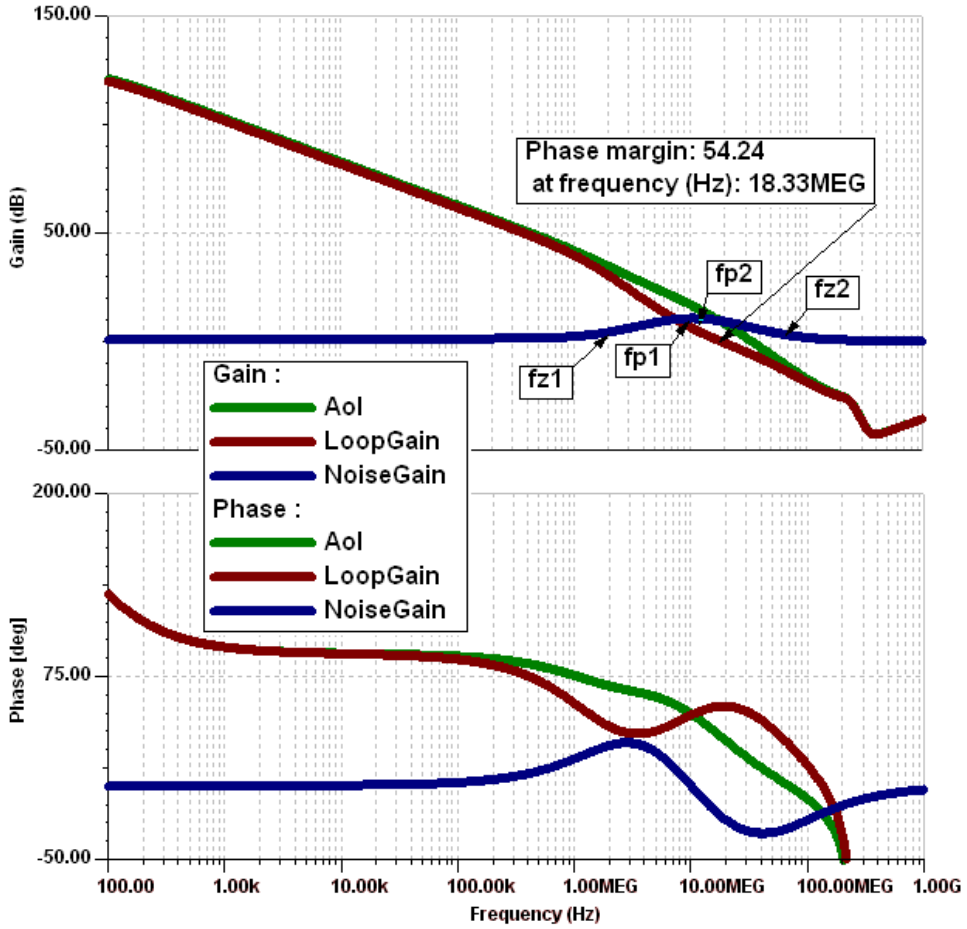

Figure 21. THS4551 Stability Results

Figure 21 highlights the results of the AC analysis demonstrating acceptable phase margin and the rate of closure between the loop gain and noise gain curves are less than 40 dB/decade. These are indications of a stable circuit. To learn more about amplifier stability, see TI's Precision Labs.

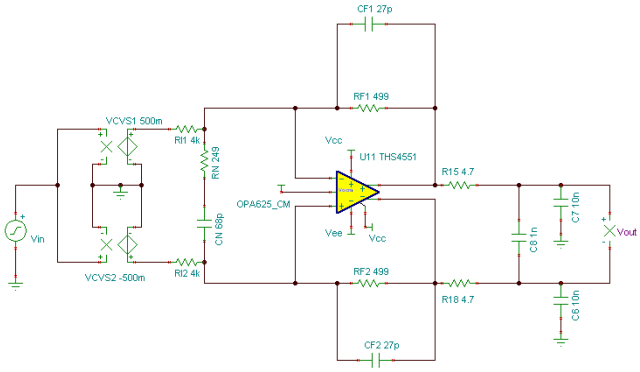

Figure 22. THS4551 TINA-TI Transient Schematic

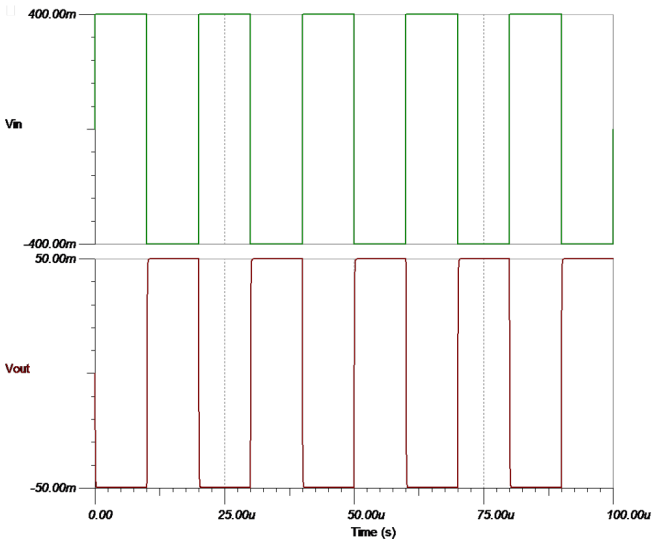

Figure 23. THS4551 TINA-TI Transient Results

Transient response simulations were also completed for the THS4551 stage to further ensure the proper functionality of this stage. As with the OPA827 simulations, a 400-mV peak-to-peak, 50-kHz square wave is input to the circuit and the output is observed. Figure 23 displays the results of the transient response simulation of the THS4551 attenuator. As seen, the output is a 50-mV square wave, which corresponds to the expected gain of 1/8. There is no oscillation present on the output so this stage is considered stable.

In Figure 10, it is seen that the Power Down pin (pin 12) of the THS4551 is connected to 5 V. The power down pin is logic low, meaning that when it is grounded, the chip is in power off mode. When this pin is high, it is in normal operation mode. For this application, the amplifier will always be in normal operation mode. Pin 17 is the thermal pad and is connected to ground to ensure that the chip has a proper heat sink. The voltage driven at the common-mode voltage pin is 2.048 V and its significance is discussed in greater detail in Section 1.4.7.5.

1.4.3 Dual OPA625 Attenuation Driver

The OPA625 is designed to drive precision (up to 18-bit) SAR ADCs at sample rates up to 2 MSPS. The combination of low output impedance (1 Ω at 1 MHz), low THD, low noise (2.5 nV/√Hz), and fast settling time (4-V step, 16-bit levels within 280 ns) make the OPA625 the ideal choice for driving both the SAR ADC inputs as well as the reference input to the ADC.

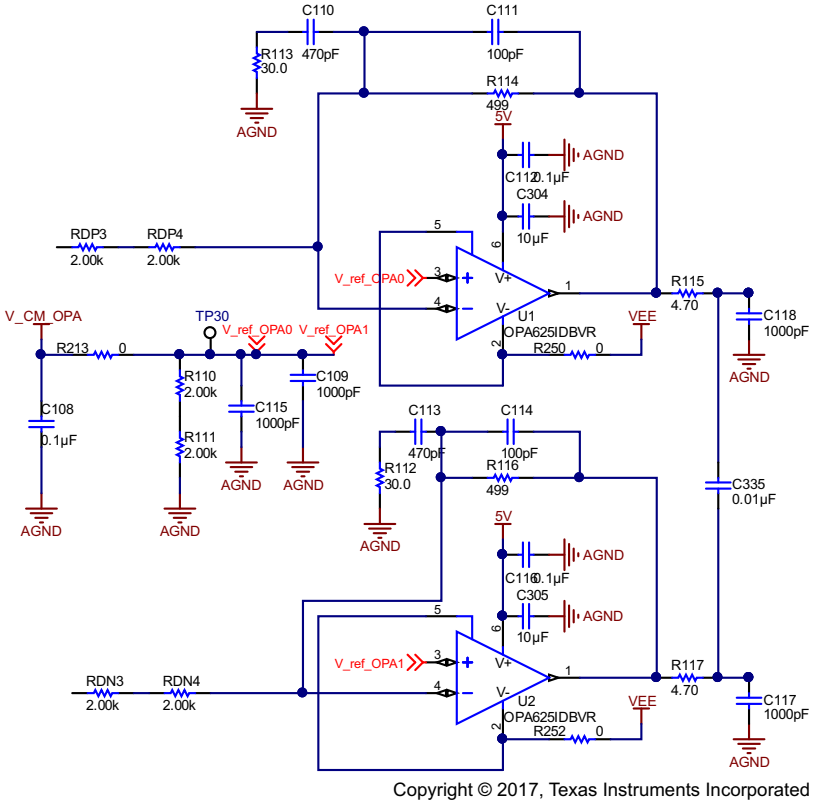

Figure 24. Dual OPA625 Stage Altium Schematic

The second channel used a different front-end attenuator driver stage so that the performance of the two could be compared. Similar to the THS4551 driver, the gain of this stage is 1/8. This is executed with RDP3, RDP4, and R114 for the positive signal and RDN3, RDN4, and R116 for the negative signal. A similar approach was taken with the OPA625s to ensure circuit stability. The value of the isolation resistance was found by comparing the output impedance with the load impedance and again a value of 4.7 Ω was chosen.

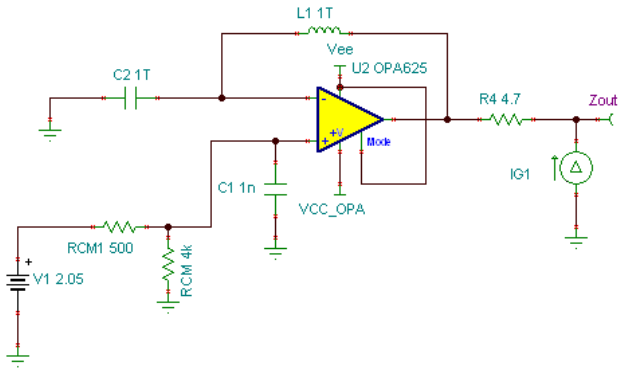

Figure 25. OPA625 Isolation Resistance

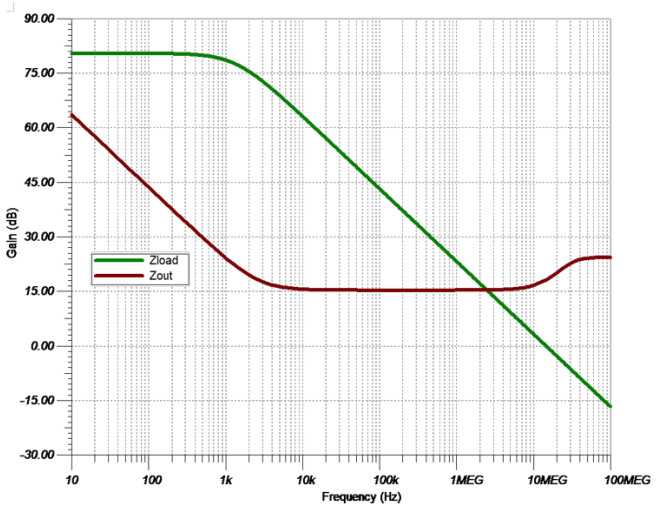

Figure 26. OPA625 Z_{OUT} versus Z_{LOAD} Fixed

Figure 25 and Figure 26 highlight the results of the OPA625 output impedance when adding the 10-Ω isolation resistance. The load impedance curve now crosses the output impedance curve at a point where the slope of the output impedance curve is 0.

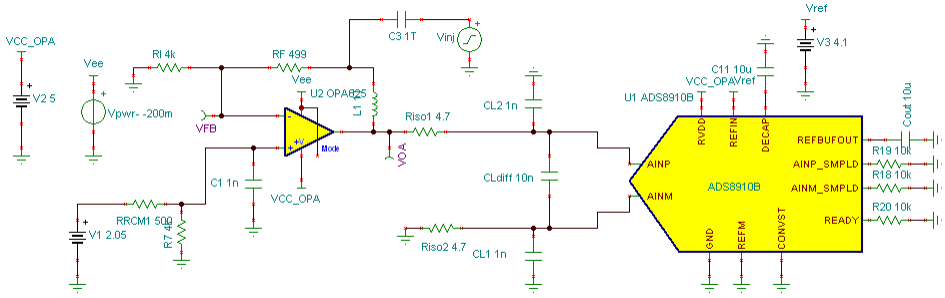

Figure 27. OPA625 Initial Stability Simulation

Next, stability simulations were performed to ensure the complete circuit would perform as expected. Figure 27 highlights the schematic used to perform this simulation. Again, a 1TF capacitor and 1TH inductor were used to break the loop in the simulation.

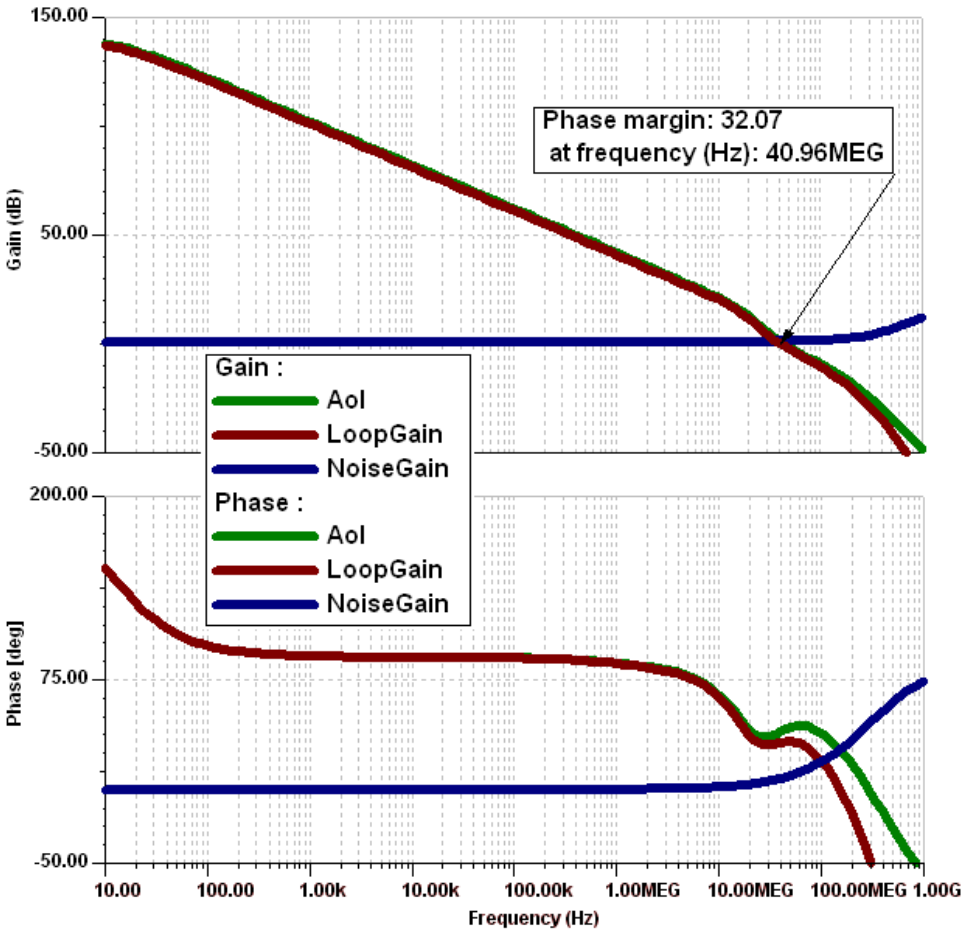

Figure 28. OPA625 Initial Stability Results

Figure 28 highlights the results of the initial stability simulations. The circuit will be marginally stable due to the phase margin being below 45 degrees. The same approach as with the THS4551 was taken here; initially a pole and zero were generated on the noise gain curve.

The formula for a zero in the noise gain curve is:

$$fz1 = \frac{1}{2\pi \times (RN + RI \,||\, RF) \times (CN)} \tag{7}$$

The formula to calculate the pole frequency is:

$$fp1 = \frac{1}{2\pi \times RN \times CN} \tag{8}$$

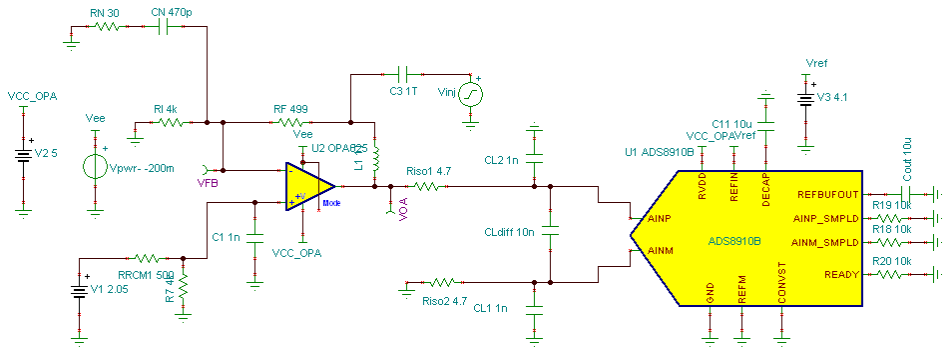

Figure 29. OPA625 First Pole and Zero Schematic

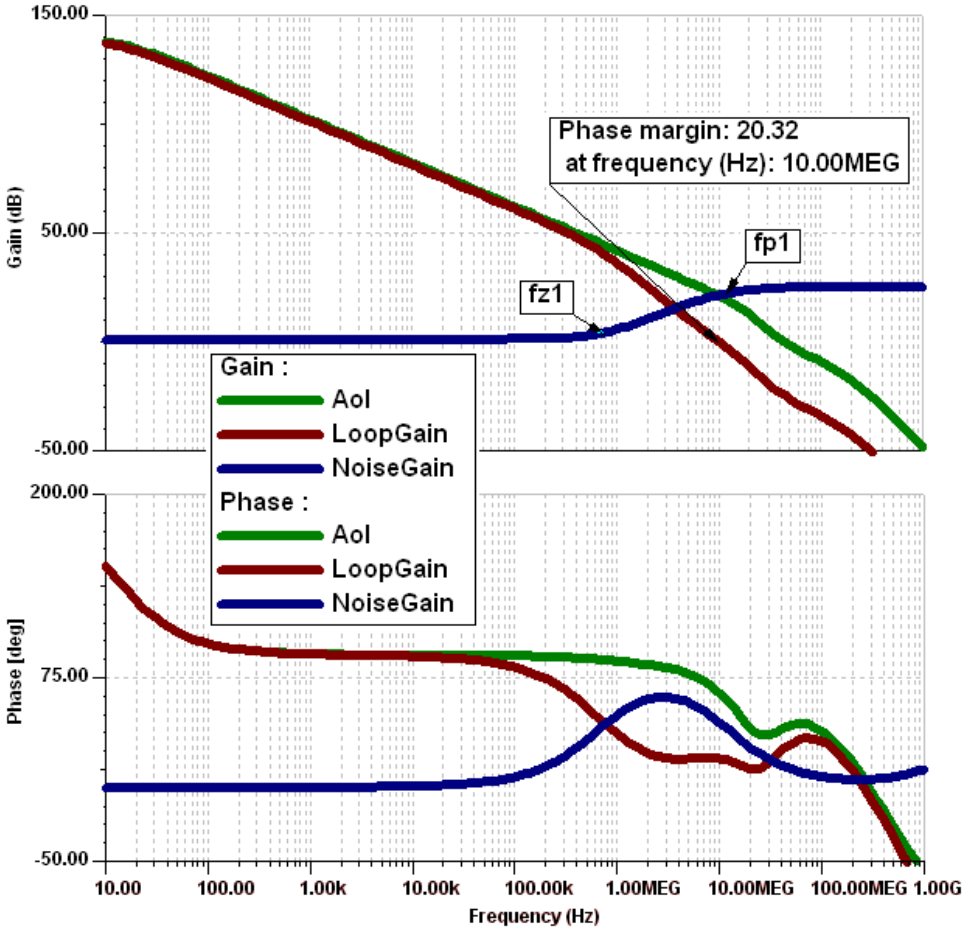

Figure 30. OPA625 First Pole and Zero Simulation Results

By adding the first pole and zero using RN and CN, there is an increase in the noise gain curve. The next step is to add a second pole and zero on the noise gain curve to bring it down during the intersection with the loaded open loop gain. This will be achieved by adding CF. The formula for the second pole is:

$$fp2 = \frac{1}{2\pi \times RF \times CF} \quad (9)$$

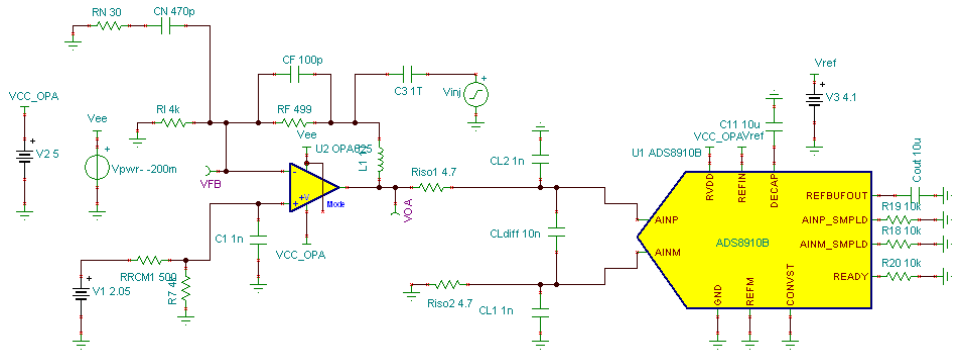

Figure 31. OPA625 Stage Stability Schematic

Figure 31 highlights the addition of the 100-pF capacitor in the feedback of the OPA625. This schematic was then simulated with an AC analysis. The results are shown in Figure 32.

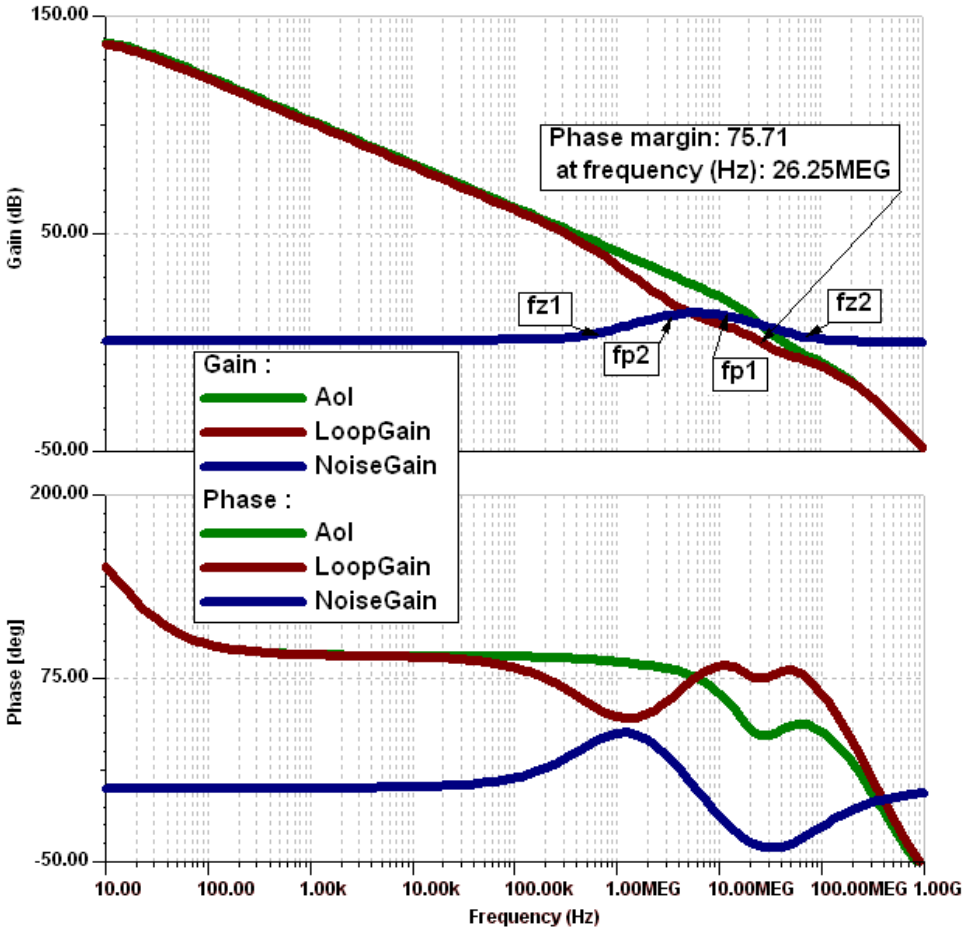

Figure 32. OPA625 Stage Stability Simulation Results

Figure 32 illustrates the results of the stability simulations of the OPA625 stage from TINA-TI. The rate of closure between the noise gain curve and the loaded open loop gain is less than 40 dB/decade. This is achieved by generating the boost in the noise gain curve with two poles and two zeros using CN, RN, and CF. An isolation resistor of 4.7 Ω is also added to improve the stability of this circuit. Figure 32 also highlights the phase margin of the OPA625 stage. The phase margin is shown to be 75.71°, which is more than sufficient for stability.

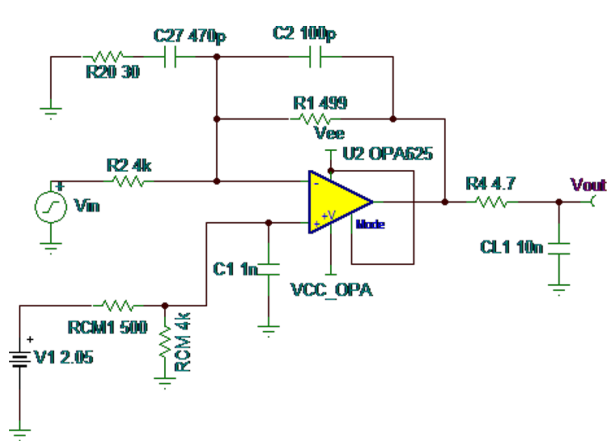

Figure 33. OPA625 TINA-TI Transient Schematic

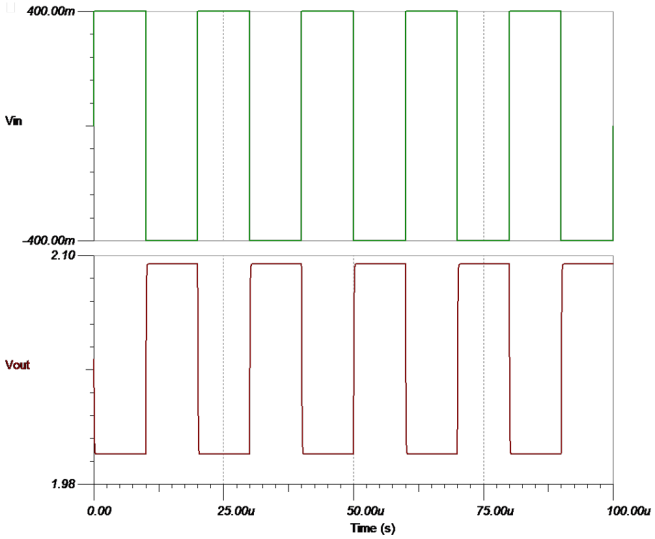

Figure 34. OPA625 TINA-TI Transient Results

The OPA625 is also simulated for its transient response to ensure proper functionality and stability of the circuit. Figure 33 illustrates the TINA-TI circuit used to complete this simulation. Again, a 400-mV amplitude, 50-kHz square wave input is used to test the transient response of this circuit. Figure 34 highlights the results from the transient simulation of the OPA625. The output is a 50-mV square wave, which corresponds to a gain of 1/8 as expected.

The output of the OPA625 is centered at 2.048 V, which is the midpoint of the reference voltage of the ADC. In Figure 24, the non-inverting inputs of the OPA625's are connected together; this is done to make the two OPA625's work in the same fashion as a fully differential amplifier.

The common-mode voltage for the OPA625's has to be slightly lower than that of the THS4551 to compensate for the OPA625 gain. Thus, another resistor divider is used to drop the common-mode voltage. The generation of the 1.82-V common-mode voltage will be discussed in further detail in Section 1.4.7.5.

1.4.4 Driver Amplifier Comparison

It is crucial that the noise of the buffer stage of an ADC driver is kept to an absolute minimum. The analog signal going into the ADC must be as pure as possible. Any noise added to the analog signal will transfer through into the digital signal leading to inaccuracies and poor data integrity. When comparing the performance of the Dual OPA625 Driver and the Single THS4551 FDA Driver, there are advantages and disadvantages to both. The final decision on which front-end to use will be based on the system bandwidth, THD and power consumption requirements.

The FDA architecture can grant a benefit in total harmonic distortion (THD) through the reduction of the second harmonic distortion (HD2). When comparing the two configurations, an improvement of up to 4 dB in THD can be observed when using an FDA.

When comparing the power consumption and noise for both ADC driver configurations the total number of amplifiers needs to be taken into consideration. Because two OPA625s are used in a single-ended configuration, the power specification found in the datasheet must be multiplied by a factor of 2 and noise specification must be multiplied by √2. This results in a total quiescent current consumption of 4 mA for the two OPA625s and noise of 3.54 nV/√Hz. Comparing this to the THS4551 where just one device is used, the total quiescent current consumption is just 1.35 mA and noise us 3.3 nV/√Hz.

The noise levels of both front-ends were compared in simulation and the results were compared. TI's Precision Labs covers amplifier noise analysis in detail and is highly recommended for understanding noise theory.

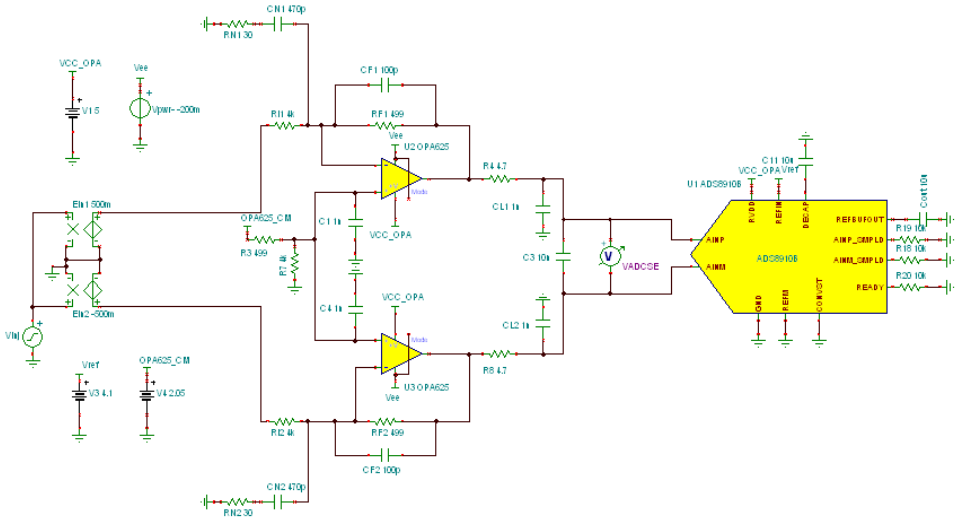

Figure 35. OPA625 TINA-TI Schematic for Noise Simulations

Figure 35 shows the schematic used to simulate the noise from the OPA625 front-end. The ADC model was also placed in this simulation to further improve the accuracy of the results.

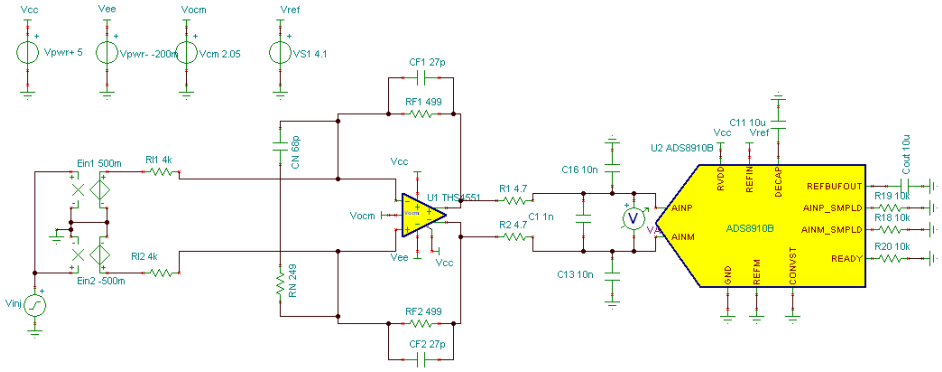

Figure 36. THS4551 TINA-TI Schematic for Noise Simulations

Figure 36 shows the schematic used to simulate the noise from the THS4551 front-end. The ADC model was also placed for this simulation to further improve the accuracy of the results.

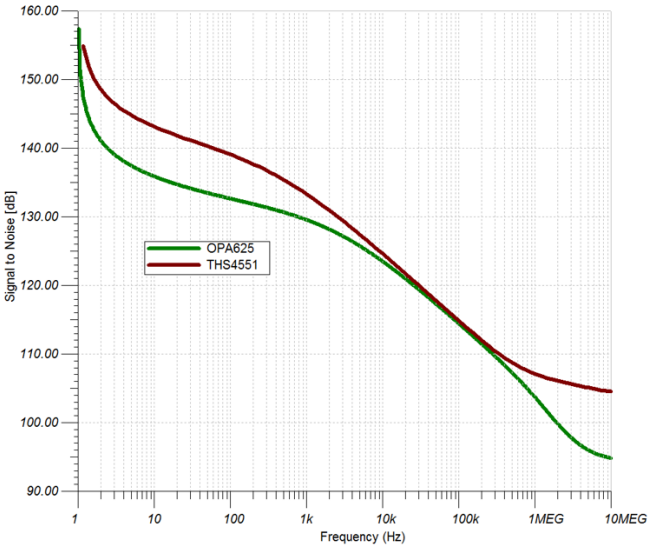

Figure 37. SNR Simulation

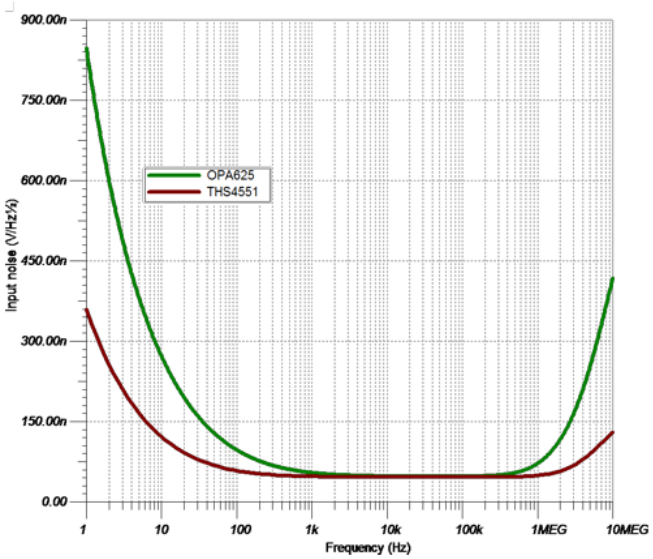

Figure 38. Input Noise Comparison

TINA-TI was also used to simulate the signal to noise ratio of both the front-ends. The plot is shown in Figure 37. Throughout the bandwidth, the THS4551 achieves better noise performance.

When comparing the input noise of both amplifiers in Figure 38, the results are similar to that of the SNR simulation.

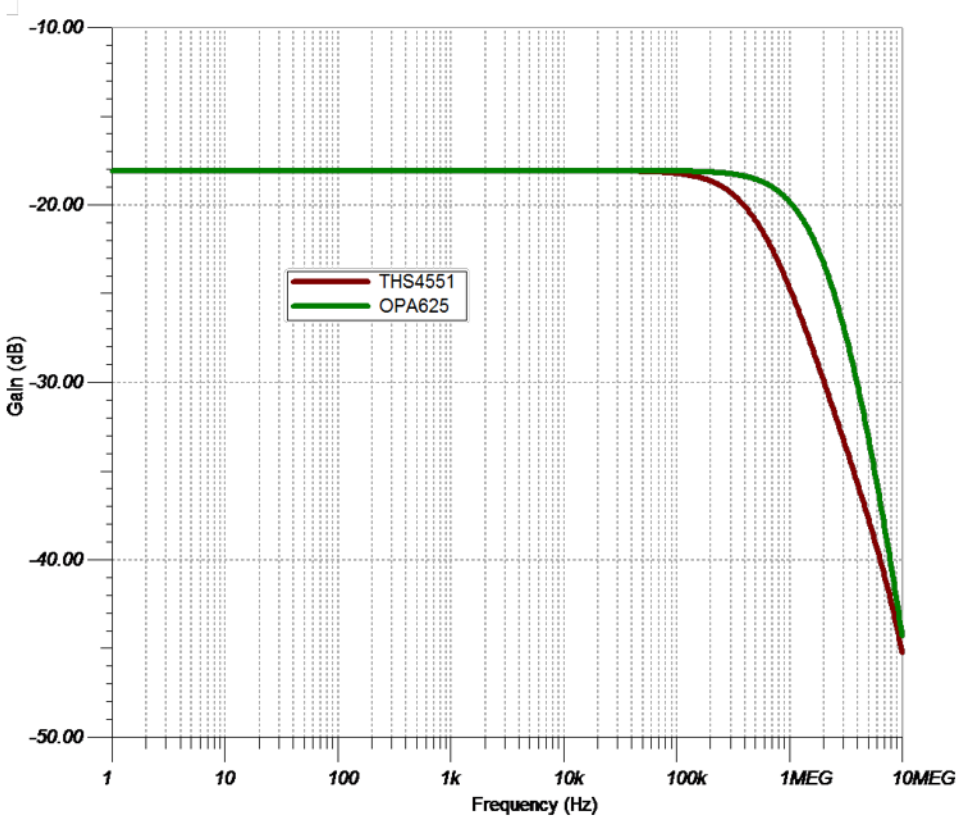

Figure 39. Loaded Bandwidth Comparison

Figure 39 highlights the loaded bandwidth of both amplifier configurations. Both front-ends are configured to have similar bandwidth to allow for a direct comparison of the front-end performance.

In this systems configuration, with a gain of 1/8, the simulated input voltage noise is 46 nV/√Hz at 10 kHz. Simulating the OPA625 in the 1/8 gain configuration, a simulated input voltage noise of 47.77 nV/√Hz is achieved. Again, this value is only slightly worse than the simulated value of the THS4551.

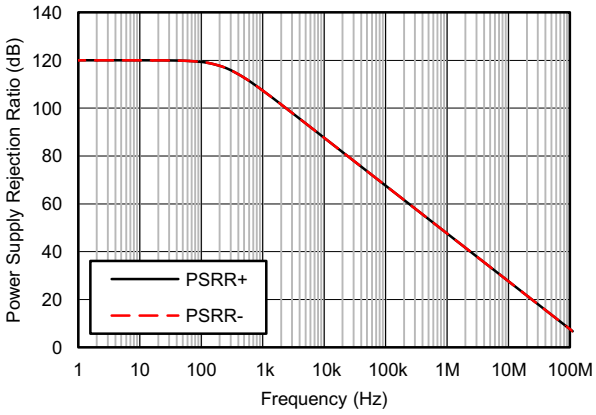

Figure 40. OPA625 PSRR

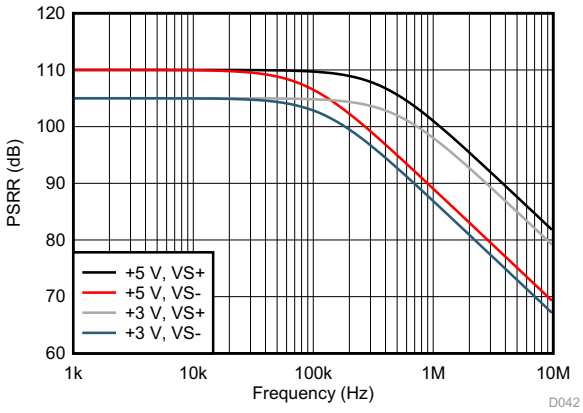

Figure 41. THS4551 PSRR

Figure 40 and Figure 41 highlight the power supply rejection ratios of both parts. The THS4551 has a much better PSRR at higher frequencies than the OPA625. This could lead to a cleaner spectrum and better SNR performance if there is some noise on the supply rails. In this reference design, the power supplies are generated using switching regulators, which results in some noise on the amplifier supplies.

In applications where power consumption is crucial, the THS4551 will most likely be the preferred device. As mentioned previously, two OPA625s have almost 3× power consumption compared to the THS4551. The slew rate of the THS4551 is also much better than that of the OPA625. The THS4551 features a slew rate of 220 V/µs while the OPA625 has a slew rate of 115V/µs. However, when configuring the OPA625 as a differential amplifier, the single-channel slew rate will be doubled. This results in a slew rate of 230V/µs for the OPA625s, which is almost identical to the THS4551. Both devices are recommended for precision SAR ADC drivers in their respective datasheets.

When comparing THD values of the two amplifiers, it is important to consider the second-order harmonic distortion as the FDA should grant further benefits. The OPA625 specifies a HD2 value of 122 dBc at 100 kHz while the THS4551 specifies an HD2 value of 128 dBc at 100 kHz at 2 V_{PP} at the output. Certain applications may be more concerned with current noise than voltage noise so this specification was also compared. As the source resistance increases, the current noise increases and may dominate the amplifier's noise performance.

Channel density is an important design characteristic for multichannel systems. Both solutions require approximately the same area if a two-channel version of the OPA625 packaged in an 8VSSOP (15 mm^2). However, the THS4551 is also available in a 10QFN (4 mm^2) and is a smaller solution if two separate OPA devices are used. The necessary external resistors and capacitors for each solution dominate required area where the THS4551 solution contains 25 external components and the dual OPA625 contains 31 components. The layout used in this TI Design is not fully optimized for space consumption as it includes many 0-Ω jumper resistors for further study. However, the fact that the OPA625 driver will require more external components still remains.

When using two OPA625s in this TI Design, it is likely that two single-chip packages will be used rather than one dual chip package. This is due to the fact that for this application, a fully differential amplifier is implemented with two single-ended amplifiers. To match the parasitics on both the positive and negative channels, it is recommended to use two single-chip packages as it is much easier to get a symmetrical layout. This is crucial in ensuring both the positive and negative signal traces are of equal length on the PCB.

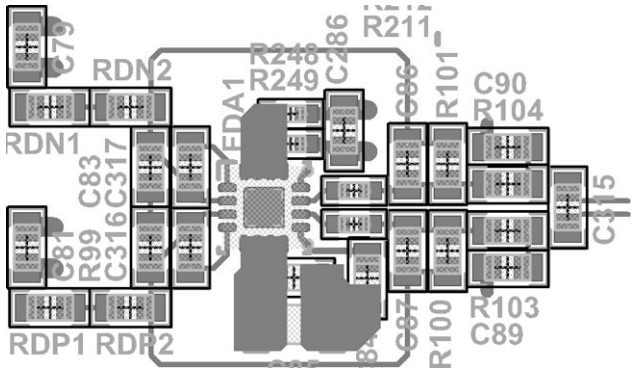

Figure 42. THS4551 Layout

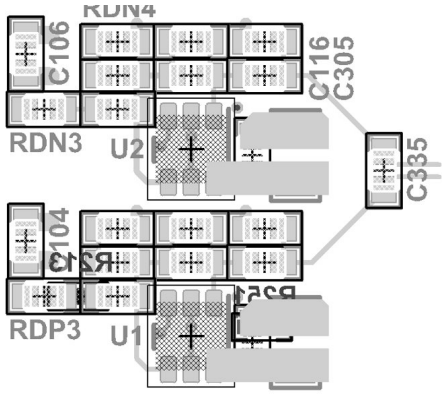

Figure 43. Dual OPA625 Layout

Figure 42 and Figure 43 highlight the differences in layout between the two amplifier options. As seen, the OPA625 configuration uses two single channel devices to ensure a symmetrical layout. This is not an issue with the THS4551 as only one chip is needed and it is much simpler to get a symmetrical layout. Also, it is evident that the OPA625 configuration requires a larger amount of external circuitry.

See the TIDA-01053 product page for the noise and THD comparison of both implementations in gain = 1 configurations.

1.4.5 ADS8910B ADC and Conversion Start Sync

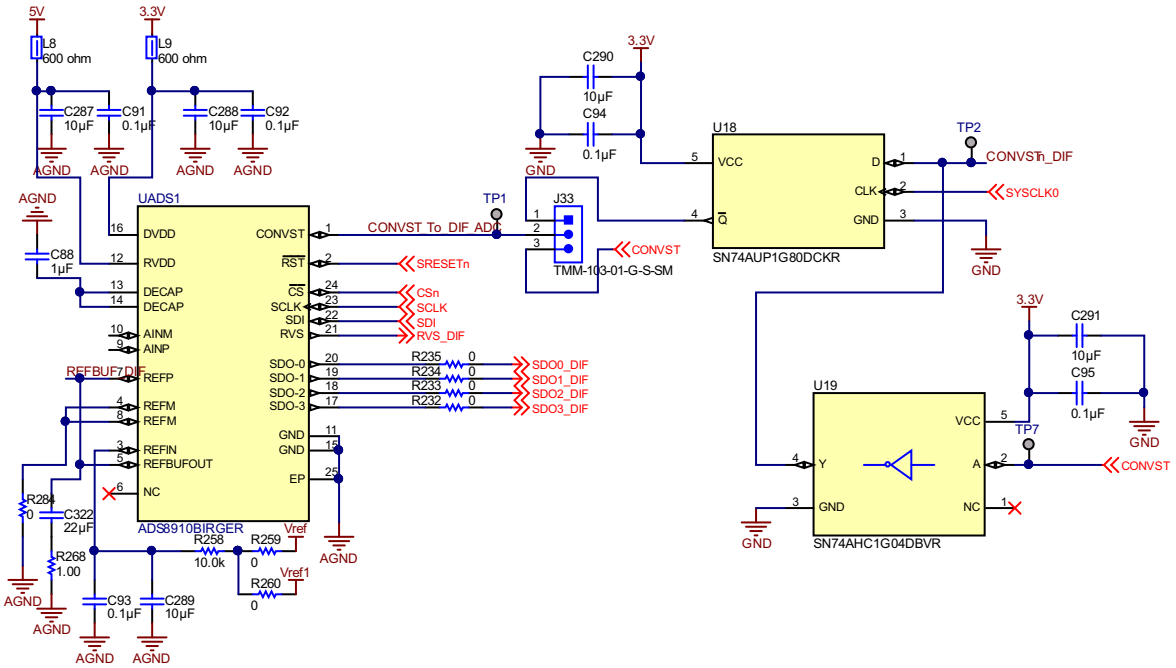

Figure 44. ADS8910B and CONVST Sync Stage Altium Schematic

Two ADS8910B high-speed SAR ADCs are used to convert data from an analog to a digital signal. The ADC is directly following either the THS4551 fully differential amplifier driver stage, or the two OPA625s configured as a differential amplifier driver stage. The outputs of the driver stages are directly fed into the AINP and AINM pins on the ADS8910B. The ADS8910B is powered by both 5 and 3.3 V. RVDD is the analog supply and DVDD is the digital supply. As seen in Figure 44, ferrite beads are placed in between the voltage input pins and the voltage rails to help filter any noise on the power supply rails. C287, C288, C91, and C92 are also added as decoupling capacitors to further help with the filtering of the power supply. For the DECAP pins (pin 13 and pin 14) a decoupling capacitor is placed here with the two pins

shorted together. This implementation is described in the ADS8910B datasheet on under Pin Functions. A 1-µF capacitor is used for DECAP as that is what is used in the Electrical Characteristics section of the datasheet. Pin 7 on the ADC or REFP/REFBUFOUT is shorted to pin 5, REFBUFOUT. This is suggested in the datasheet under Pin Functions. A 22-µF capacitor and a 1-Ω resistor were then connected between this node and ground in series. The capacitor value is suggested in the datasheet under recommended operating conditions as the nominal value for CREFBUF. The 1-Ω resistor is added as a place holder in case the impedance of the reference buffer capacitor needed to be adjusted. Pins 4 and 8, or the REFM pins were shorted together and attached to ground. These pins are the reference voltages ground potential and must be connected to ground for this application. Pin 3 is an analog input for the reference voltage, the reference voltage is generated externally to the ADC and is discussed in further detail in Section 1.4.7.5. As seen in Figure 44, two different reference voltage nodes were attached to this pin using 0-Ω resistors as placeholders to select between the two options. This is done as one of the traces on the PCB would be made much longer to observe the potential losses and the effect that has on the ADC's accuracy. R258, C289, and C93 were used as a low pass filter to remove any potential high frequency noise on the reference voltage. Pins 11 and 15 are the ground pins of the ADC and were connected to the systems ground. Pin 25 is the enable pin of the ADC; it is connected to ground to make sure the chip is always enabled.

The SDI pin on the ADC, pin 22 is connected to the SDI of the PHI connector board. This makes it so that the ADC is controlled by the FPGA on the PHI board. The SDI pin, or the serial data input pin, is used to feed data or commands into the device. The FPGA on the PHI board is generating the SDI signal. Both of the ADCs are connected to the same SDI signal because only one ADC would be tested at a time, no interference would be generated by doing this. The SCLK pin, pin 23, is the clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal. As seen in Figure 44, SCLK is coming directly from the PHI connectors. The chip-select pin is active low and requires a low input for the device to take control of the data bus. The reset pin, pin 2, is also connected to the PHI connector in the same manner as the SDI signal is. Just like with the SDI signal, both ADCs are connected to the same reset signal. A low pulse on the reset pin resets the device. All register bits will then return to the default state.

Table 2. SN74AUP1G80 Function Table

INPUTS		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L or H	X	$\overline{Q}_0$

As seen in Figure 44, a unique approach is taken with the conversion start signal. Pin 1 on the ADC, CONVST, is used to start the ADC conversion. However, the CONVST signal needs to be synchronized with the SYSCLK signal to ensure proper data integrity. To achieve this, an inverter and a D flip-flop are used to synchronize the conversion start signal coming from the precision host interface (PHI) connector to the SYSCLK signal generated by the clock circuit. The CLK input to the flip-flop is the SYSCLK signal that is consistent throughout the system. Decoupling capacitors of 1 µF and 10 µF were used on both the flip flop and inverter. J33 in Figure 44 was placed so that the unsynchronized conversion start signal could be used if wanted.

To ensure the best results, onboard clocking was implemented. When maximizing system performance, clock jitter must be kept to an absolute minimum. TI's PHI is an external device. Clock jitter can be added to the system through the connection between the PHI and the TIDA-01050 board. This is prevented by using onboard clocking and the onboard CONVST/SYSCLK synchronization.

1.4.6 Clocking

The PHI is used to analyze ADC performance however, the connection between the external PHI board and the system adds jitter. The LMK61E2 was used as the internal master clock in order to minimize the jitter effects. The LMK61E2 is an ultra-low jitter PLLatinum™ programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly used reference clocks. The outputs can be configured as LVPECL, LVDS, or HCSL. The device features self-startup from on-chip EEPROM that is factory programmed to generate a 156.25-MHz LVPECL output. The device registers and EEPROM settings are fully programmable in system through I^2C serial interface. Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V ± 5% supply. The device provides fine and coarse frequency margining options through I^2C serial interface to support system design verification tests (DVT), such as standard compliance and system timing margin testing

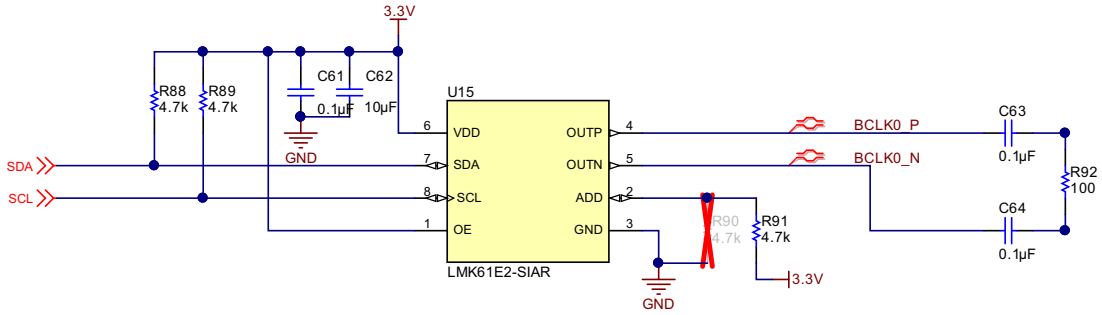

Figure 45. LMK61E2 Altium Schematic

As seen in Figure 45, pins 7 and 8 are connected to an external USB2ANY header (J3). SDA and SCL are used for the I^2C serial interface. The USB2ANY header is used to connect an external I^2C programmer. Both pins require an external pull up resistor to VCC.

VDD is connected to 3.3 V and two decoupling capacitors are used. For best electrical performance of the LMK61E2 device, it is preferred to use a combination of 10 µF, 1 µF, and 0.1 µF on its power supply bypass network. It is also recommended to use component side mounting of the power supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. The output enable pin of the LMK61E2 is also connected to VDD, this allows the output to always be enabled.

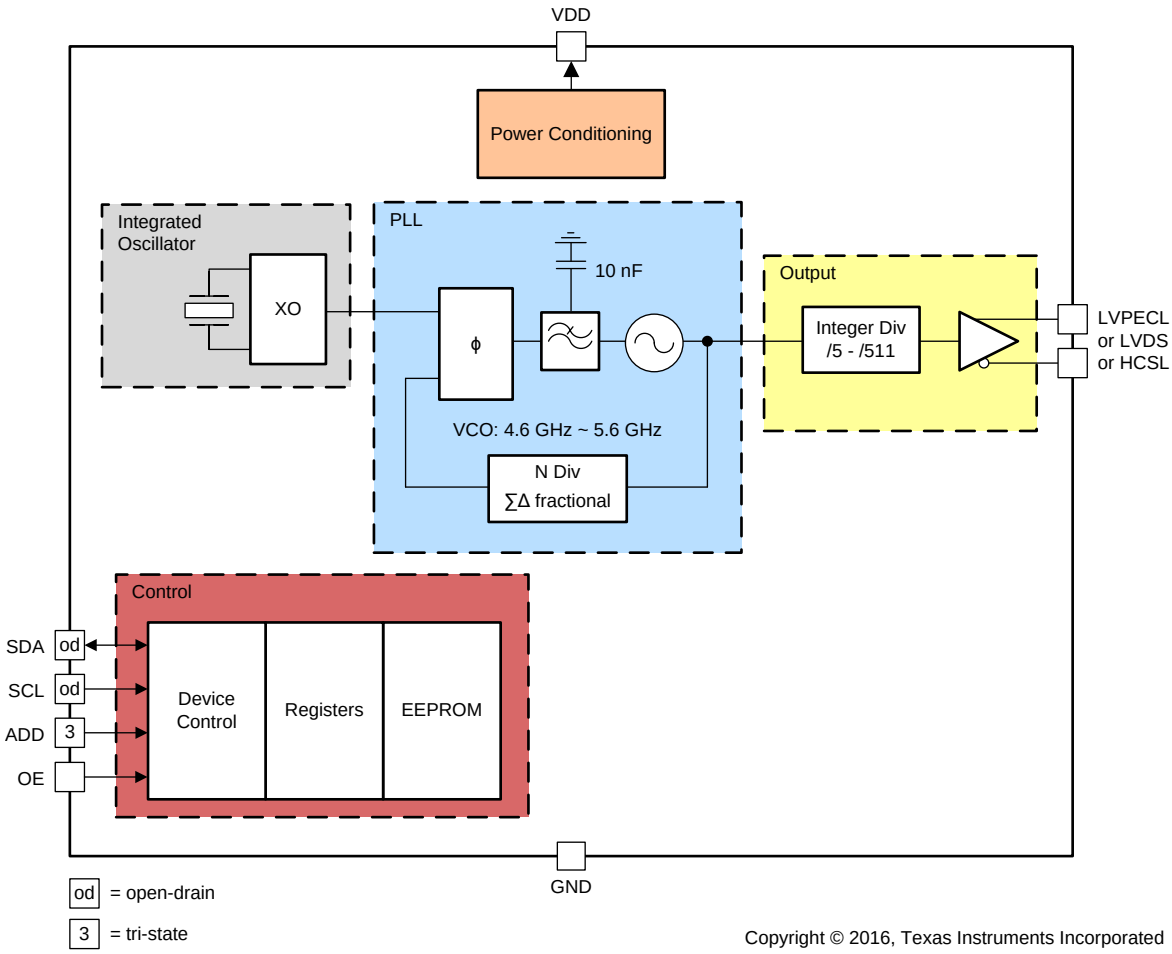

Figure 46. LMK61E2 Simplified Block Diagram

Pin 2 on the LMK61E2 is another digital control/ interface pin. When left open, LSB of the I^2C slave address is set to "01". When tied to VDD, LSB of the I^2C slave address is set to "10". When tied to GND, LSB of the I^2C slave address is set to "00". As seen in Figure 45, ADD can be connected to either VCC or GND through the configuration of the two 4.7-kΩ resistors. The default configuration is to connect ADD to VCC.

The clock generator is configured to output a 65-MHz frequency clock signal across pins 5 and 4 of the device. These two pins comprise an LVDS signal that is then passed through a 0.1-µF capacitor and terminated with a 100-Ω resistor.

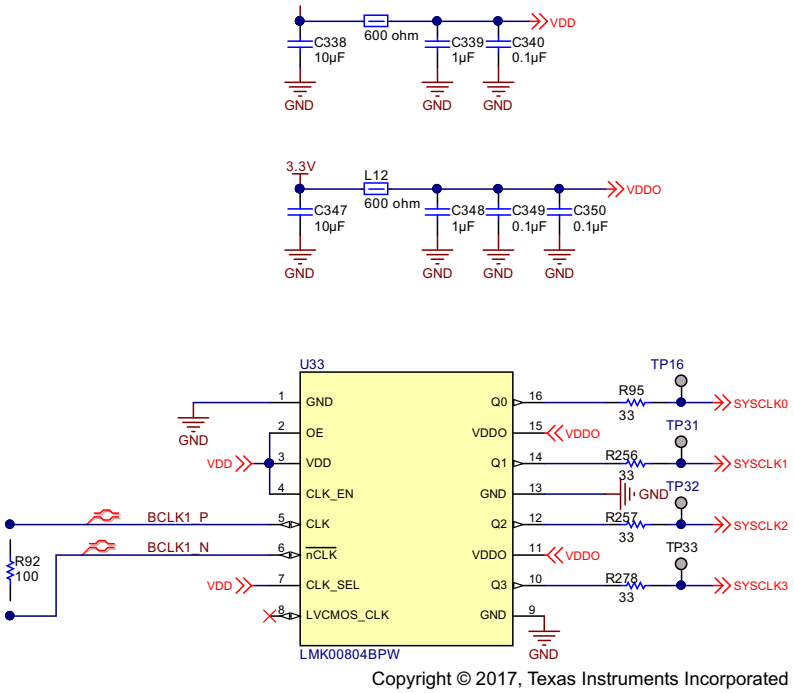

Figure 47. LMK00804BPW Clock Distributor Altium Schematic

The LMK61E2 outputs one LVDS clock signal; however, the system requires SYSCLK to go to multiple different locations. Each of these locations accepts an LVCMOS clock signal only. To handle this requirement, an LMK00804BPW is used. The LMK00804 is a clock fan-out buffer that distributes four LVCMOS clocks. The LMK00804 is configured to accept a differential input clock and distribute it to four LVCMOS clocks that are all synchronized.

Pin 7, the CLKSEL pin, is used to configure what type of input clock is used. In this system, an LVDS clock was generated from the LMK61E2 so the LMK00804 needed to be configured to accept an LVDS clock. This is done by connecting pin 7 to VDD. If pin 7 is grounded, an LVCMOS clock can be input.

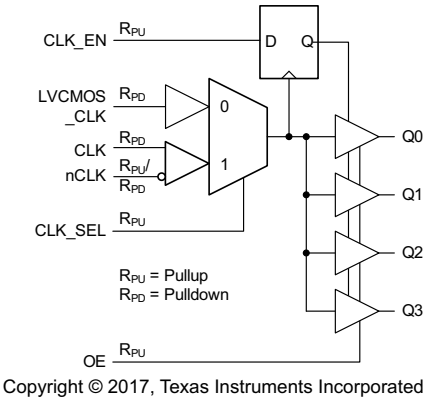

Figure 48. LMK00804BPW Functional Block Diagram

The LMK00804B is a low-skew, high-performance clock fan-out buffer, which can distribute up to four LVCMOS or LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels) from one of two selectable inputs, which can accept differential or single-ended inputs. The clock enable input is synchronized internally to eliminate runt or glitch pulses on the outputs when the clock enable terminal is asserted or de-asserted. The outputs are held in logic low state when the clock is disabled. A separate output enable terminal controls whether the outputs are active state or high-impedance state. The low additive jitter and phase noise floor, and guaranteed output and part-to-part skew characteristics make the LMK00804B ideal for applications demanding high performance and repeatability.

The four outputs from the LMK00804 go to two different places within the system. One of the clock outputs goes to the ADC conversion start synchronization logic, and the other to the PHI connectors. The LMK61E2 generates a 65-MHz LVDS clock signal and the LMK00804B distributes this clock into four synchronized 65-MHz LVCMOS clock signals.

1.4.7 Power

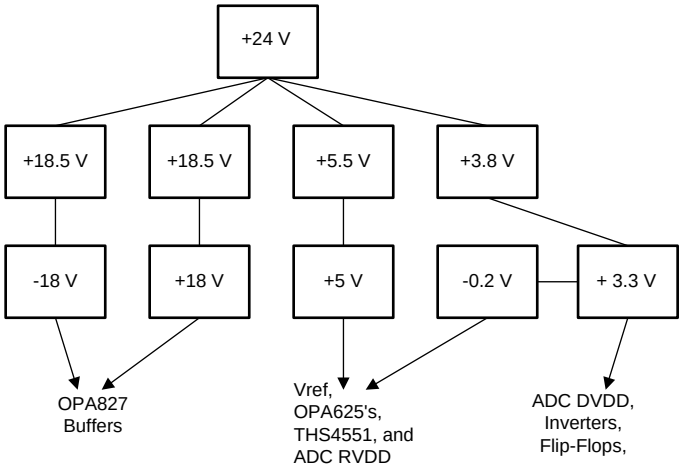

Figure 49. System Power Tree

This system requires a wide variety of voltage rails to meet the specification of the design. The input voltage required for the system is 24-V DC. The power tree in Figure 49 highlights the distribution of the power tree into the different required rails.

1.4.7.1 18-V, 5-V, and 3.3-V Rails

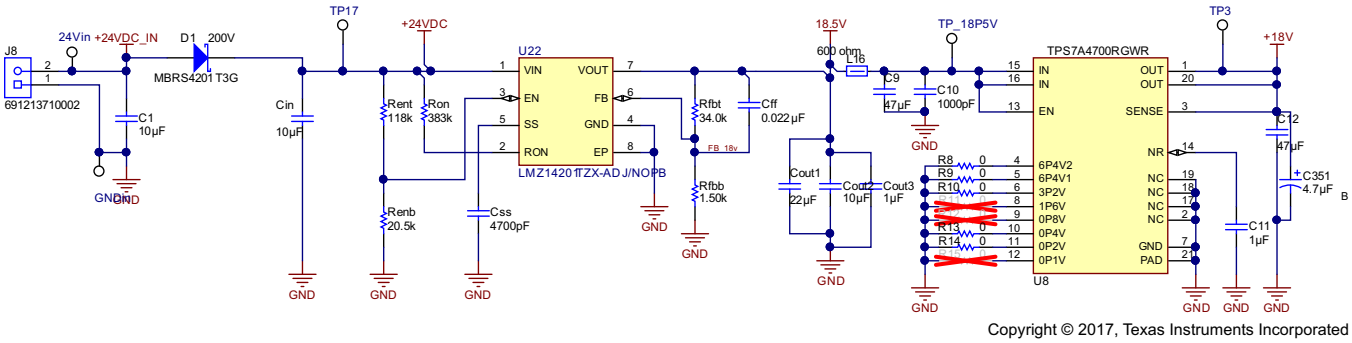

Figure 50. 18-V Rail Altium Schematic

As seen in Figure 50, a two-pin terminal block (J8) was used to connect an external 24 V into the circuit. A 10-µF capacitor (C1) is placed between these rails to help remove any noise from the input. A 200-V Schottky diode (D1) is used as a protection diode. Next, TI's WEBENCH power designer was used to generate the circuitry around the LMZ14201 (U22). On the LMZ14201, the enable input provides a precise 1.18-V band-gap rising threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage. The function of the R_{ENT}, R_{EFB} resistive divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable undervoltage lockout (UVLO). This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14201 output rail. The two resistors should be chosen based on the following ratio:

$$\frac{R_{ENT}}{R_{ENB}} = \left(\frac{V_{IN\_UVLO}}{1.18\,V}\right) \tag{10}$$

The LMZ14201 WEBENCH model suggests using 118 kΩ for R_{ENT} and 20.5 kΩ for R_{ENB} for this application. The recommended value of R_{ON} was 383 kΩ by the same model.

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The main MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur. The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\,V \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \tag{11}$$

Rearranging terms, the ratio of the feedback resistors for a desired output voltage is:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{V_O}{0.8\,V} - 1\right) \tag{12}$$

These resistors should be chosen from values in the range of 1 to 10 kΩ. For V_O = 0.8 V the FB pin can be connected to the output directly so long as an output preload resistor remains that draws more than 20 µA. Converter operation requires this minimum load to create a small inductor ripple current and maintain proper regulation when no load is present. A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

The WEBENCH model from TI.com suggested 34.0k for R_{FBT} and 1.52k for R_{FBB}.

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot. Upon turnon, after all UVLO conditions have been passed, an internal 8-µA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

$$t_{SS} = V_{REF} \times \frac{C_{SS}}{I_{SS}} = 0.8\,V \times \frac{C_{SS}}{8\,\mu A} \tag{13}$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times \frac{8\,\mu A}{0.8\,V} \tag{14}$$

None of the required CO output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst-case minimum ripple current rating of 0.5 × ILR P-P. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Ceramic capacitors or other low ESR types are recommended. See *AN-2061 LM3445 A19 Edison Retrofit Evaluation Board* for more details.

Equation 15 provides a good first-pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times \frac{V_{IN}}{\left(4 \times V_O \times \left(V_{IN} - V_O\right) \times V_{OUT-TRAN}\right)} \tag{15}$$

Solving:

$$C_O \geq 1\,A \times 0.8\,V \times 10\,\mu H \times \frac{24\,V}{\left(4 \times 3.3\,V \times \left(24\,V - 3.3\,V\right) \times 33\,mV\right)} \geq 21.3\,\mu F \tag{16}$$

The LMZ14201 demonstration and evaluation boards are populated with a 100-µF 6.3-V X5R output capacitor. Locations for other output capacitors are provided.

The LMZ14201 module contains an internal 0.47-µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be very close to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst-case input ripple current rating is dictated by Equation 17:

$$I\left(C_{IN(RMS)}\right) \cong \frac{1}{2} \times I_O \times \sqrt{\frac{D}{1-D}} \tag{17}$$

where:

- D ≅ V_O/V_IN

(As a point of reference, the worst-case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$.)

Recommended minimum input capacitance is 10-µF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. Ripple current rating of ceramic capacitors may be missing from the capacitor datasheet; if so, contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of input ripple voltage ΔV_{IN} be maintained, then Equation 18 may be used.

$$C_{IN} \geq I_O \times D \times \frac{(1-D)}{f_{SW-CCM}} \times \Delta V_{IN} \tag{18}$$

If ΔV_{IN} is 1% of V_{IN} for a 24-V input to 3.3-V output application, this equals 240 mV and f_{SW} = 400 kHz.

$$C_{IN} \geq 1\,A \times \frac{3.3\,V}{24\,V} \times \frac{\left(1 - \frac{3.3\,V}{24\,V}\right)}{\left(400000 \times 0.240\,V\right)} \geq 0.9\,\mu F \tag{19}$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

The selection of R_{ON} determines the switching frequency of the device. In this application, the switching frequency of all three switching regulators was matched by adjusting the value of R_{ON} accordingly. The formula used is:

$$f_{SW(CCM)} \cong \frac{V_O}{\left(1.3 \times 10^{-10} \times R_{ON}\right)} \tag{20}$$

This can be rearranged as:

$$R_{ON} \cong \frac{V_O}{1.3 \times 10^{-10} \times f_{SW(CCM)}} \quad (21)$$

In this system, the switching frequency on the switching regulators is set to 371 kHz.

After the voltage is dropped from 24 V to 18.5 V, an adjustable LDO is used to drop the voltage down to 18 V and to attenuate the switching voltage ripple on the rail. The TPS7A47 is ideal for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversions, maximum system performance is ensured in sensitive instrumentation, test-and-measurement, audio, and RF applications.

Pins 4 to 6 and 8 to 12 are used to adjust the nominal output voltage of the LDO. If none of the adjustment pins are connected, the output is regulated to 1.4 V. By grounding the adjustment pins, the voltage labeled on the name of that pin is added to the regulated output voltage. To get an 18-V regulated output, pins 6P4V2, 6P4V1, 3P2V, 0P4V, and 0P2V were grounded. When adding these voltages, 18 V is achieved:

$$1.4 + 6.4 + 6.4 + 3.2 + 0.4 + 0.2 = 18 \quad (22)$$

The enable pin of the TPS7A47 is connected to V_{CC} to ensure that the chip is always on. Pin 14 is the noise reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1-µF capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize AC performance and minimize noise. Pin 3 is the SENSE pin if the device output voltage is programmed using ANY-OUT (no external feedback resistors). This pin must be connected to OUT. Connect this pin to the point of load to maximize accuracy. This is the FB pin if the device output voltage is set using external resistors.

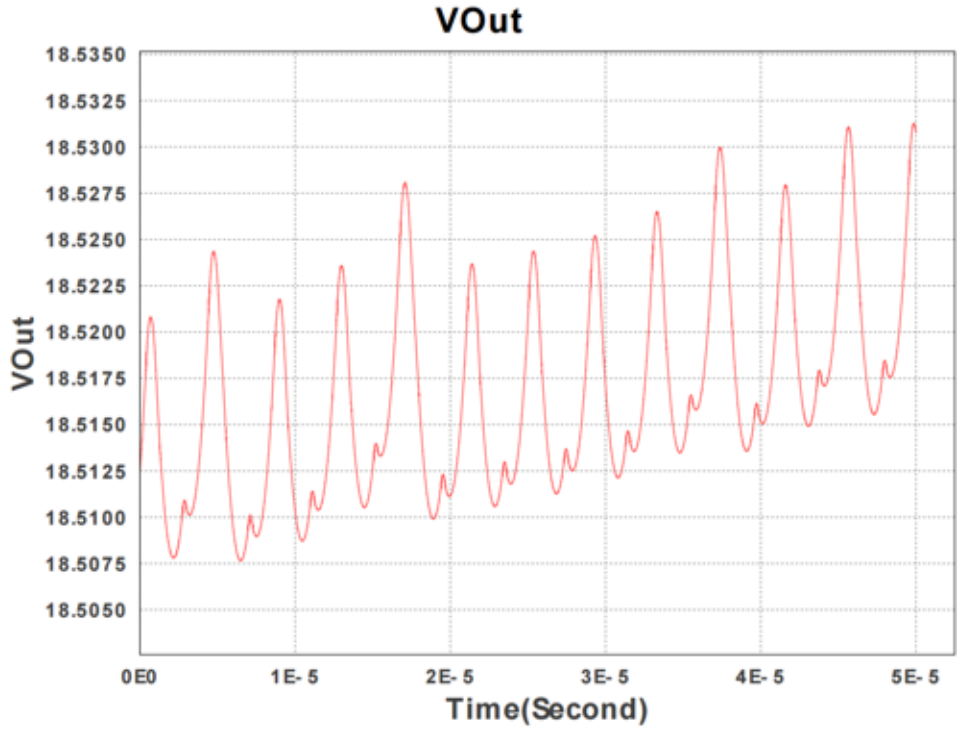

Figure 51. 18.5-V WEBENCH Results

Figure 51 displays the simulation results of the LMZ14201 from WEBENCH. As seen, the switching of this device is evident. However, the peak-to-peak output ripple voltage is only 1.565 mV. The switching frequency is 371 kHz.

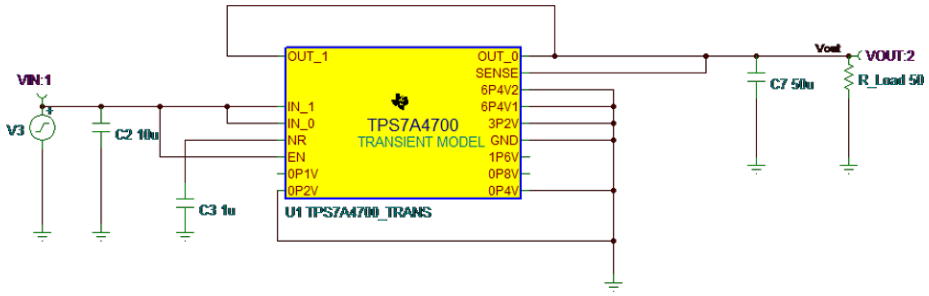

Figure 52. TPS7A47 TINA-TI Simulation Schematic

The WEBENCH results of the LMZ14201 were then taken and input to the TPS7A4700 TINA-TI model to properly simulate the entire power rail. The TPS7A4700 is set to output 18 V by the grounded adjustment pins. The first simulation done was to show the steady state reduction in switching noise. This is highlighted in Figure 53.

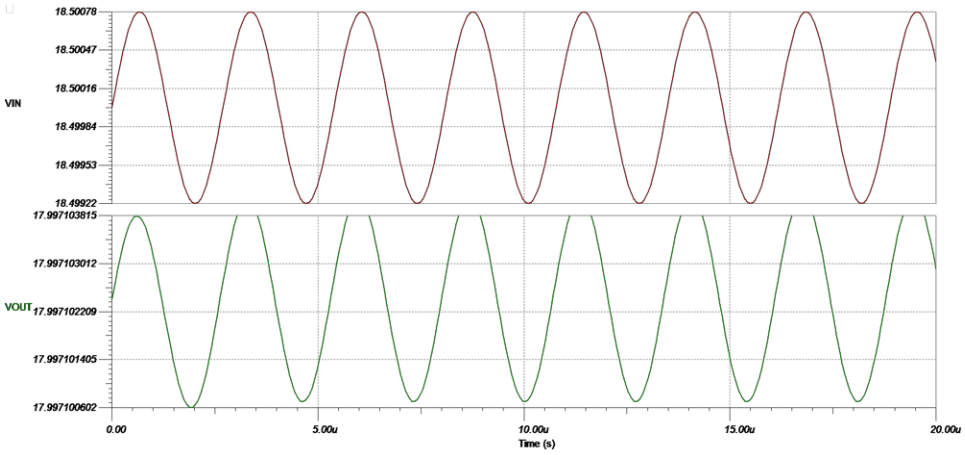

Figure 53. TPS7A4700 Steady-State Simulation

By adding the LDO in to the 18-V power circuit, the amount of switching noise gets greatly reduced. The initial switching noise peak to peak amplitude is 1.56 mV. After the LDO, the switching noise peak to peak amplitude is 3.213 µV. The LDO effectively reduces the switching ripple noise by a factor of 485.

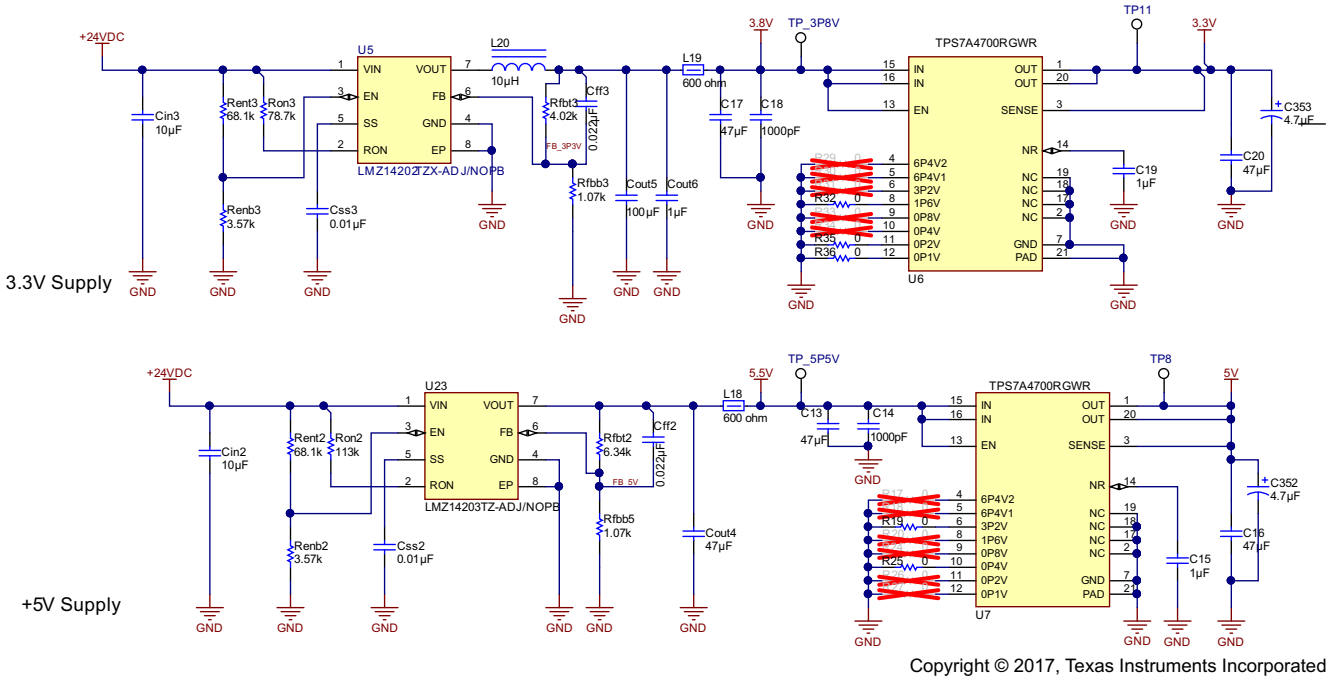

Figure 54. 3.3-V and 5-V Rail Altium Schematic

As seen in Figure 54, the same approach was taken for generating the 3.3-V and 5-V rails as for the 18-V rail. The LMZ14202 and LMZ14203 are used here as the output/input specifications are slightly different, and TI's WEBENCH power designer was used to simulate the power components. The same simulations were performed as with the 18-V rail and the switching frequencies were synchronized with the use of Equation 11. All of the LMZ142 devices were set to 371 kHz.

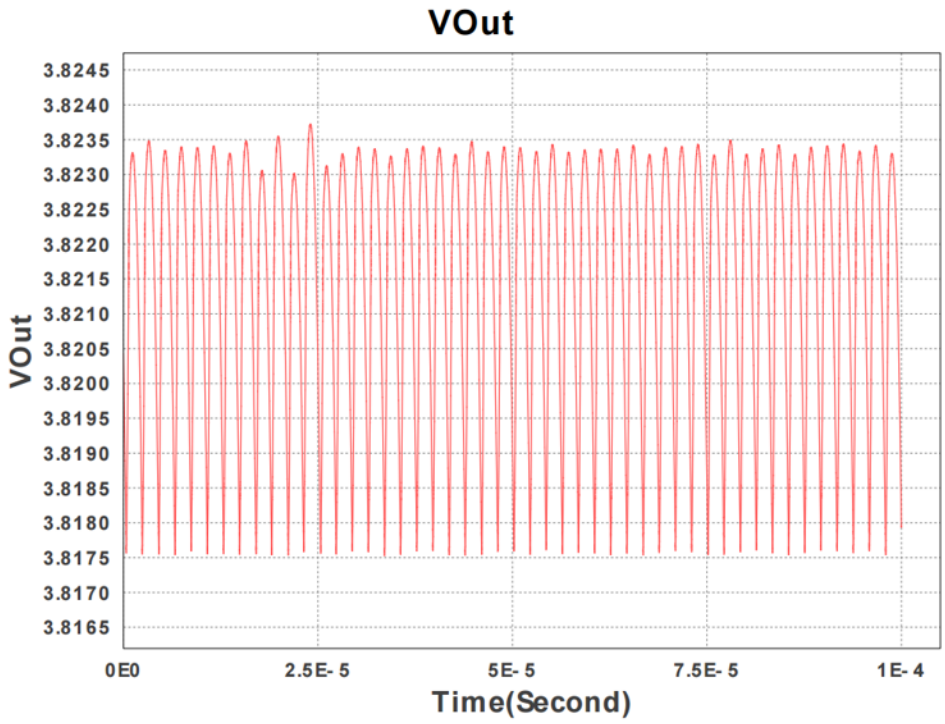

Figure 55. 3.8-V Rail WEBENCH Results

After simulating the LMZ14202, the switching frequency is also 371 kHz and the peak-to-peak output ripple voltage is 4.193 mV. By completing the same simulation in TINA-TI as with the 18-V rail using the TPS7A4700 adjustable LDO, the voltage ripple was reduced from 4.193 mV to 9.425 µV or a factor of 932x as seen in Figure 56. A 10-µH inductor is placed on the output of the LMZ14202 to help reduce the switching noise seen in the spectrum of the results.

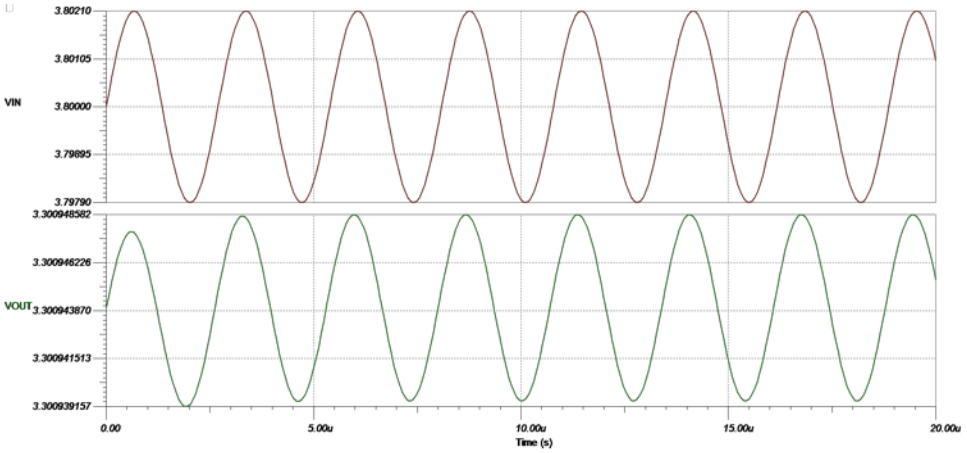

Figure 56. 3.3-V Rail TINA-TI Results

The LMZ14203 was tested under the same conditions; WEBENCH was used to initially set the resistor and capacitor values. Then the switching frequency was set to 371 kHz to match the other two switching regulators. WEBENCH was then used to simulate the LMZ14203 to observe the switching frequency and output peak-to-peak ripple voltage.

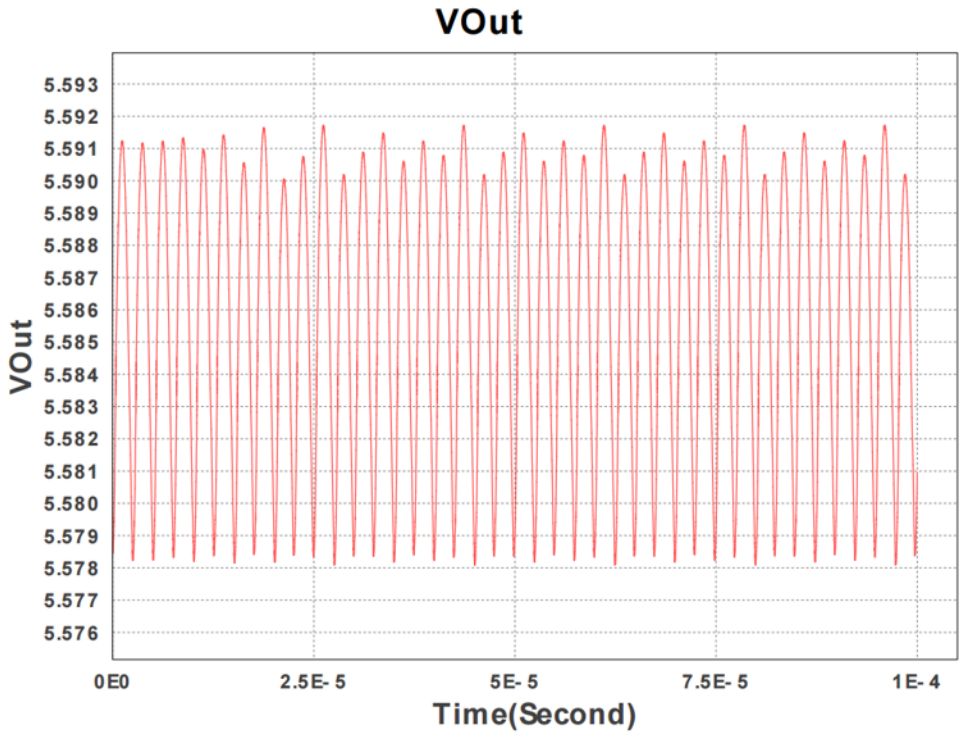

Figure 57. 5.5-V Rail WEBENCH Results

The switching frequency of the 5.5-V rail was also set to 371 kHz, which is also shown in the WEBENCH simulation. The peak-to-peak output voltage ripple for this rail is 5.692 mV. When simulating the effects of the LDO on this rail, the voltage ripple was reduced to 9.425 µV. This is shown in the TINA-TI simulation results in Figure 58.

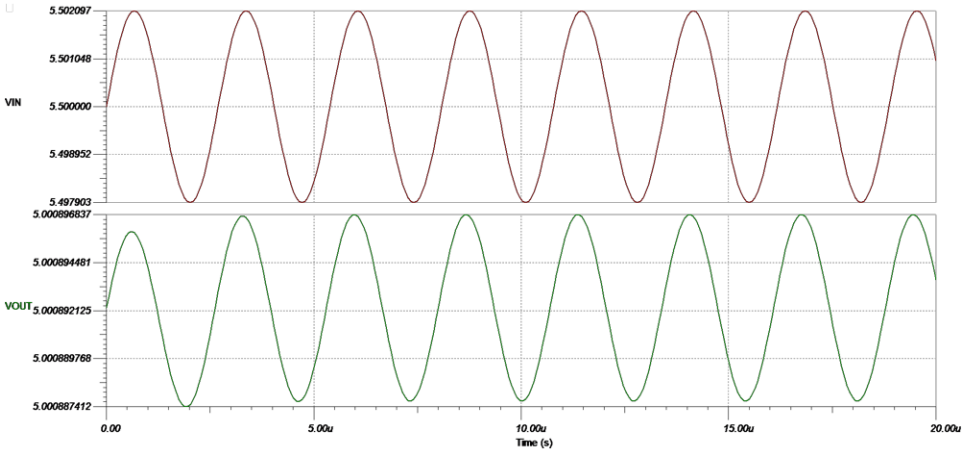

Figure 58. TINA-TI 5-V Rail Results

Further calculate the noise that will be present at the ADC by observing the power supply rejection values for each component. After the LMZ14203 was used to generate 5.5 V, there was a 5.692-mV peak-to-peak output ripple voltage at a frequency of 371 kHz. The TPS7A47 has a minimum PSRR of 50 dB, when converting this dB value to V/V the PSRR is 0.003162 V/V. Thus, the amount of calculated power supply noise after the TPS7A47 will be:

$$5.692\ \text{mV} \times 0.003162 = 17.998\ \mu\text{V} \tag{23}$$

Next, this voltage will go to both the OPA625 and the THS4551. The THS4551 has a PSRR of 105 dB at 370 kHz at a gain of 1. PSRR is equal to:

$$\text{PSRR}(\text{dB}) = -20\log_{10}\left(\frac{\Delta V_{OS}}{\Delta V_{SUPPLY}}\right) \tag{24}$$

Because this system has a gain of 1/8, the total noise gain on the non-inverting terminal is 1 + 1/8. This is a gain of 1.02 dB. The total PSRR for the THS4551 will be approximately 104 dB for this system. This is equal to 0.000006 V/V. The amount of power supply noise coupled to the ADC data lines will be:

$$17.998\ \mu\text{V} \times 0.000006 = 0.108\ \text{nV} \tag{25}$$

This noise value will then be compared to the LSB value of the ADC to ensure that it will not have an effect on signal integrity. The value of 1 LSB for an 18-bit ADC with 4.096 V as a reference voltage will be:

$$\frac{4.096}{2^{18}} = 15.625\ \mu\text{V} \tag{26}$$

$$\frac{0.108\ \text{nV}}{15.625\ \mu\text{V}} \times 100 = 0.0007\%\ \text{LSB} \tag{27}$$

This highlights that the amount of noise on the 5-V rail is much less than 1% of the LSB value of the ADC. This leads to the conclusion that there will be no negative effect. The OPA625 has a power supply rejection ratio of 55 dB at 370 kHz. At a gain of 1/8, the PSRR will be equal to 54 dB. This is equivalent to 0.001995. The power supply noise present on the OPA625's ADC will be:

$$17.998\ \mu\text{V} \times 0.001995 = 35.91\ \text{nV} \tag{28}$$

$$\frac{35.91\ \text{nV}}{15.625\ \mu\text{V}} \times 100 = 0.23\%\ \text{LSB} \tag{29}$$

The OPA625 signal chain will also have less than 1% LSB of power supply noise present at the ADC. Thus, the power rails will have no negative effect on the ADC's output data.

It is common practice to use a switching regulator followed by an LDO for sensitive analog power rails. A switching regulator is used to bring the voltage down to a range that is just above the dropout voltage of the LDO. Then the LDO is used to drop the voltage down and help remove the switching noise generated by the switching regulator. A switching regulator is much more efficient at reducing a voltage as it switches on and off. Efficiency ratings for switching regulators are typically in the 90% range. However, the switching noise created on the output rails of switching regulators is undesired in sensitive analog supply rails. Having a noisy analog supply will generate noise on the analog signals and reduce the signal integrity of the system. To minimize switching noise, the LDOs are often used. An LDO has a high power supply rejection ratio, typically in the 75-dB range. This allows the LDO to remove harmful switching noise from the supply. When using the LDO strictly for switching noise attenuation the voltage dropped across the LDO should be just above the dropout voltage of the device. This is typically in the 200- to 500-mV range. In this application, the LDO is used to drop the final analog voltage by 500 mV while simultaneously filtering the supply. When using a voltage much higher than the dropout voltage of the LDO, the efficiency of the rail power generation will be degraded. LDOs generate heat when used to reduce a voltage as power is burned. The current across the LDO must be carefully monitored to ensure the power limitations of the device are not reached. The TPS7A47 is internally limited to be able to a maximum of 1 A of current. Power dissipation by the LDO can be calculated by multiplying the difference of the input and output voltage by the current on the rail. The larger the voltage drop in the LDO, the more power the device will consume. Power consumption is to be kept at a minimum by an LDO for the system to remain efficient.

1.4.7.2 –18-V Rail Design Theory

A –18-V rail was also required in this TI Design. Both the multiplexers and the OPA827 buffer amplifiers are ran on ±18 V. To generate a –18-V rail and inverting buck-boost switching regulator was used to bring the voltage from 24 to –18.5.

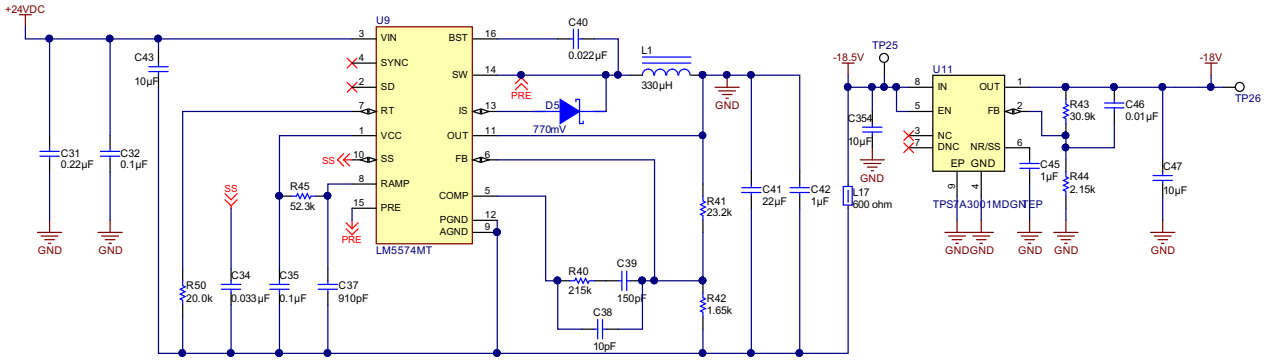

Figure 59. –18-V Rail Altium Schematic

When developing a negative voltage rail, the voltage rating of the device must be larger than the difference of the output rail and the input rail. In this case, because –18.5 V was coming out of the switching regulator and 24 V was coming in, the difference is calculated as:

$$24 - (-18.5) = 42.5 \text{ V} \quad (30)$$

The LM5574MT is rated for 75 V, so 42.5 V is well within the safe operating conditions of the device.

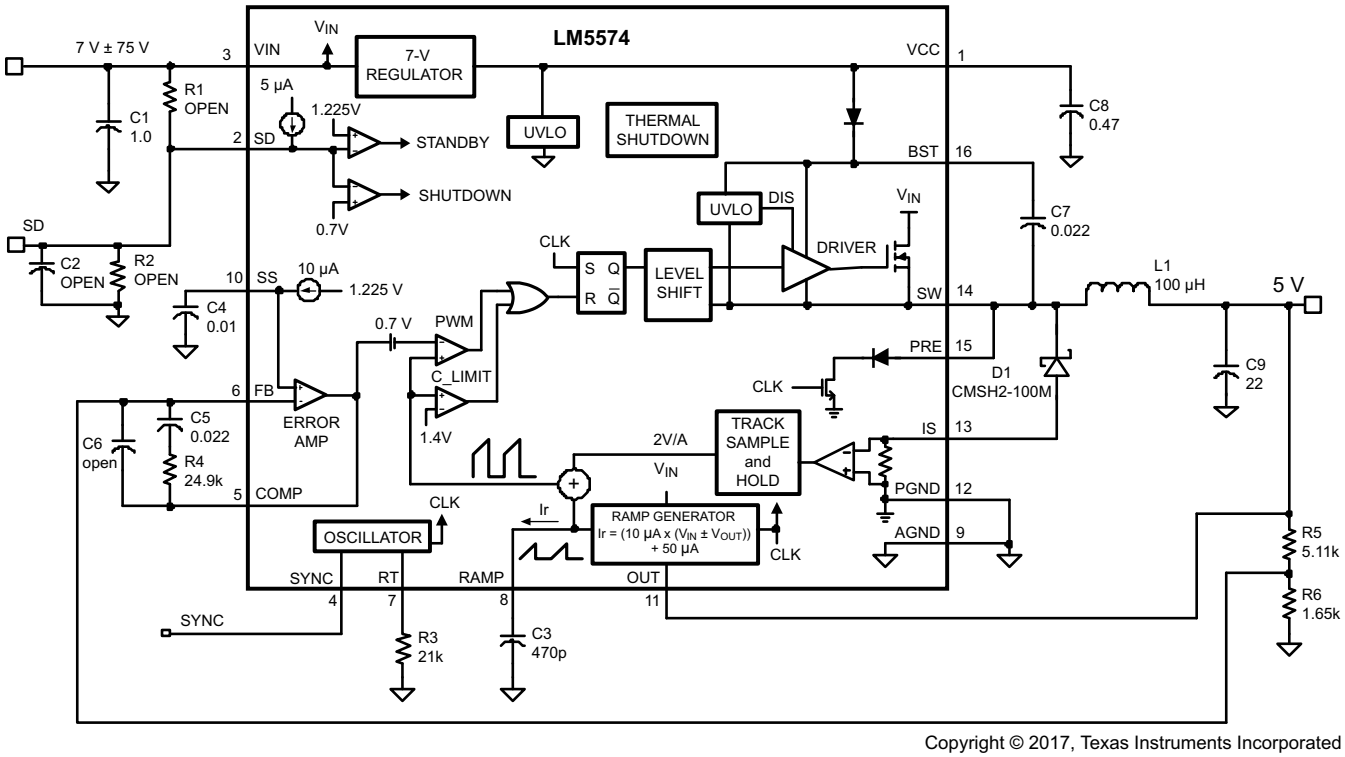

Figure 60. LM5574 Functional Block Diagram

The LM5574 switching regulator features all of the functions necessary to implement an efficient high-voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 75-V N-Channel buck switch with an output current capability of 0.5 A. The regulator control method is based on current mode control using an emulated current ramp. Peak current mode control provides inherent line voltage feedforward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 to 500 kHz. An oscillator synchronization pin allows multiple LM5574 regulators to self-synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225 V. Fault protection features include, current limiting, thermal shutdown, and remote shutdown capability. The device is available in the TSSOP-16 package.

The functional block diagram and typical application of the LM5574 are shown in Figure 60. The LM5574 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial and automotive power bus voltage ranges.

TI's WEBENCH power designer tool was used to select inductor, resistor, and capacitor values. The schematic generated by WEBENCH is shown in Figure 61. The model for the LM5574 did not allow for negative voltage rails to be simulated as the internal connections for the AGND and PGND pins were the same as the external ground. However, simulations were done with the polarity of the output switched and this granted an 18.5-V output rail. The only difference with the actual used circuit versus the simulated circuit was where the output was taken in reference to the ground. Using an inverting buck-boost module to generate a negative voltage rail is a common practice.

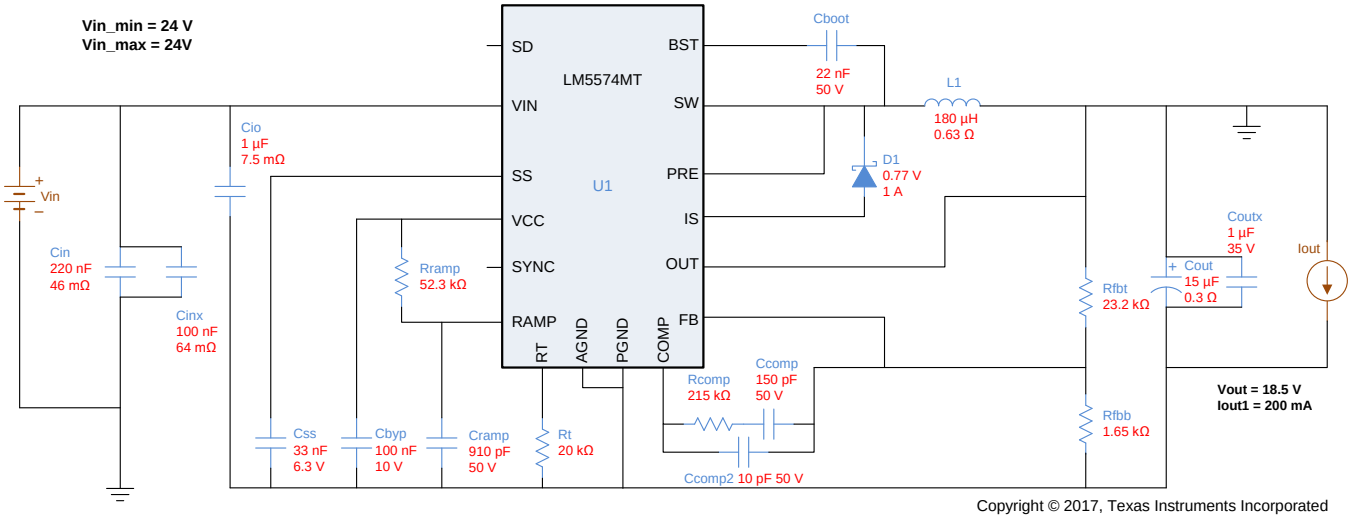

Figure 61. LM5574 WEBENCH Schematic

The LM5574 currently does not have a TINA-TI simulation model. However, a very similar part, the LM5575, does have a model that is used to simulate this schematic. The LM5575 allows for a slightly higher output current but the topologies of the two devices are the same.

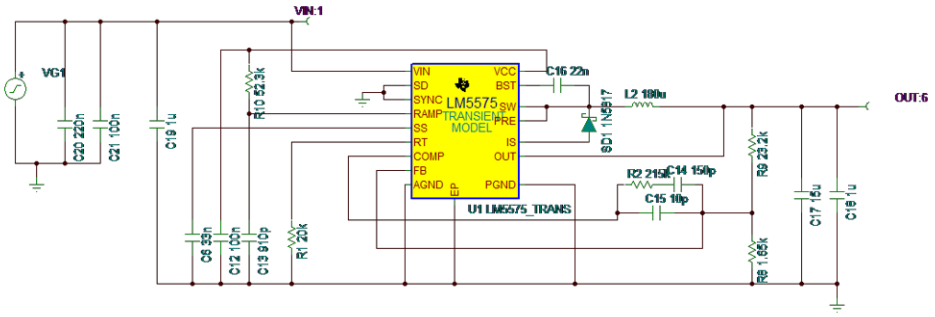

Figure 62. LM5575 Transient Simulation

As seen in Figure 62, the model could only be simulated with a positive voltage on the output. When implementing the real circuit on the board, however, the output node and ground node on the bottom of the circuit are reversed. This will then change the voltage from a positive voltage to a negative voltage.

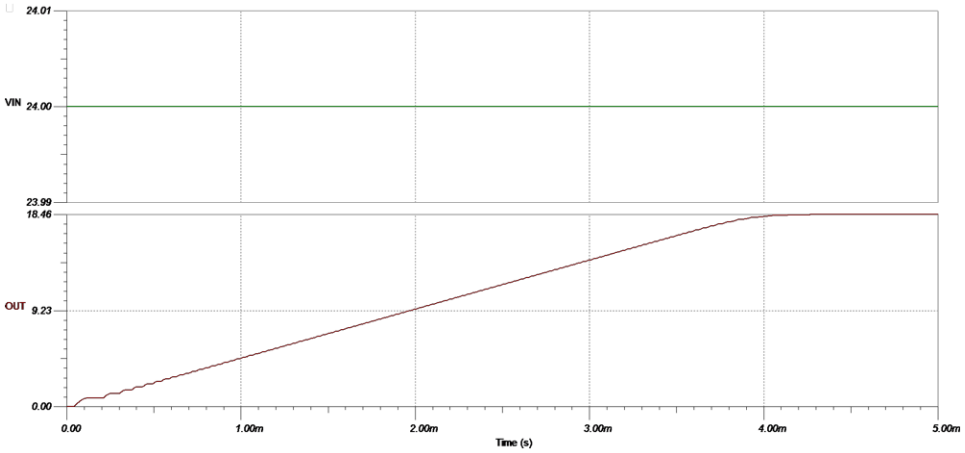

Figure 63. LM5575 Transient Simulation Results

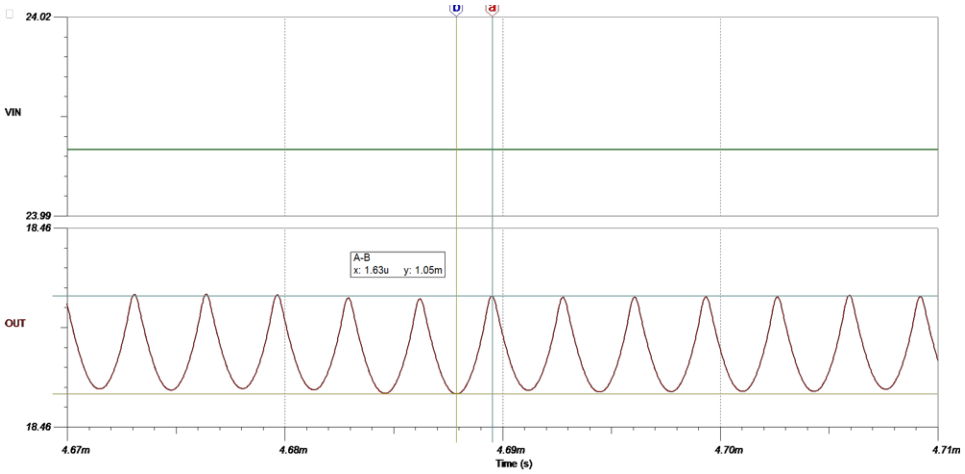

Figure 64. LM5575 Transient Simulation Output Ripple

The simulation reveals that the circuit takes about 4 ms to reach a steady 18.5 V. Upon further examination of the results, the amount of ripple on the output at 18.5 V is 1.05 mV at a frequency of 306 kHz.

After the inverting buck-boost switching regulator reduced the voltage from 24 to –18.5 V, a negative voltage LDO was used to bring the voltage down to –18 V while simultaneously reducing the switching noise.

The TPS7A3001 is a negative, high-voltage (–36 V), ultra-low-noise (15.1 μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3001 is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This TI Design makes it an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A3001 family of linear regulators is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

Again, TI's WEBENCH power designer was used to select the component values around the TPS7A3001. The output parameters of the LM5575 simulation were taken and inserted into TINA-TI model of the TPS7A3001 to highlight how the voltage ripple would be reduced.

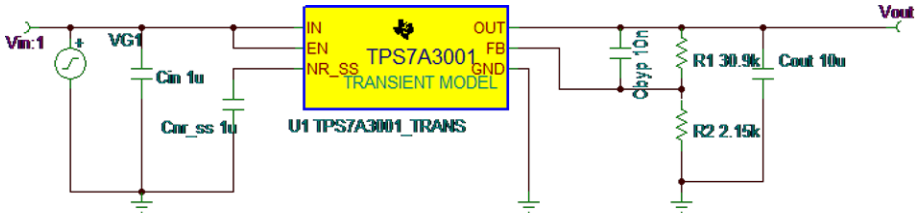

Figure 65. TPS7A3001 TINA-TI Transient Simulation

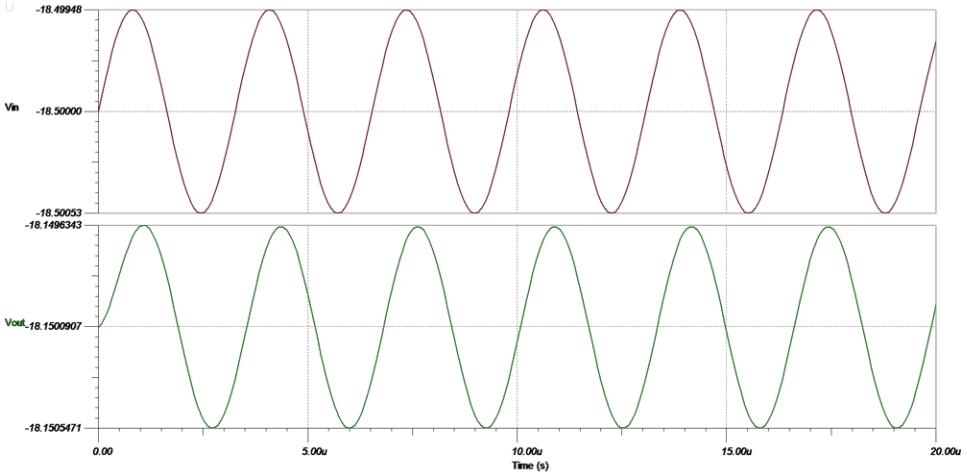

Figure 66. TPS7A3001 Transient Simulation Results

Figure 65 and Figure 66 highlight the results of the TPS7A3001 TINA-TI simulations given the input parameters developed by the simulation of the LM5575. The noise gets reduced to 920 µV and the DC level is reduced to –18 V.

1.4.7.3 –0.2-V Rail Design Theory

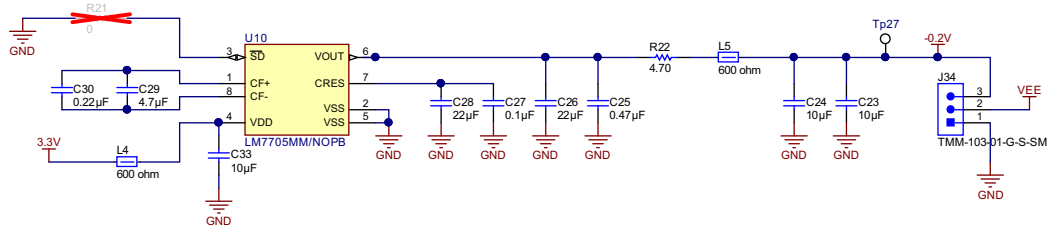

Figure 67. –0.2-V Rail Altium Schematic

To ensure the AFE can support a full voltage swing from 0 to V_{REF}, a small –0.2-V rail (VEE) was generated using the LM7705. Due to the architecture and transistor limitations, most general purpose amplifiers will saturate when the signal, at the input or output, nears the supply rails. As the signal approaches this voltage, usually within few hundred millivolts of the supply, many amplifier characteristics, such as linearity and supply rejection, start degrading. To further learn about this concept, see the TIDA-01052 TI Design. The TIDA-01052 specifically focuses on performance improvements seen with the addition of negative rail versus a ground rail on the front-end amplifiers.

1.4.7.4 Reference Voltage Design Theory

External voltage reference circuits are used in a data acquisition system if there is no internal reference in the ADC or if the accuracy of the internal reference is not sufficient to meet the performance goals of the system. These circuits must provide a low-drift, low-noise, and accurate voltage for the ADC reference input. However, the output broadband noise of most references can be in the order of a few 100 μV_{RMS}, which degrades the noise and linearity performance of precision ADCs, for which the typical noise is in the order of tens of μV_{RMS}. So, to optimize the ADC performance, the output of the voltage reference must be appropriately filtered and buffered.

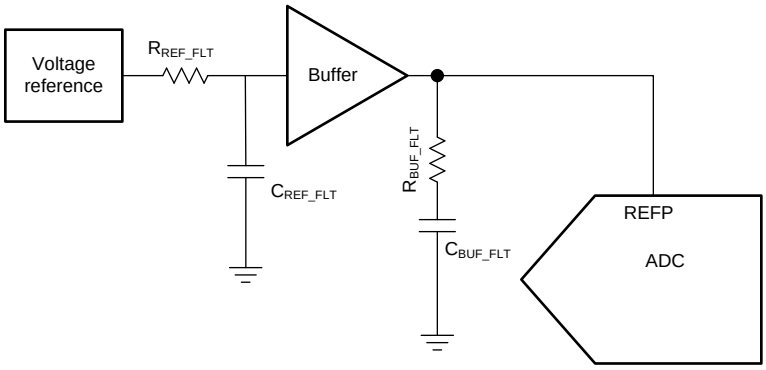

Figure 68. Simplified Schematic of Reference Driver Circuit

Most SAR ADCs, and a few delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. If a voltage reference is directly connected to the REF pin of these ADCs, the reference voltage droops because of the dynamic input signal dependent load of the binary-weighted capacitors. Because the reference voltage droop now has input signal dependence, significant degradation in THD and linearity for the system occurs.

In order to support this dynamic load and preserve the ADC linearity, distortion and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF60xx family of voltage references has an integrated low-output impedance buffer that enables the user to directly drive the REF pin of a SAR ADC, while preserving ADC linearity and distortion. In addition, the total noise in the full bandwidth of the REF60xx is extremely low, thus preserving the noise performance of the ADC.

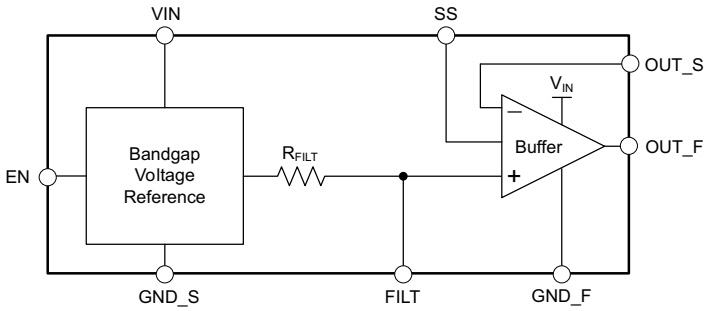

Figure 69. REF60xx Functional Block Diagram

The output voltage of the REF60xx does not droop below 1 LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8910B. This feature is extremely useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data acquisition systems.

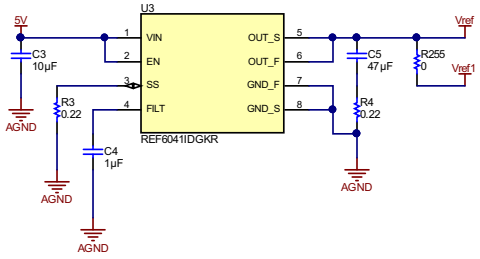

Figure 70. Reference Voltage Altium Schematic

1.4.7.5 Common-Mode Voltage Design Theory

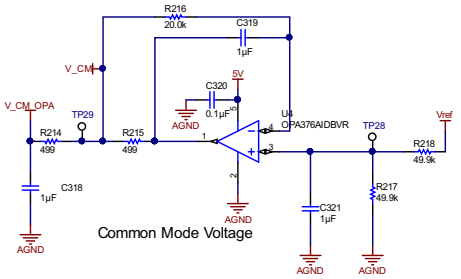

Figure 71. Common-Mode Voltage Altium Schematic

The common-mode voltage is the voltage the THS4551 and the OPA625 driver amplifiers center the output signal around. To enable full signal swing, the common mode voltage should be exactly half the reference voltage. To achieve this, an OPA376 is used with a resistor divider on the input to divide the reference voltage in half. The OPA376 is buffering the voltage from the resistor divider to the load. For the single-ended OPA625 ADC drivers the output common mode is set by applying the input common-mode voltage at the non-inverting terminal. There is a $1 + \frac{R_f}{R_g}$ gain from the non-inverting input to the output. Due to this gain, the input $\frac{V_{REF}}{2}$ voltage needed to be scaled down by a factor of $\frac{R_g}{R_f + R_g}$. This was implemented with R214, and R110 + R111.

C320, C321, and C318 in Figure 71 are used as decoupling capacitors to help reduce any noise on these rails. Components R216, C319, and R215 are placed to ensure the stability of the circuit.

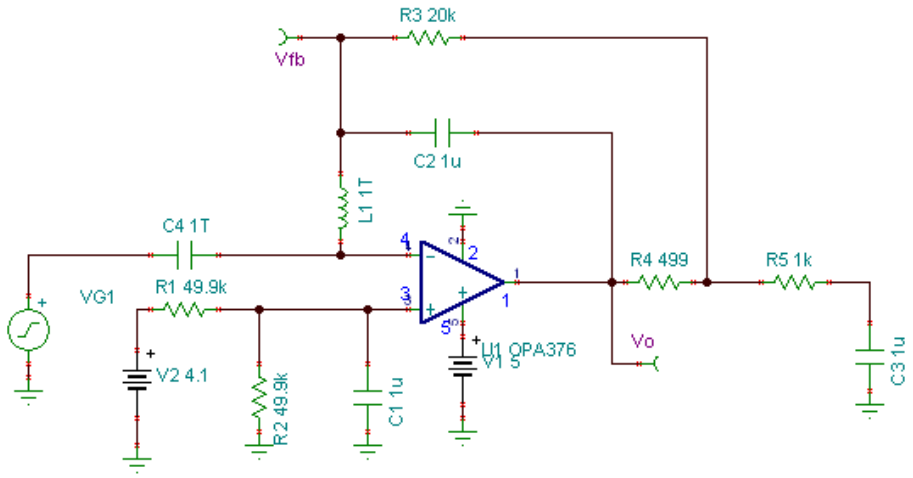

Figure 72. OPA376 Stability Simulation Circuit

TINA-TI was used to model this circuit. The simulation schematic is shown in Figure 72. The theory for completing stability simulations are covered in TI's precision labs lectures on op amps.

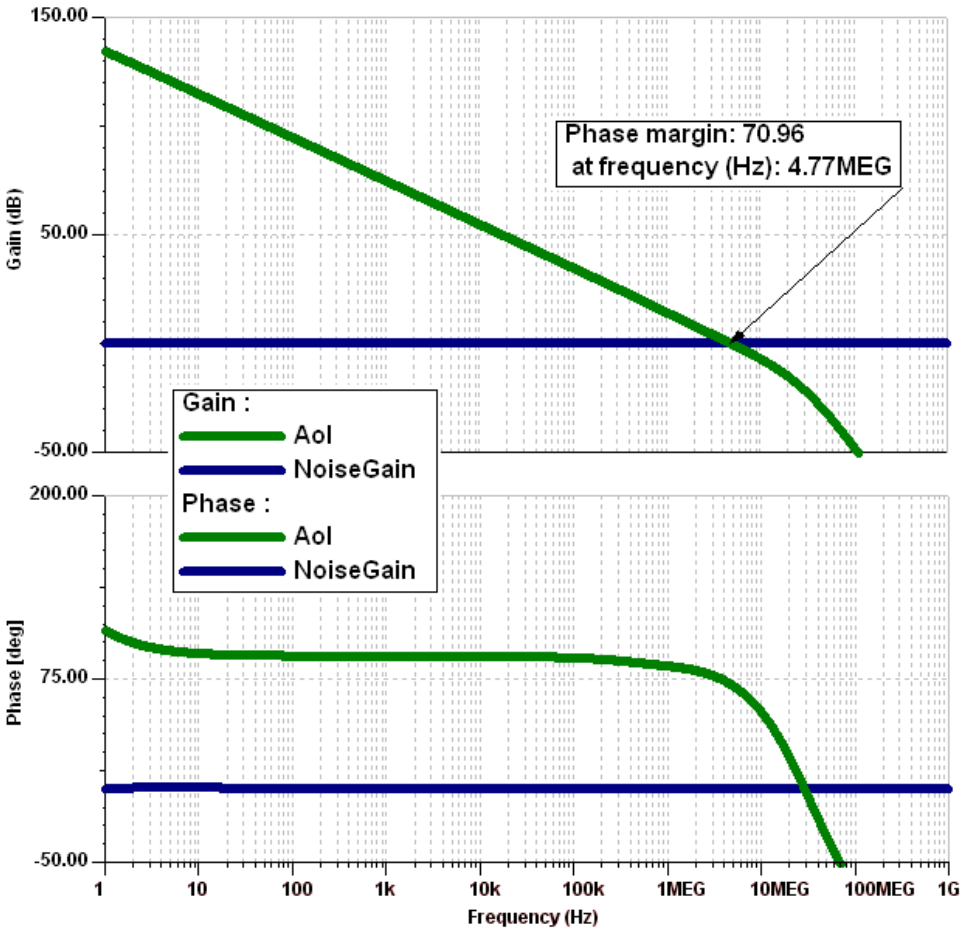

Figure 73. OPA376 Stability Simulation Results

The results from the TINA-TI simulations are shown in Figure 73. The loaded open loop gain curve intersects with the noise gain curve with a rate of closure less than 40 dB/decade. This is indicative of a stable circuit. Furthermore, the phase margin is 70.96º, which is well above the 45º threshold required for a stable circuit.

1.4.8 Host Interface

This TI Design supports PHI to evaluate system performance. PHI is TI's SAR ADC evaluation platform, which supports the entire TI SAR ADC family. By using PHI, the system easily communicates with the host PC using a USB interface. PHI supports the ADS8910 multiSPI™ and onboard configuration I^2C EEPROM interface. PHI GUI software can be used to evaluate both AC and DC parameters of the ADS8910. For more information on PHI, see the ADS8910 EVM-PDK.

The PHI module software was modified to include the ability to accept an external clock input. This same software was used in the TIDA-01035 TI Design

1.5 Highlighted Products

Key features for selecting the devices for this reference design are highlighted in the following subsections. Find the complete details of the highlighted devices in their respective product datasheets.

1.5.1 OPA827

The OPA827 series of JFET operational amplifiers combine outstanding DC precision with excellent AC performance. These amplifiers offer low offset voltage (150 µV, maximum), very low drift over temperature (0.5 µV/°C, typical), low-bias current (3 pA, typical), and very low 0.1- to 10-Hz noise (250 nV_{PP}, typical). The device operates over a wide supply voltage range, ±4 to ±18 V on a low supply current (4.8 mA/Ch, typical).

Excellent AC characteristics, such as a 22-MHz gain bandwidth product (GBW), a slew rate of 28 V/µs, and precision DC characteristics make the OPA827 series well-suited for a wide range of applications including 16- to 18-bit mixed signal systems, transimpedance (I/V-conversion) amplifiers, filters, precision ±10-V front ends, and professional audio applications. The OPA827s are used as signal buffers in this system. The OPA827 is currently the highest bandwidth 36-V op amp offered by TI.

1.5.2 OPA625

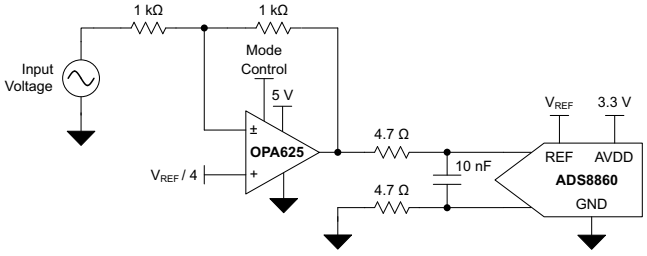

Figure 74. OPA625 SAR ADC Driver Configuration From Datasheet

The OPAx625 family of operational amplifiers are excellent 16- and 18-bit SAR ADC drivers that are high precision with low THD and noise allow for a unique power-scalable solution. This family of devices is fully characterized and specified with a 16-bit settling time of 280 ns that enables a true 16-bit effective number of bits (ENOB). Along with a high DC precision of only 100-µV offset voltage, a wide gain-bandwidth product of 120 MHz, a low wideband noise of 2.5 nV/√Hz, this family is optimized for driving high-throughput, high-resolution SAR ADCs, such as the ADS88xx family of SAR ADCs.

The OPA625 is used in many SAR ADC reference designs. It is also used in the ADS8910B evaluation model. The OPA625 is often regarded as the best 5-V ADC driver amplifier available today from Texas Instruments.

1.5.3 THS4551

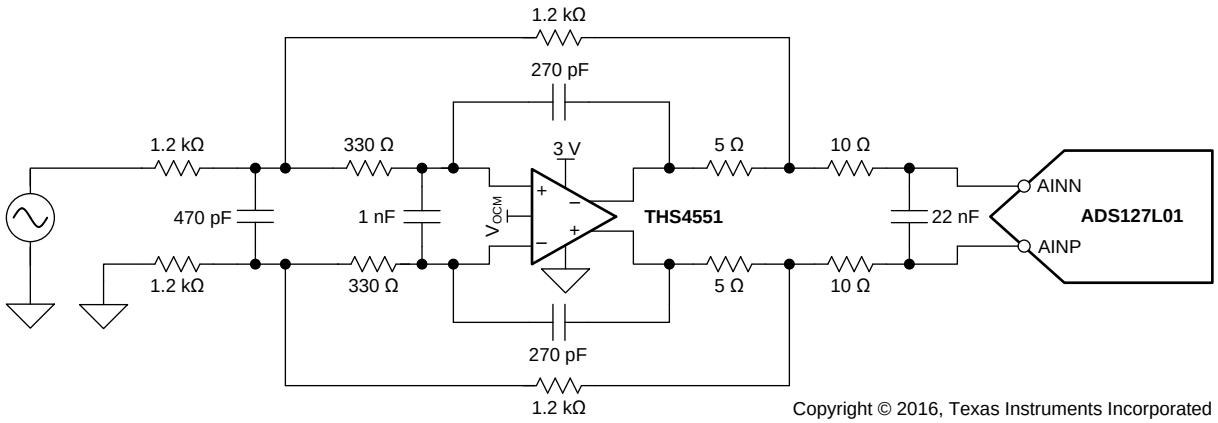

Figure 75. THS4551 SAR ADC Driver Configuration From Datasheet

The THS4551 fully differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well suited for data acquisition systems where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4551 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very low DC error and drift terms support the emerging 16- to 20-bit successive-approximation register (SAR) input requirements. A wide-range output common-mode control supports the ADC running from 1.8- to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V.

The THS4551 is commonly used in SAR ADC driver circuits. However, it is unclear where using a fully differential amplifier is beneficial over using two precision op amps and vice versa. This TI Design aims to clear up that uncertainty and distinguish benefits to using both configurations.

1.5.4 ADS8910B

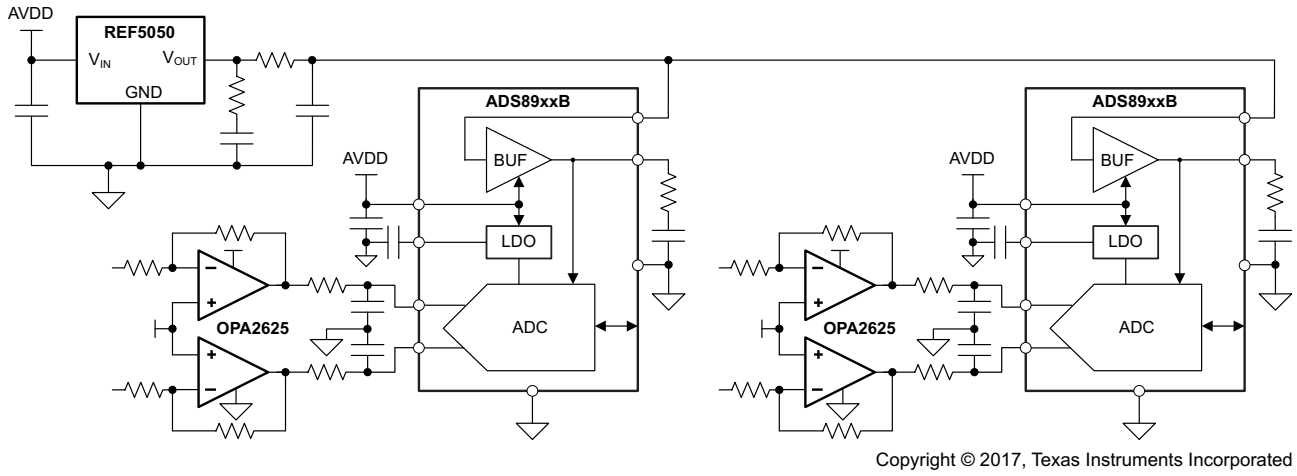

Figure 76. Multiple ADC Design From Datasheet

The ADS8910B, ADS8912B, and ADS8914B (ADS891xB) belong to a family of pin-to-pin compatible, high-speed, high-precision SAR-based ADCs with an integrated reference buffer and integrated LDO. These devices support unipolar, fully differential, analog input signals with ±0.5-LSB INL and 102.5-dB SNR specifications under typical operating conditions.

The integrated LDO enables single-supply operation with low power consumption. The integrated reference buffer supports burst-mode data acquisition with 18-bit precision for the first sample. External reference voltages in the range of 2.5 to 5 V are supported, offering a wide selection of input ranges without additional input scaling.

The integrated multiSPI digital interface is backward-compatible to the traditional SPI protocol. Additionally, configurable features simplify board layout, timing, and firmware, and support high throughput at lower clock speeds. The multiSPI digital interface allows for easy interface with a variety of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs).

The ADS8910B has a high sample rate of 1 MSPS, meeting the specification of the system. It also features single-supply low power operation. The key differentiation of the ADS8910B that makes it ideal for the multichannel simultaneous sampling Test and Measurement systems is its integrated reference buffer. In addition to the higher level of integration, which enables a smaller board footprint, it also helps to eliminate the channel-to-channel variation caused by the external reference buffer variations. Another advantage of this SAR ADC is its zero latency which makes it a perfect choice for higher sampling rate MUXed applications as the one described in the TIDA-01051 TI Design.

1.5.5 LM7705

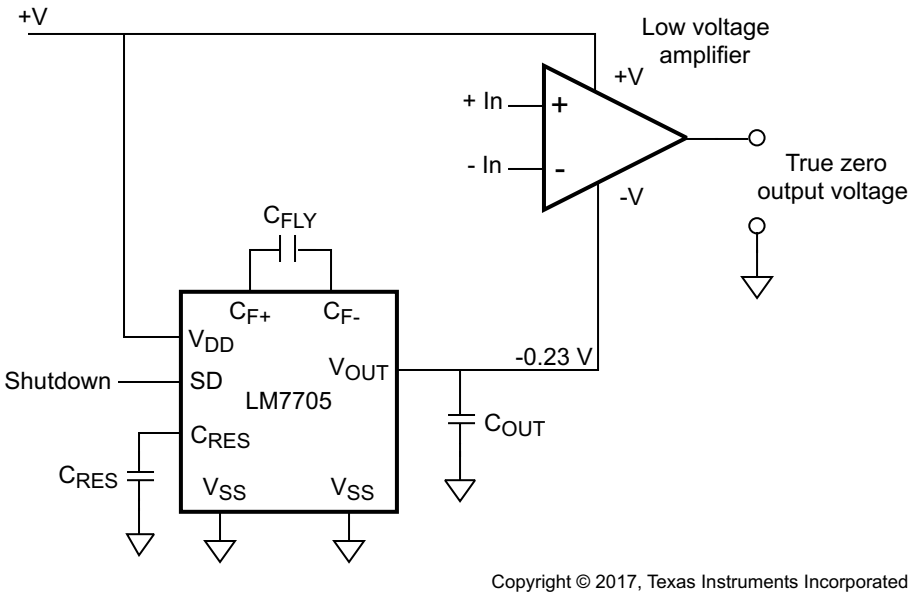

Figure 77. LM7705 Typical Application

The LM7705 device is a switched capacitor voltage inverter with a low-noise, −0.23-V fixed negative voltage regulator. This device is designed to be used with low-voltage amplifiers to enable the amplifiers output to swing to 0 V. The −0.23 V is used to supply the negative supply pin of an amplifier while maintaining less than 5.5 V across the amplifier. Rail-to-rail output amplifiers cannot output 0 V when operating from a single-supply voltage and can result in error accumulation due to amplifier output saturation voltage being amplified by following gain stages. A small negative supply voltage will prevent the amplifiers output from saturating at 0 V and will help maintain an accurate zero through a signal processing chain. Additionally, when an amplifier is used to drive an input of the ADC, the amplifier can output a zero voltage signal and the full input range of an ADC can be used. The LM7705 device also has a shutdown pin to minimize standby power consumption.

The LM7705 was selected based on its high efficiency, ease of implementation, and low quiescent current. The LM7705 is used in multiple reference designs where true rail-to-rail performance is required.

1.5.6 LMZ14201

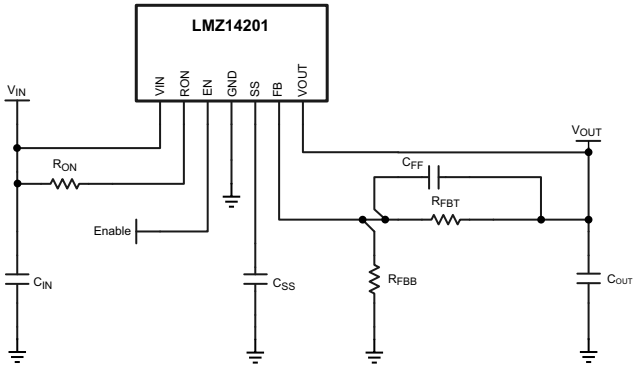

Figure 78. LMZ14201 Simplified Application Schematic

The LMZ14201 SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution that can drive up to 1-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ14201 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ14201 can accept an input voltage rail between 6 and 42 V and deliver an adjustable and highly accurate output voltage as low as 0.8 V. The LMZ14201 only requires three external resistors and four external capacitors to complete the power solution. The LMZ14201 is a reliable and robust design with the following protection features: thermal shutdown, input UVLO, output overvoltage protection, short-circuit protection, output current limit, and allows start-up into a pre-biased output. A single resistor adjusts the switching frequency up to 1 MHz.

The LMZ14201 is used to bring the 24-V input voltage down to 18.5 V in a highly efficient manner. This part was selected based on the availability of its robust simulation models, high efficiency rating, and ease of implementation. Due to it containing an integrated inductor, the LMZ14201 only requires three external resistors and four external capacitors. This low external component count largely simplifies PCB layout.

1.5.7 TPS7A47

The TPS7A47 is a family of positive voltage (36 V), ultra-low-noise (4 μV_{RMS}) LDOs capable of sourcing a 1-A load.

The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count.

The TPS7A4701 output voltage can be configured with a user-programmable PCB layout (up to 20.5 V), or adjustable (up to 34 V) with external feedback resistors.

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, ADCs, DACs, and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test-and-measurement.

In addition, the TPS7A47 is ideal for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversions, maximum system performance is ensured in sensitive instrumentation, test and measurement, audio, and RF applications.

The TPS7A47 is used to drop the output voltage of the switching regulators by 0.5 V while simultaneously filtering the voltage ripple for the analog supplies. This device was selected due to its adjustability, which allowed for it to be used in multiple places in the design.

1.5.8 LMZ14202

The LMZ14202 SIMPLE SWITCHER power module is an easy-to-use step-down DC-DC that can drive up to 2-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ14202 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ14202 can accept an input voltage rail between 6 and 42 V and deliver an adjustable and highly accurate output voltage as low as 0.8 V. The LMZ14202 only requires three external resistors and four external capacitors to complete the power solution. The LMZ14202 is a reliable and robust design with the following protection features: thermal shutdown, input undervoltage lockout, output overvoltage protection, short-circuit protection, output current limit, and allows start-up into a pre-biased output. A single resistor adjusts the switching frequency up to 1 MHz.

The LMZ14202 is used to bring the 24-V input voltage down to 3.8 V in a highly efficient manner. This part was selected based on the availability of its robust simulation models, high efficiency rating, and ease of implementation. Due to it containing an integrated inductor, the LMZ14202 only requires three external resistors and four external capacitors. This low external component count largely simplifies PCB layout.

1.5.9 LMZ14203

The LMZ14203 SIMPLE SWITCHER power module is an easy-to-use step-down DC-DC solution that can drive up to 3-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ14203 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ14203 can accept an input voltage rail between 6 and 42 V and deliver an adjustable and highly accurate output voltage as low as 0.8 V. The LMZ14203 only requires three external resistors and four external capacitors to complete the power solution. The LMZ14203 is a reliable and robust design with the following protection features: thermal shutdown, input UVLO, output overvoltage protection, short-circuit protection, output current limit, and allows start-up into a pre-biased output. A single resistor adjusts the switching frequency up to 1 MHz.

The LMZ14203 is used to bring the 24-V input voltage down to 5.5 V in a highly efficient manner. This part was selected based on the availability of its robust simulation models, high efficiency rating, and ease of implementation. Due to it containing an integrated inductor, the LMZ14203 only requires three external resistors and four external capacitors. This low external component count largely simplifies PCB layout.

1.5.10 LM5574

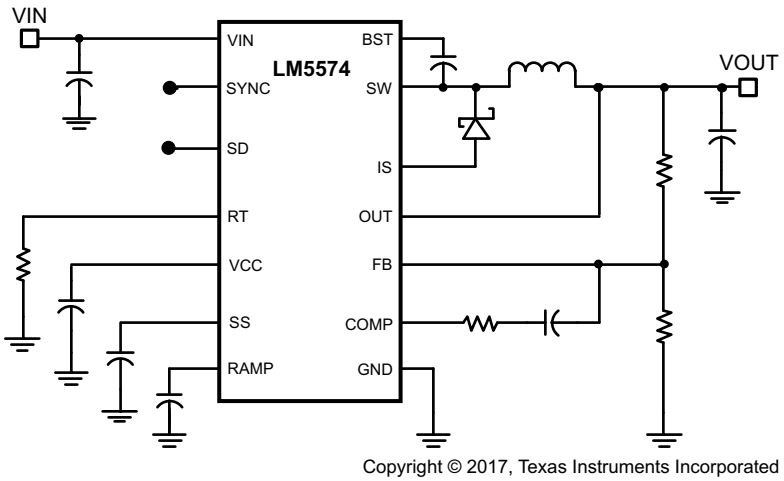

Figure 79. LM5574 Simplified Application Schematic

The LM5574 is an easy to use SIMPLE SWITCHER buck regulator, which allows engineers to design and optimize a robust power supply using a minimum set of components. Operating with an input voltage range of 6 to 75 V, the LM5574 delivers 0.5 A of continuous output current with an integrated 750-mΩ N-Channel MOSFET. The regulator utilizes an emulated current mode architecture, which provides inherent line regulation, tight load transient response, and ease of loop compensation without the usual limitation of low-duty cycles associated with current mode regulators. The operating frequency is adjustable from 50 to 500 kHz to allow optimization of size and efficiency. To reduce EMI, a frequency synchronization pin allows multiple IC's from the LM2557x family to self-synchronize or to synchronize to an external clock. The LM5574 ensures robustness with cycle-by-cycle current limit, short-circuit protection, thermal shutdown, and remote shutdown. The device is available in a TSSOP-16 package. The LM5574 is supported by the full suite of WEBENCH on-line design tools.

This device was selected due to its WEBENCH support. A full schematic meeting all the necessary requirements was generated by WEBENCH for this component. This greatly simplified implementing this component. This device is used to generate a –18.5-V rail in a highly efficient manner.

1.5.11 TPS7A3001

The TPS7A30 series of devices are negative, high-voltage (–35 V), ultra-low-noise (15.1 μV_{RMS}, 72-dB PSRR) linear regulators that can source a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A30 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This TI Design makes the device an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A30 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

The TPS7A3001 is used to drop the –18.5-V rail down to a –18-V rail.

1.5.12 REF6041

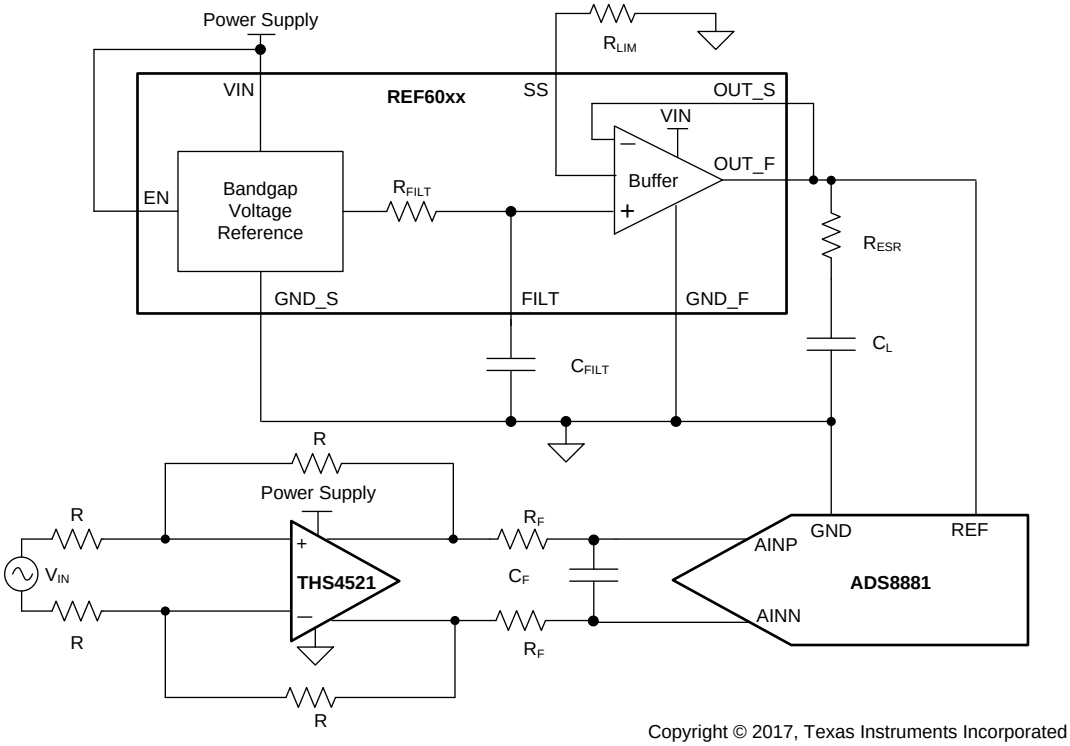

Figure 80. REF6041 Typical Application Circuit

The REF6000 family of voltage references have an integrated low output impedance buffer that enable the user to directly drive the REF pin of precision data converters, while preserving linearity, distortion, and noise performance. Most precision SAR and delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. In order to support this dynamic load the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF6000 family devices are well suited, but not limited, to drive the REF pin of the ADS88xx family of SAR ADCs, and ADS127xx family of delta-sigma ADCs, as well as other DACs.

The REF6000 family of voltage references is able to maintain an output voltage within 1LSB (18-bit) with minimal droop, even during the first conversion while driving the REF pin of the ADS8910B. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data acquisition systems. The REF60xx variants of REF6000 family specify a maximum temperature drift of just 5 ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low output impedance buffer combined

A 4.096-V reference voltage is required to meet the LSB specifications of this TI Design. The REF6041 also contains an internal buffer enabling multiple ADCs to be driven in parallel.

1.5.13 OPA376

The OPA376 family represents a new generation of low-noise operational amplifiers with e-trim™, offering outstanding DC precision and AC performance. Rail-to-rail input and output, low offset (25 µV, maximum), low noise (7.5 nV/√Hz), quiescent current of 950 µA (maximum), and a 5.5-MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making it attractive for applications that run directly from batteries without regulation. In addition to that this part is unity gain stable and capable of driving high capacitive loads which makes it an excellent choice for buffering the output common mode voltages for the THS4551 and OPA625.

1.5.14 SN74AHC1G04

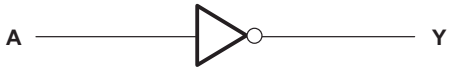

Figure 81. SN74AHC1G04 Simplified Schematic

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function Y = –A. The SN74AHC1G04 is used to help synchronize the SCLK signal with the conversion start signal at the conversion start input to the ADC.

1.5.15 SN74AUP1G80

SN74AUP1G80 is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire VCC range of 0.8 to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity.

The SN74AUP1G80 is used in coalition with the SN74AHC1G04 inverter to synchronize the conversion start signal with the SCLK signal at the ADC.

1.5.16 LMK61E2

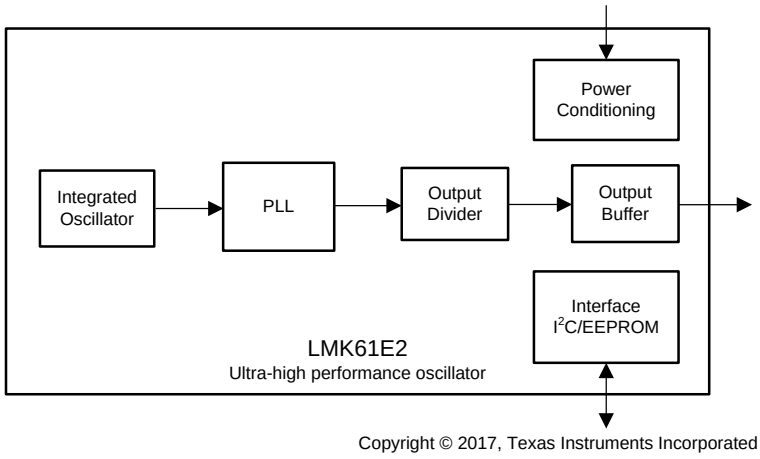

Figure 82. LMK61E2 Simplified Block Diagram

The LMK61E2 is an ultra-low jitter PLLatinum programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly used reference clocks. The outputs can be configured as LVPECL or LVDS or HCSL.

The device features self-startup from on-chip EEPROM that is factory programmed to generate a 156.25-MHz LVPECL output. The device registers and EEPROM settings are fully programmable in-system through an I^2C serial interface. Internal power conditioning provide excellent PSRR, reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V ± 5% supply.

The device provides fine and coarse frequency margining options through an I^2C serial interface to support system design verification tests (DVT) such as standard compliance and system timing margin testing.

This clock generator is used as the main system clock generator. It was selected based on its adjustability, very low jitter, low power, and robust supply noise immunity.

1.5.17 LMK00804B

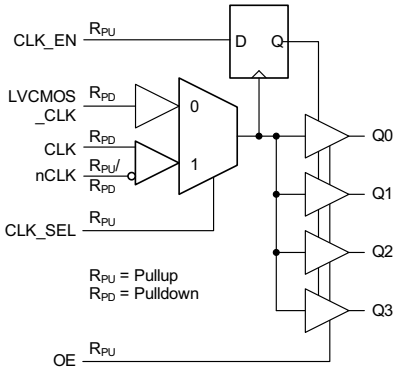

Figure 83. LMK00804B Simplified Schematic

The LMK00804B is a low skew, high performance clock fanout buffer which can distribute up to four LVCMOS or LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels) from one of two selectable inputs, which can accept differential or single-ended inputs. The clock enable input is synchronized internally to eliminate runt or glitch pulses on the outputs when the clock enable terminal is asserted or de-asserted. The outputs are held in logic low state when the clock is disabled. A separate output enable terminal controls whether the outputs are active state or high-impedance state. The low additive jitter and phase noise floor, and guaranteed output and part-to-part skew characteristics make the LMK00804B ideal for applications demanding high performance and repeatability.

The output of the LMK61E2 is a differential LVDS signal. However, all of the components requiring clocking accept a single ended LVCMOS clock input. The LMK00804B takes the LVDS signal from the LMK61E2 and splits it into 4 synchronized LVCMOS outputs. This allowed for the same buffered clock signal to be present at each clocked device. The LMK00408B was selected as it contains the correct number of outputs in the correct format, has very low additive jitter, and is easy to implement.

2 Getting Started Hardware

This section outlines the information for getting the board up and running.

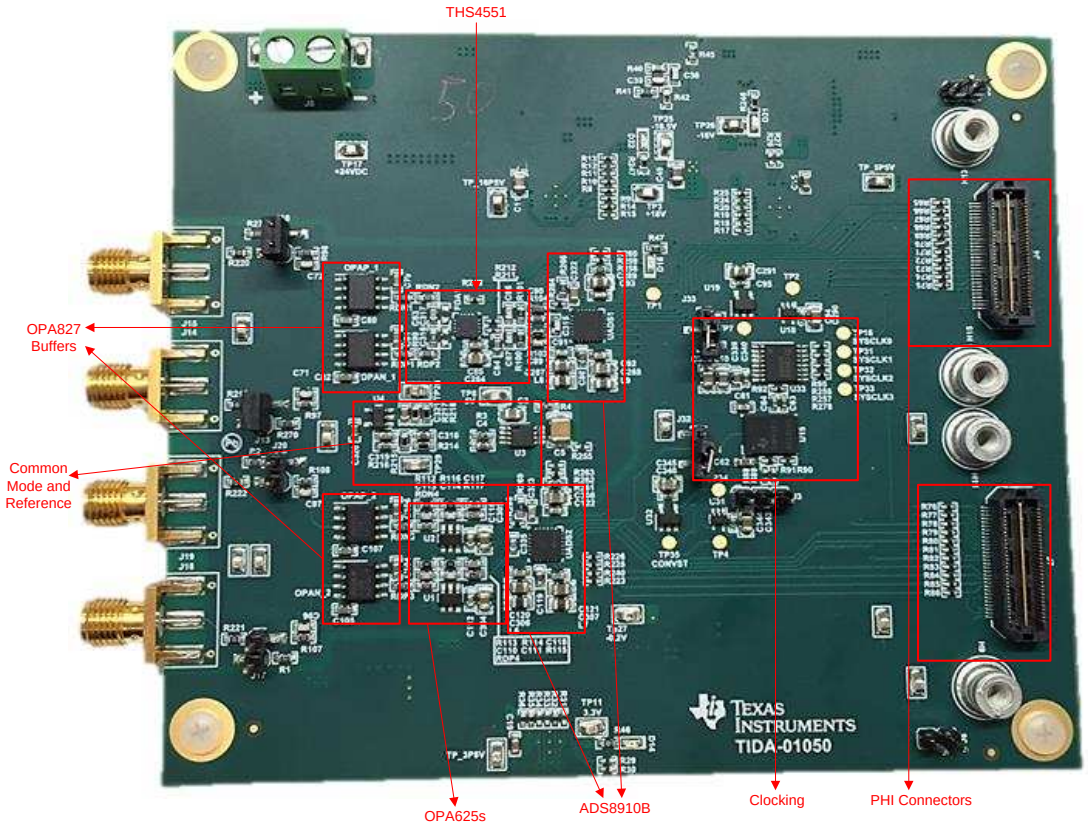

Figure 84. TIDA-01050 Hardware

2.1 Jumper Configuration

This system has a large amount of configurable options. These options are selectable through the use of three pin jumpers. Table 3 highlights the purpose of each jumper as well as the default configurations.

Table 3. Jumper Configuration

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
J32	CONVST synched with SYSCLK to ADC (jitter cleaner)	CONVST from PHI connector	Short pins 2 and 3
J33	CONVST synched with SYSCLK to ADC (jitter cleaner)	CONVST from PHI connector	Short pins 2 and 3
J5	Short to load EEPROM	Only a 2-pin header	Short
J6	Short to load EEPROM	Only a 2-pin header	Short
J13	Short when no input signal present	Only a 2-pin header	Short
J16	Short when no input signal present	Only a 2-pin header	Short
J17	Short when no input signal present	Only a 2-pin header	Short
J20	Short when no input signal present	Only a 2-pin header	Short

2.2 PHI Hardware

Before using the PHI connector, short Jumpers J5 and J6 and attach the PHI board to the onboard connector. The PHI EEPROM must be initialized first before the board can be used. To do this, launch the PHI Software Launcher software and select *EEPROM Loader*. Next, select the ADS8910B from the list of devices and click *Load*. Once the proper device is selected, click *Write* and *Verify*. The EEPROM will now be loaded and initialized for use.

2.3 Measuring SNR, THD, SFDR, SINAD, and ENOB

The TIDA-01050 hardware testing requires a high quality signal generator with a differential output because the generator's performance can limit measurement results. The Audio Precision AP-2700 series was used to generate the inputs necessary for system characterization and its characteristics are given in Table 4.

Table 4. External Source Requirements

DESCRIPTION	VALUE
External source type	Balanced differential
External source impedance (RS)	10 to 30 Ω
Maximum noise	10 μV_{RMS}
Maximum SNR	110 dB
Maximum THD	–130 dB

Using SMA cables, attach the signal from the signal generator to either the single-ended or fully differential front-end. Next, attach the PHI module to the respective connector. Set the signal generator to a 2-kHz differential output at the amplitude of choice. Remove the corresponding shorting links from the input of the system.

Install and run the ADS8910B EVM software, click on *Spectral Analysis* and set the SCLK frequency and sampling rate to the desired amounts. Once the software is configured, click *Capture*. The software will take the corresponding number of samples and calculate the SNR, THD, SFDR, SINAD, and THD.

2.4 Using Onboard Clocking and Jitter Cleaner

To program the LMK61E2, use the USB2ANY controller from Texas Instruments. Connect the SCL signal to pin 3 of J3 and connect the SDA signal to pin 2 of J3. Pin 1 of J3 will be connected to ground. Once the device is connected to the USB2ANY controller, install and run Codeloader. Once installed, click on *Select Device* and select the LMK61E2 under *Clock Conditioners*. Next, click on *Find I2C Address* to locate the I2C address of the onboard LMK61E2. Once the address has been located, select the desired clocking frequency and select LVDS as the output format. Click *Generate Configuration* and then *Program EEPROM* to set the device.

Now that the LMK61E2 is generating the clock, change the setting on Jumpers J32 and J33. This will activate the jitter cleaner and conversion start synchronization circuitry. Next, go back to the ADS8910B EVM software, select multiSPI under *SDO Mode* and select INTCLK under *Clock Source*. Make sure to set the SCLK frequency to the same frequency as the LMK61E2 frequency to receive proper measurements.

Once the hardware and software have been configured to accept the on board clock, capture data using the ADS8910B EVM software and observe the results.

3 Testing and Results

An Audio Precision 2700 series signal generator was used as the signal source to test the AFE and ADC performance. The AP2700's noise and THD has adequate performance and will not limit measurements. It is crucial to use a quality source as to not limit the systems performance by the signal source. A generic DC power supply was used to generate the 24-V DC input voltage.

Once the board was powered up and the signal was connected through an SMA cable, the shorting links on the input could be removed. Next, the PHI module is attached and the software is enabled on the host PC. Within the software, the ADC can be configured to the desired settings and tests can be run. Measuring SNR, THD, and ENOB can be performed when running a spectral analysis from the ADS8910B EVM GUI.

The AP2700 was set to output a 2-kHz 24-V pk-pk sinusoid, this was chosen as 2 kHz is the standard frequency used when measuring noise and THD. A 24-V pk-pk signal was used as it would grant full range on the THS4551 or OPA625 amplifier and would thus grant full range at the ADC from 0 to V_{REF}.

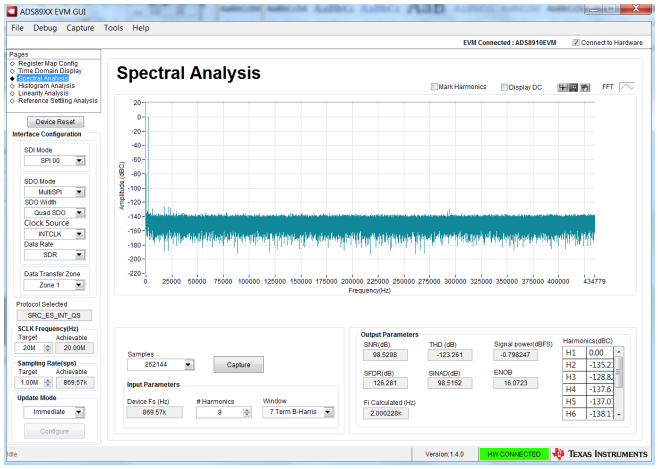

Figure 85. THS4551 Results

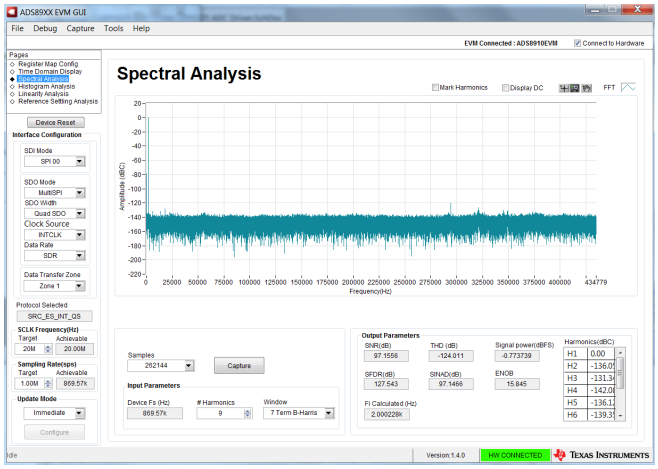

Figure 86. OPA625 Results

Figure 85 and Figure 86 highlight the results achieved with both the THS4551 and the OPA625s. The SNR is slightly better for the THS4551 than the OPA625s. The THD numbers are slightly lower than expected due to output voltage limitations of the AP2700. All of the other results are matching or exceeding the system requirements as outlined in Table 5.

Table 5. Results

SPECIFICATION	THS4551	OPA625
SNR	98.53 dB	97.16 dB
THD	–123.26 dB	–124.01 dB
ENOB	16.07	15.85
SFDR	126.28 dB	127.54 dB

When comparing the two measurement results, slightly better SNR performance have been achieved with fully differential configuration. This was an expected result as the system's bandwidth was limited to the frequency range where the noise performance of THS4551 is superior to dual OPA625 configuration. The THD measurements recorded in this TI Design may not be the best indication of system's performance. Due to the attenuator configuration, the AP2700 signal generator had to be configured to very high amplitudes for the ADC to see a full range signal. At these high amplitudes, the THD performance of the AP2700 degrades. But even with these measurement setup limitations, the THD measurement results have exceeded the systems specifications for both configurations.

When observing the spectrums for both the OPA625 and the THS4551 in Figure 85 and Figure 86, there is more noise at higher frequencies on the OPA625s spectrum than the THS4551. This result can be attributed to the parts PSRR. As described previously, the PSRR for the OPA625 is worse than the THS4551 at the higher frequencies where there is some noise coming through from the switching regulators used in this TI Design.

In conclusion, even though the results for both configurations are very comparable, there are other requirements for high channel count automatic test equipment that make differential driver solution a preferred choice. The total power consumption and the board density optimization are two key specifications for these systems. As described previously, the power consumption for the dual OPA625 configuration is about 3× larger compared to the single THS4551. In addition, the total number of external components is smaller for THS4551 as well. When these advantages are multiplied by a large number of data channels, a solution using an FDA such as the THS4551 may be preferred.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01050.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01050.

4.3 PCB Layout Recommendations

Due to the complexity of this TI Design, many design considerations need to be taken when developing the PCB layout. This TI Design features a split ground plane. The ground plane is split between an analog ground and digital ground. The two grounds meet underneath the ADCs to connect the two planes. The digital ground includes all of the power switching regulators as well as all the digital signals from the ADC. The analog ground covers all of the analog circuitry prior to the ADC. It is important to keep the differential input signal traces the same length in order to negate any potential propagation loss on these lines.

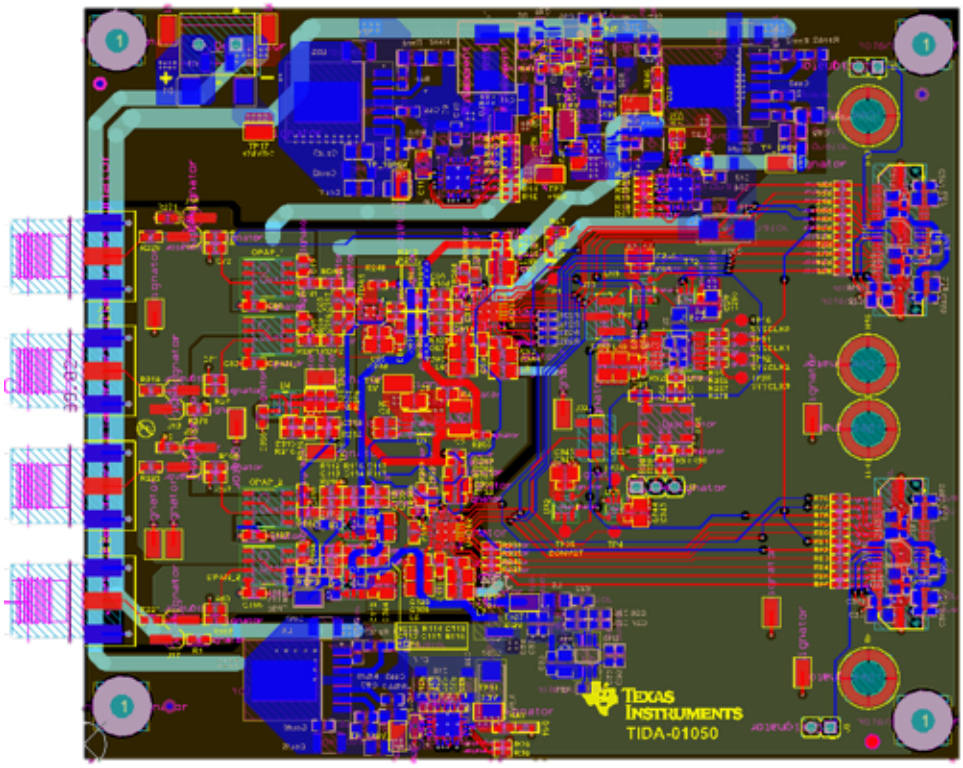

Figure 87. Layout Preview

Figure 87 highlights the layout for TIDA-01050. The brownish colored layer is the ground plane. The ground plane is split between the analog and digital sections. The split is highlighted by the black line starting at the edges of the SMA connectors and going around the ADCs. It is also evident that the signal path of the differential inputs is the same length.

4.3.1 Power Layout Design

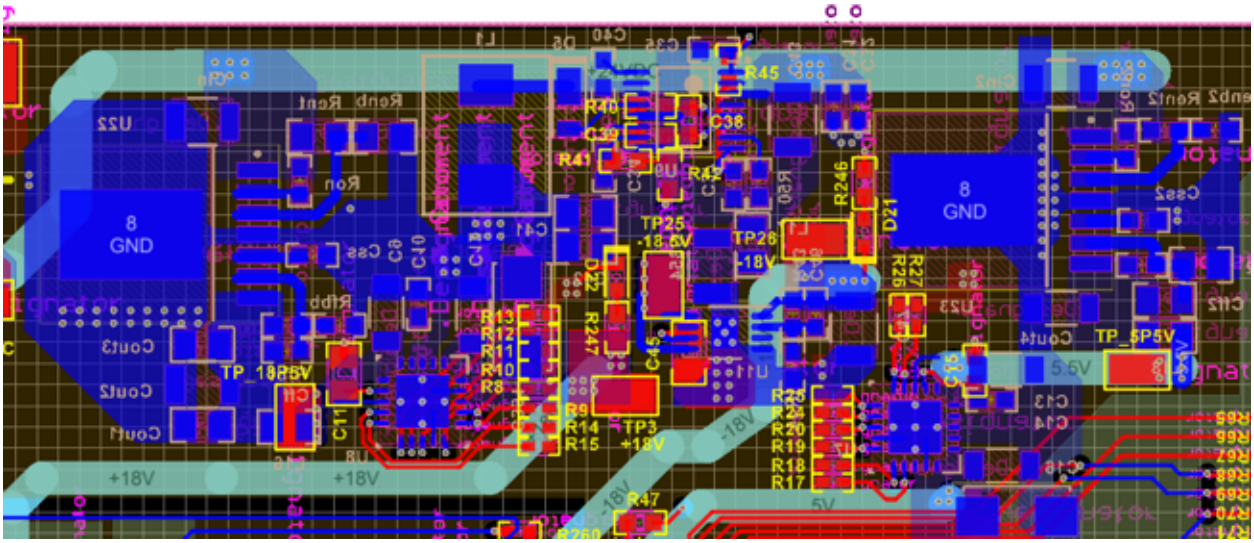

Figure 88. Power PCB Layout

For more layout guidelines, carefully analyze device datasheets when designing the layout for the power section of this TI Design. Figure 88 highlights the PCB layout for the power components. The switching regulators are placed on the outside edge of the board as far away as possible from the sensitive analog signals. The LDOs are then placed below the switching regulators to keep the power traces as short as possible to the isolated analog section. The input and output capacitors for each device are placed as close as possible to the input and output pins. Each capacitors ground is also placed on the same ground as the respective device. This same design process was taken for all of the different power rails.

For more PCB layout guidelines on power, see the device datasheets.

4.3.2 AFE Layout Design

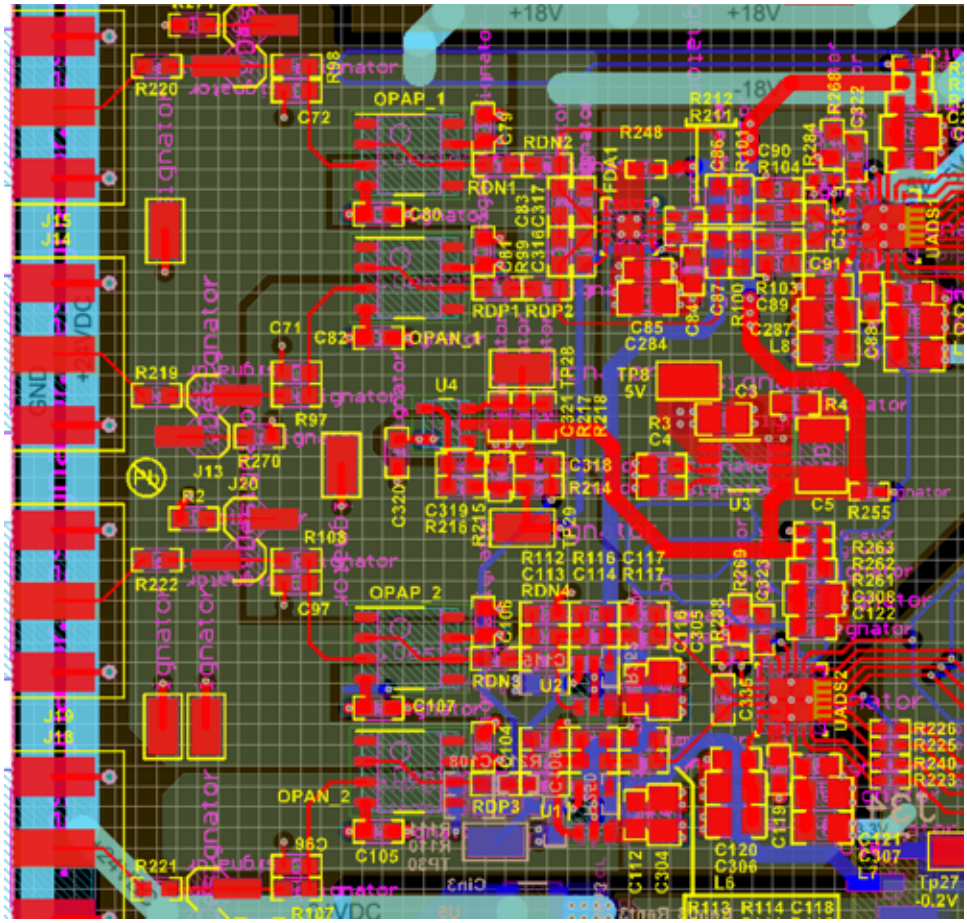

Figure 89. AFE Layout

When designing the PCB layout for the AFE, the main goal is to keep the signal path as short and symmetric as possible. The OPA827, OPA625, THS4551, and all surrounding passive components were placed and routed with signal path length being the main design concern. Input and output capacitors were placed as close as possible to the devices power and output pins as possible. See the respective device datasheets for more layout guidelines.

4.3.3 PHI Connector and Clocking Layout Design

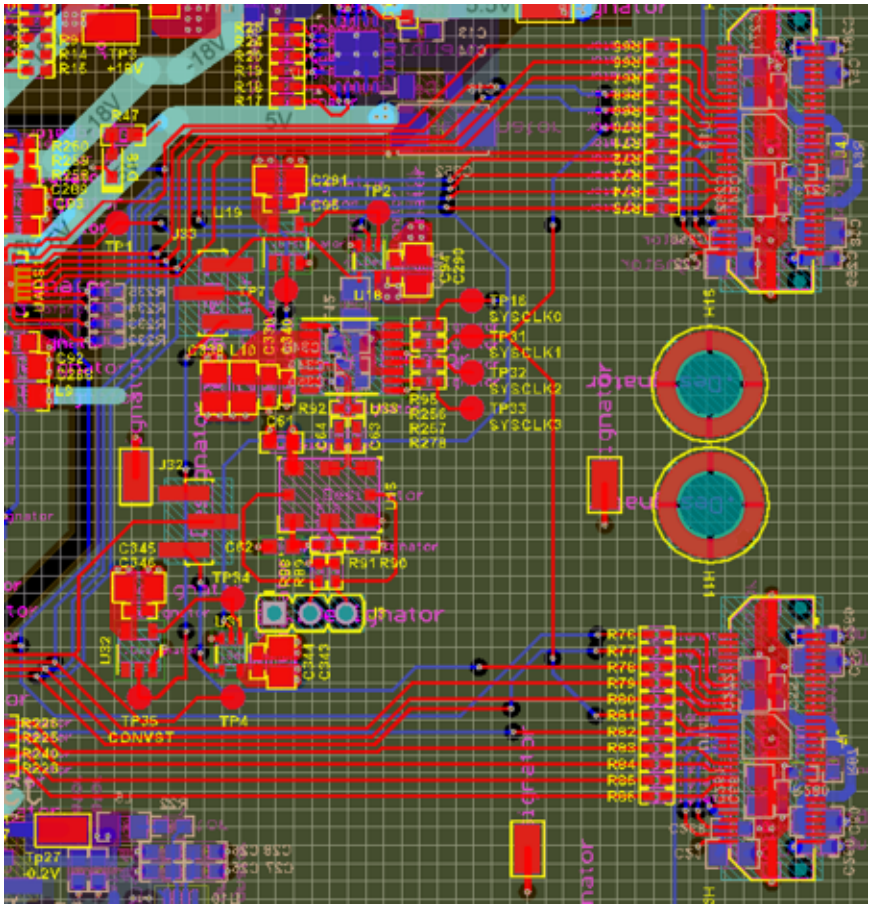

Figure 90. PHI Connector and Clocking Layout

Past the ADC, all of the signals are digital and trace length is no longer much of a concern. Again, input and output capacitors are placed as close as possible to the respective devices. Clocking is centrally placed in between the two PHI connectors on the digital ground. For more layout guidelines, see the device datasheets.

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01050.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01050.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01050.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01050.

5 Related Documentation

This design guide has no related documentation to highlight.

5.1 Trademarks

6 About the Authors

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• Changed language and images to fit current style guide	1
• Changed title from *Multi-Input Reference Design Optimizing Channel-to-Channel Variation for Semiconductor and LCD Automatic Test Equipment*	1
• Changed the result of Equation 2	5
• Changed the limit of high input amplitude signals from 263 kHz to 525 kHz	5
• Changed Figure 5	5
• Changed Figure 6	6
• Changed Figure 7	6
• Changed Figure 16	11
• Changed Figure 17	11
• Changed Figure 18	12
• Changed Equation 4	12
• Changed Equation 5	12
• Changed Figure 19	13
• Changed Figure 20	13
• Changed Equation 6	14
• Changed Figure 21	14
• Changed Figure 22	14
• Changed Figure 25	17
• Changed Figure 27	17
• Changed Figure 28	18
• Changed Equation 7	18
• Changed Equation 8	18
• Changed Figure 29	19
• Changed Figure 30	19
• Changed Equation 9	19
• Changed Figure 31	19
• Changed Figure 32	20
• Changed phase margin from 80.17° to 75.71º	21
• Changed Figure 35	22
• Changed Figure 36	22
• Changed Figure 72	45
• Changed Figure 73	45

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