TI Designs

Clocking Reference Design for RF Sampling ADCs in Signal Analyzers and Wireless Testers

Description

The TIDA-01016 is a clocking solution for high dynamic range high-speed ADCs. RF input signals are directly captured using the RF sampling approach by high-speed ADCs. The ADC32RF45 is a dual-channel, 14-bit, 3-GSPS RF sampling ADC. The 3-dB input bandwidth is 3.2 GHz, and it captures signals up to 4 GHz. This TI Design showcases the clocking solution using the LMX2582 to achieve the best SNR performance of the ADC32RF45 at higher input frequencies used in microwave backhaul applications.

Resources

TIDA-01016	Design Folder
ADC32RF45EVM	Tools Folder
ADC32RF45	Product Folder
LMX2582	Product Folder
LMK04828	Product Folder
TSW14J56EVM	Tools Folder

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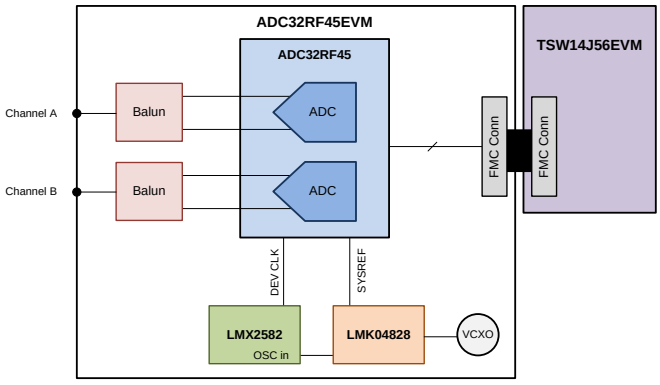
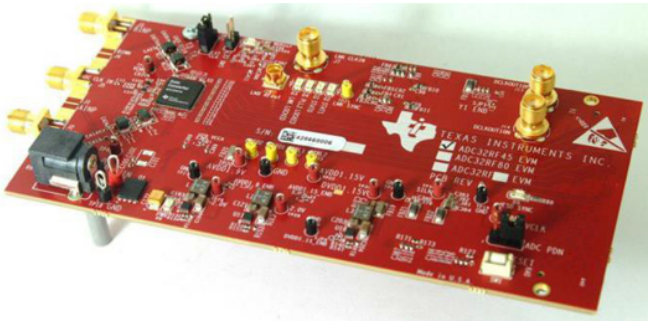
Features

- 3-GSPS RF Sampling ADC Clocking Solution
- 4-GHz High-Frequency Input Signal Capture Capability
- Low-Noise, High Dynamic Range RF Sampling Receiver Solution
- Low-Phase Noise Clocking Solution for RF Sampling ADC

Applications

- Wireless Communication Test Equipment
- Vector Signal Analyzer
- RADAR
- Microwave Backhaul
- Software Defined Radio (SDR)





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1 System Overview

1.1 System Description

This reference design implements the clocking solution for RF sampling receiver capable of capturing signals up to 4 GHz that can be used in microwave backhaul applications. This TI Design focuses on the LMX2582 RF synthesizer as an input clock source for the ADC32RF45 to achieve optimum signal chain SNR performance. A low-jitter clocking solution is required in high dynamic range ADC to achieve better SNR performance at high input frequencies. The LMX2582 can generate clocks up to 5.5 GHz with low jitter.

In this solution, the LMX2582 generates the DEVCLK (sampling clock) for the ADC32RF45. The LMK04828 generates the reference clock for the LMX2582. The LMK04828 also generates the SYSREF and other clocks required for a JESD204B interface between the ADC32RF45 and FPGA.

Wireless communication test equipment and microwave backhaul equipment requires a high dynamic range and wide receiver bandwidth for 3G and later standards. The ADC32RF45 ADC is well suited for these requirements. The clocking solution described in this TI Design provides an optimum solution for clocking the ADC32RF45 to achieve both high dynamic range and wide receiver bandwidth for these applications.

Software Defined Radio (SDR) technology needs high dynamic range, highly re-configurable receiver bandwidth and input frequency range. This TI Design can meet many of the requirements of the high performance SDRs in terms of dynamic range and re-configurability.

Furthermore, RADAR systems require high dynamic range, wide receiver bandwidth, and low latency. The signal chain solution based on the ADC32RF45, LMK04828, and LMX2582 helps to achieve optimum performance for radar applications.

1.2 Key System Specifications

The objective of the TI Design is to achieve optimum signal chain performance (SNR) and to provide a clocking solution for the same. The system level specifications outlined in Table 1 are only for the signal chain from clocking solution perspective. System level SNR is specified after considering the impact of the baluns and other elements in the ADC32RF45EVM. Table 1 shows key system level specifications.

Table 1. Key System Level Specifications

PARAMETER	SPECIFICATION	CONDITIONS
Signal-to-noise ratio (SNR in dBFS)	61.1	at 100-MHz input signal
	60.0	at 900-MHz input signal
	57.1	at 1780-MHz input signal
	56.4	at 2100-MHz input signal
	52.4	at 2700-MHz input signal
	51.7	at 3500-MHz input signal
	51.0	at 3650-MHz input signal

1.3 Block Diagram

The block diagram of the clocking solution for the ADC32RF45 and data capture using the TSW14J56EVM are shown in Figure 1. Each channel of the ADC32RF45 contains baluns to convert the single-ended input signal to differential and is provided to ADC inputs.

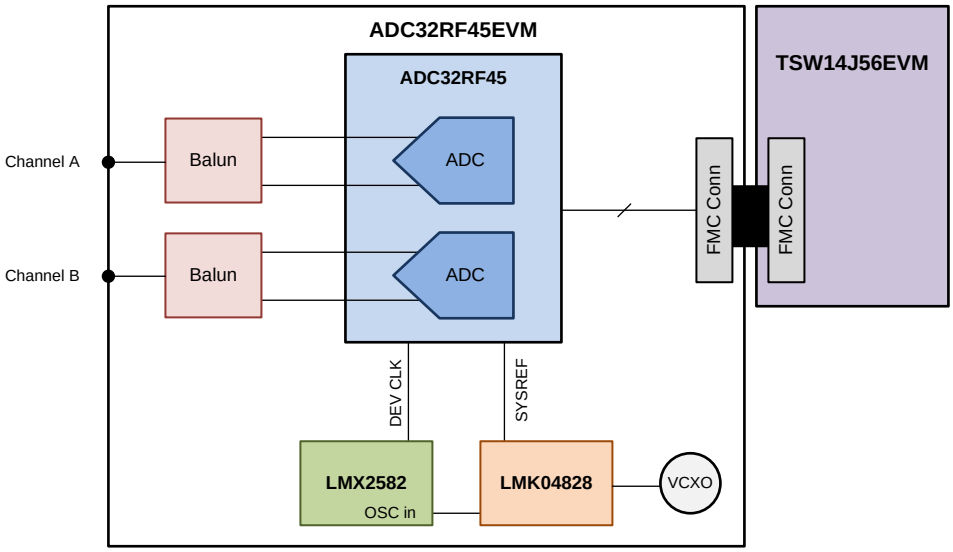

Figure 1. Block Diagram of ADC32RF45EVM and TSW14J56EVM Test Setup

1.4 Highlighted Products

1.4.1 ADC32RF45

The ADC32RF45 is a dual-channel, 14-bit, 3-GSPS ADC with built-in decimation. It has a 3-dB input bandwidth of 3.2 GHz and is usable up to 4 GHz. The ADC32RF45 employs two DDCs per channel. Each DDC incorporates decimation from 8 to 32 and an independent 16-bit NCO to support multi-band applications. The ADC32RF45 supports the JESD204B serial interface with data rates up to 12.0 Gbps using up to four lanes per ADC. The device input is buffered with an on-chip 50-Ω differential termination.

In this solution, the large receive bandwidth and high dynamic range of the ADC32F45 helps to achieve required system performance up to 3.65 GHz.

1.4.2 LMX2582

The LMX2582 is a wideband RF synthesizer with a range from 20 to 5500 MHz. It has extremely low phase noise performance, which is critical for RF sampling ADCs. The phase noise at a 3-GHz output at 1-MHz offset is –140 dBc/Hz. This performance rivals that of bench test equipment. The LMX2582 receives its reference frequency of 122.88 MHz from the LMK04828. The LMX2582 is programmed to 2949.12 MHz and its output feeds the ADC32RF45 clock input.

1.4.3 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator. An onboard 122.88-MHz VCXO provides the reference frequency. This can be locked to an external 10-MHz reference if desired. The LMK04828 supplies the JESD204B SYSREF clocks to the ADC and FPGA and passes the 122.88-MHz reference signal to the LMX2582 for its reference.

2 Getting Started Hardware and Software

2.1 Hardware Configuration

2.1.1 ADC32RF45EVM Setup

Figure 2 shows the block diagram for the setup of the ADC32RF45EVM. Follow the ADC32RF45EVM user's guide (SLAU620) for the ADC32RF45EVM hardware setup procedure. The ADC32RF45EVM has both internal as well as external options for the clock to the ADC. Selecting the DEV_CLK will be set using a switch JP3. In external clock mode, connect a signal generator set for 2.94912 GHz to the external clock input J5 and to LMK04828 reference clock input J7 using a splitter (to synchronize the same time base to both clocks).

An internal clock can be generated by the LMX2582 or LMK04828, and these devices use an onboard VCXO as reference signal. In this design, the LMX2582 provides DEV_CLK to the ADC in the internal clock configuration and the LMK04828 provides SYSREF to the ADC along with FPGA clocks for a high-speed serial interface.

Internal clock frequency will be filtered when the LMX2582 generates clock at RFoutB (J16) and is given to a BPF. This filtered output is provided to the external clock input J5, and JP3 is set to external mode.

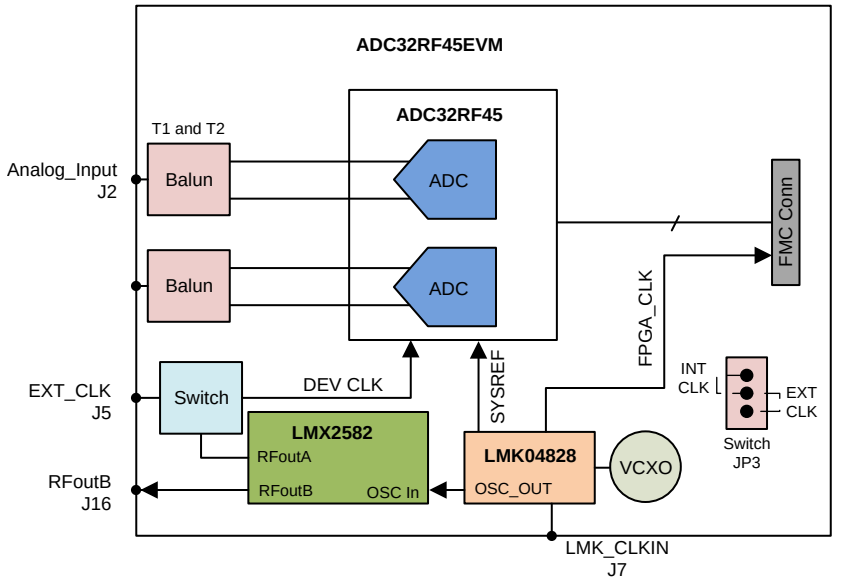

Figure 2. Block Diagram of ADC32RF45EVM

The onboard baluns T1 and T2 support up to a 3-GHz input frequency range. The input frequency range is enhanced up to 4 GHz by replacing T1 and T2 with TC1-1-43+.

2.1.2 TSW14J56EVM Setup

Follow the procedure in the TSW14J56EVM user's guide (SLWU086) to set up the TSW14J56EVM hardware.

2.2 Software Configuration

2.2.1 ADC32RF45 Programming

The ADC32RF45EVM is put into bypass mode to use the full Nyquist zone of the device. The device is setup using a five-sample mode with a JESD lane configuration corresponding to 82820. Follow the ADC32RF45EVM user's guide (SLAU620) to load the configuration file "ADC32RF4x_12bit_LMFS_82820" once the clock signal is established.

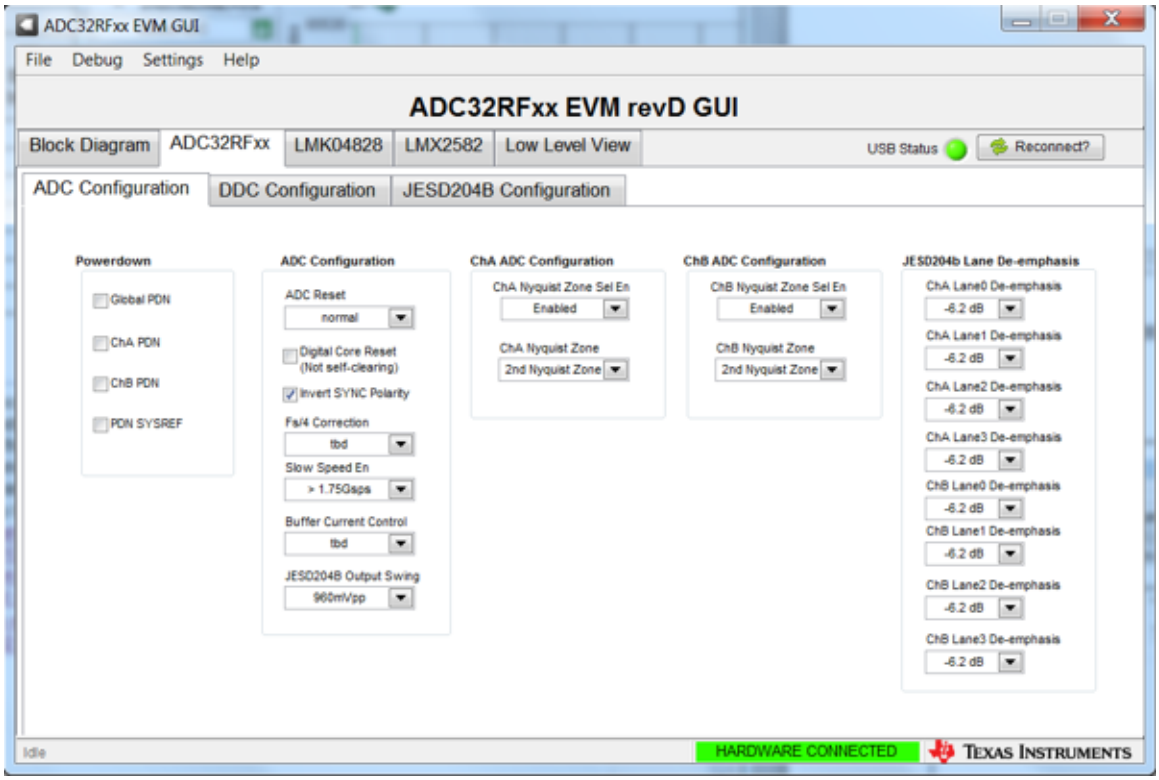

Figure 3. ADC32RF45 Programming Tab

2.2.2 LMK04828 Programming

The LMK04828 is programmed to generate the low-frequency SYSREF signal to the ADC32RF45 for JESD204B SERDES interface and FPGA clocks.

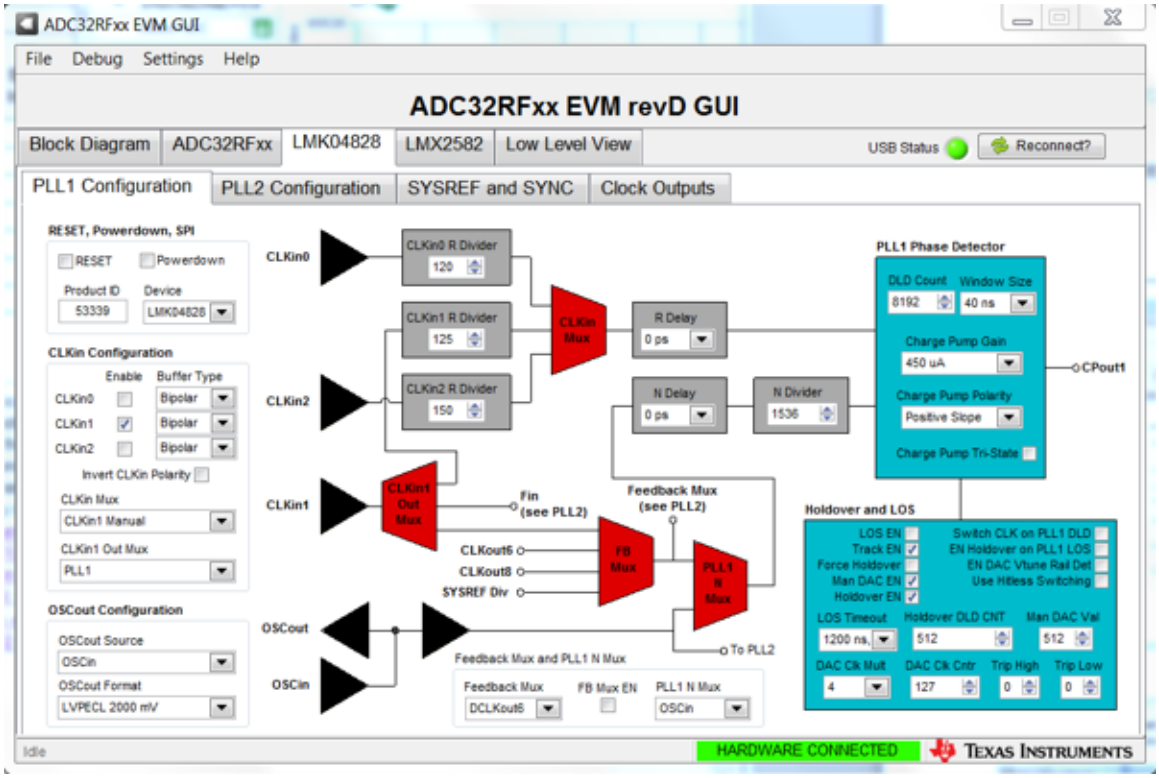

Figure 4. LMK04828 Programming Tab

2.2.3 LMX2582 Programming

The LMX2582 programming tab is shown in Figure 5. The LMX2582 is programmed to 2949.12 MHz. The VCXO reference frequency is 122.88 MHz, which is passed through from the LMK04828. The EVM has a hardware jumper to set the RF switch to the internal clock, which properly routes the LMX2582 output to the ADC clock input. Ensure that the clock signal is present before programming registers of the ADC.

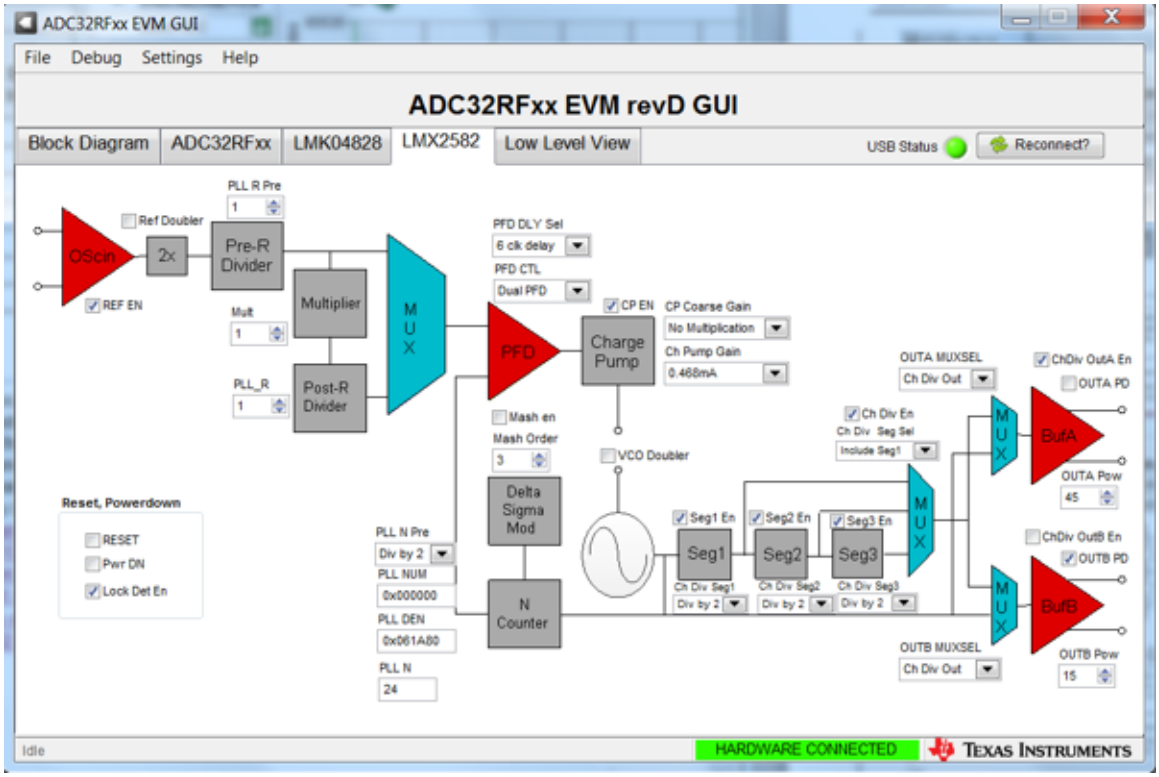

Figure 5. LMX2582 Programming Tab

2.2.4 HSDC Pro Setup

The HSDC Pro software interfaces with the TSW14J56 to capture and analyze the digital data from the ADC32RF45. Follow the TSW14J56EVM user's guide (SLWU086) for HSDC pro setup and to capture and analyze the data.

3 Testing and Results

3.1 Test Setup

SNR measurement was performed at various configurations with and without filters at the analog input as well as the clock input to the ADC32RF45. Measured results are tabulated in Section 3.2. The ADC32RF45EVM connects to the TSW14J56 EVM capture card, which is interfaced by the HSDC Pro software to capture and analyze the data.

A low-noise signal generator generates the required single-tone signal. A band-pass filter suppresses the signal-generator harmonics in the input signal as well as clock signal. T1 and T2 baluns are replaced with TC1-1-43+ to enhance the input frequency range up to 4 GHz.

3.1.1 External Clock Signal to ADC

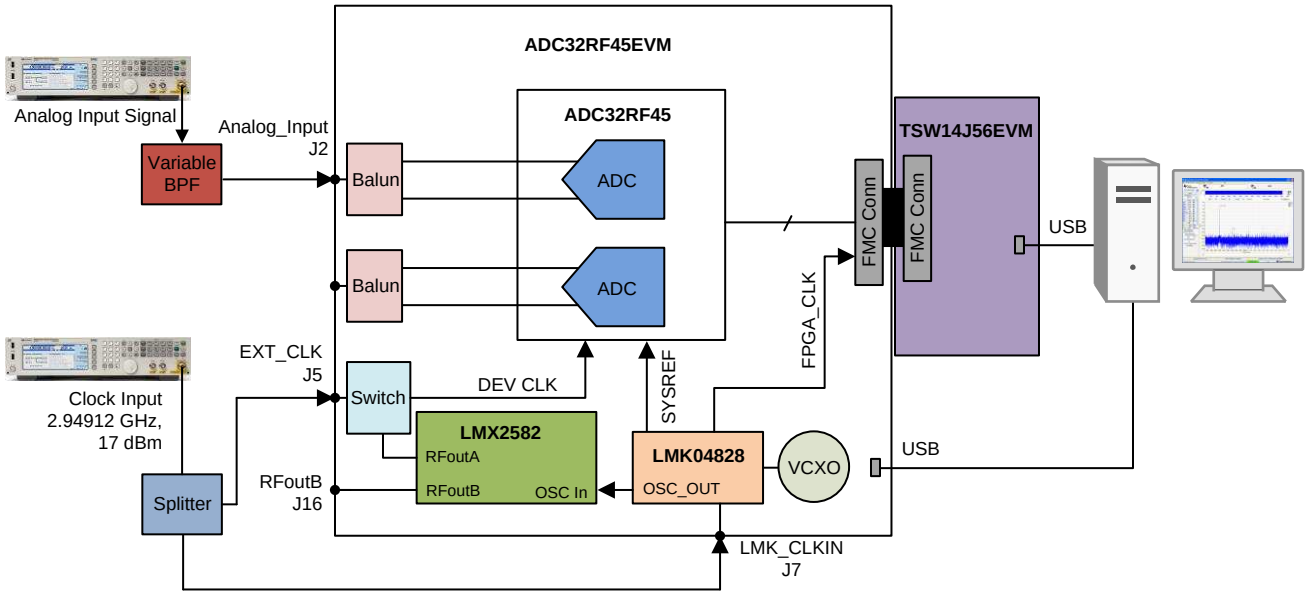

Figure 6. Test Setup for External Clock Signal

3.1.2 External Clock Signal With BPF to ADC

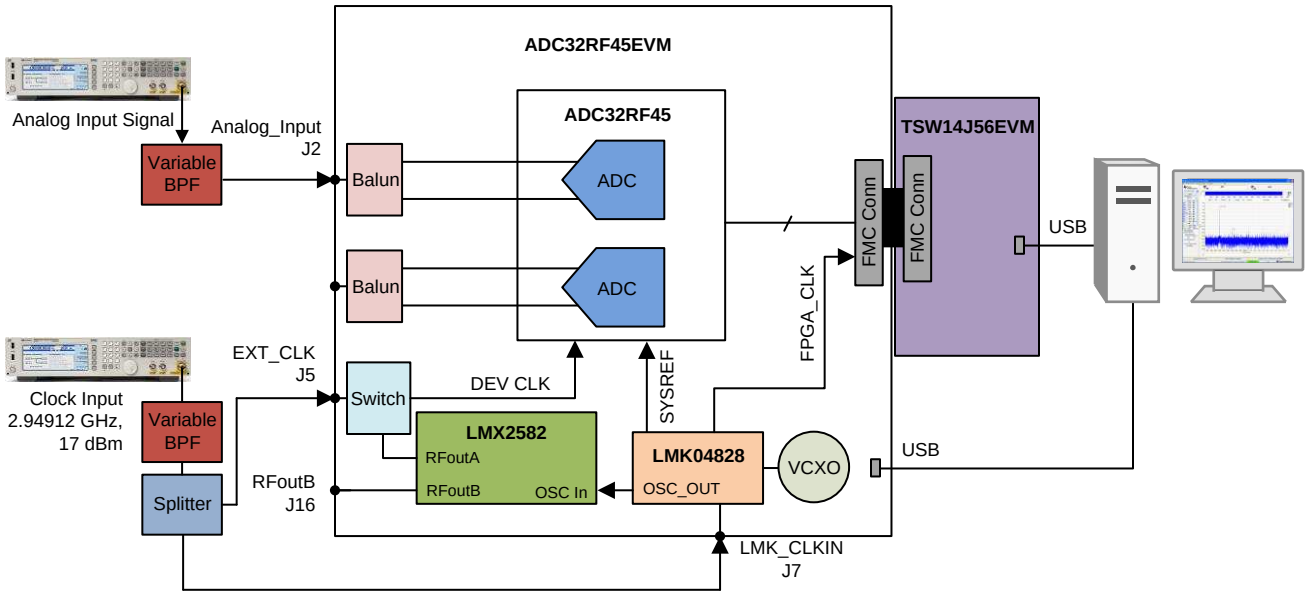

Figure 7. Test Setup for External Clock Signal With BPF

3.1.3 Internal Clock (LMX2582) Signal to ADC

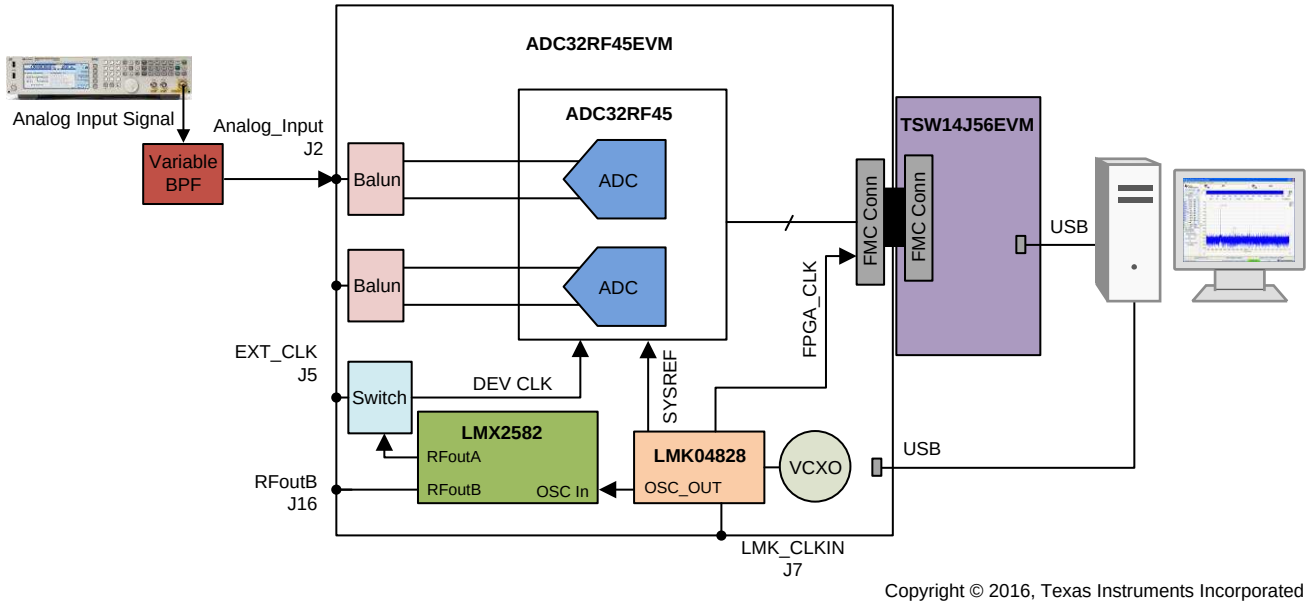

Figure 8. Test Setup for Internal Clock Signal

3.1.4 Internal Clock (LMX2582) Signal With BPF to ADC

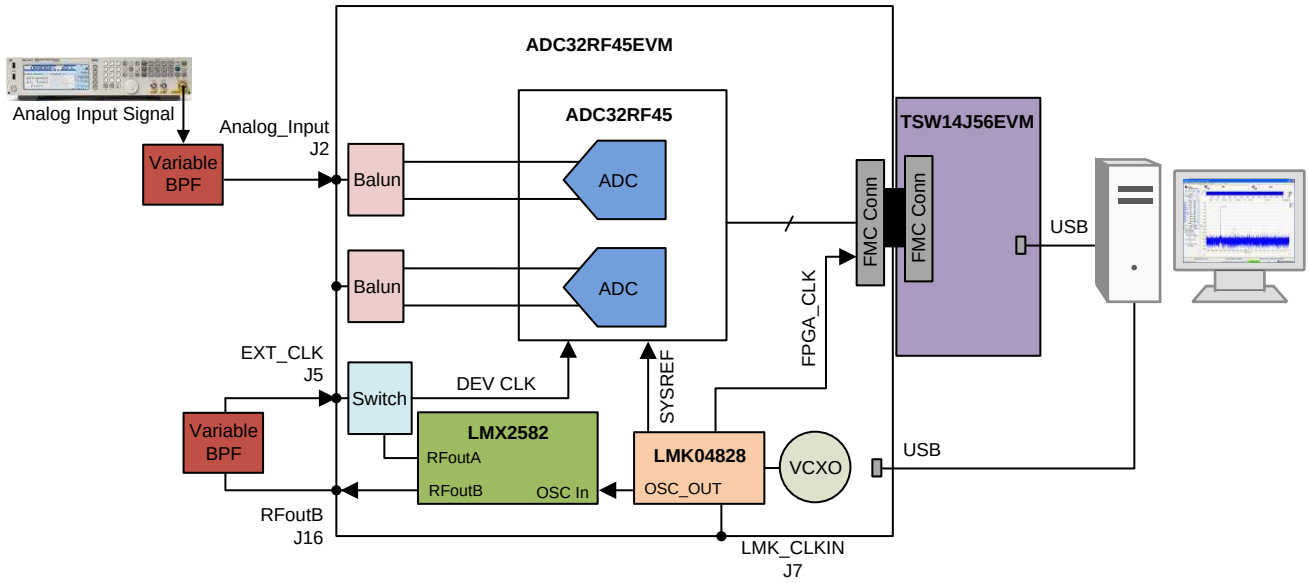

Figure 9. Test Setup for Internal Clock Signal With BPF

3.2 Results

Table 2 shows the measured SNR performance at various frequencies for a –2-dBFS differential input. The test results include enhanced input frequency to the ADC up to 3.65 GHz (for the microwave backhaul application).

Table 2. Measured Results

INPUT FREQ (MHz)	EXPECTED SYSTEM LEVEL SNR (dBFS)	EXTERNAL CLOCK		INTERNAL CLOCK (LMX2582)	
		MEASURED SNR, BPF AT INPUT (dBFS)	MEASURED SNR, BPF AT INPUT AND CLK (dBFS)	MEASURED SNR, BPF AT INPUT (dBFS)	MEASURED SNR, BPF AT INPUT AND CLK (dBFS)
100	61.1	61.12	61.17	61.12	61.09
900	60.0	58.59	60.48	59.43	60.13
1780	57.1	54.48	58.37	56.44	57.76
2100	56.4	53.84	57.53	55.48	56.90
2700	52.4	50.61	53.22	51.75	52.86
3500	51.2	48.46	51.71	50.18	51.33
3650	51.0	48.19	51.60	50.01	51.33

Figure 10 shows the measured SNR performance with internal clock at various frequencies. SNR performance is improved using the BPF at clock signal.

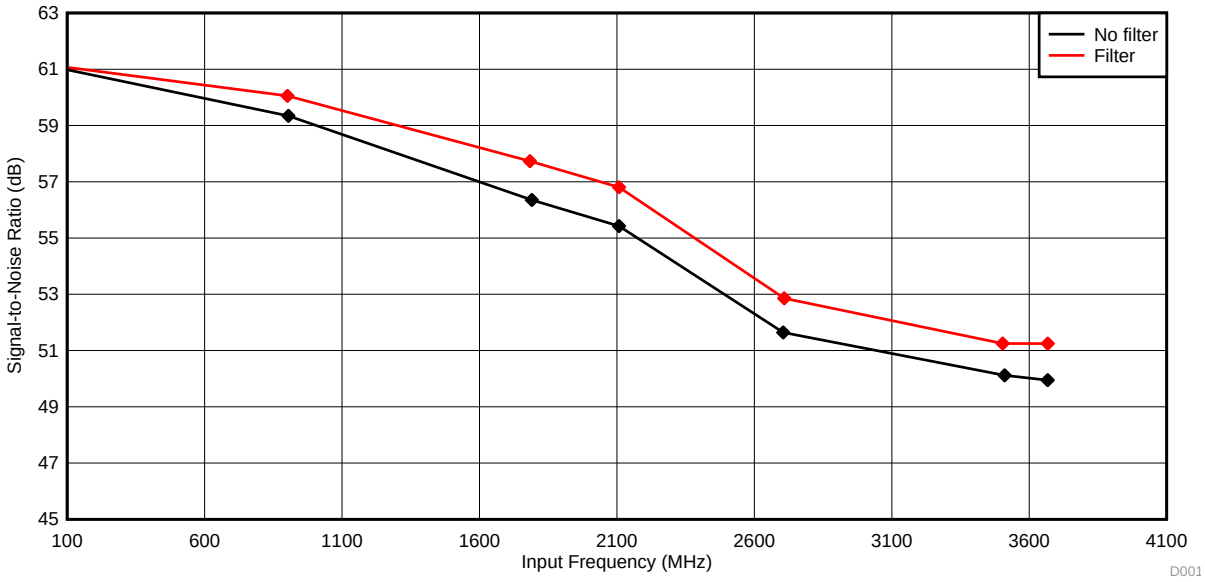

Figure 10. Measured SNR With Internal Clock

The ADC32RF45 is a direct RF sampling ADC capable of supporting up to a 4-GHz input signal frequency with a receiver bandwidth greater than 1 GHz. In order to achieve the best signal chain performance, a low-noise clocking solution is required. In this TI Design, an external precision signal generator clock source is first used in order to establish baseline SNR performance and is then compared to the integrated onboard solution using the LMK04828 and LMX2582. In both cases, measured results are presented with and without a bandpass filter to demonstrate how it can be used to minimize out of band noise, increasing the signal chain SNR by more than 1.3 dB. Finally, the results demonstrate that the integrated solution using the LMX2582 matches the SNR performance using external high-precision signal generator clock source.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01016.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01016.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01016.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01016.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01016.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01016.

5 Software Files

To download the software files, see the design files at TIDA-01016.

6 Related Documentation

1. Texas Instruments, *ADC32RF45/RF80 EVM Quick Startup Guide*, ADC32RF45EVM User's Guide (SLAU620)
2. Texas Instruments, *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card*, TSW14J56 User's Guide (SLWU086)

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7 About the Authors

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2016) to A Revision	Page
• Changed title from *Reference Design for Clocking High Dynamic Range RF Sampling ADCs in Microwave Backhaul Application*	1
• Changed from preview draft	1

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