TI Designs

Precision PWM Dimming LED Driver Reference Design for Automotive Lighting

Overview

This TI Design details a solution on how to PWM dim an automotive front light or tail light with a precision of better than 2% duty cycle without the necessity of using a microcontroller. This design uses the following devices: the TPS92691-Q1 multi-topology LED driver in boost and boost-to-battery configuration to control the LEDs and the TLC555-Q1 LinCMOS™ timer together with the OPA2377-Q1 operational amplifier to measure and generate the accurate PWM signal by applying a feedback loop and a precision shunt regulator for setting the accurate duty cycle. The input stage of the design is EMI- and EMC-filtered and can be directly supplied by a car battery.

Features

- Precision PWM Dimming
- Efficiency-Optimized Design
- Operation Through Cold Crank
- Load Dump Tolerant

Featured Applications

- Automotive Front Lighting
- Automotive Tail Light
- Automotive Interior Lighting

Resources

TIDA-01183	Design Folder
TPS92691-Q1	Product Folder
TLC555-Q1	Product Folder
OPA2377-Q1	Product Folder
TL431A-Q1	Product Folder

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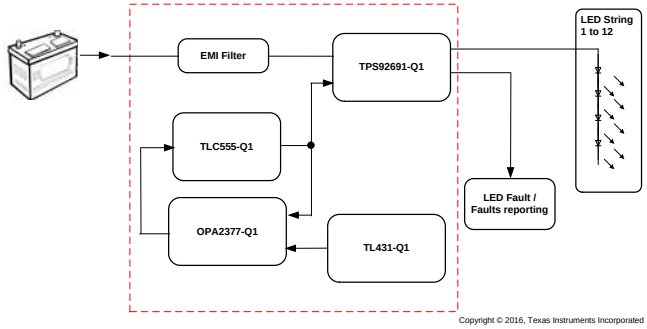

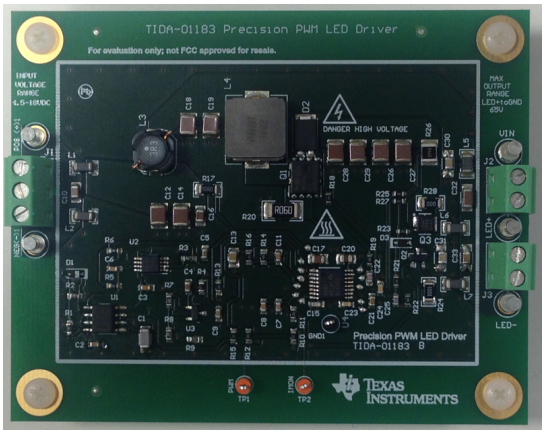

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1 System Overview

1.1 System Description

This system has been designed to be a solution to precision pulse width modulation (PWM) dimming an automotive front light or tail light with an accuracy better than 2% duty cycle without the necessity of using a microcontroller (MCU). The design includes key peripherals like electromagnetic interference (EMI) and electromagnetic compatibility (EMC) filtering-voltage-conditioning (shunt regulator), precision clock generation, and LED drive.

The TIDA-01183 has been designed with the following points in consideration:

- The design must be able to generate a precision PWM signal in the range of 5% to 50% duty cycle
- Satisfy power requirements for one TPS92691 device driving a string of 1 to 12 LEDs for a front light or tail light
- Operate over the full range of automotive battery conditions
  - VIN(min) down to 5 V simulating a cold-cranking condition (ISO 7637-2:2004 pulse 4)
  - VIN(max) up to 18 V simulating the upper range of normal battery operation
- Survive and continue operation through:
  - Load dump (ISO 7637-2:2004 pulses 5a)
  - Double battery condition
- Output protected against short-to-battery and GND voltage
- Optimize the individual blocks for smallest power dissipation and highest efficiency
- The layout of the board must be set up in such a way to minimize the footprint of the solution while maintaining high performance
- Provide flexible board interface to either mate to custom board through screw terminals
- Provide power for TLC555

1.2 Key System Specifications

Table 1. Electrical Characteristics

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
SYSTEM INPUT AND OUTPUT						
V_{IN}	Operating input voltage	Battery-voltage range; outputs are functional	5	14	18	V
V_{UVLO}	Input UVLO setting	Undervoltage lockout (UVLO)	—	4.5	—	
V_{SWMax}	Vmax switch	Maximum switch node voltage	—	—	100	V
V_{OUT}	Output voltage	LED+ to LED– (Boost)	21	—	60	V
V_{OUT}	Output voltage	LED + to V_{IN} (Boost-to-Battery)	3	—	36	
V_{TR}	Transient immunity	Load dump (ISO7637-2)	—	—	60	V
V_{IN_MIN}	Minimum input voltage	Cold crank (ISO 7637-2)	5	—	—	V
I_{IN}	Input current	Output at full load	—	2	—	A
I_{OUT}	Output current	Maximum current per string	62.5	350	1070	mA
Maximum output power	—	—	—	—	25	W
PWM dimming range	240-Hz PWM frequency	—	—	20:1	—	
$LED_{Open\ and\ short\ detect}$	LED open and short detection	—	—	Yes	—	
$LED_{Single\ short\ detect}$	LED single-short detection	—	—	No	—	
V_{TP1}	Voltage at PWM input	Amplitude dimming clock	—	5	—	V
V_{TP2}	Voltage at TP2	Voltage proportional to ouput current	—	—	5	V
ONBOARD VOLTAGES						
V_{5V5}	Auxiliary supply, shunt regulator	TLC555, op amp supply, and reference generation	—	5	—	V
VCC	Bias	Supply shunt regulator (TLE431-Q1)	—	5	—	V
V_{PREC_PWM}	TLC555 out	Amplitude TLC555 clock at ouput	—	5	—	V
V_{TP1}	Voltage at PWM input	Amplitude dimming clock	—	5	—	V
V_{TP2}	Voltage at TP2	Voltage proportional to output current	—	—	5	V
CLOCKS						
f_{PREC_PWM}	Square wave frequency	Frequenc at TLC555-Q1 out, U1	240	—	—	Hz
D_{OUT}	Square wave duty cycle	Duty cycle of f_{PREC_PWM}	5	—	50	%
D_{ACC}	Duty cycle accuracy	Accuracy of D_{OUT}	2%	—	—	
f_{OSCL}	Oscillator frequency	LED driver, TPS92691-Q1	—	390	—	kHz
THERMAL						
T_A	Temperature range	Operating/ambient temperature	–40	—	105	C
PULSE TOLERANCE						
Cold crank	Operational					
Jump start	Operational					
Jump start	Operational					
BASEBOARD						
Number of layers	Two layers, single-side populated					
Form factor	87 mm × 70 mm					

1.3 Block Diagram

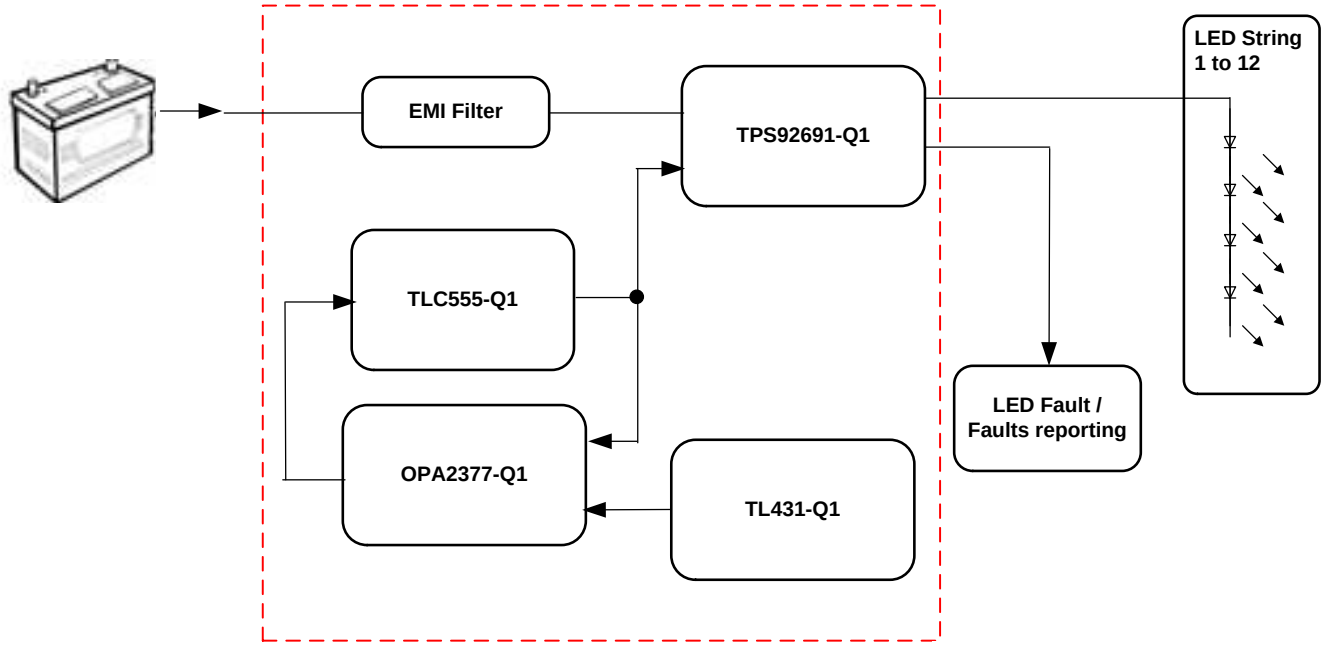

Figure 1. TIDA-01183 Block Diagram

1.4 Highlighted Products

1.4.1 TLC555-Q1

The TLC555 is a monolithic-timing circuit fabricated using the TI LinCMOS™ process (see Figure 2). The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Because of the high input impedance of this device, it uses smaller timing capacitors than those used by the NE555 device. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage. The advantage of the TLC555-Q1 is that it exhibits greatly reduced supply-current spikes during output transitions. Although the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the main reason the TLC555-Q1 is able to have low current spikes is because of its edge rates. This feature minimizes the requirement for the large decoupling capacitors required by the NE555.

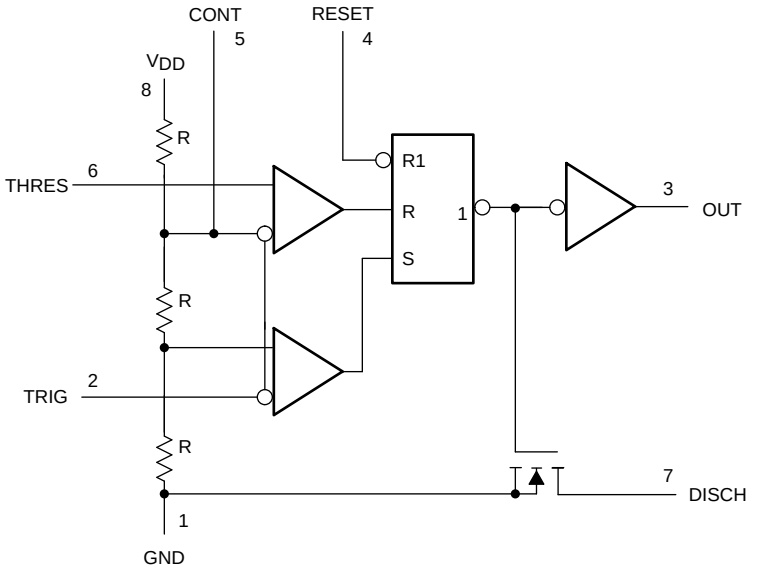

Figure 2. TLC555 Functional Block Diagram

1.4.2 OPA2377-Q1

The OPA2377-Q1 is a wide-bandwidth CMOS amplifier that provides very low noise, low input bias current, and low offset voltage while operating on a low quiescent current of 0.76 mA (typical).

The OPA2377-Q1 operational amplifier (op amp) is optimized for low voltage, single-supply applications. The exceptional combination of AC and DC performance makes the device ideal for a wide range of applications, including small signal conditioning and active filters. In addition, this part has a wide supply range with excellent power supply rejection ratio (PSRR), which makes it appealing for applications that run directly from batteries without regulation.

Figure 3 shows a block diagram of the OPA2377-Q1 op amp.

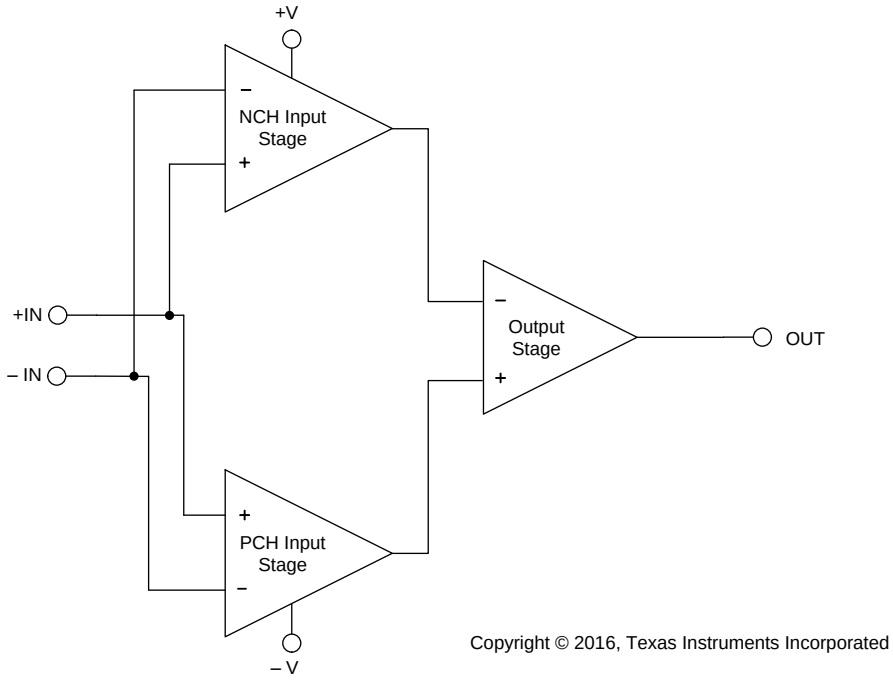

Figure 3. OPA2377 Functional Block Diagram

1.4.3 TL431-Q1

The TL431-Q1 is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive temperature ranges (see Figure 4). The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V, with two external resistors. This device has a typical output impedance of 0.2 Ω. Active output circuitry provides a sharp turnon characteristic, making this device an excellent replacement for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

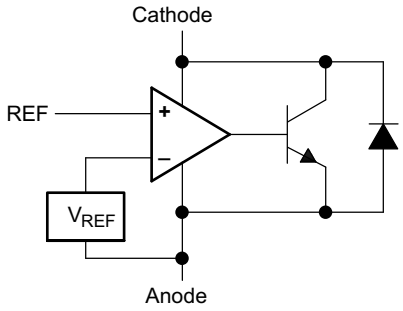

Figure 4. TL431-Q Functional Block Diagram

1.4.4 TPS92691-Q1

The TPS92691-Q1 is a versatile LED controller that can support a range of step-up or step-down driver topologies (see Figure 5). The device implements a fixed-frequency, peak-current-mode control technique with programmable switching frequency, slope compensation, and soft-start timing. The device incorporates a high voltage (65-V) rail-to-rail current sense amplifier that can directly measure LED current using either a high-side or a low-side series sense resistor. The amplifier is designed to achieve low input offset voltage and attain better than ±3% LED current accuracy over a junction temperature range of 25°C to 140°C and output common-mode voltage range of 0 V to 60 V.

LED current can be independently modulated using either analog or PWM dimming techniques. A linear analog dimming response with a 15:1 range is obtainable by varying the voltage from 140 mV to 2.25 V across the high impedance analog adjust (IADJ) input. PWM dimming of LED current can be achieved by modulating the PWM input pin with the desired duty cycle and frequency. Use the DDRV gate driver output to enable series FET dimming functionality to obtain over a 1000:1 contrast ratio.

The TPS92691-Q1 supports continuous LED status check through the current monitor (IMON) output. This feature allows for LED short circuit or open circuit detection and protection. Additional fault protection features include VCC UVLO, output OVP, switch cycle-by-cycle current limit, and thermal protection.

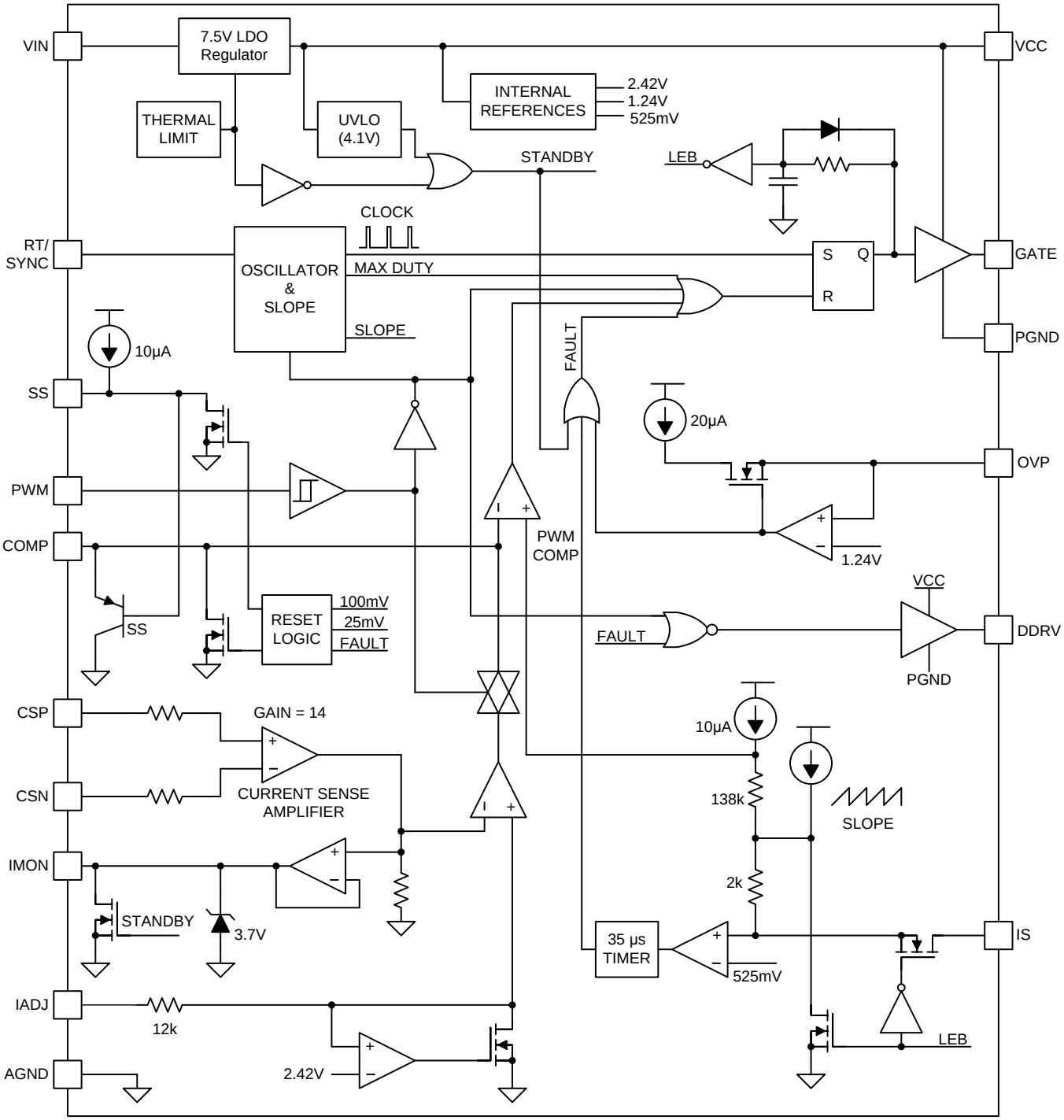

Figure 5. TPS92691-Q1 Functional Block Diagram

2 System Design Theory

2.1 PCB and Form Factor

This design is not intended to fit any particular form factor. The specific and primary objective of the design with regards to the PCB is to make a solution that is compact, while still providing a way to test the performance of the board. Figure 6 shows a 3D rendering of the board.

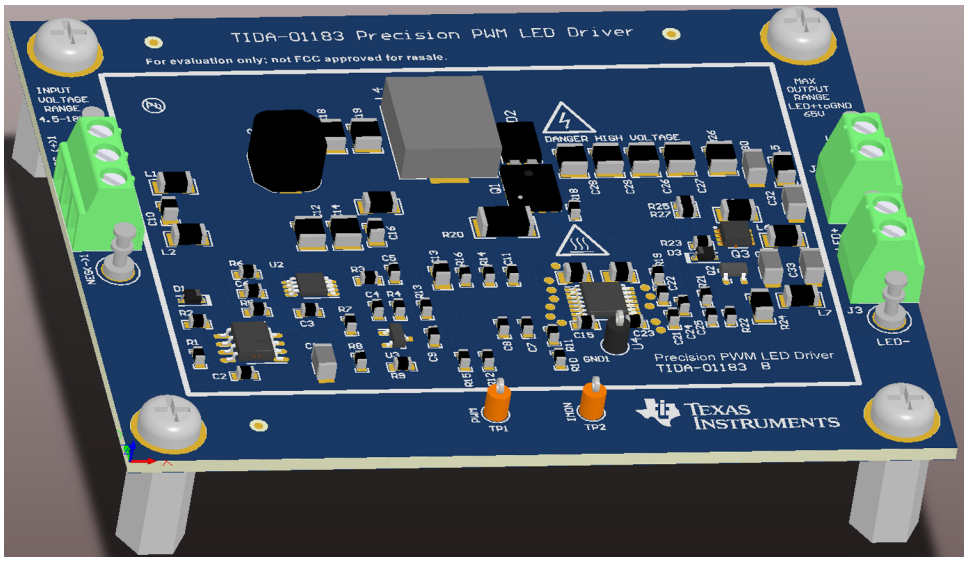

Figure 6. 3D Render of TIDA-01183 Board

In a final-production version of this design, several techniques may be used to reduce the size of the solution:

- Test points, headers, sockets, standoffs, and banana plugs can be removed; these blocks can be removed because they do not service a direct function for the board
- The number, size, and value of capacitors in the system can be optimized
- The application may not require an input-conducted emissions EMI (PI) filter

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2.2 Optimizing Board Performance Based on LED String Voltage and Current

The default board schematic has been configured to operate over a wide range of LED currents (62.5 mA to 1.07 A) and string configurations (1 to 20 LEDs). The driver operation, efficiency, and transient response can be improved by reconfiguring the schematic for a given LED current and LED string forward-voltage drop. The LED current sense resistor (R_{CS} = R26) value can be calculated based on the maximum allowable differential voltage of 172 mV, which is achieved by pulling the IADJ pin to VCC through an external resistor. The slope compensation voltage can be adjusted by changing the switch current sense resistor, R_{IS} = R20, based on the maximum expected LED stack voltage. The proportional integral compensation network can be tuned to achieve high bandwidth and desired phase margin for a specified range of input and output voltages. Refer to the TPS92691-Q1 data sheet [2] for more details.

2.3 Clock Generation (PWM)

Connecting TRIG to THRES, as Figure 7 shows, causes the timer to run as a multivibrator. The capacitor C1 charges through R1 and D1 to the threshold voltage level (approximately 0.67 V_{DD}) and then discharges through R2 only to the value of the trigger voltage level (approximately 0.33 V_{DD}). As Figure 8 shows, the output is high during the charging cycle ($t_{c(H)}$) and low during the discharge cycle ($t_{c(L)}$).

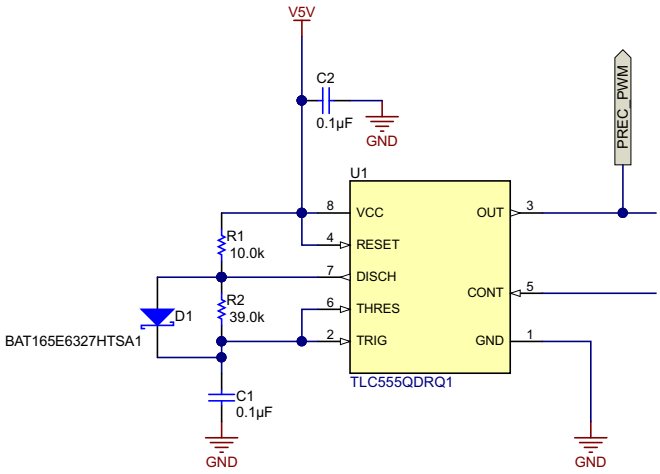

Figure 7. TLC555-Q1 Clock Generation

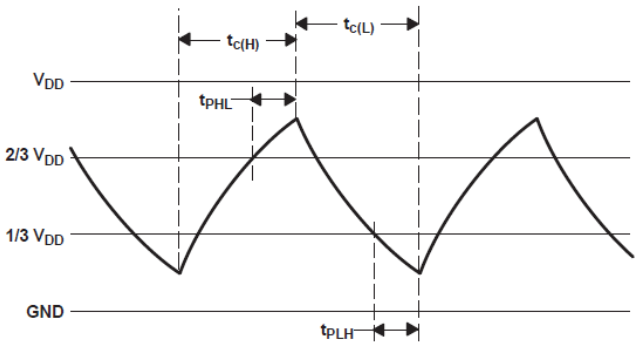

Figure 8. Trigger and Threshold Voltage Waveform

The values of R1, D1, R2, and C1 control the duty cycle, as the following equations show:

$$t_{c(H)} \approx C_T R_1 \ln 2$$

$$t_{c(L)} \approx C_T R_2 \ln 2$$

$$\text{Period}: t_{c(L)} + T_{c(H)} \approx C_T R_2 \ln 2$$

$$\text{Output waveform duty cycle}: \frac{t_{c(H)}}{T_{c(L)} + t_{c(H)}} \quad (1)$$

$t_{c(H)}$ = 100 nF × 10 kΩ × ln 2 = 693 µs

$t_{c(L)}$ = 100 nF × 39 kΩ × ln 2 = 2.7 ms

Period = $t_{c(H)}$ + $t_{c(L)}$ = 3.39 ms

Output waveform duty cycle = 20.4%

The preceding formulas do not allow for any propagation delay times from the TRIG and THRES inputs to DISCH. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the internal ON-state resistance (r_{ON}) during discharge adds to R2 to provide another source of timing error in the calculation when R2 is very low or r_{ON} is very high. These errors can be canceled out by applying a feedback loop.

2.4 Onboard Supply and Setting Duty Cycle

The supply for the TLC555-Q1 device, the OPA2377-Q1 op amp, as well as the reference voltage for setting the duty cycle is derived from the precision shunt regulator (0.5%) TL431-Q1 (see Figure 9). The device is supplied by the VCC (7.5 V) output of the TPS92691 device and regulates this voltage down to a precision 5 V (V5V) set by the resistors R7, R8, and R9. Additionally, the reference voltage for the op amp, which is used to set the duty cycle, is derived from this voltage that resistor divider R8 and R9 generate.

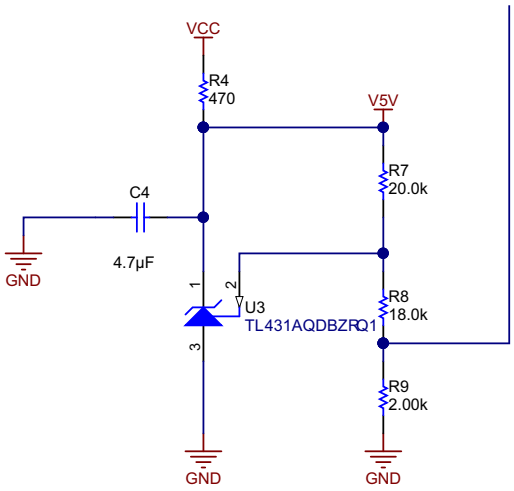

Figure 9. TL431-Q1 Precision Voltage Generation

2.5 Buffering, Averaging, and Filtering

The OPA2377-Q1 dual op amp, low-noise, rail-to-rail input and output, and low offset, makes this device ideal for these type of applications. The output stage of the TLE555-Q1 as Section 1.4.1 describes is hooked up through a 1-K resistor to the PWM input of the TPS92691 device, which dims the LEDs and also connects to a buffer stage and a second-order filter formed by the dual OPA2377 op amp (see Figure 10). The buffer stage is placed to avoid changing impedance from input to output so as not to interfere with the shape or timing of the squarewave generated by the TLC555. The waveform after the buffer stage is then averaged by the next op amp stage, which forms a second-order filter that is compared against a reverence voltage set by the resistor divider from the precision reference. The output of the second-order filter is hooked up to the CONT pin of the TLC555-Q1 closing the loop. The CONT input of the TLC555 allows the upper and lower trigger threshold of the timing duty cycle to be changed by varying the voltage level at this pin, which is performed by the output of the second-order filter.

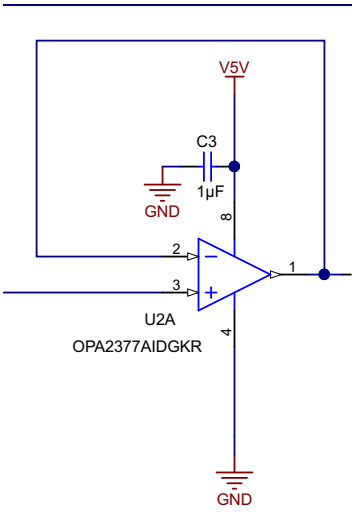

Figure 10. Buffer

Use the following parameters for this design example:

- Gain = 19.2 V/V (inverting gain)
  - Low-pass cutoff frequency = 31.67 Hz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

Figure 11 shows the infinite-gain multiple-feedback circuit for a low-pass network function.

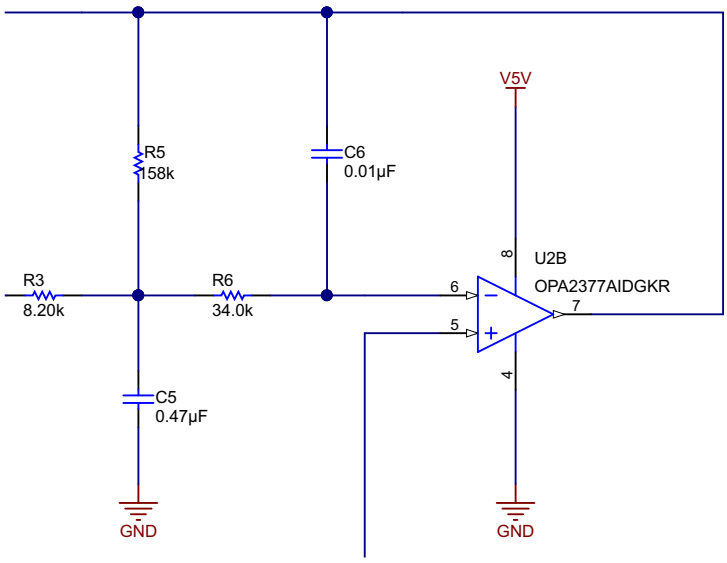

Figure 11. Second-Order Filter and Averaging

Use the following Equation 2 to calculate the voltage transfer function:

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{\frac{-1}{R_1 R_3 C_2 C_5}}{s^2 + \left(\frac{s}{C_2}\right) \times \left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_4}\right) + \frac{1}{R_3 R_4 C_2 C_5}} \quad (2)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by the following Equation 3:

$$\text{Gain} = \frac{R_5}{R_3}$$

$$f_c = \frac{1}{2\pi} \sqrt{\frac{1}{R_6 \times R_5 \times C_5 \times C_6}} \quad (3)$$

Gain = 19.2

*f*c = 31.67 Hz

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer enables designers to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

3 Boost Converter

The TPS92691/-Q1 controller is suitable for implementing step-up or step-down LED driver topologies (see Figure 12). In this design, the boost and the boost-to-battery configuration are used. Use the detailed design procedure of the data sheet in Section 8 to select component values for the TPS92691/-Q1 device. This section addresses the design process for the boost converter. The expressions derived for boost can also be altered to select components for a 1:1 boost-to-battery converter.

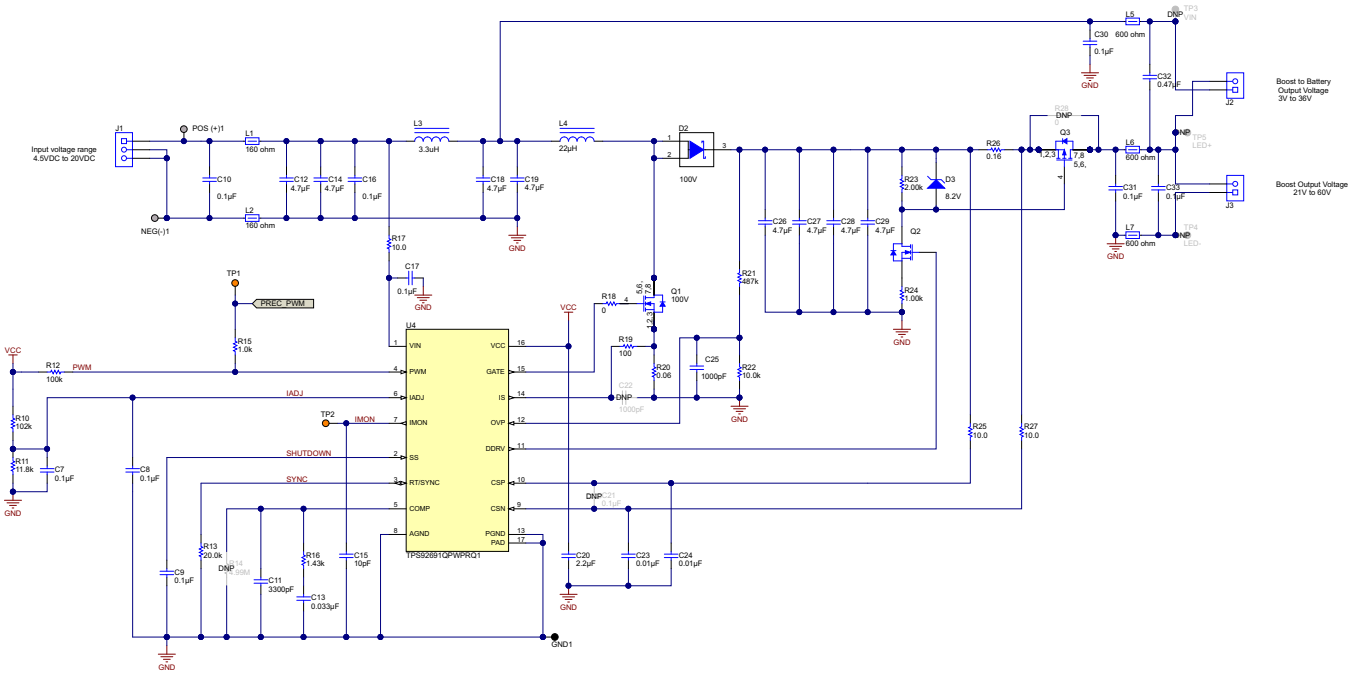

Figure 12. TPS92619-Q1 LED Driver in Boost (J3) and Boost to Battery configuration (J2)

DC-DC converters can couple large amounts of energy (especially at the fundamental switching frequency) back through the battery inputs and into the remainder of the vehicle. This energy is produced because of the switching action of the input-current waveform that is translated into voltage noise by the equivalent series resistance (ESR) of the input capacitors that carry most of this current. A low-pass filter, placed between the input of the module and the DC-DC converters, has been added to attenuate this noise. The low-pass filter also filters incoming noise that enters the system. The low-pass filter can be designed empirically or theoretically (by calculation and simulation). The empirical approach is to design the system without the EMI filter, measure the conducted emissions with a spectrum analyzer, and compare it to the standard that must be passed. Next, calculate the attenuation required to pass at certain frequencies and place the corner frequency of the filter low enough to achieve the desired attenuation.

NOTE: This method requires waiting on hardware to begin the design, gaining access to a testing lab, then modifying the hardware and retesting. Most designers will not have immediate access to a testing chamber and will want to pass the desired standard on the first try or with minor adjustments

The theoretical approach is more complicated. Ensure the assumption is that the boost converter is the problem and that the noise generated by the downstream circuitry is to be filtered by the boost inductor or capacitors.

NOTE: The main sources of noise are fundamental at the switching frequency of the boost (400 kHz) and the harmonics. If the amplitude of the noise at that frequency can be estimated and attenuated appropriately, the harmonics can also be attenuated.

The input voltage is the voltage generated by the ripple current through the ESR of the input capacitors. Because ceramic capacitors are used, this ESR is very low (approximately 3 mΩ). The peak amplitude of the input voltage ripple is approximately 2.7 mV (see Equation 4). The concern is the frequency content at 400 kHz, not the time domain.

$$3\ m\Omega \times 0.9\ A = 2.7\ mV \tag{4}$$

Use the Fourier transform of this asymmetric-triangle waveform to find the coefficients and amplitudes of each component frequency. The coefficient of the fundamental for this type of waveform is 0.8. Multiply the coefficient times the time domain amplitude to find the energy at 400 kHz (see Equation 5).

$$0.8 \times 2.7\ mV = 2.16\ mV \tag{5}$$

Using Equation 6, convert the product of Equation 5 to dBμV to make it easier to analyze based on the CISPR -25 standards.

$$20 \times \log\left(\frac{2.16\ mV}{1\ \mu V}\right) \approx 67\ dB\mu V \tag{6}$$

Compare the 67 dBμV to the CISPR-25 specification and calculate how much to attenuate. The CISPR-25 specification does not define a limit at 400 kHz, but the limit at 530 kHz for Class 5 conducted emissions is 54 dBμV (peak). An attenuation of at least 13 dB is required. Make the goal 40-dB attenuation at the switching frequency. Calculate where to place the corner frequency of the filter when attenuation at 400 kHz is known. The second-order low-pass filter has a rolloff of –40 dB per decade. Place the corner frequency at 40 kHz to attain 40 dB of attenuation at 400 kHz. The corner frequency is related to the values of the filter inductor and capacitor, calculated by using Equation 7:

$$2 \times \pi \times f = \frac{1}{\sqrt{L \times C}} \tag{7}$$

Choose an L of 3.3uH. There is approximately 47 nF, calculating out for C. To keep the ESR low, put two capacitors in parallel and choose 4.7 μF for C12, C14 and C18, C19. Choosing a larger value lowers the corner frequency of the filter, which provides more attenuation at 400 kHz. Also, ceramic capacitors suffer from DC bias effects and operate at a capacitance that is less than their rating. To filter the high-frequency noise content, a 100-nF capacitor is added.

4 Getting Started Hardware (and Software if applicable)

4.1 Hardware

Connect the desired number of LEDs per string at the output screw terminals to get started with the TIDA-01183 board. Figure 13 shows an screen shot of the TIDA-01183 board.

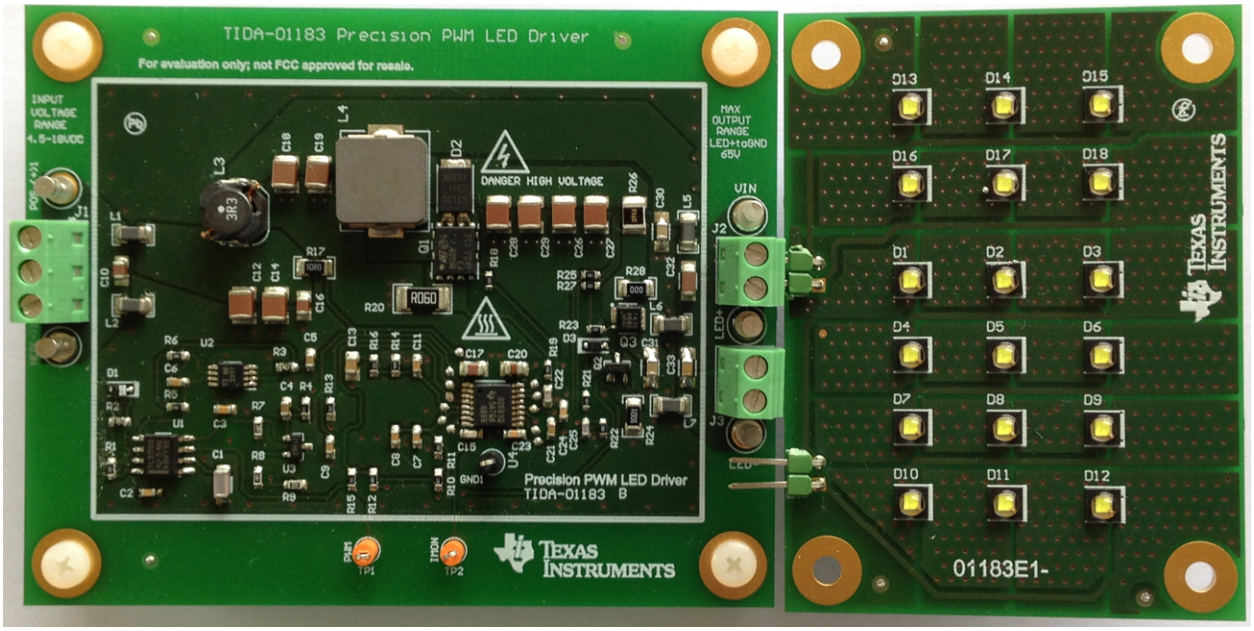

Figure 13. TIDA-01183 With LED Daughter Board

4.2 Configuring for Boost or Boost to Battery (J2, J3)

The TPS92691 can be configured as a boost regulator or a boost-to-battery regulator simply by connecting the LED load to either connector J2 or to connector J3 as described in this section. Do not attempt to use J2 and J3 simultaneously.

4.2.1 J1, VIN, LED+ (Boost-to-Battery)

The screw-down connector, J2, marked LED+ and VIN is for connecting the LED load to the board in the boost-to-battery (buck-boost) configuration. The positive terminal of the LED load connects to LED+ while the negative terminal connects to VIN. The leads to the LED load must be twisted and kept as short as possible to minimize voltage drop, inductance, and electromagnetic interference (EMI) transmission. The boost-to-battery design is for approximately 1 to 12 white LEDs.

4.2.2 J3, LED+, LED– (Boost)

The screw-down connector, J3, marked LED+ and LED– is for connecting the LED load to the board in the boost configuration. The leads to the LED load must be twisted and kept as short as possible to minimize voltage drop, inductance, and EMI transmission. The boost design is for approximately 6 to 20 white LEDs.

4.2.3 J1, POS(+), NEG(–)

The screw-down connector, J1, marked POS(+) and NEG(–) is for connecting the board to the DC input voltage supply. One other POS(+) and NEG(–) test turret is provided on the board that can also be used.

4.2.4 TP2 IMON

The IMON test point connects directly to the IMON pin of the TPS92691-Q1 device. The IMON voltage, corresponding to measured LED current by integrated rail-to-rail current sense amplifier, can be monitored with this test point. The pin can be connected to an external comparator or MCU to detect LED short-circuit, LED+ to VIN, and LED+ to GND fault conditions.

4.2.5 TP1 PWM

The PWM test point connects through a 1-kΩ resistor to the PWM pin of the TPS92691-Q1 device. Leave this point open for normal operation. An oscilloscope can be connected here to visualize the square waveform

4.2.6 Duty Cycle Adjust

Per default the duty cycle of this system has been set by resistors R8 and R9 to the minimum of 5%. If the duty cycle needs to be changed adjust resistors R8 and R9 accordingly. See the preceding Figure 9.

5 Testing and Results

Several tests were conducted to verify the accuracy of the duty cycle.

1. Board continuously running with fixed duty cycle set and duty cycle continuously recorded with oscilloscope and standard deviation calculated (see Figure 14)

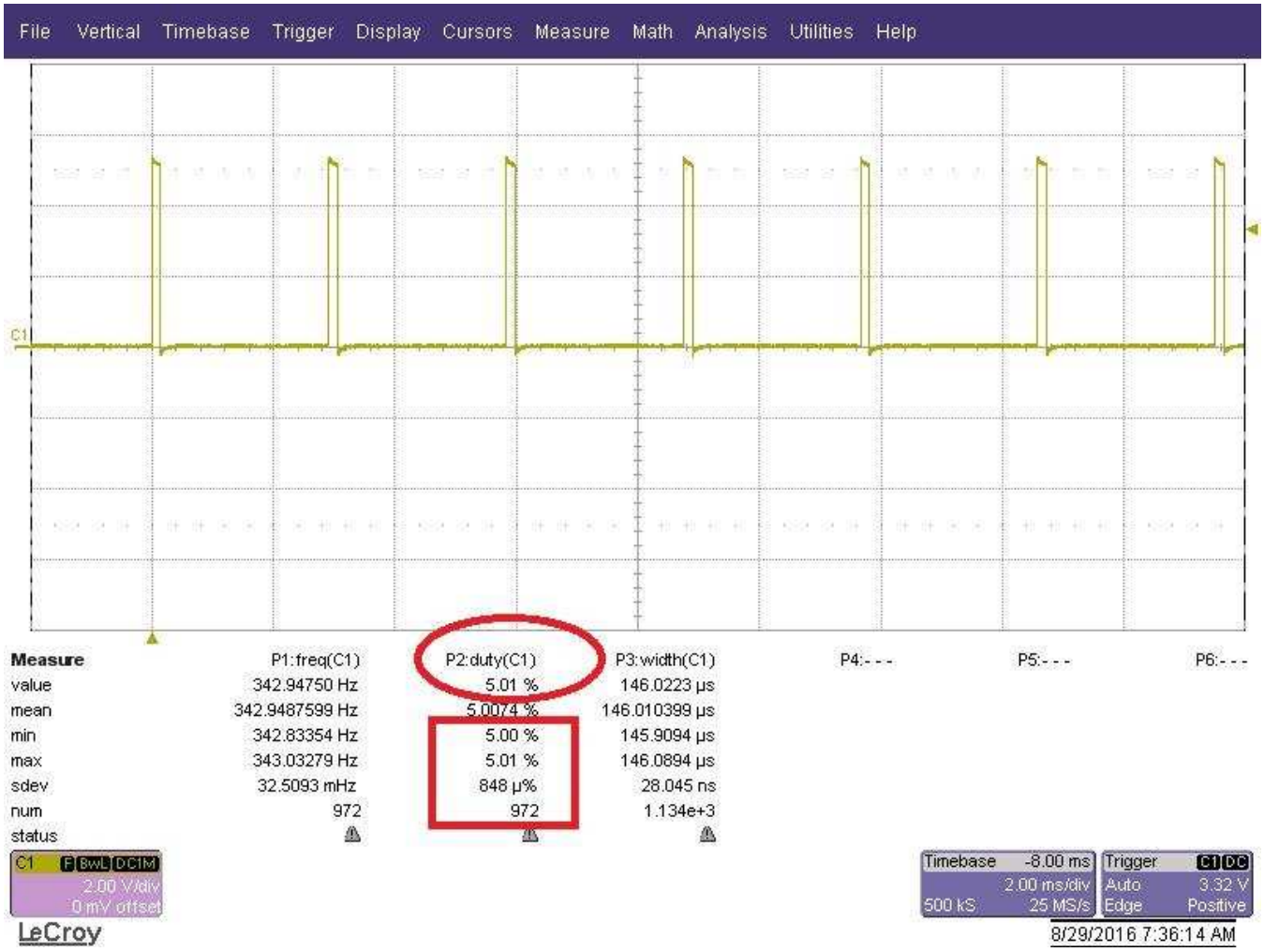

Figure 14. Duty Cycle Accuracy

The result was a very accurate duty cycle with a standard deviation of 848u%.

2. Different clock devices TLC555 from different production batch tested on same board

   The result was a very accurate duty cycle with a standard deviation of less than 0.5%.

3. Temperature test: –40°C to 110C°. Board continuously running with fixed duty cycle set and duty cycle continuously recorded with oscilloscope and standard deviation calculated.

   The result was a very accurate duty cycle with a standard deviation of less than 0.5%.

6 Accuracy Calculation

The influencing factors responsible for creating inaccuracies in the duty cycle and causing a frequency shift can be broken down to the accuracy of the reference voltage. All other inaccuracies are cancelled out and regulated against by the feedback loop formed by the op amp feeding its output voltage back to the CONT input of the TLC555-Q1, which moves up and down the threshold for creating the duty cycle and frequency.

That means with changing the reference voltage at the positive input of the op amp the frequency can change, but the duty cycle adjusts to the point it is set to and remains constant.

So, to determine the accuracy of the duty cycle, the designer must factor in the tolerance of the shunt regulator U3, the resistor divider R7, R8, and R9 and the offset voltage of the op amp (U2B).

Definitions

The following symbols and notation schemes are used in this calculation:

- R8 and R9 are the nominal values of the resistor divider, whereas the actual value is the nominal value , plus an absolute error. The absolute errors are notated as ΔR1 and ΔR2 and are expressed in Ohms (Ω).
- The relative errors in R1 and R2 are represented by t1 and t2. These values are the ratio of the absolute error in each resistor to its nominal value and are bounded by the tolerance of each resistors.
- In this calculation, relative errors and resistor tolerances are both expressed as decimal ratios rather than percentages: for example, ±0.01 rather than ±1%.
- The actual value of the power supply output voltage is V_O. Like the aforementioned resistances, it is made up of a nominal value V_O, and an absolute error, ΔV_O.
- Likewise, the value of the power supply reference voltage is $V_{REF} + \Delta V_{REF}$.

Calculation:

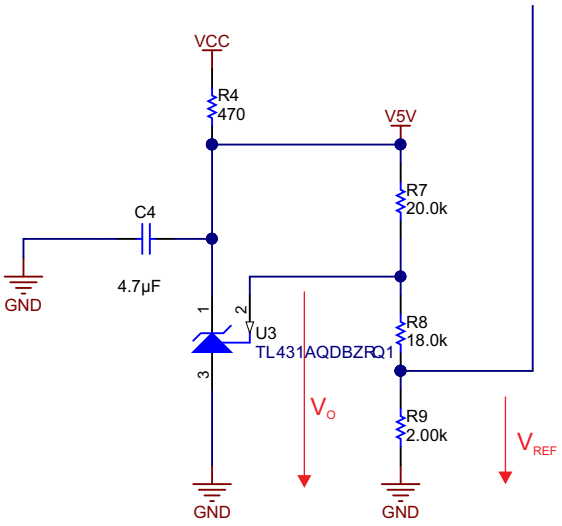

Figure 15. Duty Cycle Accuracy Calculation

$$\frac{V_O}{V_{REF}} = \frac{R8 + R9}{R9} \tag{8}$$

Solving for V_{REF} in Equation 9:

$$V_{REF} = \frac{R9}{R8 + R9} \times V_O \tag{9}$$

The reference voltage and both resistances can be expressed in terms of their nominal values and absolute errors (see Equation 10):

$$V_{REF} + \Delta V_{REF} = \frac{R9}{R8 + R9} \times (V_O + \Delta V_O) \tag{10}$$

V_O can be expressed as the following Equation 11:

$$V_O = \frac{R8 + R9}{R9} \times V_{REF} \tag{11}$$

ΔV_O can be expressed as the following Equation 12:

$$\Delta V_O = V_O \times \tau \tag{12}$$

τ = the decimal tolerance of 0.01, which is 1%. Solve the preceding Equation 12 for ΔV_{REF} and substitute in the following Equation 13:

$$\Delta V_{REF} = V_{REF} + \frac{V_O \times \tau \times R9}{R8 + R9} - V_{REF} \tag{13}$$

Substitute the preceding Equation 13 to simply Equation 14:

$$\Delta V_{REF} = \left(\frac{V_O \times \tau \times R9}{R8 + R9} \right) \tag{14}$$

The preceding Equation 14 calculates the absolute output voltage error at the center point of the resistor divider R8 and R9. To also account for the overall failure of the system, tsystem, the offset voltage VOS failure of the system must also be taken into account and must be added to the ΔV_{REF} (see Equation 15).

$$\Delta V_{REF} + VOS = \left(\left(\frac{V_O \times \tau \times R9}{R8 + R9} \right) \right) + VOS \tag{15}$$

In this application, thinking of the output voltage error in relative terms rather than absolute terms is helpful. The relative output voltage error can be found by dividing both sides of this equation by the nominal output voltage desired V_{REF}, which provides the overall relative failure of the system (see Equation 16):

$$\tau system = \frac{\Delta V_{REF} + VOS}{V_{REF}} = \frac{\left(\left(\frac{V_O \times \tau \times R9}{R8 + R9} \right) \right) + VOS}{V_{REF}} \tag{16}$$

For example, the resistor values in this design result in a nominal V_{REF} voltage of 0.2495 V. The offset voltage VOS of the op amp is 0.25 mV and the nominal V_O voltage of 2.495 V. So the overall system is very accurate if it features a tolerance of less than 1% (see Equation 17).

$$\tau system = \frac{\left(\left(\frac{2.49\ V \times 0.005 \times 2k}{18k + 2k} \right) \right) + 0.25\ mW}{0.2495} = 0.000125\% \tag{17}$$

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-01183.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01183.

7.3 PCB Layout Recommendations

7.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01183.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-01183.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01183

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01183.

8 Related Documentation

1. Texas Instruments, *TLC555-Q1 LINCMOS™ TIMER*, Data Sheet (SLFS078)
2. Texas Instruments, *TPS92691/-Q1 Multi-Topology LED Driver With Rail-to-Rail Current Sense Amplifier*, Data Sheet (SLVSD68)
3. Texas Instruments, *OPAx377-Q1 Low-Noise, Low Quiescent Current, Precision Automotive Grade Operational Amplifier*, Data Sheet (SBOS797)
4. Texas Instruments, *TL431-Q1 ADJUSTABLE PRECISION SHUNT REGULATOR*, Data Sheet (SGLS302)
5. Texas Instruments, *TPS92691 Boost and Boost-to-Battery LED Driver Evaluation Board*, User's Guide (SLVUAO7)

8.1 Trademarks

9 About the Author

ROBERT REGENSBURGER is a Systems Architect at Texas Instruments where he is responsible for developing reference design solutions for the Automotive Body and Lighting segment. Robert brings his extensive experience of more than 15 years of automotive analog applications to this role. Robert earned his Engineering Diploma in Electrical Engineering from the Advanced Technical High School in Regensburg, Germany.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to A Revision	Page
• Changed entry and link for "TPS92630-Q1" to "TPS92691-Q1" in *Resources* section	1
• Changed caption for *Figure 6* from "3D Render of TIDA-00678 Board" to "3D Render of TIDA-01183 Board"	8

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