

TI Designs

Isolated Self-Powered AC Solid-State Relay With MOSFETs



Description

The TIDA-01065 reference design is a relay replacement that enables efficient power management for a low-power alternative to standard electromechanical relays. The galvanic isolation is implemented capacitively, creating a cost-efficient, reduced footprint solution for multiple relay replacement in thermostats and other similar equipment.

Resources

TIDA-01065	Design Folder
ATL431	Product Folder
LMV339	Product Folder
SN74LVC1G74	Product Folder
SN74LVC1G08	Product Folder
CSD18541F5	Product Folder
TIDA-00377	Tools Folder
TIDA-00751	Tools Folder
TIDA-01064	Tools Folder

Features

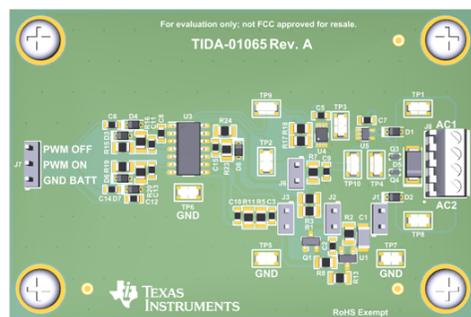
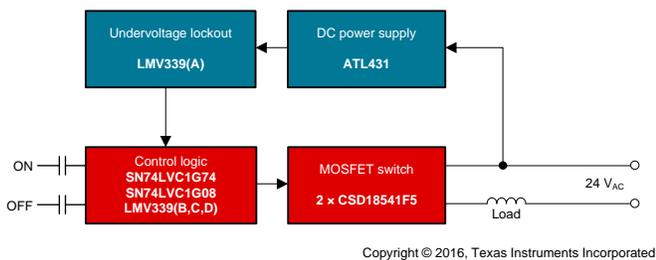
- No Clicking Sound
- MOSFET Based Design for Fast ON and OFF
- Galvanic Isolation
- Self-Powered
- Zero Power From Thermostat Battery
- Inherent Snubber Circuit Reducing Voltage Spike Created by Inductive Loads
- Undervoltage Protection
- Cost-Efficient BOM
- Reduced Footprint

Applications

- Thermostats
- HVAC Systems
- Building Automation



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1 System Overview

1.1 System Description

A solid-state relay (SSR) is an electronic switching device that switches on or off when a small external voltage is applied across its control terminals. SSRs consist of an input logic to respond to an appropriate input (control signal), a solid-state electronic switching device to switch power to the load circuitry, and a coupling mechanism to enable the control signal to activate this switch without mechanical parts. The SSR may be designed to control either an AC or DC voltage or current load. It serves the same function as an electromechanical relay, but has no moving parts.

SSRs use power semiconductor devices such as thyristors or transistors to switch currents up to 100 A. SSRs have fast switching speeds compared with electromechanical relays and have no physical contacts to wear out. To apply an SSR, the user must consider their lower ability to withstand momentary overload compared with electromechanical contacts and their initial higher "on" state resistance. Unlike an electromechanical relay, an SSR provides only limited switching arrangements (single-pole, single-throw switching).

This SSR is an isolated, self-powered reference design for mechanical relay replacement in thermostat applications, where the thermostat is battery powered and includes more than one relay. The SSR is self-powered through the AC line of the HVAC system and provides undervoltage lockout (UVLO). See [Figure 1](#) for the block diagram.

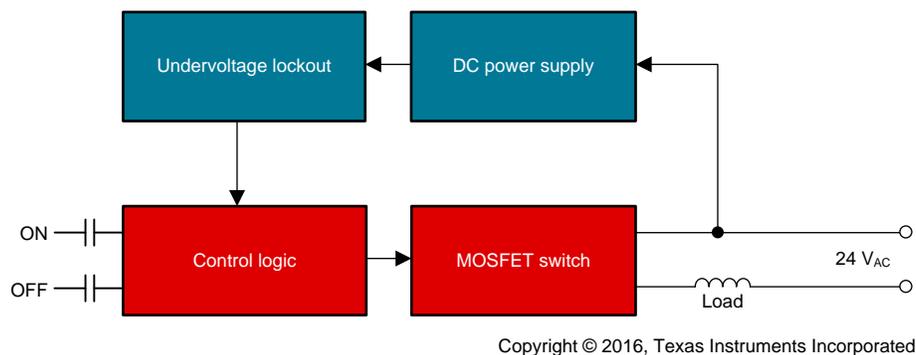


Figure 1. TIDA-01065 SSR With MOSFETs Block Diagram

1.1.1 Choosing Between SSR Reference Designs

The TI Designs portfolio has four available SSR reference designs: TIDA-00377, TIDA-00751, TIDA-01064, and TIDA-01065. They differ in terms of power consumption, galvanic isolation, voltage and current protection, and cost. See [Table 1](#) for a feature comparison between the three designs.

Table 1. Comparison of SSR Reference Designs

PARAMETER	TIDA-00377	TIDA-00751	TIDA-01064	TIDA-01065
Self-powered	√		√	√
Isolation		√		√
Snubber circuit	√	√	√	√
UVLO	√		√	√
OCP	√			
Low cost			√	

1.1.1.1 Power Consumption

The TIDA-00377, TIDA-01064, and TIDA-01065 do not consume any power from the thermostat battery. They are self-powered and consume < 0.4 mA from the HVAC system. Alternatively, the TIDA-00751 consumes power from the thermostat battery during both on- and off-states. The SSR consumes 1.2 mA from the battery during on-state and < 0.2 mA during off-state.

1.1.1.2 Galvanic Isolation

The TIDA-00751 and TIDA-01065 include galvanic isolation, whereas the TIDA-00377 and TIDA-01064 do not. The TIDA-00377 and TIDA-01064 are designed for single relay replacement in low-cost thermostats. Considering that this TI Design is replacing a single relay, isolation is not needed. If galvanic isolation is necessary, use the TIDA-00751 or TIDA-01065. The isolation for the TIDA-00751 and TIDA-01065 are performed using magnetic coupling and capacitive coupling, respectively.

1.1.1.3 Voltage and Current Protection

The TIDA-01064 and TIDA-01065 include UVLO, TIDA-00377 includes both UVLO and overcurrent protection (OCP) circuits, and TIDA-00751 includes neither. UVLO protects the low AC power supply, which also translates to the DC power supply of the SSR. This will enable the self-powering feature. OCP protects the MOSFET switch from overcurrent and to detect short circuits.

1.1.2 N-Channel Power MOSFET

In residential as well as commercial building automation applications, 24 V_{AC} is used as the standard power supply voltage. When an isolated SSR is used in thermostat applications as a replacement for the mechanical relay, the maximum operating voltage of the power switch is peak voltage of one transformer. Taking into account the input voltage variations, 20 to 30 V_{AC}, the peak DC voltage rises up to 43 V. For that reason, this design uses power MOSFETs with a breakdown voltage of 60 V.

1.1.3 Input Logic Control

In thermostat applications, power consumption is one of the main concerns. To ensure a long battery life, the control logic, in most cases a dedicated microcontroller, provides a control signal for a short period of time before it goes in a low-power or sleep mode. Turnon and turnoff signals are two different signals that are active for short periods of the time. For that reason, the input control logic uses the Texas Instruments D-type flip-flop, SN74LVC1G74 with a 5-V supply voltage. This circuit will set the output signal high on a short, low ON pulse and reset the output signal low when a short, low OFF signal is applied.

1.1.4 Galvanic Isolation

In thermostats that include more than one relay, it is important that each relay be galvanically isolated. These types of systems can include two separate transformers with two separate grounds. Connection of these grounds could cause interference and potentially damage the thermostat and the SSR. A cost-effective and space conscious way to perform isolation is with capacitors. Capacitors block common-mode (DC) voltage and allow the passing of alternating (AC) signals. An AC signal from the primary side of the capacitor (thermostat) can be used as a logic control signal on the secondary side of the capacitor. The secondary control signal is created by converting the AC signal to a DC signal by means of diodes and an RC network. Due to the need for a low pulse at the inputs of the D-type flip-flop, two of the comparators from the LMV339 are used to invert and level shift the signal. AC signals at high frequencies allow the use of small capacitors resulting in reduced power loss. For this reason, 0.015- μ F capacitors were chosen. The voltage rating for the capacitors was chosen to be 100 V, which is above the maximum peak load voltage of 43 V and lowest in cost.

1.1.5 Gate Driver

Fast turnon and turnoff time of the power MOSFETs are necessary for the self-powering function of this SSR. The time is controlled by the current flow during the gate-to-source capacitance charge and discharge of the MOSFETs. The positive AND gate SN74LVC1G08 with a 5-V supply rail is able to provide the necessary charge and discharge current for fast turnon and turnoff. It also provides 5 V_{GS} to keep the on-state resistance low. Also, it will fully discharge the gate-to-source capacitance to ensure complete turnoff of the MOSFETs. The two inputs of the AND gate incorporate the control from the D-type flip-flop and the UVLO.

1.1.6 Power Management

Power consumption is another main concern in thermostat applications because the circuitry, which makes up the thermostat control consumes its power from an onboard battery. To avoid additional power consumption and extend the lifetime of the battery, this SSR reference design is self-powered through the 24-V_{AC} power line. By using the body diodes of the power MOSFETs and two additional diodes, the 24 V_{AC} is rectified to 33 V_{DC}, which is further stepped down to provide power to the remaining of the SSR circuitry. The voltage regulation is performed by one low-power shunt regulators, the ATL431, with quiescent current of only 25 μA.

1.1.7 Undervoltage Lockout

For proper voltage regulation of the control logic power supply, the input DC voltage must maintain a certain minimum threshold level. If the AC voltage or rectified AC voltage of the load, V_{DC}, drops below the desired rail voltages, the shunt regulator will no longer be able to regulate, disabling the operability of the SSR. Due to the nature of the DC power supply during the ON time of the MOSFETs, the DC supply capacitor will have a tendency to fully discharge. To prevent this, a reference voltage is set on the UVLO to shortly turn off the MOSFETs when the minimum voltage is met and allows the DC supply capacitor to recharge without affecting the load. This will keep V_{DC} at a voltage where the shunt regulator can regulate properly. To perform this function, one of the comparators from the LMV339 is used.

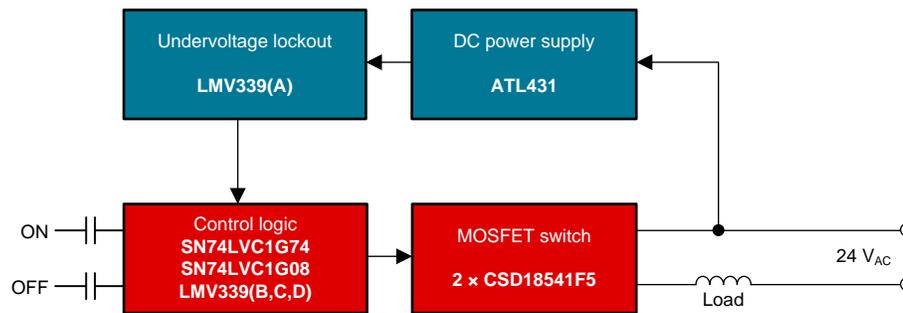
1.2 Key System Specifications

Table 2. Key System Specifications

SPECIFICATION	VALUE	DETAILS
Logic input level	3.3 V	See Section 1.1.3
AC voltage input range	20 to 30 V	See Section 1.1.1
Maximum current	2 A ⁽¹⁾	—
Turnon and turnoff time	< 2 μs	See Section 4.2
On-state current consumption (typ)	165 μA	See Section 4.2
Off-state current consumption (typ)	240 μA	See Section 4.2
Operating temperature	0°C to 60°C	—
Working environment	Indoor building automation	—

⁽¹⁾ Typical R_{θJA} = 245°C/W

1.3 Block Diagram



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Figure 2. TIDA-01065 SSR With MOSFET Block Diagram With Component List

1.4 Highlighted Products

The SSR reference design features the following devices:

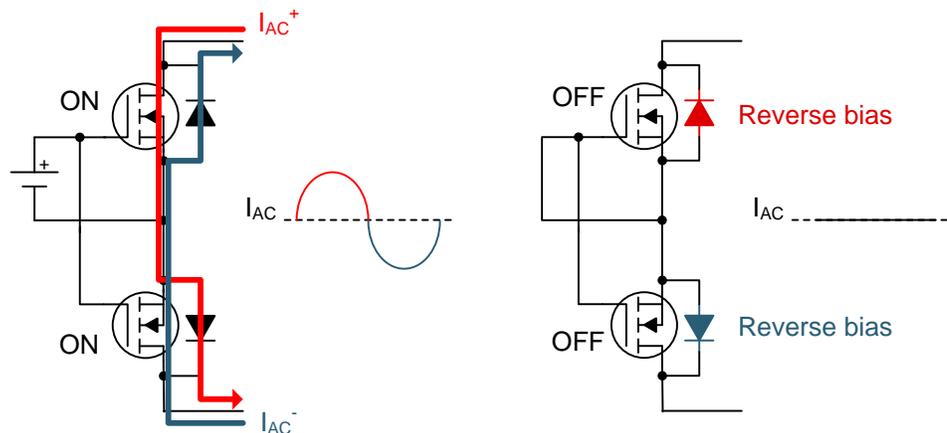
- CSD18541F5: 60-V N-Channel FemtoFET Power MOSFET
- SN74LVC1G74: Single Positive-Edge-Triggered D-Type Flip-Flop
- SN74LVC1G08: Single 2-Input Positive-AND Gate
- ATL431: 2.5-V Low I_q Adjustable Precision Shunt Regulator
- LMV339: Quad General Purpose Low-Voltage Comparators

2 System Design Theory

2.1 Basic SSR Theory

An alternative to the electromechanical switch is an SSR with a MOSFET. SSRs are integrated electrical circuits that act as a mechanical switch. The relays can be switched much faster and are not prone to wear because of the absence of moving parts. Another advantage is that less current and voltage is needed for SSRs to control high-voltage AC loads.

This design uses a two N-channel MOSFET topology serving two main functions. The first function is to perform the switching. By using two MOSFETs, both positive and negative current are allowed to flow during the ON time, as shown in Figure 3a. During the OFF time, the body diodes block the current flow because the top and bottom body diode become reverse bias, shown in Figure 3b.



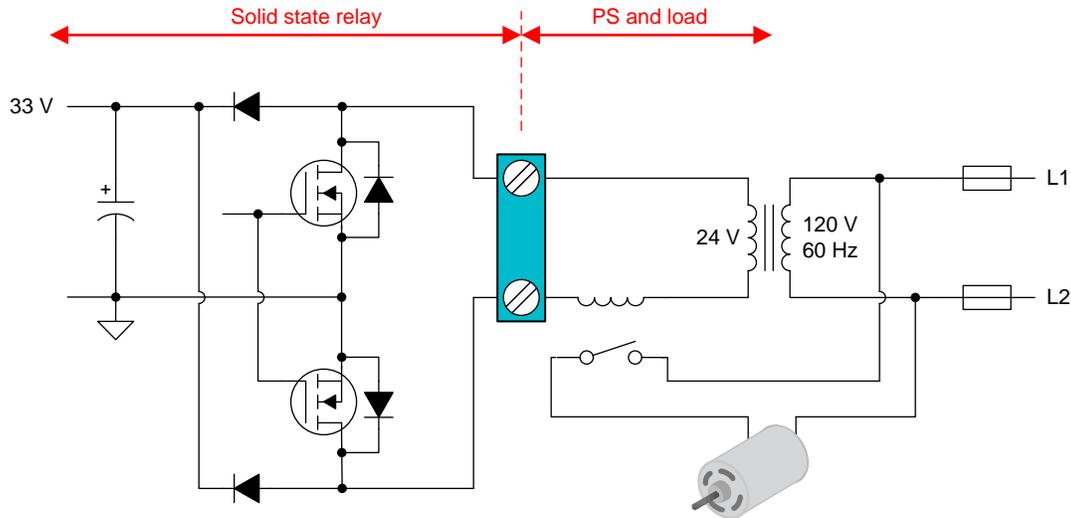
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Figure 3. Functionality of MOSFETs for (a) ON and (b) OFF Times

The second function of the two N-channel MOSFET topology is to self-power the system by assisting in the AC voltage rectification. See Section 2.2 for more details.

2.2 Basic Power Management Theory

The two MOSFET body diodes of the switch and two external diodes create a full-wave rectification circuit that converts the AC power supply at the terminals to a DC voltage that can then be stepped down to desired levels. The control logic and gate driver are powered by the resulting DC voltage and therefore does not consume any power from the thermostat battery.



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Figure 4. Power Supply of SSR in HVAC System

2.2.1 Full-Wave Rectification

When the SSR is not active, the 24- V_{AC} voltage from the HVAC system, across HV1 and HV2, is rectified using external diodes in addition to the two body diodes of the MOSFETs. When the MOSFETs are off, the resulting full-wave rectified waveform has a peak DC voltage of 34 V, calculated by Equation 1.

$$V_{P_DC} = \sqrt{2} \times V_{AC} - 2 \times V_F \quad (1)$$

With the addition of the capacitor, the rectified AC waveform is smoothed out providing a nominal average DC voltage. The ripple of the DC voltage is determined by the value of the capacitor and the current flowing through it over a period of time, as described in Equation 2.

$$\Delta V_{DC} = \frac{i \times \Delta t}{C_{DC}} \quad (2)$$

The resulting waveforms are shown in Figure 5.

2.2.2 DC Power Supplies

The single DC rail voltage used in this reference design 5 V. The 5-V supply rail is chosen based on the gate-to-source voltage on the MOSFETs to provide a low on-state resistance (see Figure 6).

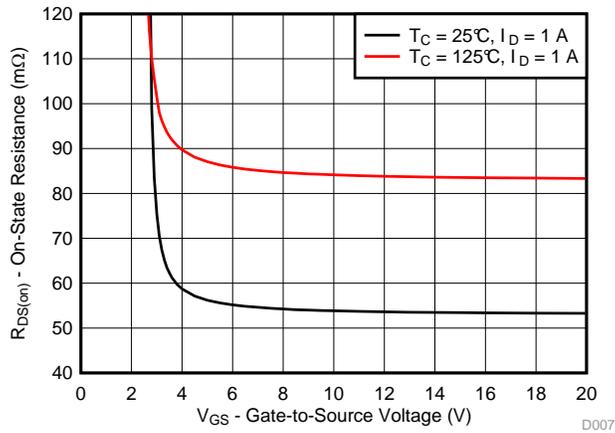
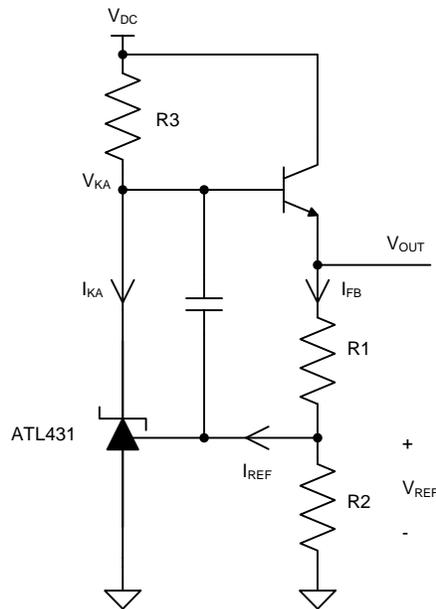


Figure 6. On-State Resistance as Function of Gate-to-Source Voltage of CSD18541F5

2.2.2.1 5-V Power Supply

The 5-V supply uses the low I_Q adjustable precision shunt regulator ATL431. Along with the regulator are three resistors with the DC supply voltage provided by the rectified AC input voltage. One of the resistors, R3, provides the cathode current, I_{KA} , and the other two, R1 and R2, create a resistive divider to set the output voltage, V_{OUT} . The NPN transistor provides current to the remaining blocks of the SSR, reducing the total power consumption of R3.



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Figure 7. Schematic of 5-V Supply

Table 3. ATL431 Electrical Characteristics Over Recommended Operating Conditions 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}, I_{KA} = 1 \text{ mA}$	2475	2500	2525	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range	$V_{KA} = V_{REF}, I_{KA} = 1 \text{ mA},$	ATL43xAI; $T_A = -40^\circ\text{C}$ to 85°C	5	15	mV
			ATL43xAQ; $T_A = -40^\circ\text{C}$ to 125°C	6	34	
$\Delta V_{REF} / \Delta V_{KA}$	Ratio of change in reference voltage to the change in cathode voltage	$I_{KA} = 1 \text{ mA}$	$\Delta V_{KA} = 10 \text{ V} - V_{REF}$	-0.4	-2.7	mV/V
			$\Delta V_{KA} = 36 \text{ V} - 10 \text{ V}$	-0.1	-2	
I_{REF}	Reference input current	$I_{KA} = 1 \text{ mA}, R1 = 10 \text{ k}\Omega, R2 = \infty$	30	150		nA
$I_{I(dev)}$	Deviation of reference input current over full temperature range	$I_{KA} = 1 \text{ mA}, R1 = 10 \text{ k}\Omega, R2 = \infty$	20	50		nA
I_{MIN}	Minimum cathode current for regulation	$V_{KA} = V_{REF}$	20	35		μA
I_{OFF}	Off-state cathode current	$V_{KA} = 36 \text{ V}, V_{REF} = 0$	0.05	0.2		μA
$ Z_{KA} $	Dynamic impedance	$V_{KA} = V_{REF}, f \leq 1 \text{ kHz}, I_{KA} = 1 \text{ to } 100 \text{ mA}$	0.05	0.3		Ω

Table 3 specifies when $V_{KA} = V_{REF}$ and I_{KA} is 1 mA the nominal V_{REF} , (labeled as V_{NOM}) is 2.5 V. The reference voltage varies with cathode voltage at two different rates: -0.4 mV/V from V_{REF} to 10 V, and -0.1 mV/V above 10 V. The nominal reference pin current is 30 nA.

The Z_{KA} parameter offsets V_{REF} by $(I_{KA} - I_{NOM}) \times Z_{KA}$. In addition, the $\Delta V_{REF} / \Delta V_{KA}$ parameter offsets V_{REF} by either $-0.4 \text{ mV} \times (V_{KA} - 2.5 \text{ V})$, if $V_{KA} \leq 10 \text{ V}$, or $-10.5 \text{ mV} - 0.1 \text{ mV/V} \times (V_{KA} - 10 \text{ V})$ if $V_{KA} > 10 \text{ V}$. The -10.5 mV constant is the V_{REF} offset as V_{KA} changes from V_{NOM} to 10 V, $(10 \text{ V} - 2.5 \text{ V}) \times -0.4 \text{ mV/V}$.

For the 5-V supply, the parameters for $V_{KA} < 10 \text{ V}$ are used for Equation 3 because $V_{KA} = 5.6 \text{ V}$ due to the voltage drop across the NPN transistor.

$$V_{REF} = V_{NOM} + (I_{KA} - I_{NOM}) \times Z_{KA} + (V_{KA} - V_{NOM}) \times \Delta V_{REF} / \Delta V_{KA} \quad (3)$$

Now that V_{REF} is solved, R1 and R2 can be determined.

$$R1 = \frac{(V_{KA} - V_{REF})}{I_{FB}} \quad (4)$$

$$R2 = \frac{V_{REF}}{(I_{FB} - I_{REF})} \quad (5)$$

NOTE: R2 current is smaller than R1 current.

The design goal is to set the cathode of the ATL431 to 5.6 V by providing a minimum cathode current of 20 μA , and a feedback current and resistor bridge that will keep V_{KA} within a narrow supply range of $\pm 3\%$ to $\pm 3\%$. The following parameters are calculated using the formula derived in the general example for $V_{KA} < 10 \text{ V}$.

$$V_{REF} = 2.500 \text{ V} + (20 \mu\text{A} - 1 \text{ mA}) \times 0.05 \Omega + (5.6 \text{ V} - 2.5 \text{ V}) \times -0.4 \text{ mV/V}$$

$$V_{REF} = 2.4987 \text{ V}$$

$$R1 = \frac{(5 \text{ V} - 2.4987 \text{ V})}{2 \mu\text{A}}$$

$$R1 = 1.251 \text{ M}\Omega$$

$$R2 = \frac{2.4987 \text{ V}}{(2 \mu\text{A} - 30 \text{ nA})}$$

$$R2 = 1.268 \text{ M}\Omega$$

The closest standard 1% resistor value for R1 is 1.24 M Ω and for R2 is 1.27 M Ω .

To calculate R3, it is necessary to know the base current of the NPN transistor. Use the maximum required emitter current of 300 μ A to sufficiently supply the 5-V load current.

$$I_B = \frac{I_C}{h_{FE}} \quad (6)$$

$$I_B = \frac{300 \mu\text{A}}{400}$$

$$I_B = 750 \text{ nA}$$

Use the maximum required base current, the minimum UVLO voltage of 13 V, the maximum cathode voltage, and the maximum value for the minimum cathode current of 35 μ A to calculate the resistance R3.

$$R3 = \frac{(V_{DC} - V_{KA})}{(I_{KA} + I_B)} \quad (7)$$

$$R3 = \frac{(13 \text{ V} - 5.7 \text{ V})}{(35 \mu\text{A} + 750 \text{ nA})}$$

$$R3 = 204.196 \text{ k}\Omega$$

The closest standard 1% resistor value for R3 is 205 k Ω .

For stability reasons, a ceramic capacitor is placed in the feedback loop of the regulator, between the cathode and reference nodes. The capacitor introduces a zero to the system, and when properly placed will increase the phase margin of the regulator to avoid oscillation and decrease ringing on the output.

2.3 MOSFET Selection

Thermostats consisting of multiple relays control heating and cooling systems that can be connected up to two separate 24- V_{AC} connections, one transformer for the heating system and one for the cooling system. This reference design is for thermostats and HVAC systems where the red (RH and RC) wires of the thermostat are not connected. This means that the two heating and cooling system transformers are not connected and each SSR will connect to a single transformer.

Power relays with a standard 24- V_{AC} excitation and contact rating of 40 A have a coil resistance of 660 Ω . The 120- to 24- V_{AC} transformer output voltage can range from 20 to 30 V_{AC} . Therefore, each MOSFET must be able to handle a drain-to-source voltage and current of 43 V_{DC} and 0.12 A, respectively. The CSD18541F5 was chosen for its 60-V drain-to-source voltage package size and cost.

When SSR is used to turn on and off inductive loads, take care to limit overvoltage spikes during the turnoff process. The DC supply capacitor and external rectification diodes create a snubber circuit to absorb the energy from inductive load during turnoff. When the switch is turned off, the current from the inductive load is interrupted causing the voltage to spike. For additional precaution, a transient voltage suppression (TVS) diode is added across the MOSFETs. For the DC application unidirectional TVS is sufficient, where for an AC application a bidirectional TVS is required.

2.4 Undervoltage Lockout Design Theory

When the relay is not active, the DC supply capacitor charges from the 24-V AC power supply. When the relay is active, the voltage across the MOSFETs reduces down to zero, causing the DC supply capacitor to start to discharge, as shown in Figure 8 and Figure 9. If the DC source voltage becomes too low, the ATL431 shunt regulator will not regulate and the SSR will no longer be able to function. An UVLO is included in this reference design to momentarily turn off the MOSFETs and allow the DC supply capacitor to recharge.

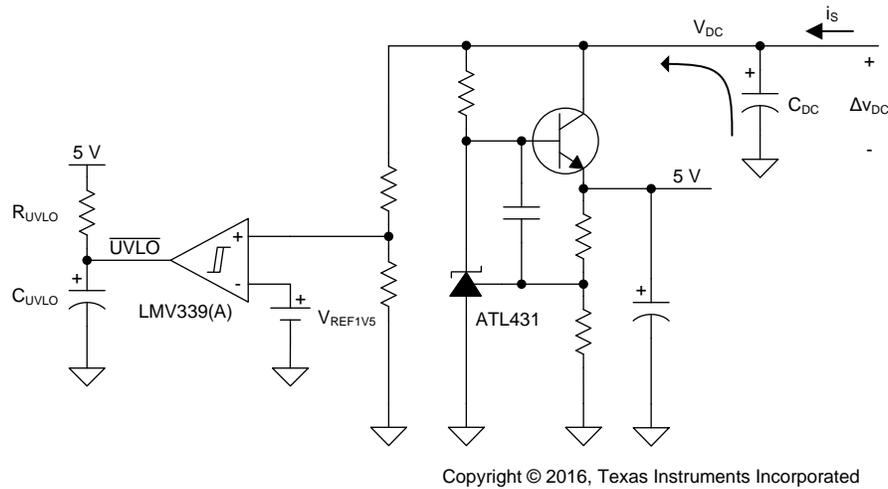


Figure 8. DC Power Supply and UVLO Circuit

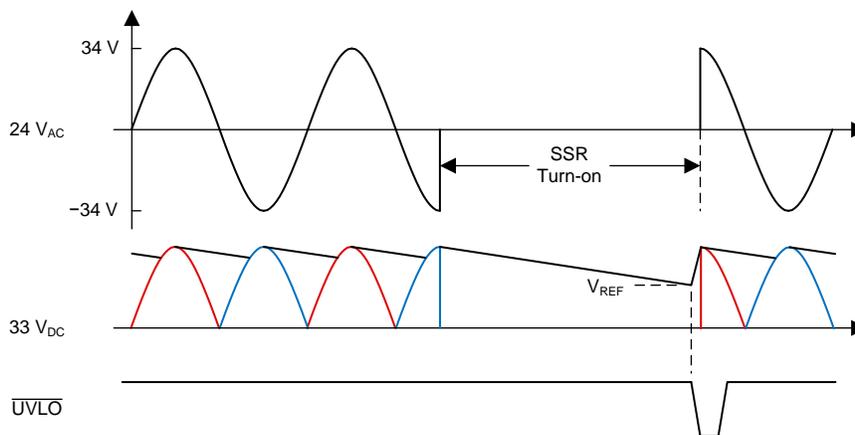


Figure 9. Resulting Waveforms for DC Supply and UVLO When SSR Cycles are ON and OFF

A minimum voltage of 13 V is chosen to maintain the DC source voltage above the ATL431 cathode voltage. When the DC source voltage goes below 13 V, the LMV339 will output a logic low, which will be sent to the logic control to turn off the MOSFETs. The duration of the low output is determined by the time constant for the RC network at the output of the UVLO comparator.

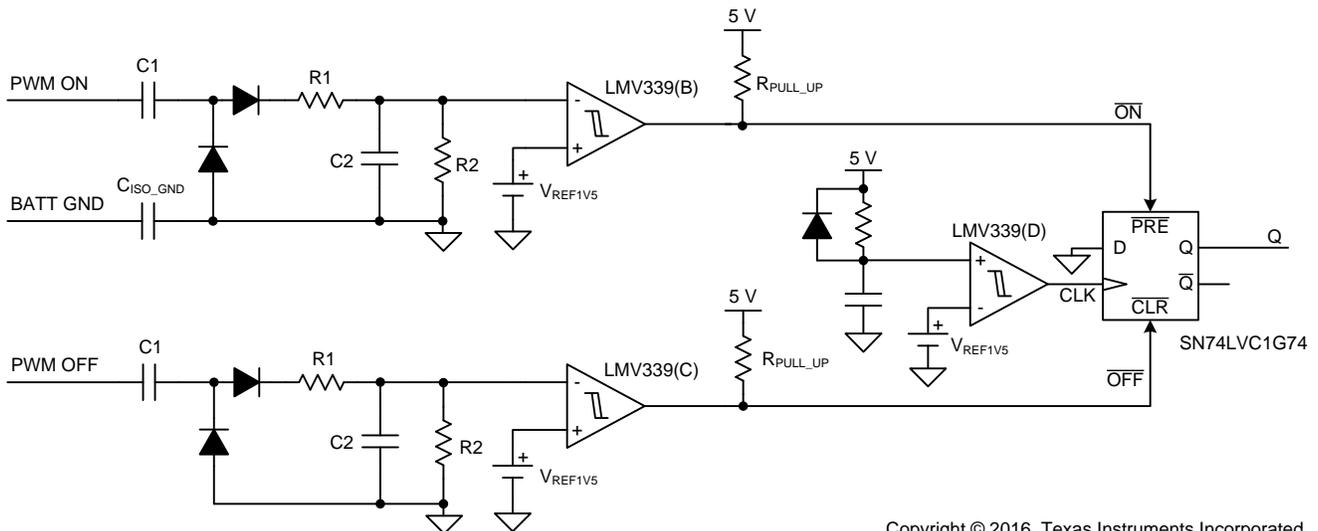
To calculate values of the RC network, use the desired delay time and Equation 8 and Equation 9.

$$\tau = R_{UVLO} \times C_{UVLO} \tag{8}$$

$$V_{UVLO}(t) = 5\text{ V} \times \left(1 - e^{-\frac{t}{\tau}}\right) \tag{9}$$

2.5 Isolation Design Theory

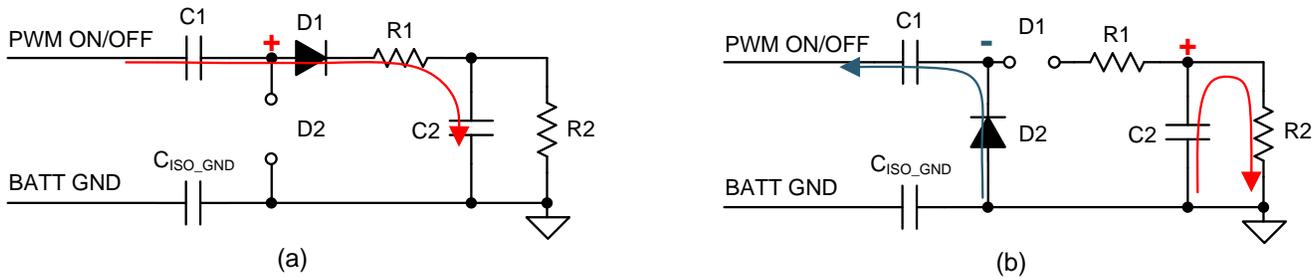
The galvanic isolation for the SSR is performed using capacitors, C1 and CISO_GND shown in Figure 10. The capacitors block direct current (DC), enabling each side of the capacitor to operate at different common voltages, separating the grounds. Alternating current (AC) is allowed to flow enabling the transfer of the control signal from the primary side to the secondary side. This is done using a square wave signal through C1 and CISO_GND providing an isolated ground path for the return current. To provide the proper logic level required by the D-type flip-flop, the input PWM signal must be converted to a DC signal, then inverted and level shifted.



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Figure 10. Capacitive Isolation Network With Logic Control

The control AC to DC signal conversion is achieved using the diodes and passive network shown at the input of the comparators in Figure 10. When the AC signal is applied and is logic level HIGH, D1 will conduct allowing C2 to charge as shown in Figure 11a. When the PWM signal is logic level LOW, D1 is reverse biased and D2 conducts discharging C1 shown in Figure 11b. By choosing a large value for R2, the discharge time for C2 will be slow enough to hold the charge until the AC is again logic level HIGH. For the duration the AC signal is applied, C2 will continue to charge to a voltage set by the capacitive divider, C1 and C2, and resistive divider, R1 and R2. When the voltage across C2 increases above the reference voltage of the LMV339, the open collector output will pull the voltage low, enabling the preset or clear of the output of the flip-flop.



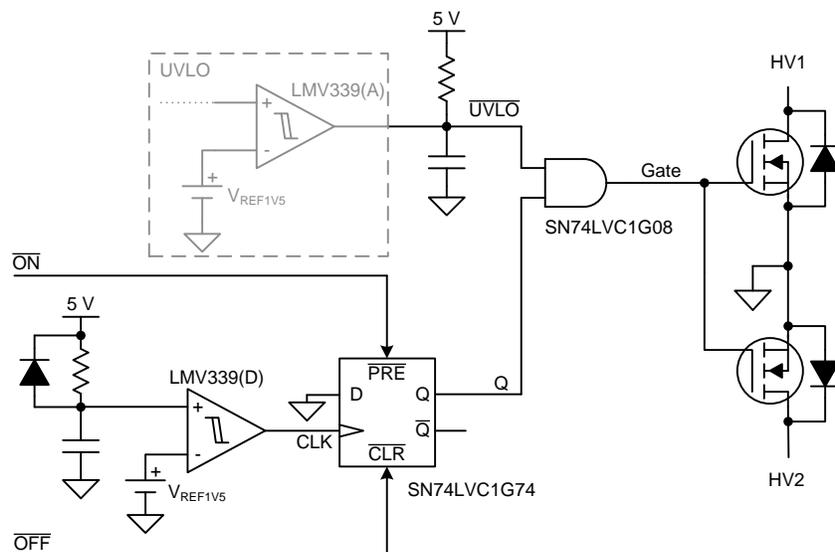
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Figure 11. Mode of Isolation Network During (a) V_{HIGH} and (b) V_{LOW} of PWM Input Signal

When the AC signal is removed, C2 will discharge through R2. When the voltage across C2 decreases below the reference voltage of LMV339, the output will be pulled high by the pullup resistors at the output of the comparator shown in Figure 10 disabling the preset of the flip-flop.

2.6 Control Logic Design Theory

The control logic circuitry uses short, LOW logic level pulses at the inputs of the D-type flip-flop, the SN74LVC1G74, to turn on and off the MOSFETs. See Table 4 for the logic levels of the output Q in reference to the input logic levels of /PRE and /CLR. Output Q is sent to one input of the AND gate, the SN74LVC1G08, whose other input is connected to the output of the UVLO comparator, as shown in Figure 12. The AND gate incorporates the control functionality of the UVLO with the input enable signal and drives the MOSFET gates.



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Figure 12. Control Logic and Gate Driver Schematic

Table 4. SN74LVC1G74 Logic Levels for /PRE, /CLR and Q

/PRE	/CLR	CLK	D	Q
L	H	X	X	H
H	L	X	X	L
H	H	↑	L	L

When the SSR is initially connected to the power source, the flip-flop output will be in an unknown state. To initialize the flip-flop in the desired off-state, connect an RC network to the positive input of the comparator and connect D to GND. After the rail voltages are stable, the signal at the comparator input will increase depending on the time constant of the network. When the RC signal passes the V_{REF1V5} threshold, the Q output will be set to a logic level LOW setting the SSR in an off-state.

For the full logic sequence to turn on and off the switch through the D-type flip-flop, see [Figure 13](#).

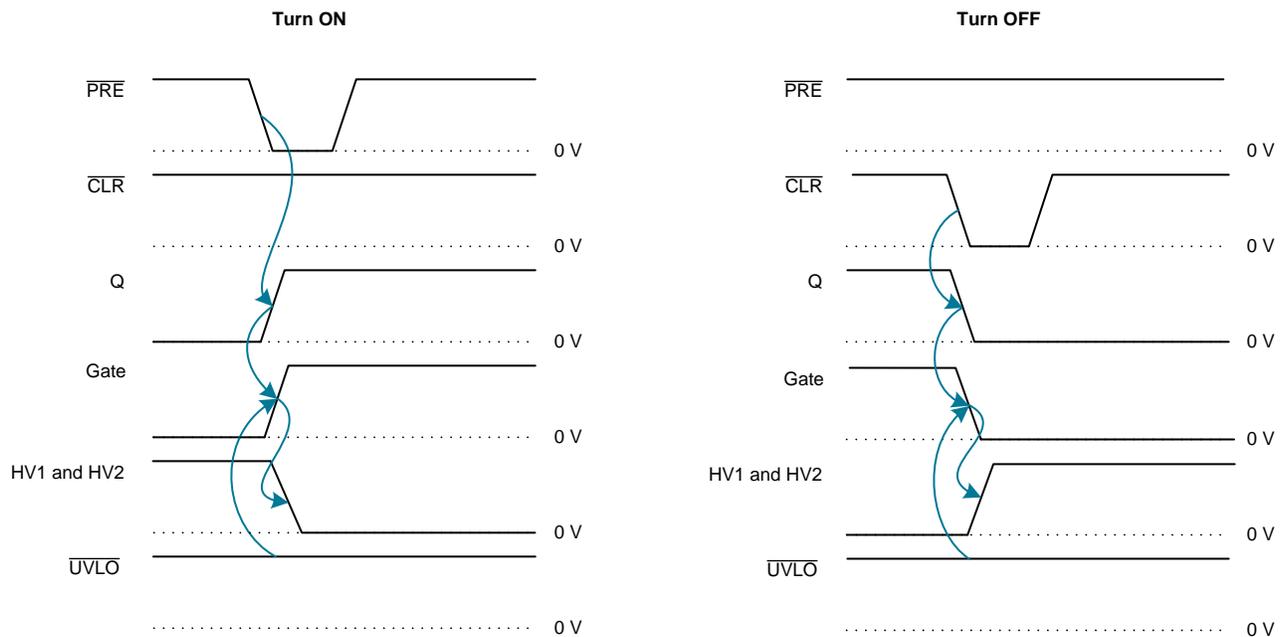


Figure 13. SSR Turnon and Turnoff Logic Sequence

3 Getting Started Hardware

3.1 Board Overview

For ease of use, all of the components, headers, and test points are located on the top side of the board, shown in Figure 14. The signal chain starts on the left side of the board and moves to the right side of the board in a linear fashion. The input header, J7, is located on the left edge of the board and has connection points PWM OFF, PWM ON, and GND BATT for pulse width modulated (PWM) waveform inputs and primary-side ground for the isolation network. Moving to the right of the board are four headers, J1, J2, J3, and J6. The left-most header, J3, connects the 5-V_{DC} supply rail to the isolation, logic control, and gate driving networks. To the right, the rectified AC voltage is connected the DC power supply through J1 and to the input of UVLO through J2. The remaining two pin header, J6, connects the output of the UVLO to the gate driver. On the far right is the terminal block, J5, which connects the circuit to the 24-V_{AC} HVAC load. The ten surface mount test points provide access to different signals and ground.

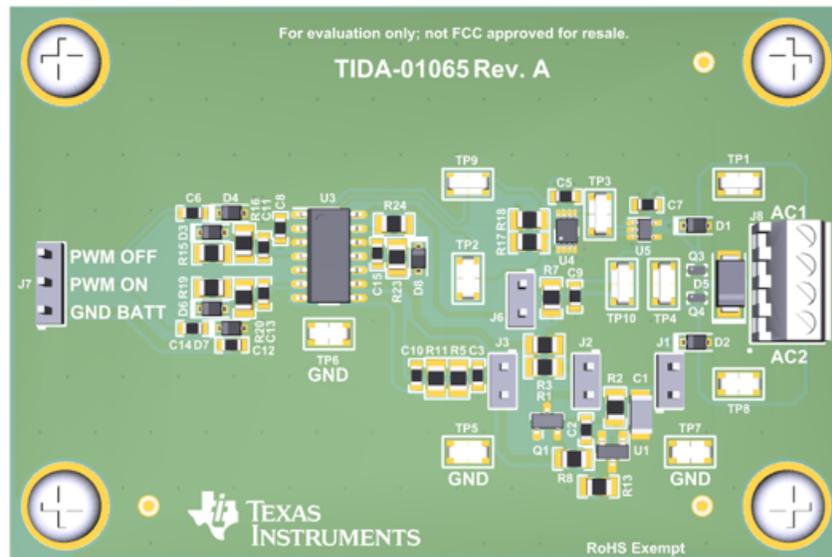


Figure 14. TIDA-01065 Reference Design Hardware

3.2 Operating the Circuit

Before powering the board, set the headers in the orientation described in Table 5. Connect the HVAC system load last to power the board.

Table 5. Header Connections at Start-up

HEADER	CONNECTION
J1	Short
J2	Short
J3	Short
J6	Short
J7	Pin 2 and Pin 3 to PWM sources (initially off), Pin 1 to battery GND
J8	24-V _{AC} HVAC load

When the board is first powered on, the rectification diodes will provide the voltage to the DC power supply, which will enable, logic control, and gate driver. To turn on the MOSFETs, provide a PWM (3.3-V square wave, 400-kHz) signal to PWM ON for a short duration through pin 2 of J7. To turn off the MOSFETs, provide a PWM (3.3-V, 400-kHz) signal to PWM OFF for a short duration through pin 1 of J7. Do not apply PWM ON and PWM OFF signals at the same time, which will provide an unstable condition of the flip-flop.

4 Testing and Results

4.1 Test Setup

Following the header orientation listed in [Table 5](#), the circuit is tested using a Honeywell 120- to 24-V_{AC} 40VA transformer, AT140B1214, similar to what is used in HVAC systems. A 24-V lightbulb is connected in series across terminal block J8 to provide a 0.18-A load, as shown in [Figure 15](#). The initial testing procedure was to activate and deactivate the switch to see the light turn on and off. There was no flicker in the light, providing the initial results that the charging time of the DC supply capacitor was not too long.

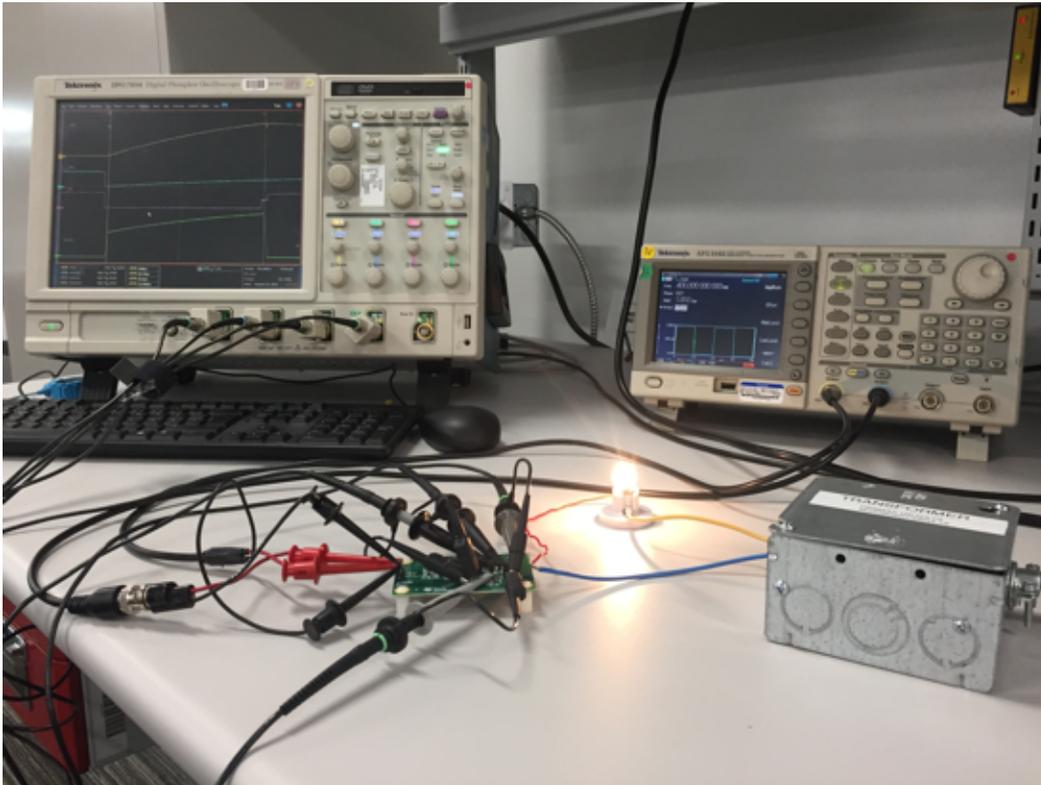


Figure 15. Test Setup of TIDA-01065 EVM, Light Bulb, and Transformer

To verify specific functionality of this reference design, there are two necessary tests: current consumption from the 24-V_{AC} line, and timing of the signal chain waveforms to validate self-powering and fast switching. The first test performed is the current consumption. These values were collected measuring the current flow through available headers using an ampere-meter during on- and off-states. The data was then verified by calculating the current through resistors by means of voltage measurements in addition to current rating of components from their datasheets.

The second test is to measure the timing of the control signals, which includes three sets of signals. The first set of signals measures the charging time of the DC supply capacitor. This is seen by probing J2, TP10, TP4, and AC1/AC2 as shown in [Figure 16](#).

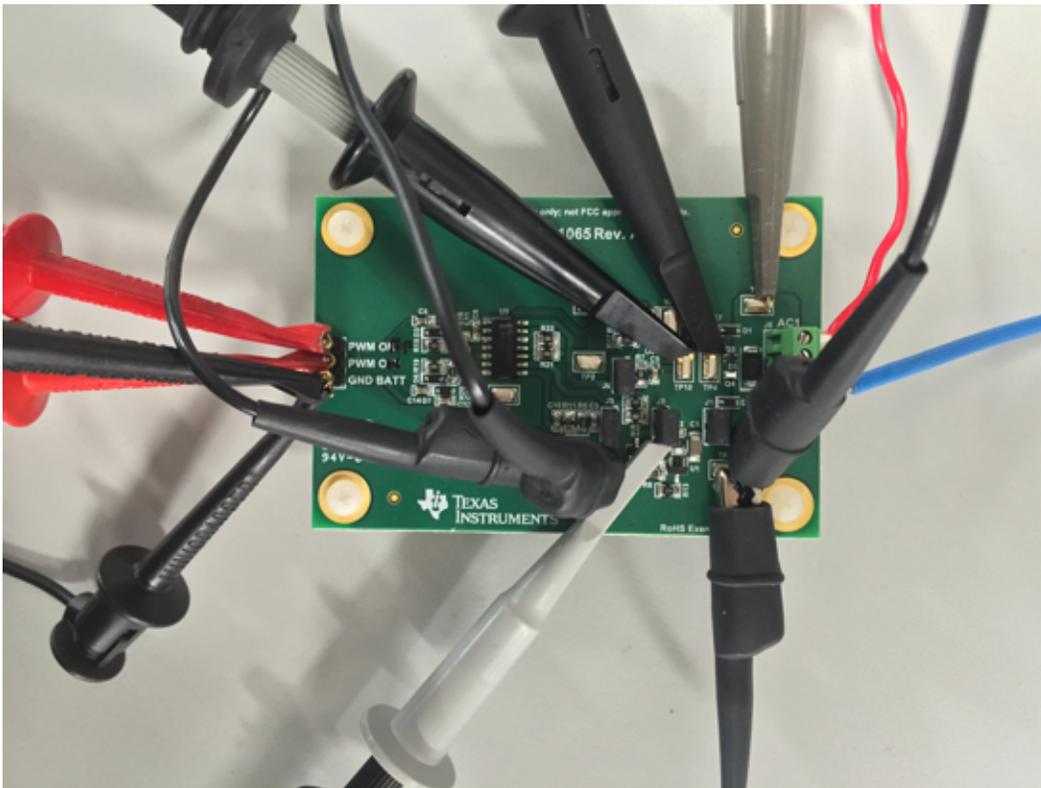


Figure 16. Probe Connections for Signal Chain Waveforms

The second and third signals are to check the turnon and turnoff delay of the MOSFETs. The turnon and turnoff functionality has been verified visually by the light bulb, but it is important to verify the speed of the switching as to efficiently charge the DC supply capacitor during active time. The waveforms captured are PWM ON or PWM OFF, TP3, TP4, and AC1/AC2, which can be found in [Figure 20](#) and [Figure 21](#) in [Section 4.2](#).

4.2 Test Data

The total steady-state current consumption for both on and off times are found in [Table 6](#). The steady-state currents for each block of the SSR for both on and off times are shown in [Figure 17](#) and [Figure 18](#).

Table 6. Total Measured Steady-State Current Consumption

STATE	CURRENT (μA)
ON time	164.83
OFF time	239.33

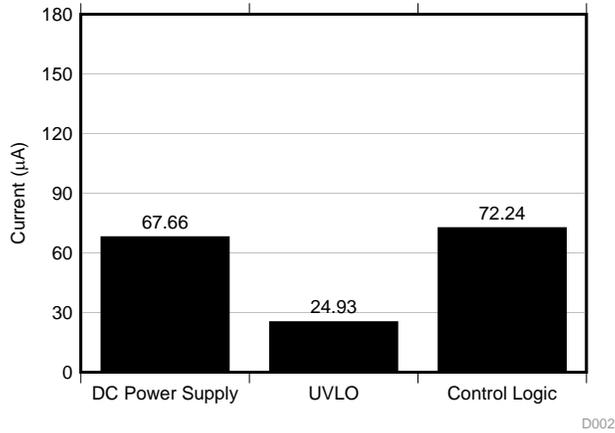


Figure 17. Measured Steady-State Current Consumption During ON Time

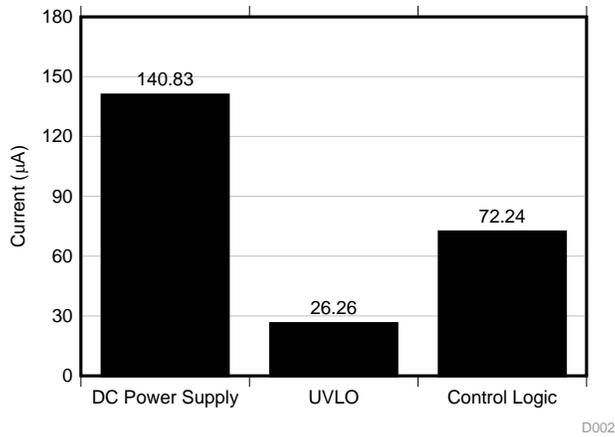


Figure 18. Measured Steady-State Current Consumption During OFF Time

Figure 19 displays charging time of the DC supply capacitor during the active time of the SSR. Active time of the SSR is when it is controlling the HVAC load and MOSFETs are ON also cycling through ON and OFF recharging the DC supply capacitor. The time between the rising and falling edge of the AC1 and AC2 waveform corresponds with the V_{DC} charging time of $\sim 65 \mu\text{s}$, as shown in Figure 19. This also corresponds with the edges of TP10 (UVLO) and TP4 (V_{GS}), with the consideration of delay.

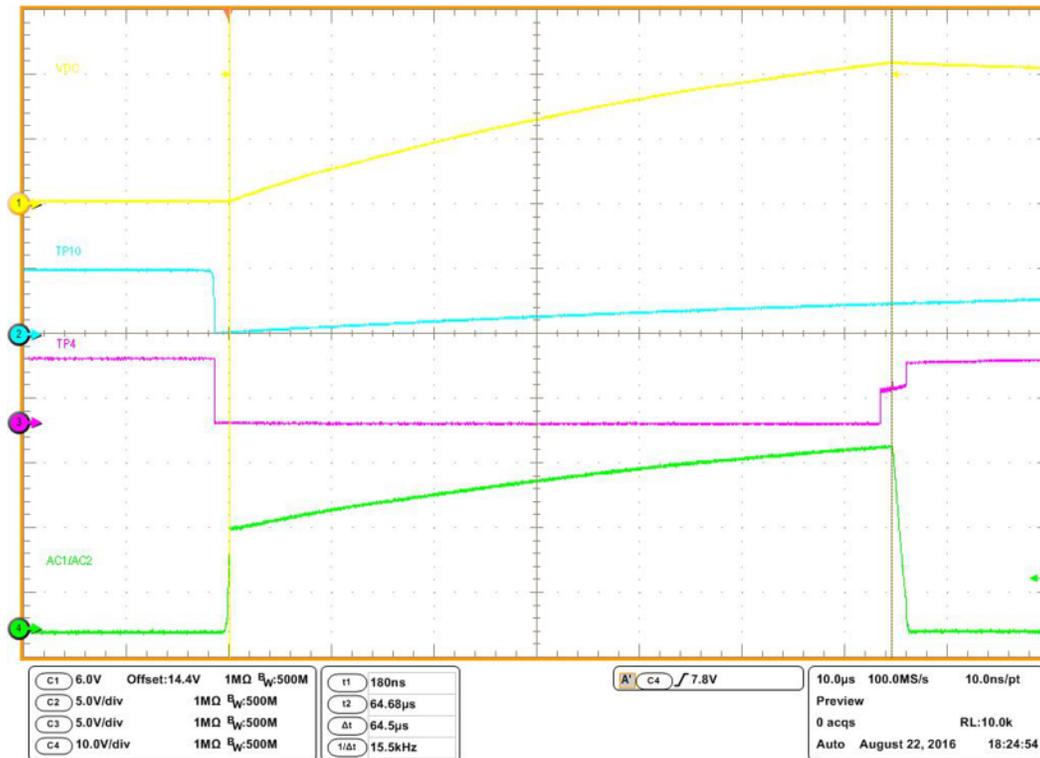


Figure 19. Charging Time of DC Supply Capacitor (Yellow) in Reference to TP10 (Blue), TP4 (Purple), and AC1/AC2 (Green)

Figure 20 shows the turnon delay time through an input PWM (3.3-V, 400-kHz) signal to PWM ON of the isolation network. From the rising edge of the PWM signal to the HIGH-to-LOW transition of the drain-to-source voltage (V_{DS}) of the MOSFET is 16.25 μ s. In this TI Design, the turnon time of the MOSFETs ($AC1/AC2 = V_{DS}$) is 0.75 μ s.

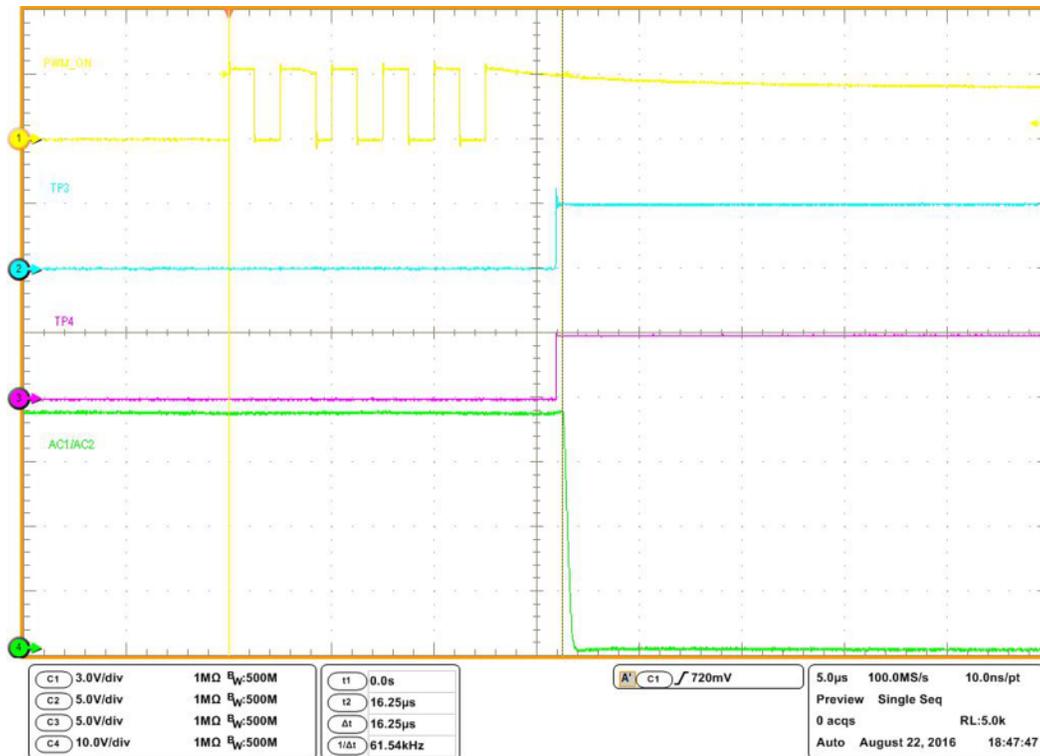


Figure 20. ON Delay Waveforms From PWM ON Input (Yellow) to TP3 (Blue), TP4 (Purple), and V_{DS} of MOSFETs (Green)

Figure 21 shows the turnoff delay time through an input PWM (3.3-V, 400-kHz) signal to PWM OFF of the isolation network. From the rising edge of the PWM signal to the LOW-to-HIGH transition of the drain-to-source voltage (V_{DS}) of the MOSFETs is 17.9 μ s. The turnoff time of the MOSFETs ($AC1/AC2 = V_{DS}$) is 0.75 μ s.

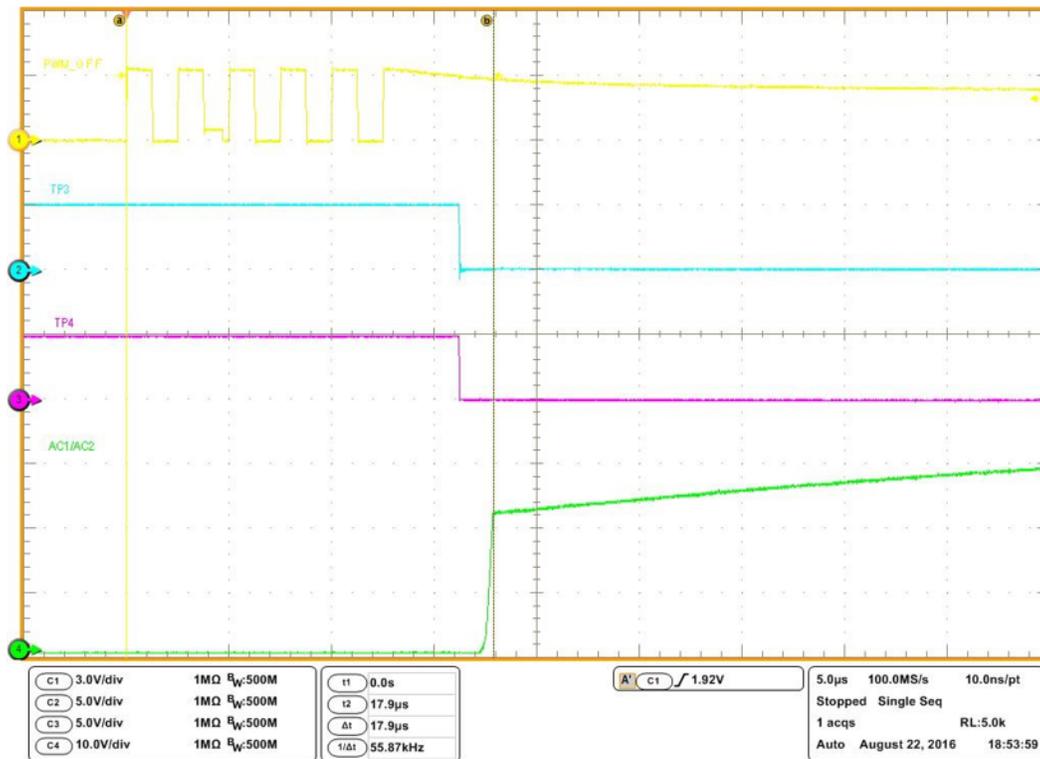


Figure 21. OFF Delay Waveforms From PWM OFF Input (Yellow) to TP3 (Blue), TP4 (Purple), and V_{DS} of MOSFETs (Green)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at [TIDA-01065](#).

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01065](#).

5.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting later on.

5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01065](#).

5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01065](#).

5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01065](#).

5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01065](#).

6 Related Documentation

1. Texas Instruments, [Solid State Relay 24-V AC Switch With Galvanic Isolation](#), TIDA-00751 Design Guide (TIDUB92)
2. Texas Instruments, [Self-Powered AC Solid State Relay With MOSFETs](#), TIDA-00377 Design Guide (TIDUBR5)
3. Texas Instruments, [Low-Cost AC Solid-State Relay With MOSFETs](#), TIDA-01064 Design Guide (TIDUC87)
4. Texas Instruments, [Designing with the "Advanced" TL431, ATL431](#), Application Report (SLVA685)
5. Texas Instruments, [Setting the Shunt Voltage on an Adjustable Shunt Regulator](#), Application Report (SLVA445)
6. Texas Instruments, [Compensation Design With TL431 for UCC28600](#), Application Report (SLUA671)
7. Texas Instruments, TI E2E Community: Industrial Strength, [Click! Clack! What's the setback in your thermostat?](#), (2016, June 28) Retrieved from http://e2e.ti.com/blogs_/b/industrial_strength/archive/2016/06/28/click-clack-what-s-the-setback-in-your-thermostat
8. Texas Instruments, TI E2E Community: Industrial Strength, [A modern approach to solid-state relay design](#), (2016, July 26) Retrieved from https://e2e.ti.com/blogs_/b/industrial_strength/archive/2016/07/26/a-modern-approach-to-solid-state-relay-design
9. Texas Instruments, TI E2E Community: Industrial Strength, [How to power your thermostat using solid state relays](#), (2016, August 11) Retrieved from https://e2e.ti.com/blogs_/b/industrial_strength/archive/2016/08/11/how-to-power-your-thermostat-using-solid-state-relays
10. JEDEC Solid State Technology Association. (2006). *Interface Standard for nominal 3 V/3.3 V Supply Digital Integrated Circuits (JESD8C.01)*. Arlington, VA : JEDEC Solid State Technology Association

6.1 Trademarks

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